Doc version: HME-HRDSE04, Sept. 2018

For more information about HR Family, please go to www.hercules-micro.com

Some of the device information comes from CME.

1. Overview

Introduction and Architecture

HME-HR family FPGA has a very low power feature that make they are fit for mobile fields.

The architecture of this family consists of 4 fundamental programmable functional blocks which are the PLBs, IOBs, EMB and PLLs, see the figure below.

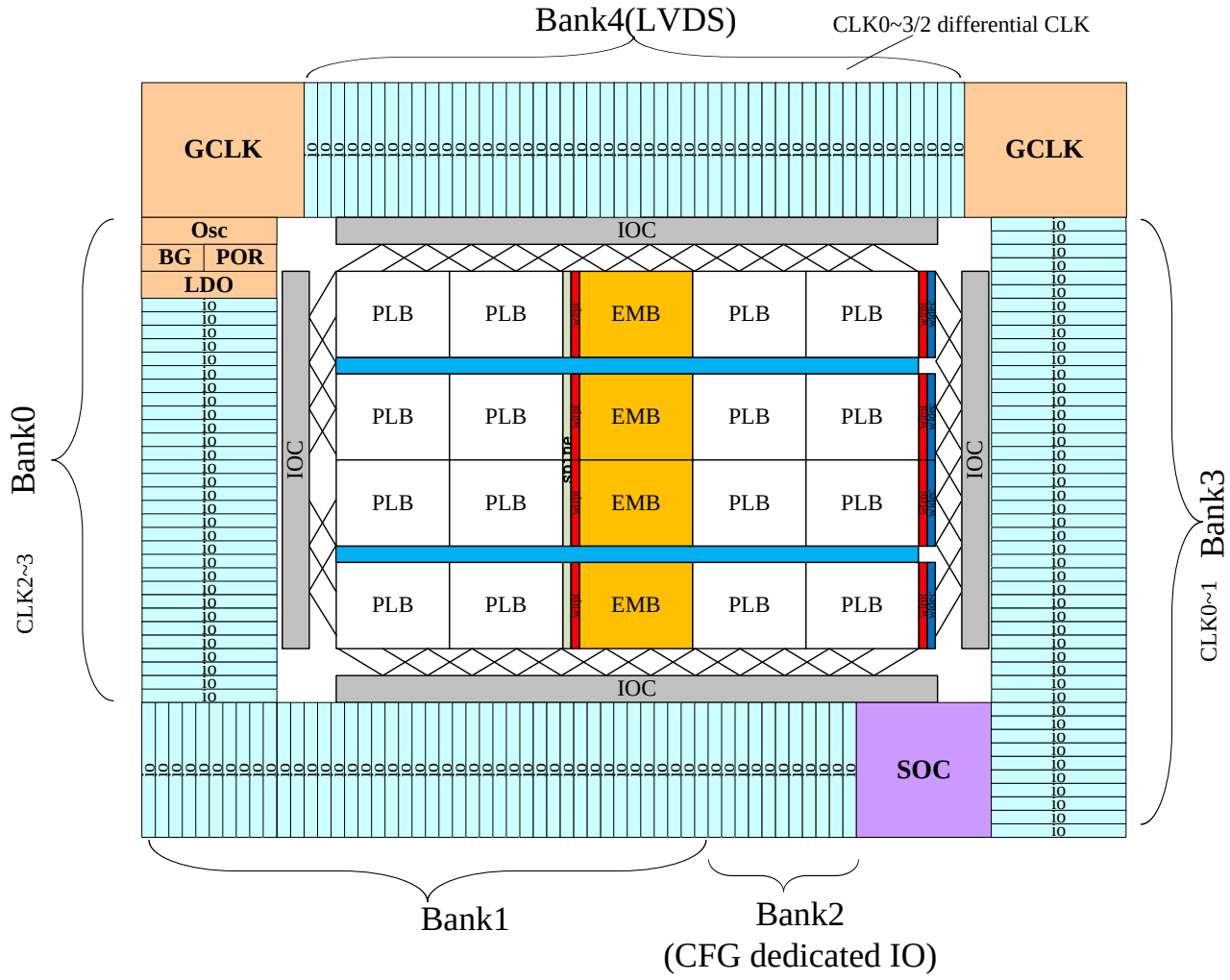


Figure 1 HME-HR FAMILY FPGA Architecture

As shown in figure above:

- Programmable Logic Blocks (PLBs) contain RAM-based Look-Up Tables (LUT-4) to implement logic and storage elements that can be used as flip-flops. PLBs can be programmed to perform a wide variety of logical functions as well as to store data.
- Embedded Memory Block provides data storage in the form of 4.5K bit dual-port blocks.
- Phase (PLL) blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals.
- Input/output Blocks (IOBs) control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation.

Feature

- **SRAM-based FPGA Fabric**
  - Up to 3072 4-input Look-up Tables, 2048 DFF-based registers
  - Performance up to 200MHz
- **Embedded RAM Block Memory**
  - 16 4.5Kbit programmable dual-port DPRAM memory EMB5K blocks
- **Clock Network**
  - 8 de-skew global clocks
  - 2 PLLs support frequency multiplication, frequency division, phase-shifting, de-skew
  - 8 external input clocks
- **Multi-voltage, multi-standard, multi-banks I/O**
  - 3.3V to 1.5V single-ended LVCMOS/ LVTTL standards
  - LVDS25/ sub-LVDS IO standard
  - SDR/DDR mode for general and LVDS I/O
  - Up to 800 Mbps data transfer rate per differential I/O
  - Programmable driving strength
  - Schmitt trigger inputs, to 200 mV typical hysteresis
- **Low power Features**
  - Ultra Low Power Devices
  - Advanced 40 nm low power process
  - As low as 32 μW standby power
  - Programmable low swing differential I/Os
  - Dynamic clock switch and gating in system to reduce dynamic power
- **Configuration**
  - JTAG Mode
  - AS Mode
  - PS Mode
- **Security**
  - 128b ASE for configuration
  - 256b Efuse

Feature Summary and Package Information

Part Number		HR01PN0	HR02PN0	HR02PN3	HR03PN0	HR03PN3
Programmable Logic Block (PLB)	LUT	768	1536	1536	3072	3072
	Register	512	1024	1024	2048	2048
Embedded Memory Block (EMB)	4.5Kb	16	16	16	16	16
	Max	72Kb	72Kb	72Kb	72Kb	72Kb
PLL		1	2	2	2	2
On Chip OSC		1	1	1	1	1
Efuse/128bitAES		256b	256b	256b	256b	256b
Max User I/O		97	97	97	128	128
Differential I/O Pairs		12	12	12	16	16
SPI Flash				4Mb		4Mb
Leakage Current		70μA	120μA	120μA	200μA	200μA
Package (unit: mm)		Max User IO (LVDS Channels)				
W36 (2.9x2.4x0.5, 0.4 pitch)					26(5)	26(5)
W24(2.9x2.0x0.5, 0.4 pitch)				16(6)		
Q32(5x5x0.85, 0.5 pitch)		25(3)	25(3)		25(3)	
Q32(4x4x0.55, 0.4 pitch)				18(0)		
Q68(8x8x0.85, 0.4 pitch)					55(7)	
U36 (3x3x0.96, 0.4 pitch)			28(3)		28(3)	
C192 (9x9x1.2, 0.5 pitch)					128(16)	
T100 (14x14x1.0, 0.5 pitch)					74(9)	

This part introduces the HR family with its PLB, EMB, Input/Output I/O, PLL, OSC, and CMB.

2. FPGA

The HME-HR FAMILY FPGA consists of up to 3072 LUTs, 16 EMB 4.5K blocks and 2 PLLs. This chapter describes the element blocks.

Programmable Logic Block (PLB)

The Programmable Logic Block (PLB) is the fabric basic logic tile that is composed of Logic Engine (LE) and Xbar. The PLB is the basic tile of the Fabric. Their organization is shown as in figure below. One LE contains four interconnected Logic Parcels (LP). The LE constitutes the main logic resource for implementing synchronous as well as combinatorial circuits.

The Xbar switches and passes the signals between the tile elements.

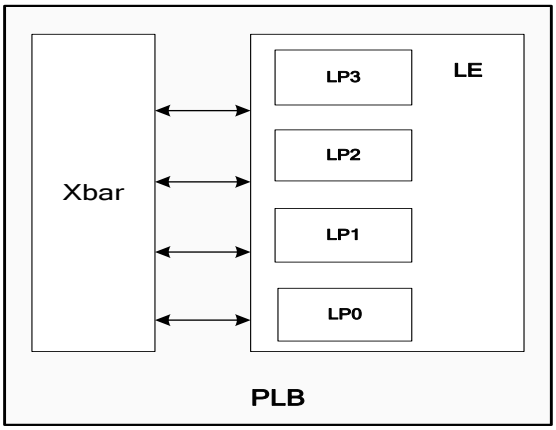


Figure 2 PLB Schematic Diagram

The PLBs are arranged in a regular array of rows and columns as shown in figure above.

The HME development software designates the location of a PLB according to its C and R coordinates, starting in the bottom left corner, as shown in figure above. The letter ‘C’ followed by a number identifies columns of PLBs, incrementing from the left side of the die to the right. The letter ‘R’ followed by a number identifies the position of each PLB in the CLB row, incrementing from the bottom of the die.

Logic Parcel (LP)

LP is the basic programmable logic element. The LP has the following elements to provide logic, arithmetic functions as shown in figure below.

- **Three 4-input LUT function generators**
- **Two registers**
- **Carry, cascade and arithmetic logic**

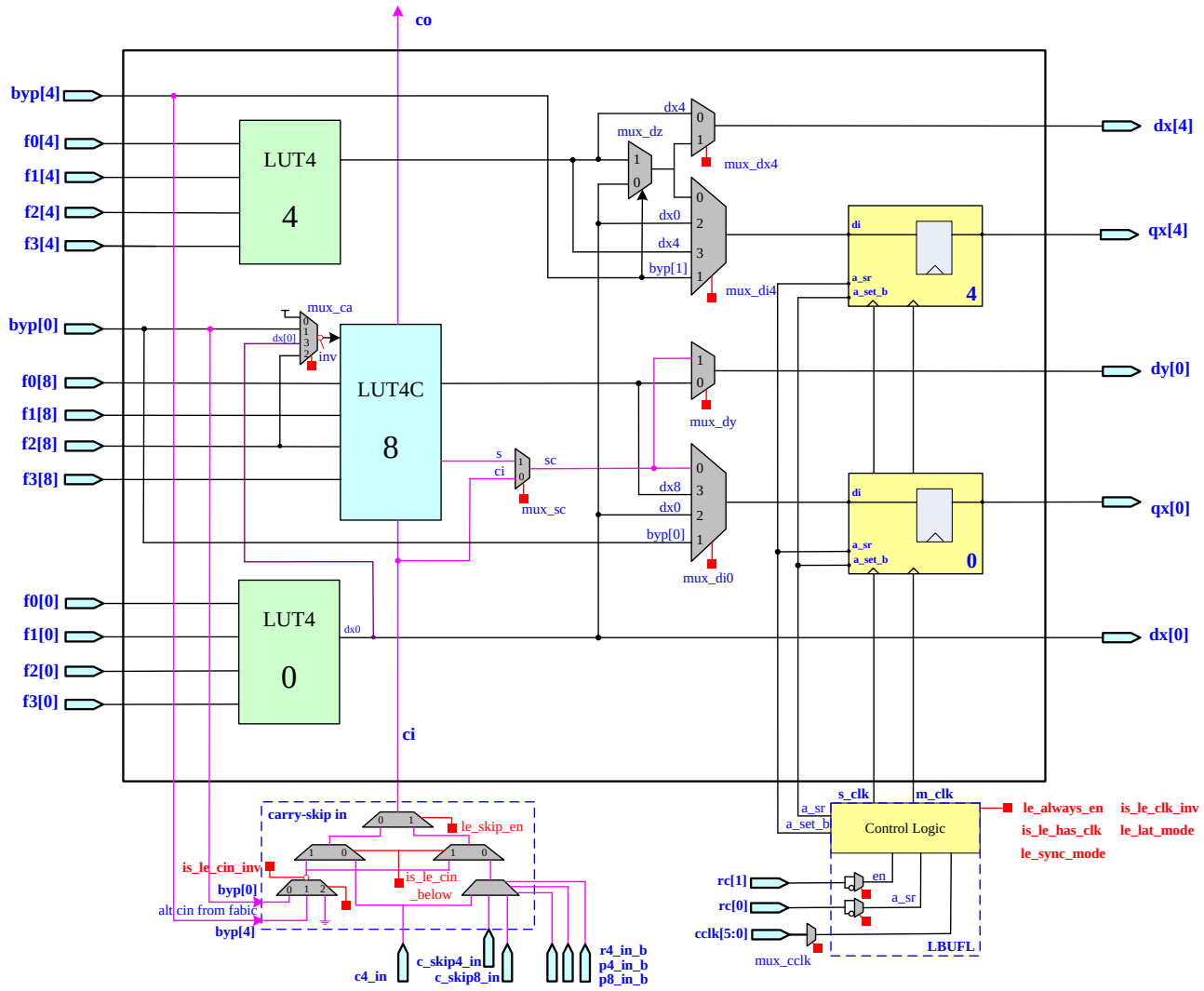


Figure 3 LP Schematic Diagram

(1) Look-Up Table (LUT)

The Look-Up Table or LUT is a RAM-based function generator and is the main resource for implementing logic functions. Each of the three LUTs in a LP has four logic inputs (f0-f3) and a single output (d). Any four-variable Boolean logic operation can be implemented in one LUT. Functions with more inputs can be implemented by cascading LUTs that are in one LP or adjacent LPs.

(2) Register

The register is a programmable D-type flip-flop, which can also be configured as a T-latch. There is a multiplexer on the D input select of the registers. The multiplexer selects either a LUT combinatorial output, adder output or the bypass signal byp[x].

(3) Carry, Cascade and Arithmetic Logic

The carry chain, together with various dedicated arithmetic logic gates, support fast and efficient implementations of math operations such as adders, counters, comparators, multipliers, wide logic gates, and related functions. The carry logic is automatically used for most arithmetic functions in a design. The gates and multiplexers of the carry and arithmetic logic can also be used for some general-purpose logic, including simple wide Boolean functions (e.g. wide AND and OR functions).

The carry input from LUT4C of the neighboring LP below enters the LUT4C and the LUT4C generates

the carry out which can be cascaded to the neighboring LUT4C above.

Logic Engine (LE)

The LE contains 4 LPs, fast carry, and Register Control circuitry. The LEs can implement flexible carry function with fast carry logic to speed up multi-byte adders.

Interconnect

In all the HME-HR family devices, tiles include Xbar that is interconnect, also called routing resources, and Logic Engine (LE) or special function block (EMB or DSP). The Xbar passes signals among the various functional tiles of the HME-HR family devices. There are four kinds of interconnect: Octal lines, Triple lines, Single lines, and Diagonal lines.

Octal lines span the die both horizontally and vertically and connect to Xbars four and eight tiles away (see figure below).

Triple lines connect horizontally and vertically to Xbars one, two and three tiles away (see figure below).

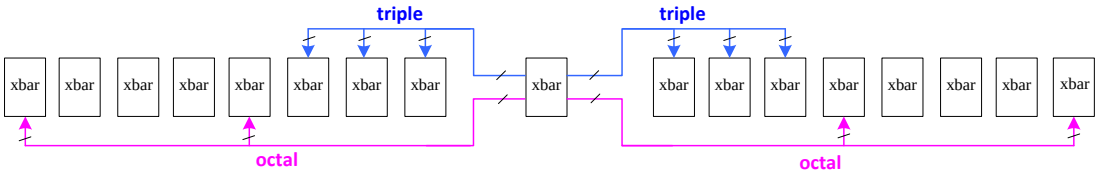


Figure 4 Octal and Triple Lines

Single and Diagonal lines directly connect routing signals to neighboring tiles: vertically, horizontally and diagonally.

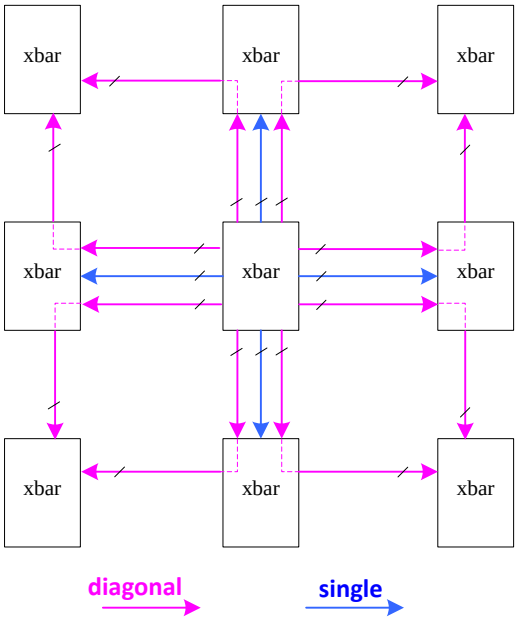


Figure 5 Single and Diagonal Lines

Embedded Memory Block (EMB)

HME-HR family device supports embedded memory block (EMB), which is organized as one column of EMB4.5K. EMB4.5K module is a true dual-port memory that permits independent access to the common EMB block. Each port has its own dedicated set of data, control, and clock lines for synchronous read and write operations. EMB provides the following features shown below:

- **4.5Kbits**
- **Mixed clock mode**
- **A, B data width configured independently**
- **Support WRITE_FIRST (write through), READ_FIRST and NO_CHANGE modes**
- **Bypass or Output registered option**
- **Parity bit**

  The EMB blocks support a parity bit for each byte. The parity bit, along with ECC macro, can implement parity checking or error correction (SECDED) to ensure data integrity. Parity-sized data words can be used to store user-specified control bits.

- **Initialization file to pre-load memory content in RAM and ROM modes**

  The format of initialization file is either .hex or .dat (a hexadecimal number on each line, the number of lines depends on depth of EMB). Initialization files initialize EMB memory during configuration.

- **Three Memory Modes available**

  EMB can be configured into the following modes:

  - emb_tdp : True Dual Port
  - emb_sdp : Simple Dual Port
  - emb_sp : Single Port

EMB Operation Mode

(1) EMB True Dual-port

EMB supports any combination of dual-port operation: two read ports, two write ports, or one read and one write at different clock frequencies. The figure below shows true dual-port memory configuration.

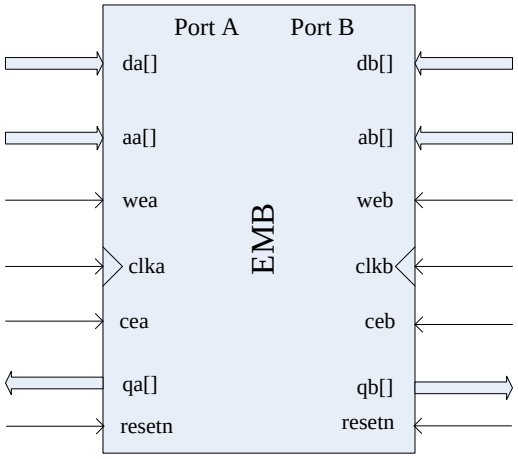


Figure 6 True Dual-port Memory Mode

Table 1 Port Descriptions of True Dual-port Memory Mode

Port name	Type	Description
aa,ab	Input	Port A (B) Address.
da ,db	Input	Port A (B) Data Input.
qa ,qb	Output	Port A (B) Data Output.
wea ,web	Input	Port A (B) Write Enable. Data is written into the dual-port SRAM upon the rising edge of the clock when both wea (b) and cea (b) are high.
cea,ceb	Input	Port A (B) Enable. When cea (b) is high and wea (a) is low, data read from the dual-port SRAM address aa (b). If cea (b) is low, qa (b) retains its value.
clka ,clkb	Input	Port Clock.
rstna,rstnb	Input	Reset the output register, low active.

Table 2 EMB4.5K True Dual-port Configurations

A Port	B Port						
	4K×1	2K×2	1K×4	512×8	512×9	256×16	256×18
4K × 1	√	√	√	√			
2K × 2	√	√	√	√			
1K × 4	√	√	√	√			
512 × 8	√	√	√	√			
512 × 9					√		
256 × 16							
256 × 18							

(2) EMB Simple Dual-port

EMB also supports simple dual-port memory mode: one read port while one write port. The figure below shows simple dual-port memory configuration.

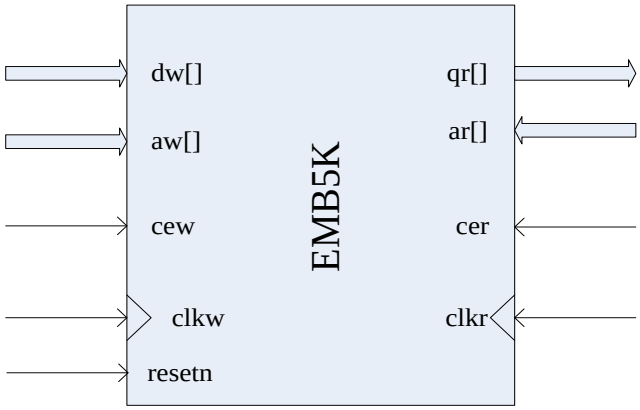


Figure 7 Simple Dual-port Memory Mode

Table 3 EMB4.5K Simple Dual-port Configurations

Write Port	Read Port						
	4K×1	2K×2	1K×4	512×8	512×9	256×16	256×18
4K × 1	√	√	√	√		√	
2K × 2	√	√	√	√		√	
1K × 4	√	√	√	√		√	
512 × 8	√	√	√	√		√	
512 × 9					√		√
256 × 16	√	√	√	√		√	
256 × 18					√		√

(3) EMB Single-port

EMB also supports single-port memory mode shown as figure below.

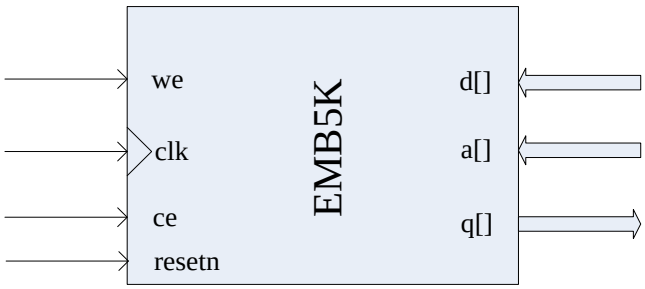


Figure 8 Single-port Memory Mode

Table 4 Pin Description of Single-port Memory Mode

Port name	Type	Description
d	Input	Write Data
a	Input	Write Address.
we	Input	Write Enable. Active high.
clk	Input	Write Clock.
ce	Input	Port Enable. Active high.
q	Output	Read Data
rstn	Input	Reset the output register, low active.

Table 5 EMB4.5K Single-port Configuration

Port						
4K×1	2K×2	1K×4	512×8	512×9	256×16	256×18

EMB Operations

Writing data to and accessing data from the block RAM are synchronous operations that take place independently on each of the two ports.

When the we and ce signals enable the active edge of CLK, data at the d input bus is written to the block RAM location addressed by the addr lines.

There are a number of different conditions under which data can be accessed at the q outputs which are No_Change, Write_First and Read_First operations.

Choosing a third attribute called NO_CHANGE puts the q outputs in a latched state when asserting we. Under this condition, the q outputs will retain the data driven just before we was asserted. NO_CHANGE timing is shown in the portion of Figure 9 during which WE is High.

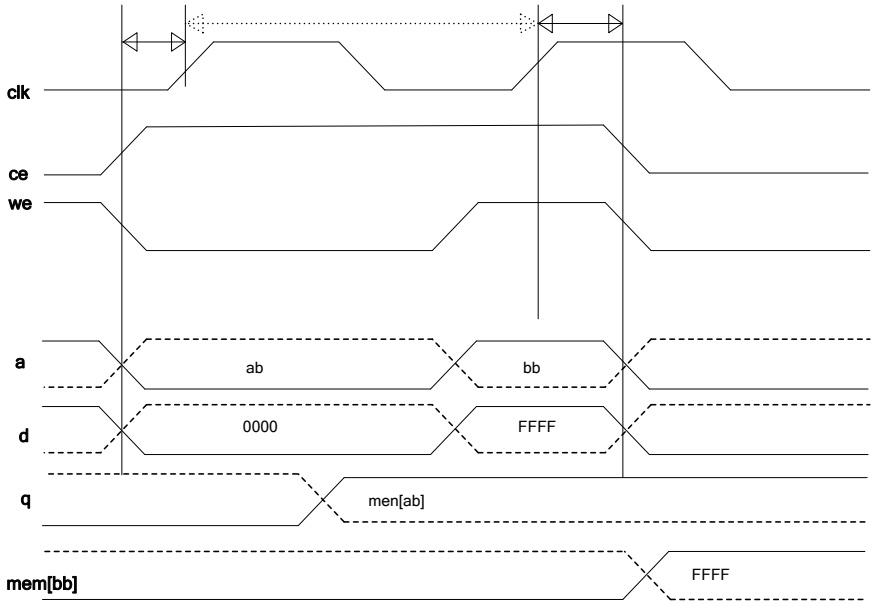


Figure 9 EMB No_Change Operation Waveforms

Choosing the Write_First attribute, data is written to the addressed memory location on an enabled active CLK edge and is also passed to the q outputs. Write_First timing is shown in the portion of Figure 10 during which WE is High.

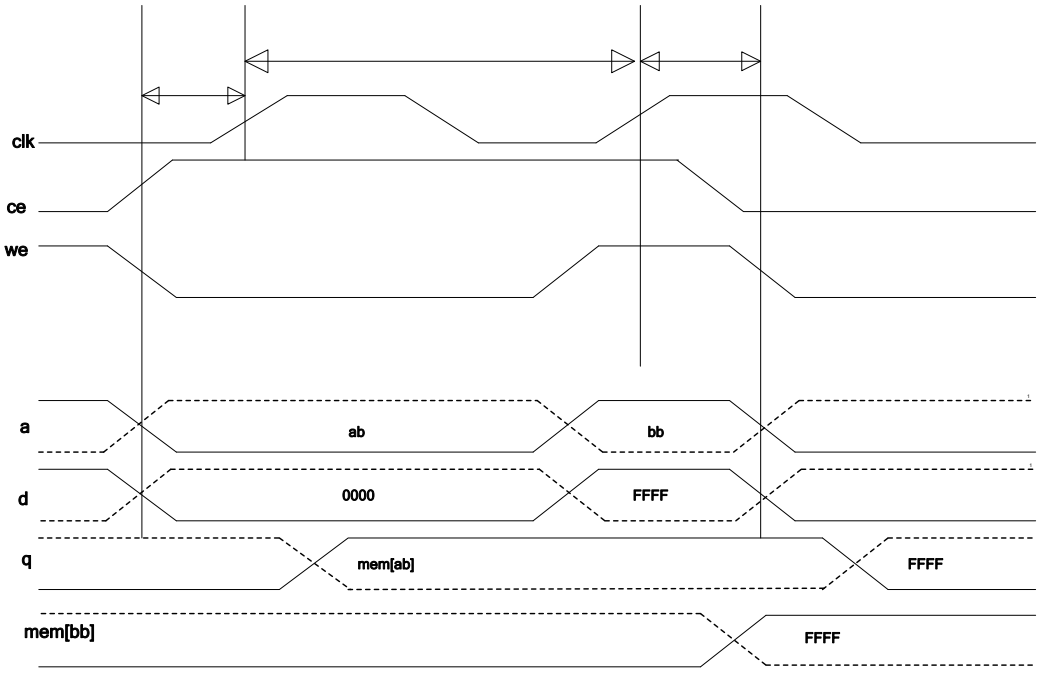


Figure 10 EMB Write_First Operation Waveforms

Choosing the Read_First attribute data already stored in the addressed location pass to the q outputs

before that location is overwritten with new data from the d inputs on an enabled active CLK edge. Read_First timing is shown in the portion of Figure 11 during which WE is High.

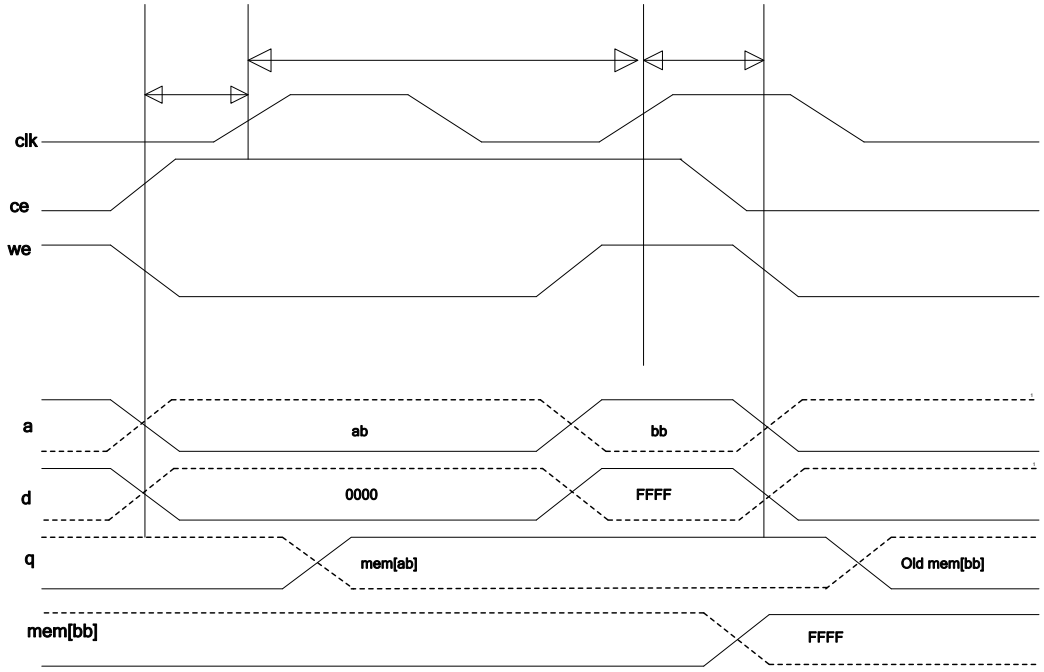


Figure 11 EMB Read_First Operation Waveforms

Input/Output (I/O)

The Input/Output Block (IOB) provides a programmable, bidirectional interface between the I/O pin and the FPGA's internal logic.

All I/O pins are organized into 5 banks which include the general I/O banks, LVDS I/O banks, and configuration I/O banks. Each bank has several common VDDIO_X output supply-voltage pins, which also powers certain input buffers.

The I/O provides the following features:

- **3.3V to 1.8V single-ended I/O standards and protocols for general I/O banks**
- **3.3V to 1.5V single-ended I/O standards and protocols for LVDS I/O bank**
- **Up to 800 Mbps data transfer rate per differential I/O**
- **DDR/SDR mode for general and LVDS IO**
- **Pull-up, Pull-down and bus keeper**
- **Schmitt trigger input**

Block Diagram

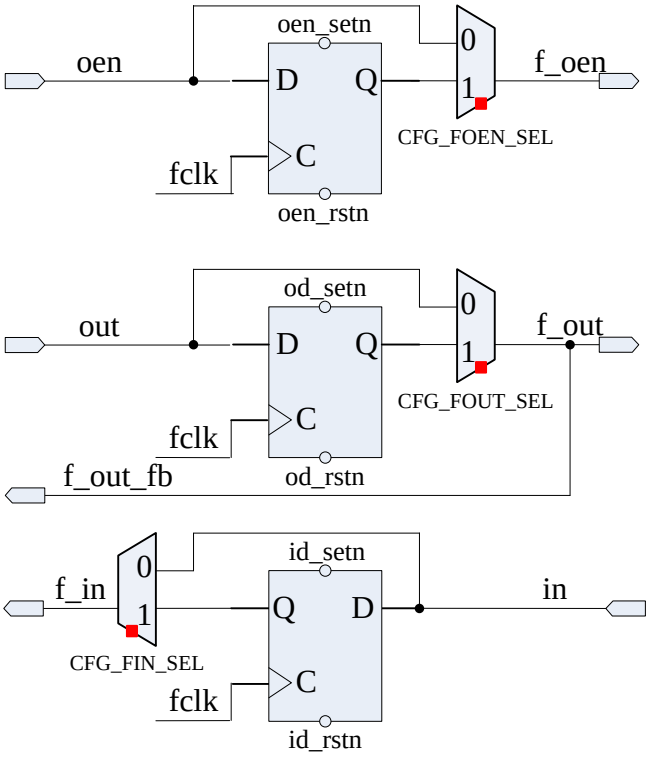


Figure 12 General Single-ended IO

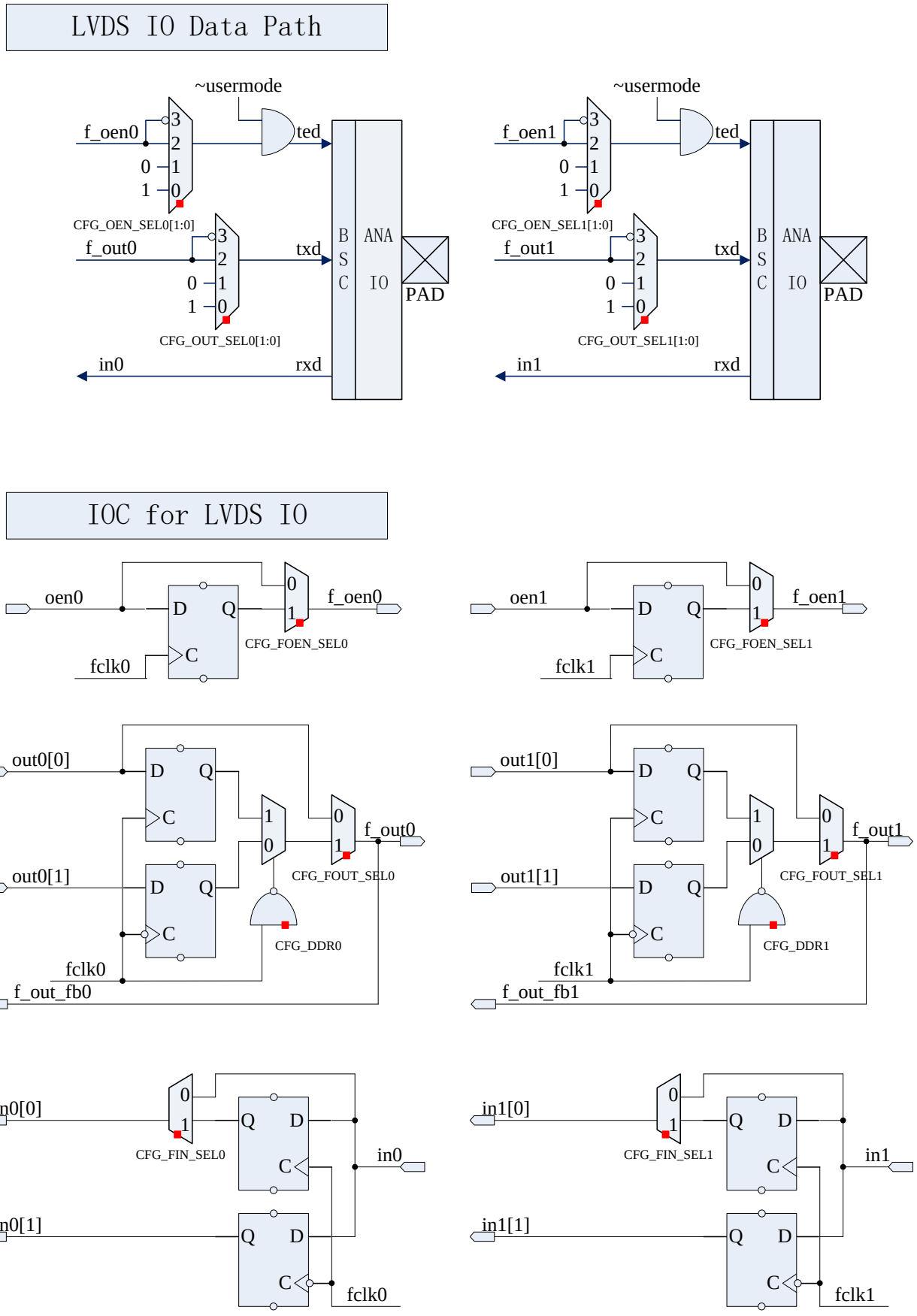


Figure 13 Differential LVDS IO

Pull-Up/Down/Keeper Resistors

The optional pull-up and pull-down resistors are intended to establish logic High or Low at unused I/Os. The pull-up resistor optionally connects each IOB pad to VDDIO_X and the pull-down resistor optionally connects each IOB pad to GND. The resistors are about 50K~100KΩ. Each I/O has an optional keeper circuit that retains the last logic level on a line after all drivers have been turned off. This is useful to keep bus lines from floating when all connected drivers are in a high-impedance state. These resistors are designated with the “pull up”, “pull down” and “bus keeper“ attributes in Fuxi. aoc file.

Drive Strength

The LVTTL, LVCMOS standards support several drive strength levels.

These programmable current strength settings are a valuable tool in helping decrease the effects of simultaneously switching outputs (SSO) and reducing system noise. The supported settings ensure that the device driver meets the specifications for IOH and IOL of the corresponding I/O standard.

Schmitt Trigger Input

Each HR I/O pin has a schmitt trigger input that is capable of transforming a slowly changing input signal into a sharply defined, jitter-free output signal.

ESD Protection

The Electro-Static Discharge (ESD) protection circuitry protects all device pads against damage from ESD as well as excessive voltage transients.

The VIN absolute maximum rating in Table 20 (see page 34) specifies the voltage range that the I/Os can tolerate.

The Organization of IOBs into Banks

The IOBs are allocated among 5 banks as shown in Figure 1 (see page 1). For all packages, each bank has its independent VDDIO_X lines. For example, the VDDIO_X Bank 1 lines are separate from the VDDIO_X lines going to all other banks.

The I/Os during Power-On, Configuration, and User Mode

With no power applied to the FPGA, all I/Os are in a high-impedance state. The VDD_CORE and VDDIO_X supplies may be applied in any order. Before power-on can finish, VDD_CORE and VDDIO_X must have reached their respective minimum recommended operating levels. At this time, all I/O drivers will also be in a high-impedance state.

At this point, the configuration data is loaded into the FPGA. The I/O drivers remain in a high-impedance state throughout configuration. The signal is released during Start-Up, marking the end of configuration and the beginning of the design operation in the user mode. At this point, those I/Os to which signals have been assigned will go active, while all unused I/Os will remain in a high-impedance state.

Phase-Locked Loop (PLL)

HR devices have two phase-locked loops (PLLs) that provide robust clock management and synthesis for device clock controllers, external system clock management, and I/O interfaces.

The left dedicated pin CLK0~CLK3, XIN and OSC (internal configuration oscillator) and FPGA logic feed

the left PLL's reference clock input. The right dedicated pin CLK0~CLK3, XIN and OSC (internal configuration oscillator) and FPGA logic feed the right PLL's reference clock input. The external feedback fbclkin must come from the dedicated pin CLK0~CLK3 or internal clkout0 if the PLL used as external feedback mode.

Features

- **Input frequency: 5~133MHz**
- **PFD input frequency: 5 ~ 133MHz**
- **Output frequency: 16 ~ 400MHz**
- **VCO operating range: 533 ~ 1066MHz**
- **Fixed VCO quadrant phase shift: 0°, 45°, 90°, 135°, 180°, 225°, 270°, 315°**
- **Output clock duty-cycle: 45-55%**
- **Power current consumption: Analog< 6mA,digital <1mA**
- **Total typical power down current: 200nA**
- **PLL outputs: CO0, CO1, CO2, CO3**
- **Lock detector and lock output**
- **De-skew mode**
- **Dynamic reconfiguration**

Block Diagram

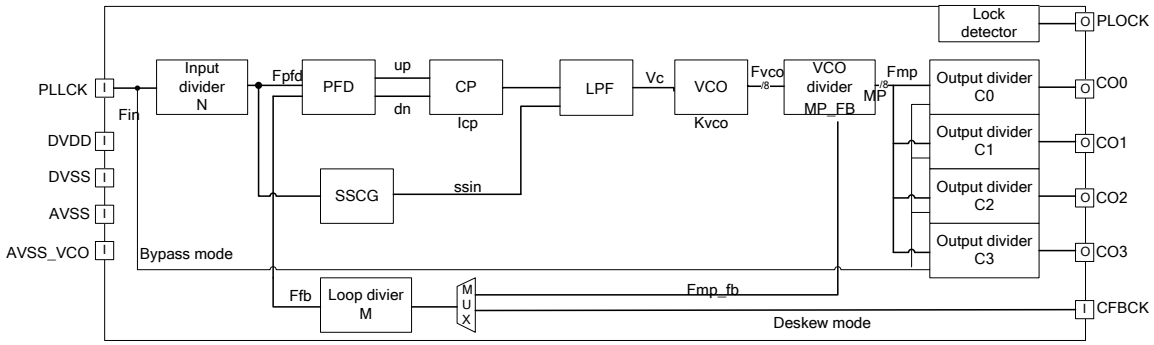


Figure 14 PLL Diagram

PLL primitive

Table 6 Port Descriptions of PLL

Port/Parameter	Type	Description
refck	Input	PLL reference clock.
cfbck	Input	Feedback clock for deskew mode.
fp_pll_pdb	Input	Power-down mode control 0: PLL power-down (default) 1: PLL work normally
CO0	Output	PLL output clock channel 0.
CO1	Output	PLL output clock channel 1.
CO2	Output	PLL output clock channel 0.

Port/Parameter	Type	Description
CO3	Output	PLL output clock channel 0.
fp_pll_lock	Output	PLL lock. 0: PLL not lock 1: PLL lock
fp_cf_shiftin	Input	PLL reconfigure serial shift in data.
fp_cf_clk	Input	PLL reconfigure clock.
fp_cf_enable	Input	PLL reconfigure enable.
fp_cf_update	Input	PLL reconfigure data update to PLL configuration register.
fp_cf_shiftout	Output	PLL reconfigure serial shift out data.

Description

This PLL is a general purpose, high-performance PLL-based clock generator. It is designed to operate with low jitter and low power consumption.

For wide output frequency range, four VCO operating ranges are provided setting by 2bits. This PLL has programmable output frequency, which ranges from 10MHz to 1250MHz configured using a 8-bit input divider (DIVN), a 8-bit feedback divider(DIVM), a 3-bit post-VCO divider (DIVMP), a 1-bit feedback-VCO divider (DIVFB) and four 8-bit output dividers (DIVCx). Around 50% duty cycle of output clocks can be achieved by enabling the output divider. It can also be used as a clock buffer through a bypass mode. A full power-down mode is also available.

There are two types operation modes: frequency synthesize and deskew modes.

Frequency synthesize Mode

The PLL's frequency synthesize mode block diagram is shown below.

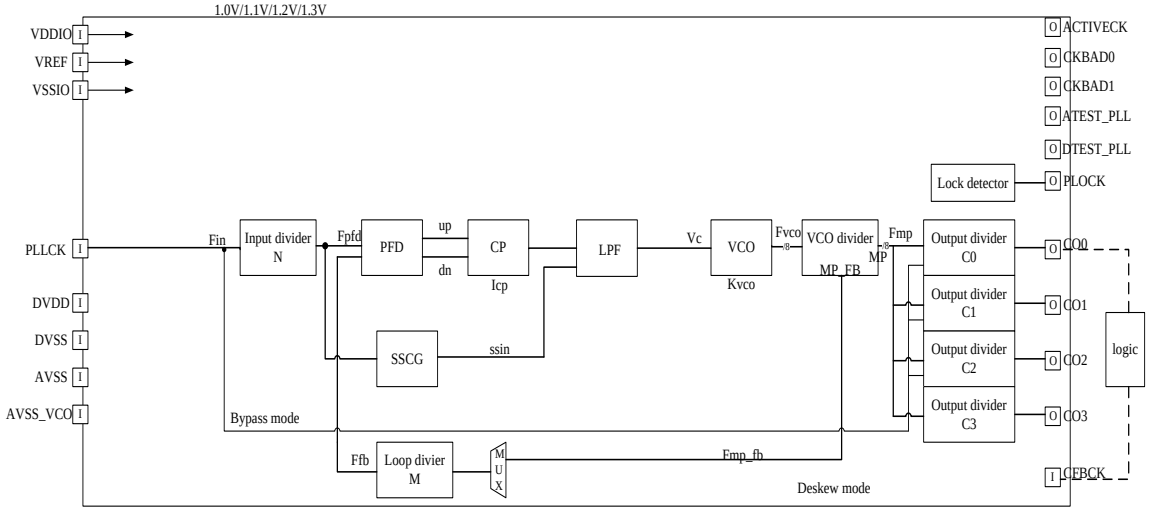


Figure 15 PLL Frequency synthesize Mode

The output clock frequency Fcon is programmable through the divider setting of DIVN[7:0], DIVM[7:0], DIVMP[2:0],DIVFB and DIVCx[7:0].

$$Fcox = Fin \cdot \frac{Nfb \cdot Nm}{Nmp \cdot Nn \cdot Ncox} \quad (x=0,1,2,3)$$

$$Fvco = Fin \cdot \frac{Nfb \cdot Nm}{Nn}$$

Input divider value Nn=DIVN[7:0]+1

Feedback divider value Nm=DIVM[7:0]+1

Feedback-VCO divider value Nfb=DIVFB+1

Output divider value Ncox=DIVCx[7:0]+1

Frequency synthesize mode provides better jitter performance because clock feedback into the PFD does not pass through as much circuitry.

Deskew Mode

The PLL's frequency deskew mode block diagram is shown below.

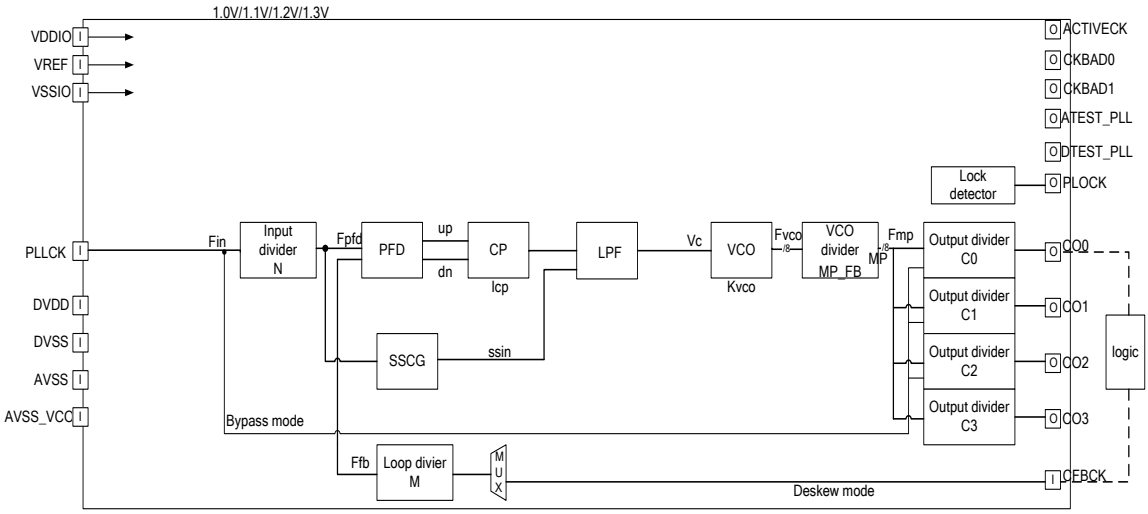


Figure 16 Deskew Mode

The PLL feedback path source is a global or regional clock network, minimizing clock delay to registers for that clock type and specific PLL output.

The output clock frequency Fcox is:

$$Fcox = Fin \cdot \frac{Nm \cdot Nco0}{Nn \cdot Ncox} \quad (x=0,1,2,3)$$

$$Fvco = Fin \cdot \frac{Nm \cdot Nmp \cdot Nco0}{Nn}$$

The PLL support up to three different deskew modes. Each mode allows clock multiplication and division, phase shifting.

Source-Synchronous Mode

If the data and clock arrive at the same time at the input pins, the phase relationship between the data and clock remains the same at the data and clock ports of any I/O element input register.

Source-synchronous mode compensates for delay of the clock network used, including any difference in the delay between the following two paths:

- **Data pin to I/O element register input**
- **Clock input pin to the PLL phase-frequency detector input**

Phase relationship between data and cock in Source-Synchronous Mode

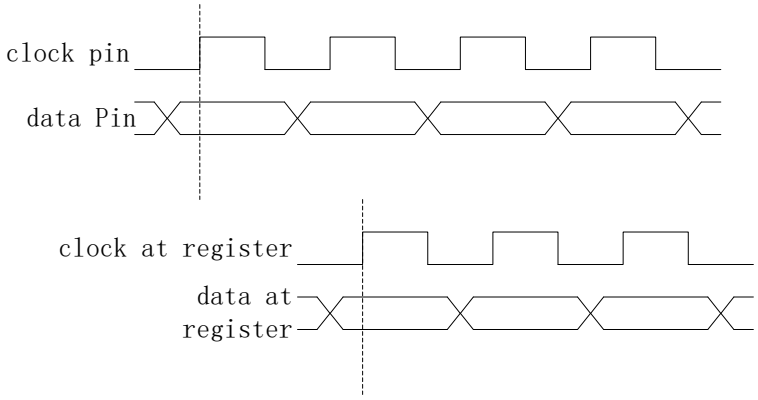


Figure 17 PLL Source-Synchronous Mode Waveform

Normal Mode

An internal clock in normal mode is phase-aligned to the input clock pin. The external clock output pin has a phase delay relative to the clock input pin if connected in this mode.

In normal mode, the PLL fully compensates the delay introduced by the clock network.

Phase Relationship clock pin Data and Clock in Normal Mode

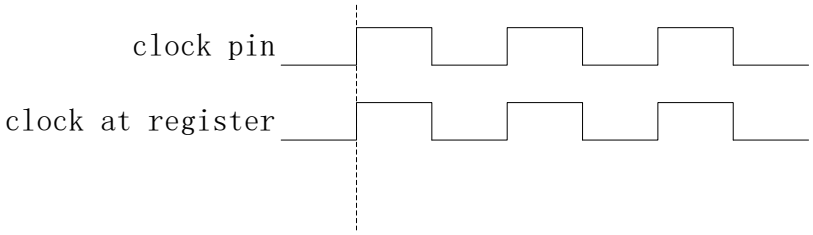


Figure 18 PLL Normal Mode Waveform

Zero Delay Buffer (ZDB) Mode

In zero delay buffer (ZDB) mode, the external clock pin is phase-aligned with the clock input pin for zero delay through the device.

When using this mode, use the same I/O standard on the input clock and output clocks to guarantee clock alignment at the input and output pins.

Phase Relationship between Data and Clock in Zero Delay Buffer (ZDB) Mode

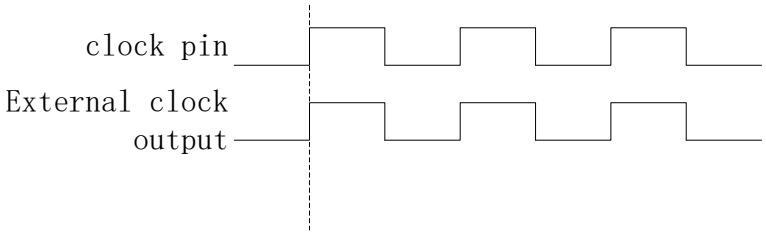


Figure 19 PLL Zero Delay Buffer Mode Waveform

Advance Mode

There are two Phase control circuit which are used to adjust the PLL out0 CO0 and LVDS clock pad to PLL feedback CFBCK paths delay. The phase control circuit is shown below. There are total 32 DLY cells in the phase control block, and one DLY cell can delay the clock 1, 2 or 3 MUX delay step. So the actual delay is delay step * fp_co0_phase. The delay scale is from min delay (1 MUX delay * 1 DLY cell + fixed delay) to max delay (3 MUX delay * 32 DLY cell + fixed delay).

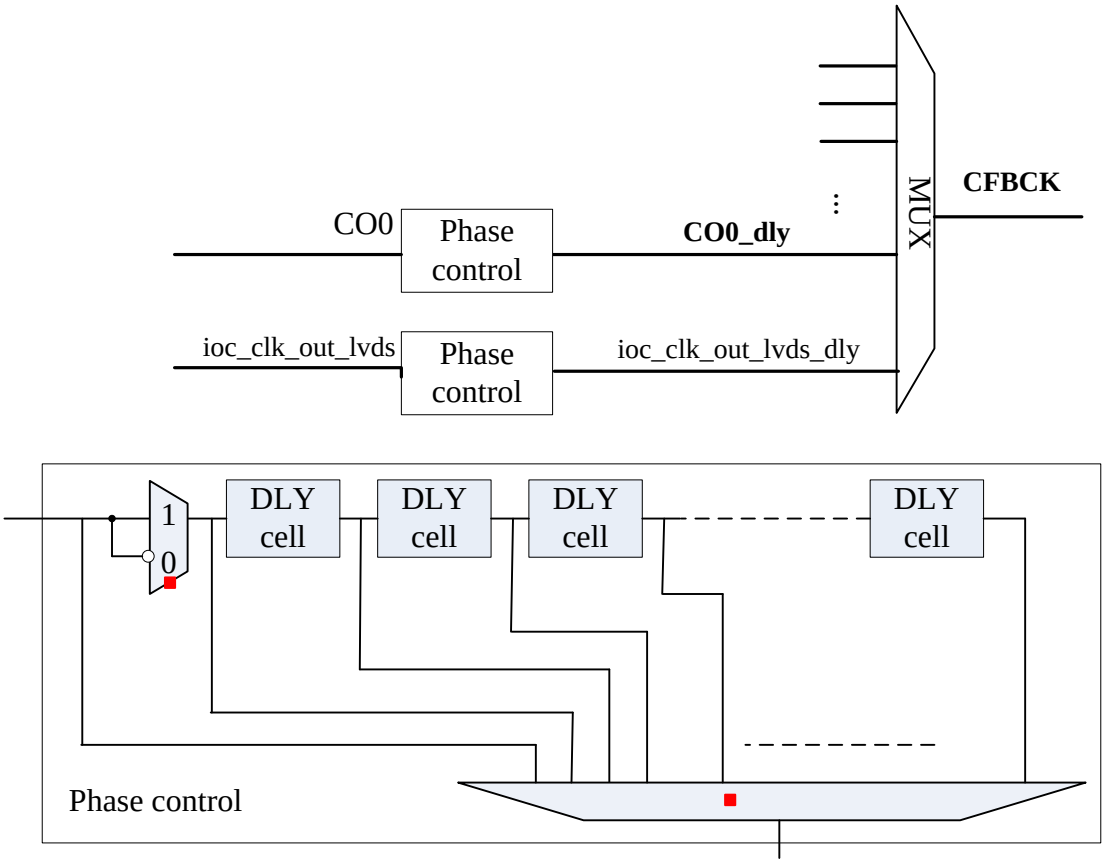


Figure 20 Phase Control Circuit

Using the PLL advance mode, user can generate the clock precisely to meet the different applications.

Bypass Mode

Fin is buffered directly to Cox, bypassing the PLL without power-down the internal loop of PLL.

Power-down Mode

The entire PLL cell is powered down internally, and Cox is set to 0. A Tlock time (pull-in and lock time) is required for the PLL to when switching from Power-down Mode to Normal Mode (Frequency synthesize Mode or Deskew Mode).

Output clock delay implementation

Output clock delay is used to implement a robust solution for clock delays. It is implemented with a combination of the VCO multi-phase outputs and the counter starting time. The VCO multi-phase outputs and counter starting time are the most accurate methods of inserting delays, because they are purely based on counter settings, which are independent of process, voltage, and temperature.

Output clock delay is consisted of fine tune and coarse tune. Fine tune using VCO multi-phase taps, and coarse tune using counter starting time.

Because the VCO is four-stage differential structure, so it has 8-phases output clock (CKvco), which frequency is Fvco. VCO-post divider divide the signal of CKvco by DIVMP[2:0] and generate 8-bit output clock of CKmp. The minimum delay time that you can insert using this method is:

$$Td\_fine = T_{mp}/8 = 1/(8*Fmp) = Nmp/(8*Fvco)$$

in which Fvco is the VCO frequency.

Coarse tune is implemented by delaying the start of the counters for a predetermined number of counter clocks. Ncox is the count value set for the counter delay time for channel x. The minimum delay time that you can insert using this method is:

$$Td\_coarse = T_{mp}*Ncox = Ncox/Fmp = (Ncox*Nmp)/Fvco \quad (Ncox \text{ is from 0 to 255})$$

So totally delay for each channel is: Tdx=Tdx_fine+Tdx_coarse.

Following Figure shows an example:

Assume DIVMP[2:0]=010, we have Fmp=Fvco/4

Assume:

MKEN0=1	BPS0=0	SELC0PHASE[2:0]=000	CO0DLY[7:0]=8'd0	DIVC0[7:0]=8'd1
MKEN1=1	BPS1=0	SELC1PHASE[2:0]=001	CO1DLY[7:0]=8'd0	DIVC1[7:0]=8'd1
MKEN2=1	BPS2=0	SELC2PHASE[2:0]=000	CO2DLY[7:0]=8'd1	DIVC2[7:0]=8'd1
MKEN3=1	BPS3=0	SELC3PHASE[2:0]=001	CO3DLY[7:0]=8'd1	DIVC3[7:0]=8'd1

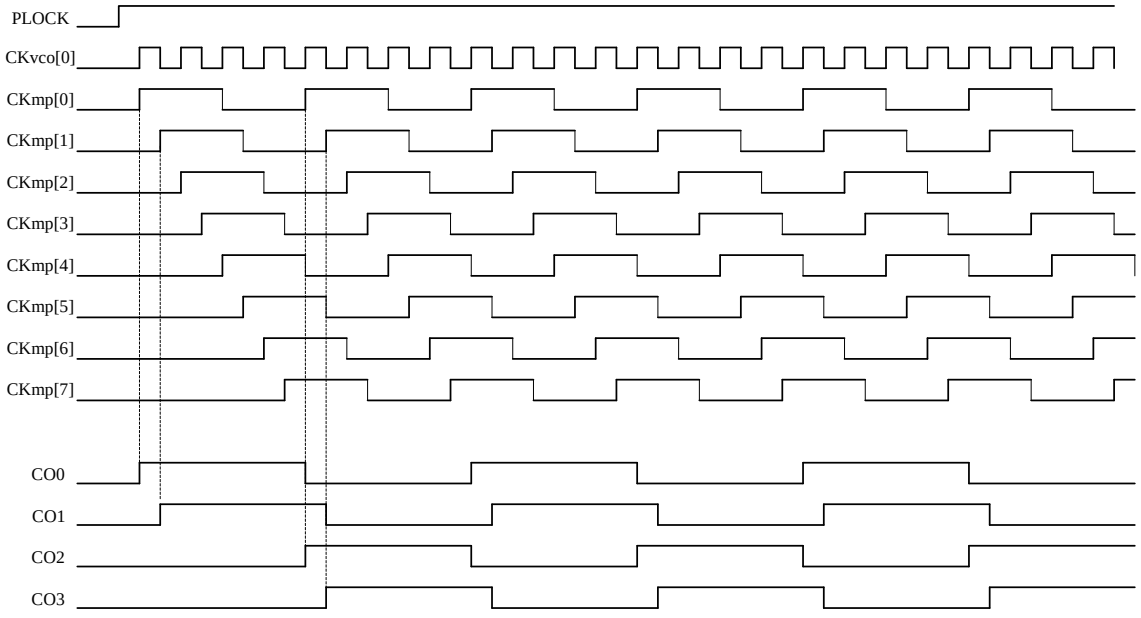


Figure 21 PLL Output Phase Waveform

PLL Reconfiguration

HME-HR PLLs can reconfigure input divider value, feedback divider, feedback-VCO divider and output divider settings perform frequency synthesis to change the PLL output clock in real time.

The ability to reconfigure the PLL in real time is useful in applications that operate at multiple frequencies. It is also useful in prototyping environments, allowing you to sweep PLL output frequencies dynamically. For example, a system generating test patterns is required to generate and transmit patterns at 75 or 150 MHz, depending on the requirements of the device under test. Reconfiguring the PLL components

in real time allows you to switch between two such output frequencies within a few microseconds. This approach eliminates the need to regenerate a configuration file with the new PLL settings.

The primitive CFG_DYN_SWITCH h is used to implement the clock dynamic switching in system.

Table 7 PLL Reconfiguration Port

Port Name	Type	Description
fp_cf_clk	Input	Reconfiguration input clock.
fp_cf_enable	Input	Reconfiguration enable, high active.
fp_cf_shiftin	input	Reconfiguration serial input data.
fp_cf_update	input	Update all the reconfiguration data to PLL
fp_cf_shiftout	Output	PLL reconfiguration serial output data.

Table 8 PLL reconfiguration bit definition

Bit	Map	Description
[0]	PLL_DIVFB	VCO-post divider control for feedback path 0: divide by 1 (default) 1: divide by 2
[3:1]	PLL_DIVMP[2:0]	VCO post divider control for output path 000: divide by 1 (default) 001: divide by 2 010: divide by 4 011: divide by 8 100~111: divider by 16
[11:4]	PLL_DIVC3[7:0]	Output divider control for channel 3, range within[1,256] Input divider value C0=DIVC0<7:0>+1
[19:12]	PLL_DIVC2[7:0]	Output divider control for channel 2, range within[1,256] Input divider value C0=DIVC0<7:0>+1
[27:20]	PLL_DIVC1[7:0]	Output divider control for channel 1, range within[1,256] Input divider value C0=DIVC0<7:0>+1
[35:28]	PLL_DIVC0[7:0]	Output divider control for channel 0, range within[1,256] Input divider value C0=DIVC0<7:0>+1
[43:36]	PLL_DIVM[7:0]	Loop divider control, range within[1,256] Input divider value M=DIVM<7:0>+1
[51:44]	PLL_DIVN[7:0]	nput divider control, range within[1,256] Input divider value N=DIVN<7:0>+1
[52]	LKDCK	
[54:53]	PLL_KVSEL[1:0]	VCO output frequency range select 00: 600M~800M 01: 800M~1000M 10: 1000M~1200M 11: >1200M (default)
[57:55]	PLL_CPSEL_FN[2:0]	Select Charge pump current, fine tune 000: Icoarse*1/8 001: Icoarse*2/8 010: Icoarse*3/8 011: Icoarse*4/8 100: Icoarse*58 (default) 101: Icoarse*6/8 110: Icoarse*7/8 111: Icoarse*8/8
[59:58]	PLL_CPSEL_CR[1:0]	Select Charge pump current, coarse tune 00: 1.56u 01: 6.25u (default) 10: 14.1u 11: 25u

Bit	Map	Description
[61:60]	PLL_LPF[1:0]	Loop filter resistance value adjustment 00: 5.8KOhm 01: 7.8KOhm 10: 11.8KOhm (default) 11: 21.5KOhm

Use the following procedure to reconfigure the PLL dividers:

1). Make fp_cf_enable active to high, the first bit of scandata(Dn).

2). Shif the serial data(fp_cf_shiftin) at the rising edge follow from the the [61] bit, the second is fp_cf_clk is shifted into the scan chain on the second rising edge of scanclk.

3). After all 234 bits (Top/Bottom PLLs) or 180 bits (Left/Right PLLs) have been scanned into the scan chain, the scanclkenasignal is de-asserted to prevent inadvertent shifting of bits in the scan chain.

4). The configupdatesignal is asserted for one scanclkcycle to update the PLL counters with the contents of the scan chain.

5). The scandonesignal goes high indicating the PLL is being reconfigured. A falling edge indicates the PLL counters have been updated with new settings.

6). Reset the PLL using the aresetsignal if you make any changes to the M, N,or post-scale C counters or the Icp, R, or C settings.

7). Steps 1 through 5 can be repeated to reconfigure the PLL any number of times.

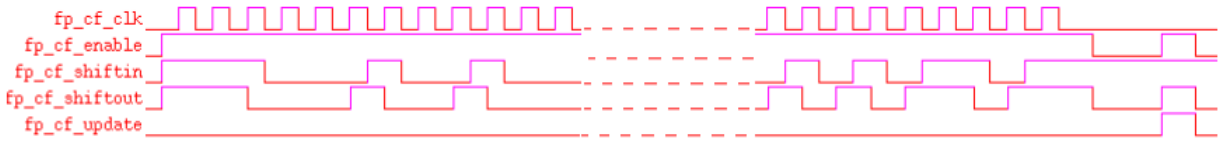


Figure 22 PLL Reconfiguration Waveform

Oscillator (OSC)

HR has a on chip oscillator which can be used for configuration and user design.

Features

- **Operation power: 1.1V core power, 2.5V or 3.3V IO power**
- **16 frequency levels for user select, range : 2.39MHz~131.4MHz**
- **Frequency accuracy (for PVT): ±20%**
- **Duty cycle: 50%±5%**
- **Power-down mode**
- **Standby mode**

Block Diagram

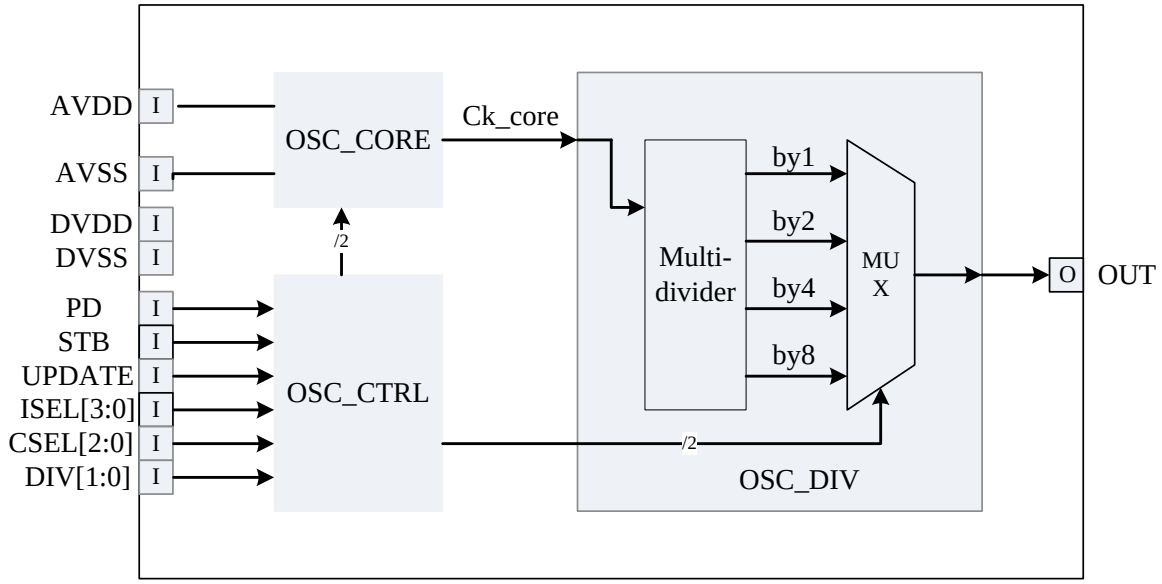


Figure 23 OSC Diagram

Description

A user-programmable internal oscillator is included on chip. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the system clock PLL using general routing resources. The oscillator frequency ranges from 2.39 MHz to 131.4 MHz for 3.3V IO power supply.

The on-chip oscillator has two power saving features. Power down mode will turn off all the device. Standby mode will turn on the io device and turn off the most core device, it can reduce the stable time in this way.

Table 9 Oscillator frequencies list and setting

No.	Control bit				Oscillator frequencies (MHz)	
	ISEL[1]	ISEL[0]	DIV[1]	DIV[0]	For 3.3V io power	For 2.5V io power
1	0	0	1	1	**2.39**	2.30
2	0	0	1	0	**4.78**	4.60
3	0	1	1	1	**6.76**	6.52
4	0	0	0	1	**9.55**	9.20
5	1	0	1	1	**10.81**	10.43
6	0	1	1	0	**13.52**	13.03
7	1	1	1	1	**16.43**	15.88
8	0	0	0	0	**19.10 (default)**	18.39 (default)
9	1	0	1	0	**21.62**	20.86
10	0	1	0	1	**27.04**	26.06
11	1	1	1	0	**32.85**	31.75
12	1	0	0	1	**43.24**	41.72
13	0	1	0	0	**54.08**	52.13
14	1	1	0	1	**65.70**	63.50
15	1	0	0	0	**86.49**	83.45

No.	Control bit				Oscillator frequencies (MHz)	
	ISEL[1]	ISEL[0]	DIV[1]	DIV[0]	For 3.3V io power	For 2.5V io power
16	1	1	0	0	**131.40**	127.00

Clock Management Block

Each HME-HR FPGA has four Clock Management Blocks (CMBs), each consisting of one PLL, one DLL and one Clock Switcher. The CMB's clock inputs can from Each CMB can generate four global clocks, 4 CMBs generate 16 global clock(GCLK[15:0]) low-capacitances, low-skew interconnect global clock lines for PLBs, IOBs, EMBs, DSPs, SRAM, AHB bus, peripherals and ARM core. These clock lines well-suited to carrying high-frequency signals throughout the FPGA, minimizing clock skew and improving performance, and should be used for all clock signals and also can be used for high-fanout signals.

Global Clock Diagram

The PLL's clock input sources are listed below:

- **Dedicated clock pin(clk[3:0]): There are two groups clk[3:0] which are hard connected the four CMBs.**
- **XTAL: external crystal input**
- **FP signals**
- **Other CMB's global clock output**

The DLL's clock input sources are listed below:

- **Dedicated clock pin(clk[3:0]): There are two groups clk[3:0] which are hard connected the four CMBs.**
- **PLL's output**
- **FP signals**
- **Other CMB's global clock output**

Each CMB outputs 4 global clocks to global clock tree from clk[3:0], PLL and DLL outputs and FP signals, so there are total 16 global clocks .

Clocks from the clock generators are distributed to the GBUFs in a skew-balanced tree. LBUFs are the last stage in the clock tree. They directly drive the flipflops. LBUFs provide local, precise clock gating.

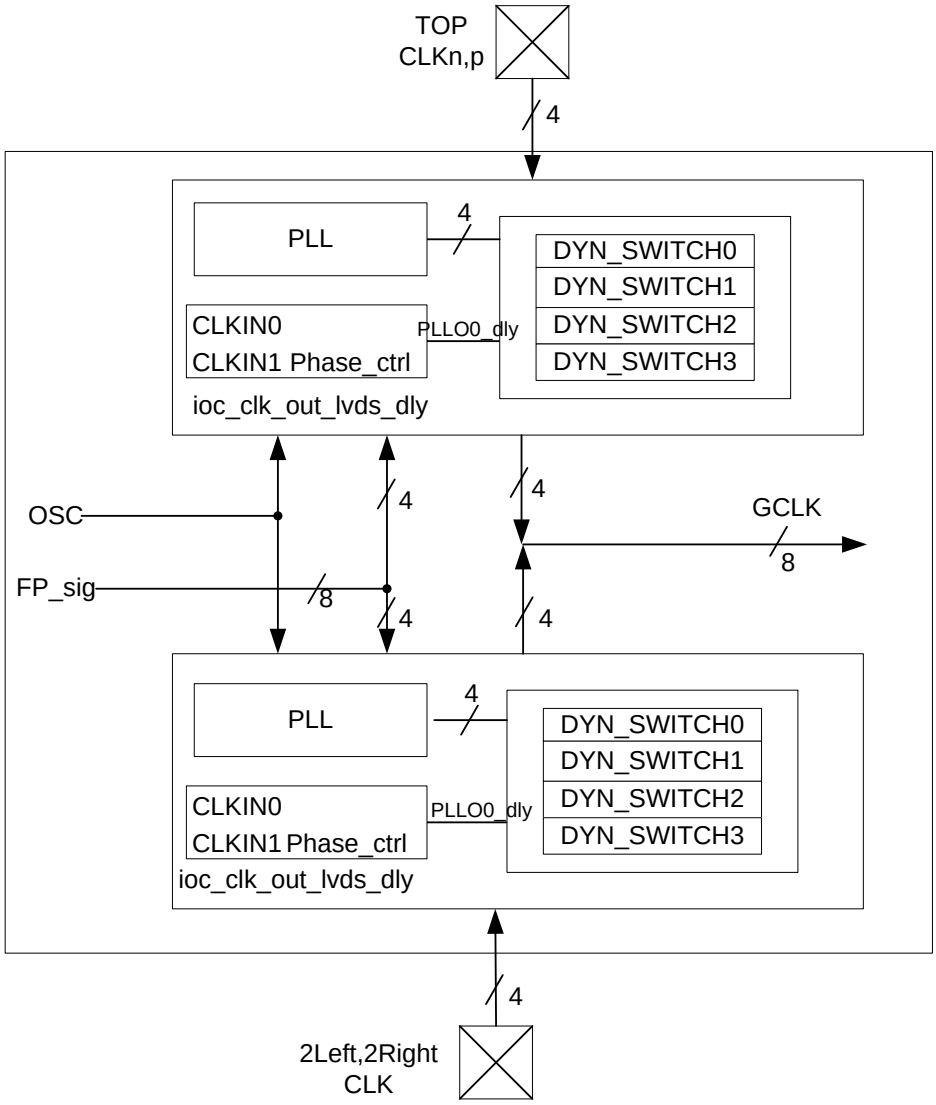


Figure 24 Clock Diagram

GBUF

The GBUF that is generated by the Wizard allows a clock or general signal to enter the Global Clock Network directly.

Table 10 GBUF port definition

Port Name	Type	Description
in	Input	GBUF input
out	Output	GBUF clock output

HR is designed with two gated global clocks that can be easily controlled by using GBUF_GATE.

Table 11 GBUF_GATE port definition

Port Name	Type	Description
clk	Input	Clock input
en	Input	Clock enable, high active
clk_out	Output	GBUF clock output

LBUF

The LBUF that is generated by the Wizard allows a clock or general signal to enter the local clock network directly.

Table 12 LBUF port definition

Port Name	Type	Description
in	Input	LBUF input
out	Output	LBUF clock output

Clock Switch

One CMB has four deglitch CFG_DYN_SWITCH multiplexers. Each of the four CFG_DYN_SWITCH multiplexer generates a gclk clock. The CFG_DYN_SWITCH multiplexer not only can be used as a static clock path but also can provide seamless clock dynamic switchover between two clock sources in system, for both startup sequencing and entering and exiting low-power operating modes.

The primitive CFG_DYN_SWITCH h is used to implement the clock dynamic switching in system.

Table 13 CFG_DYN_SWITCH Port Definition

Port Name	Type	Description
in0	Input	GCLK clock source 0 input.
in1	Input	GCLK clock source 1 input.
out	Output	Global clock to GBUF.
fp_sel	input	Clock source select, 0: in0; 1: input1

Table 14 Parameter Descriptions of CFG_DYN_SWITCH

Port Name	Type	Description
gclk_mux	digital	Define the CFG_DYN_SWITCH location.
SEL	Bit	Must be 111 if the primitive is be used

Table 15 Clock Routability Table

GCLK	IN0				IN1			
GCLK[0]/ gclk_mux 0	PLLO0	PLLO1	osc	CLK0	PLLO2	PLLO3	CLK1	FP
GCLK[1]/ gclk_mux 1	PLLO1	PLLO3	osc	CLK1	PLLO3	PLLO0	CLK2	FP
GCLK[2]/ gclk_mux 2	PLLO2	PLLO3	osc	CLK2	PLLO0	PLLO1	CLK3	FP
GCLK[3]/ gclk_mux 3	PLLO3	PLLO0_ DLY	osc	CLK3	PLLO1	PLLO2	DLL0	FP

For each of the four GCLK, the CFG_DYN_SWITCH input in0 and in1 only can be fed as the table. The PLL and LVDS IO clock phase delay out to the input0 and input1 must come from the same clock generator.

This part lists the Configuration and Debug data for users to quickly search.

3. Configuration and Debug

HME-HR devices are configured by loading application-specific configuration data (the Bitstream) into internal memory. HME devices must be configured each time when they are powered-up because their configuration memory are volatile.

Configuration Modes and Pins

The bitstream is loaded into the device through special configuration pins. These configuration pins serve as the interface for a number of different configuration modes:

There are 3 configuration modes: JTAG, AS and PS mode which are defined by two dedicated JM_B and SS pins. The two pins values are latched for mode selection when the devices are power on or reset. The configuration modes are described in table below.

Table 16 Configuration Mode

Mode pin		Mode	Description
JM_B	SS		
X	1	AS	Active Serial mode. The chip will be configured automatically. Configuration data is stored in the SPI flash.
X	0	PS	Chip acts as slave. External microcontroller feeds configuration data into the chip.
0	X	JTAG	JTAG-based configuration. This mode takes high privilege over AS and PS modes.
1	X	AS/PS	JTAG can't configure the HME-HR.

Table 17 Configuration Pins

SPI serial configuration Pins		
SCLK	Input/output	In passive serial configuration mode, SCLK is a clock input used to clock configuration data from external device source into device. In active serial configuration mode, SCLK is a clock output from device. The pin can be used as regular user I/Os after configuration.
SDI	output	Dedicated configuration data output pin in AS mode. No configuration function in PS mode. The pin can be used as regular user I/Os after configuration in AS mode
SDO	Input	Serial data input from external master in PS mode or from spi flash in AS mode. The pin can be used as regular user I/Os after configuration.

SPI serial configuration Pins		
SS	output or input	Chip select output to enable a SPI Flash in AS mode or input as a HME device select. This output is used during AS mode. The pin can be used as regular user I/Os after configuration in AS mode. it is used as chip selection control (input) during PS.The pin can be used as regular user I/Os after configuration in PS mode. The pin value will be latched for mode selection when the devices are power on or reset. 1:Active Serial mode, 0: Passive Serial mode
Dedicated Configuration Pins:		
CFGDONE	output	This is a dedicated configuration status pin, the pin will output high during configuration. The pin can be used as regular user I/Os after configuration.
nCONFIG	input	Chip global reset input. Active low.
Dedicated Pins: JTAG		
JM_B	input	The pin value will be latched for mode selection when the devices are power on or reset. 1: TCK/TDI/TDO/TMS pins are no JTAG functions, only user I/Os. 0: TCK/TDI/TDO/TMS pins are only used as JTAG functions.
TCK	input	TCK Input Boundary-Scan Clock.
TDI	input	TDI Input Boundary-Scan Data Input.
TDO	output	TDO Output Boundary-Scan Data Output.
TMS	input	TMS Input Boundary-Scan Mode Select.

Configuration Process

The whole configuration process includes these procedure:

- **Power Up**
- **Reset**
- **Initialization**
- **Configuration**
- **User Mode**

If the device is powered up from the power-down state, VDD_CORE, VDDIO_33 (for the I/O banks in which the configuration and JTAG pins reside) must be powered up to the appropriate level for the device to exit from POR.

After power up, HR devices go through POR. During POR, the device resets, holds CFGDONE low, and tri-states all user I/O pins. When the device exits POR, all user I/O pins continue to tri-state. While nCONFIGis low, the device is in reset. When nCONFIG goes high, the device enters the initialization step. In HR devices, the initialization clock source is the internal oscillator. The device provides itself with enough clock cycles for proper initialization to clear the configuration memory.

When the initialization is finished, the device is ready to receive configuration data and the configuration

stage starts. The total configuration clock number is about 693146. After the configuration data is accepted and CFGDONE goes high, HR and enter user mode.

The POR circuit has the following features:

- **Power up/down monitor, trigger point:**
  - VDD_CORE: 0. 8V
  - VDDIO_33: 1.86V
- **The rising time range of VDD_CORE and VDDIO_X is from 200ns to 1s**

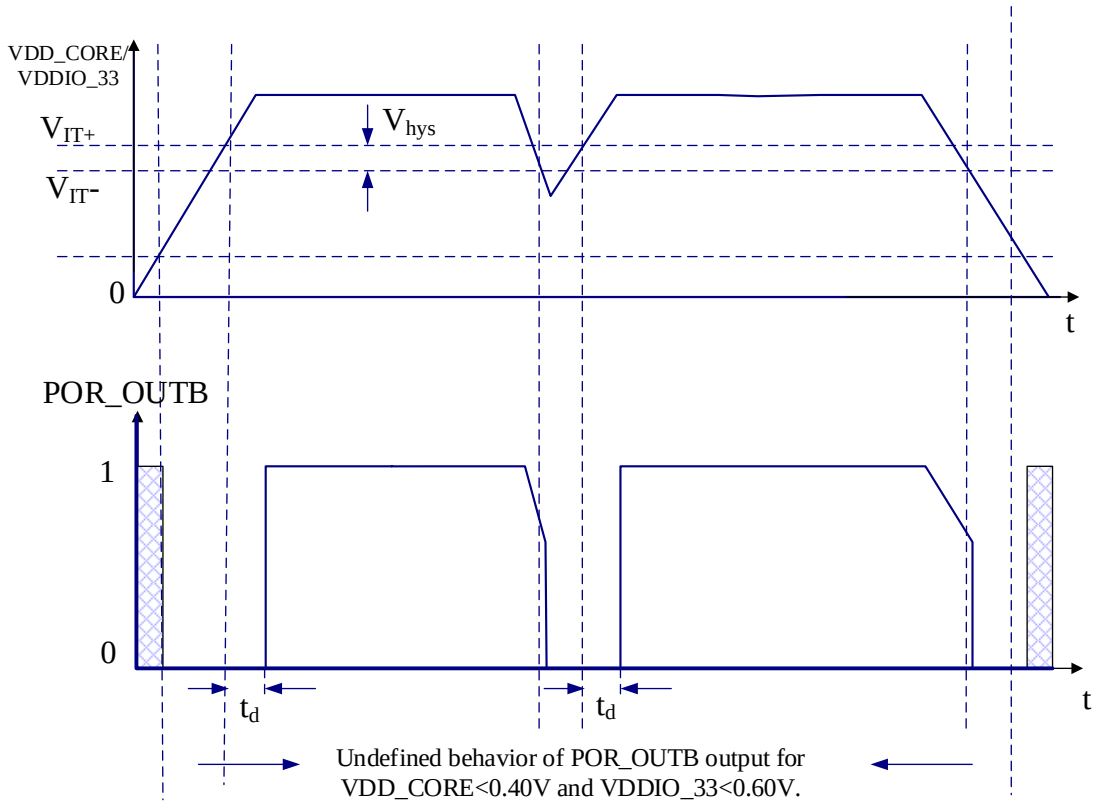


Figure 25 POR waveform

Caution: VDD_CORE must reach the trigger point voltage before the VDDIO_33.

Configuration Scheme

AS Mode

HME download cable can operate the SPI Flash by the JTAG indirectly.

The following figure describes the AS configuration scheme using JTAG indirectly.

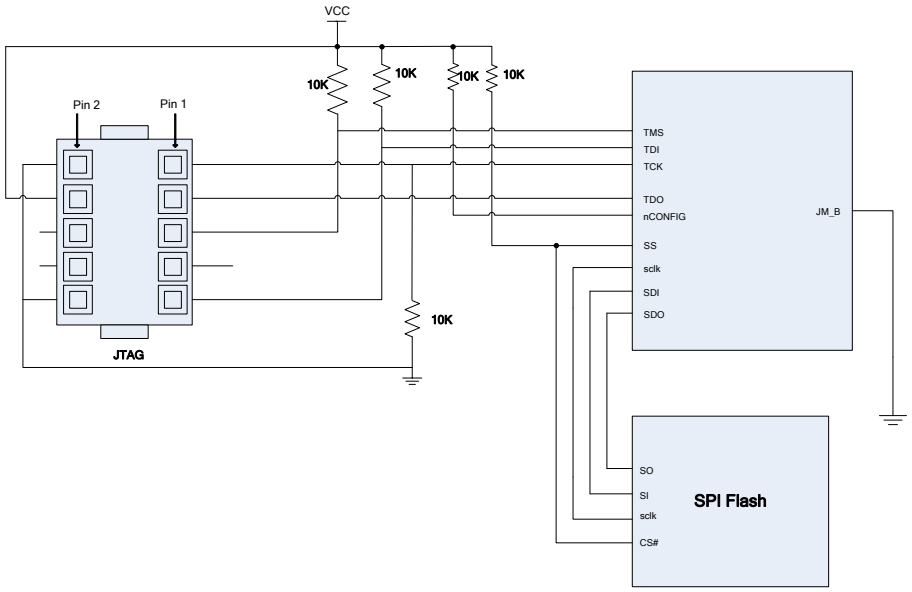


Figure 26 AS Configuration using JTAG

PS Mode

In the PS mode, HME-HR family works as slave device, receive configuration data from external master controller passively. SPI Master can't read configuration data from HME-HR family, so the PS master or HME cable can't operate the HR's embedded Efuse which must be programmed by JTAG.

The figure below describes HME-HR family in PS configuration.

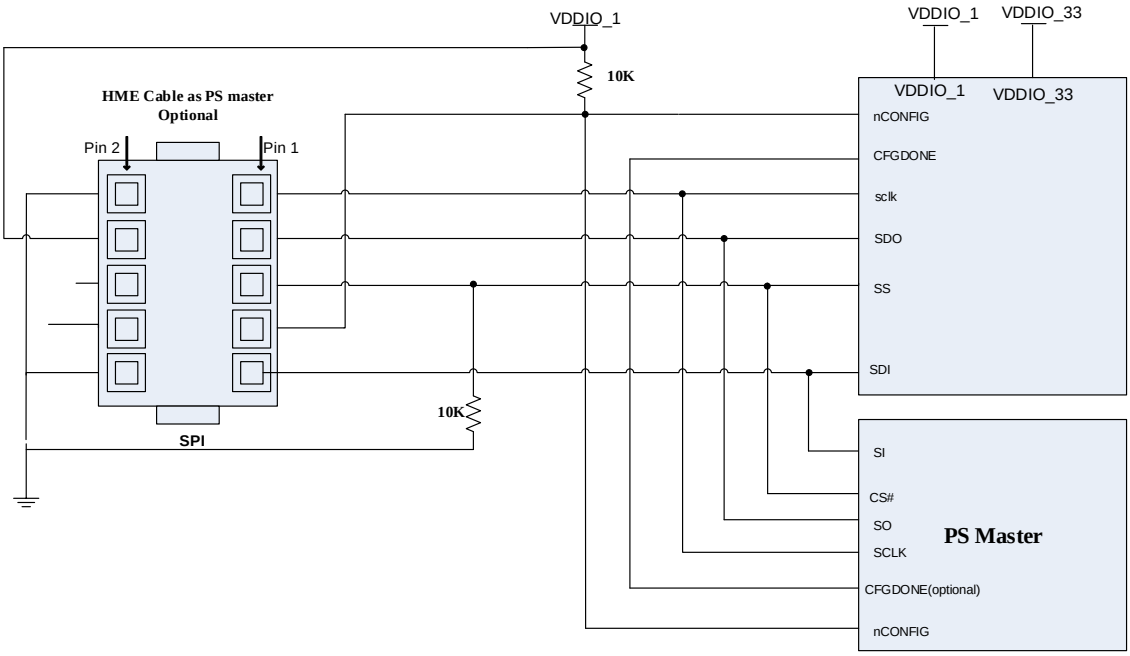


Figure 27 PS Configuration

JTAG Mode

There are two JTAG devices inside HME-HR family for fabric debugging and configuration.

JTAG interface can access and debug configuration and program HR's embedded Efuse.

The figure below describes HME-HR family in JTAG configuration.

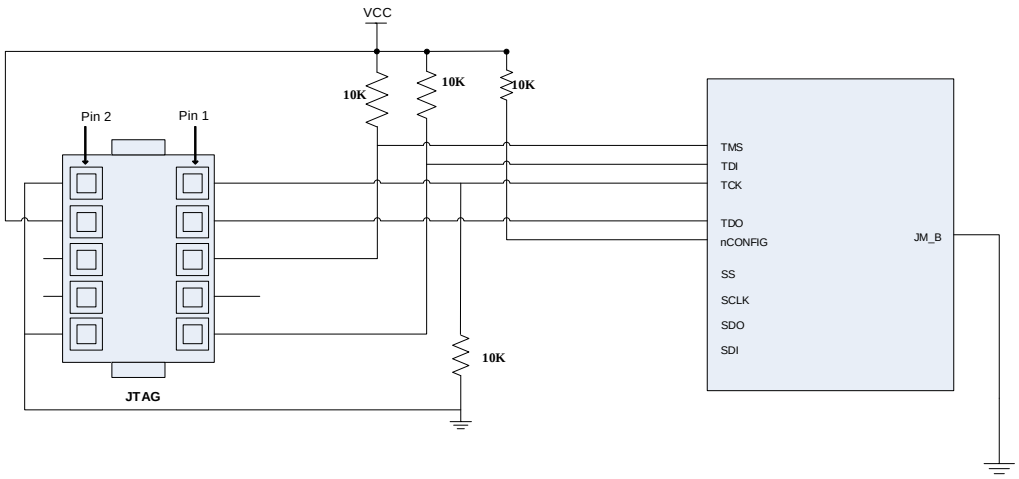


Figure 28 JTAG Configuration

eFUSE

HME-HR has one 256 bit eFUSE which is a One Time Program electrically programmable fuses memory. The eFuse can store the 128 bit AES key for bitstream decryption and other setting data for user.

Using Fuxi tool E-Fuse Burner can program the eFUSE via HME download cable.

The eFUSE can support program, compare operations, to see the HME-HR_Configuraiton_User_Guide_EN for detail description.

eFUSE field description

Table 18 eFUSE field

Bit	Description
Reserved region	
255:248	Crc check for reserved region
247:182	Reserved
181:166	User can program by JTAG and get the content from the efuse_idx16 primitive.
165	efuse_lock_bit, user can program the bit. 0: efuse can program 1: efuse is locked and can't be programmed.
164	Secure_efuse_aes, user can program the bit. 0: Disable the AES. 1: Enable the AES.

163	Reserved
162	Secure_efuse_jtag, user can program the bit. 0: JTAG can access the HR device. 1: JTAG can't access the HR device.
161:160	Reserved
159:152	Crc check for user low region
151:129	Reserved
128	User_efuse_lock_bit_low
127:0	AES key[127:0]

Table 19 Efuse Primitive efuse_idx16 Description

Port name	Type	Description
out[15:0]	Output	16 bit user output. The out[15:0] = above table effuse content[181:166].

AES Security

Advanced Encryption Standard (AES) is a specification for the encryption of electronic data. The AES algorithm is adopted to encrypt the configuration bitstream using a 128-bit key. The HME-HR family will decrypt the encrypted bitstream using the 128-bit key which is stored in Efuse. The configuration will success if the two 128-bit keys are matching, otherwise the configuration will fail and the device can't work.

The encryption and decryption process is shown in figure below.

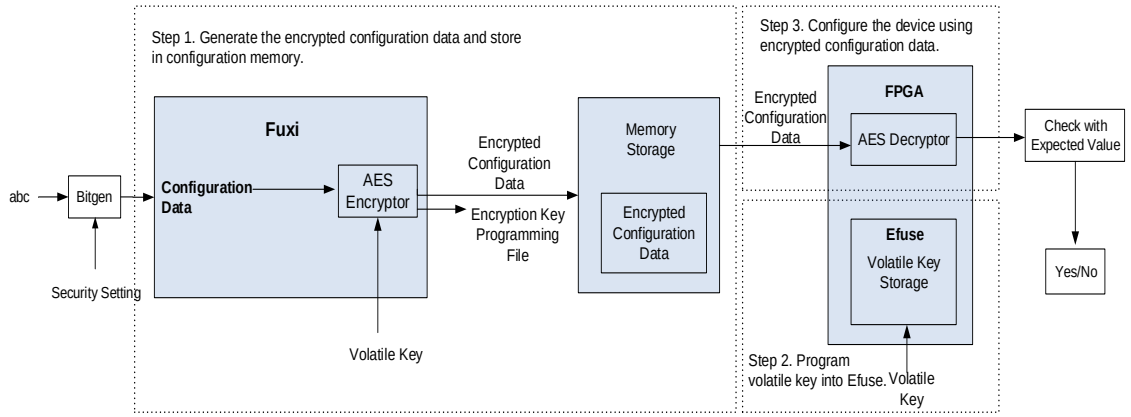


Figure 29 Encryption and Decryption Process

4. DC & Switching Characteristics

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **The following applies unless otherwise noted: AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.** All parameters representing voltages are measured with respect to GND.

DC Electrical Characteristics

Absolute Maximum Ratings

Stresses beyond those listed under

Table 20: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 20 Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Max	Units
VDD_CORE	Internal supply voltage		-0.5	1.3	V
VDDIO_X	I/O driver supply voltage		-0.5	3.63	V
VDDIO_33/25	JTAG/Flash/ Bank2 IO Power		-0.5	3.63	V
VDD_PLL	PLL power		-0.5	3.63	V
VIN	Voltage applied to all User I/O pins and dual-purpose pins	Driver in a high-impedance state	-0.95		V
	Voltage applied to all Dedicated pins		-0.8		V
VESD	Electrostatic Discharge Voltage	Human body model	0	±2000	V
		Charged device model	-	±500	V
		Machine model	-	±200	V
TJ	Junction temperature		-40	100	°C
TSTG	Storage temperature		–65	150	°C

Power Supply Specifications

Table 21 Supply Voltage Thresholds for Power-On Reset

Symbol	Description	Min	Max	Units
VDD_CORET	Threshold for the VDD_CORE supply	0.81		V
VDDIO_33T	Threshold for the VDDIO_X supply	1.91		V

Table 22 Supply Voltage Ramp Rate

Symbol	Description	Min	Max	Units
TVDD_CORET	Ramp rate from GND to valid VDD_CORE supply level	1		us
TVDDIOR	Ramp rate from GND to valid VDDIO_X supply level	1		us

Notes: The VDD_CORE must be powered to the threshold before the VCCIO.

General Recommended Operating Conditions

Table 23 Recommended Basic Operating Conditions

Symbol	Parameter	Min	Typ	Max
TJ	Junction temperature	-40°C	25°C	125°C
VDD_CORE	Core power	1.045V	1.1V	1. 155V
VDDQ	eFuse program power	2.25V	2.5V	2.75V
VDDIO_X	I/O supply voltage @ 3.3V	3.135V	3.3V	3.465V
	@2.5V	2.375V	2.5V	2.625V
	@1.8V	1.71V	1.8V	1.89V
	@1.5V	1.425V	1.5V	1.575V
VDDIO_33/25	JTAG/FLASH power	3.135V/ 2.375V	3.3V/ 2.5V	3.465V/ 2.625V
VDD_PLL	PLL power	3.135V	3.3V	3.465V
V_I	Input Voltage	-0.5	-	VDDIO_X +0.3
V_O	Output Voltage	-0.3	-	VDDIO_X
I_L	Input Leakage Current	±1μA		

General DC Characteristics for I/O Pins

Table 24 I/O Pin Leakage Current

Symbol	Parameter	Min	Typ	Max
I_{oz}	Tristated I/O pin leakage Current	-10uA	-	10uA
I_L	Input Leakage Current	-10uA	-	10uA
I_{CL}	VCC core leakage current		37uA	

Table 25 Single-ended I/O Pin Driving Strength

Supported Voltage and Current Capabilities	Attributes	Value
Drive strength	I/O supply voltage @ 3.3V	4mA
		8mA
		12mA
		16mA
	I/O supply voltage @ 2.5V	4mA
		8mA
		12mA
		16mA
	I/O supply voltage @ 1.8V	2mA
		4mA
		8mA
		12mA
	I/O supply voltage @ 1.5V	2mA
		4mA
		8mA

Note: All IOs support single-ended IO standards, such as LVCMOS. Measured between 10% and 90% VDDIO_X.

Table 26 Single-ended I/O Pull-Up and Pull-Down Resistor

Symbol	Parameter	Min	Typ	Max	Units
R_{PU}	Value of the I/O pin pull-up resistor		70		kΩ
R_{PD}	Value of the I/O pin pull-down resistor		50		kΩ

I/O Standard Specifications

Table 27 Single-ended I/O Standard Input DC Specifications

I/O Standard	VDDIO_X (V)			Vref (V)			Vil (V)	Vih (V)
	Min	Typ	Max	Min	Typ	Max	Max	Min
3.3V LVTTL and LVCMOS	3.135V	3.3	3.465V	-	-	-	0.8	2
2.5V LVTTL and LVCMOS	2.375V	2.5	2.625V	-	-	-	0.7	1.7
1.8V LVTTL and LVCMOS	1.71V	1.8	1.89V	-	-	-	0.35 x VDDIO_X	0.65 x VDDIO_X
1.5V LVCMOS	1.425V	1.5	1.575V	-	-	-	0.35 x VDDIO_X	0.65 x VDDIO_X

Table 28 Single-ended I/O Standard Output DC Specifications

I/O Standard	Test Conditions		Voltage Threshold	
	Iol (mA)	Ioh (mA)	Maximum Vol (V)	Minimum Voh (V)
3.3V LVTTL			0.4	2.4
3.3V LVCMOS			0.4	VDDIO_X – 0.5
2.5V LVTTL and LVCMOS			0.4	2.1
1.8V LVTTL and LVCMOS			0.45	VDDIO_X – 0.5
1.5V LVTTL and LVCMOS			0.375	VDDIO_X – 0.4

Table 29 Differential I/O Standard Input DC Specifications

I/O Standard	Vccio (V)			Vid (V)			Vicm (V)			Vinp (input voltage)	
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
LVDS	2.375	2.5	2.625	0.25	0.35	0.45	Vccio/2-0.3	Vccio/2	Vccio/2+0.3	0	2.5
subLVDS	1.71	1.8	1.89	0.1	0.15	0.2	Vccio/2-0.25	Vccio/2	Vccio/2+0.25	0	1.8

Table 30 Differential I/O Standard Output DC Specifications

I/O Standard	Vod (mV)			Delta(Vod) (mV)		Vocm (V)			Voh (V)		Vol (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max
LVDS		300					1.25					
subLVDS		350					0.9					

Switching Characteristics

Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics.

Clock Performance

Table 31 Global Clock Performance

Symbol	Max Frequency	Units
GCLK	400	MHz

PLL Specifications

Table 32 PLL Specifications

Symbol	Description	Min	Typ	Max	Unit
REFCK	Input clock freq.	5		133	MHz
Fpfd	PFD input freq.	5		133	MHz
Fout	Output freq.	16		400	MHz
Fvco	VCO operation freq.	533		1066	MHz
Tlock	Lock time			100	us

Symbol	Description	Min	Typ	Max	Unit
Duty	Output clock duty cycle	45	50	55	%
N	Input divider	1		256	--
M	Loop divider	1		256	--
MP *1	VCO post divider	1		16 *1	--
C0~C3	Output divider	1		256	--
Ntmp	Output clock delay	1		256	--
Terr	Static phase error	-10		10	Degree
Ivddpll	power consumption		14*2		mA
Trst	Pulse width on reset signal	20			us
Ipd	Total power-down current		150		nA
Ibp *2	Total bypass current		300		nA
Tmux	Phase control Delay cell 1 MUX delay	0.15	0.2	0.25	ns
Tfixed	Phase control input to CFBCK delay except the MUXs	2.4	2.45	2.5	ns

Note *1: The value of VCO post divider MP is 1,2,4,8 and 16

Note *2: test under VCO = 1066MHz, 4 channel output=66MHz

OSC Specifications

Table 33 OSC Specifications

Symbol	Description	Min	Typ	Max	Unit
Fout	Output clock freq.	2.39		131.4	MHz
T_{dt}	Output clock duty cycle	45	50	55	%
Ivddc	Power consumption for core power			108	uA
Ivddosc	Power consumption for high voltage		40.2		uA
Ipd	Total power-down current			1	uA
Tjit	Jitter performance		0.1		UIPP
Tstalbe_pup	PD low to OSC stable			0.5	us
Tstalbe_stb	STB low to OSC stable			0.2	us

I/O Timing

Table 34 Single-Ended I/O Performance

IO Standard	Primary Usage	Driving Strength	Max Frequency
	3.3v general purpose	16mA	250MHz
	2.5v general purpose	16mA	250MHz
	1.8v general purpose	12mA	155MHz
	1.5v general purpose	8mA	155MHz

Table 35 Differential IO target working frequency

IO standard	Primary usage	Frequency requirement
LVDS TX	2.5v	400 MHz
	1.8v	300 MHz
LVDS RX	2.5v	400 MHz
	1.8v	300 MHz

LP Timing

Table 36 LP Timing

Symbol	Description	Min	Max	Units
tco	When reading from the Flip-Flop, the time from the active transition at the CLK input to data appearing at the QS (QX) output	446	497	ps
tsu	Time from the setup of data at the LUT input to the active transition at the CLK input of the Reg	7	989	ps
th	Time from the active transition at the CLK input to the point where data is last held at the input	-878	177	ps
tp	The time it takes for data to travel from the LP's Flip-Flop input to the output	68	1062	ps

PLB Performance

Table 37 PLB Performance

Symbol	Description	Min	Max	Units
ADD16	16 bit adder performance @ recommended operating condition.		225	MHz
ADD32	32 bit adder performance @ recommended operating condition.		210	MHz
ADD64	64 bit adder performance @ recommended operating condition.		200	MHz
CNT8	8 bit counter performance @ recommended operating condition.		382	MHz
CNT16	16 bit counter performance @recommended operating condition.		290	MHz
CNT32	32 bit counter performance @ recommended operating condition.		240	MHz

EMB Performance

Table 38 EMB Performance

Symbol	Description	Min	Max	Units
EMB5K	Using register path.		300M	MHz
	Not using the register path.		250M	MHz
EMB18K	Using register path.		300M	MHz
	Not using the register path.		250M	MHz

Configuration Spec

Table 39 Configuration spec

Symbol	Description	Min	Max	Units
TCK	JTAG TCK configuration frequency		50M	MHz
SCLK	PS configuration clock SCLK frequency		20M	MHz
OSC	AS configuration clock frequency			

This part lists the Pins and Package information for users to quickly search

5. Pins and Package

Pins Definitions and Rules

Table 40 Pins Definitions and Rules

Pin Name	Direction	Description
User I/O Pins		
IOXX_# IO_XXY_#	inout	General-purpose user-I/O pin. XX represents the I/O number in the bank. Y represents p or n for the differential I/O pairs.
Multi-Function Pins		
IOXXX/ZZZ_#		Multi-function pins are labeled IOXXX/YYY_#, where YYY represents one or more of the following functions in addition to being general purpose user I/O. If not used for their special function, these pins can be user I/O.
Multi-Function Pins: SPI serial configuration Pins		
SCLK	Input/output	In passive serial configuration mode, SCLK is a clock input used to clock configuration data from external device source into device. In active serial configuration mode, SCLK is a clock output from device. The pin can be used as regular user I/Os after configuration.
SDI	output	Dedicated configuration data output pin in AS mode. No configuration function in PS mode. The pin can be used as regular user I/Os after configuration in AS mode
SDO	Input	Serial data input from external master in PS mode or from spi flash in AS mode. The pin can be used as regular user I/Os after configuration.
SS	output or input	Chip select output to enable a SPI Flash in AS mode or input as a HME-HR device select. The pin value will be latched for mode selection when the devices are power on or reset. 1: Active Serial mode, 0 Passive Serial mode. This output is used during AS mode. The pin can be used as regular user I/Os after configuration in AS mode. it is used as chip selection control (input) during PS.The pin can be used as regular user I/Os after configuration in PS mode.
Multi-Function Pins: Configuration Pins		

Pin Name	Direction	Description
CFGDONE	output	This is a dedicated configuration status pin, the pin will output high during configuration. The pin can be used as regular user I/Os after configuration.
nCONFIG	input	Chip global reset input. Active low.
Multi-Function Pins: Clock Pins		
CLKX	input	These clock pins connect to Global Clock Buffers. These pins become regular user I/Os when not needed for clocks.
Dedicated Pins: JTAG		
TCK	input	TCK Input Boundary-Scan Clock.
TDI	input	TDI Input Boundary-Scan Data Input.
TDO	output	TDO Output Boundary-Scan Data Output.
TMS	input	TMS Input Boundary-Scan Mode Select.
JM_B	input	The pin value will be latched for mode selection when the devices are power on or reset. 1: TCK/TDI/TDO/TMS pins are no JTAG functions, only user I/Os. 0: TCK/TDI/TDO/TMS pins are only used as JTAG functions.
Dedicated Pins: Power		
VDDIO_X	N/A	Digital power for IO. Along with all the other VCCO pins in the same bank. 1.5V, 1.8V, 2.5V, and 3.3V are selectable.
VDD_CORE	N/A	Digital power for core.
VDDIO_33	N/A	Digital power for configuration bank.
VDDQ	N/A	Digital power for Efuse Programming, 2.5V. If Efuse is not used, the pin should be connected to ground with a 1k resistor.
VDD_PLL	N/A	PLL power
GND	N/A	Digital ground.
Flash Pins		
FLS_WPB	input	Write Protect Input
FLS_DO	output	Data Output
FLS_VSS	N/A	Ground
FLS_CSB	input	FLASH Chip Select Input
FLS_VDD	N/A	FLASH power, 2.5V, and 3.3V are selectable.

Caution:

1) **If Efuse is not used, the VDDQ pin should be connected to ground with a 1k resistor and there is no power sequence requirement.**
2) **There is a power sequence requirement when Efuse is used: The VDD_CORE must be power on before the VDDQ.**
3) **For HR01/02 QFN32 package device, the pins of power supply and GND are**

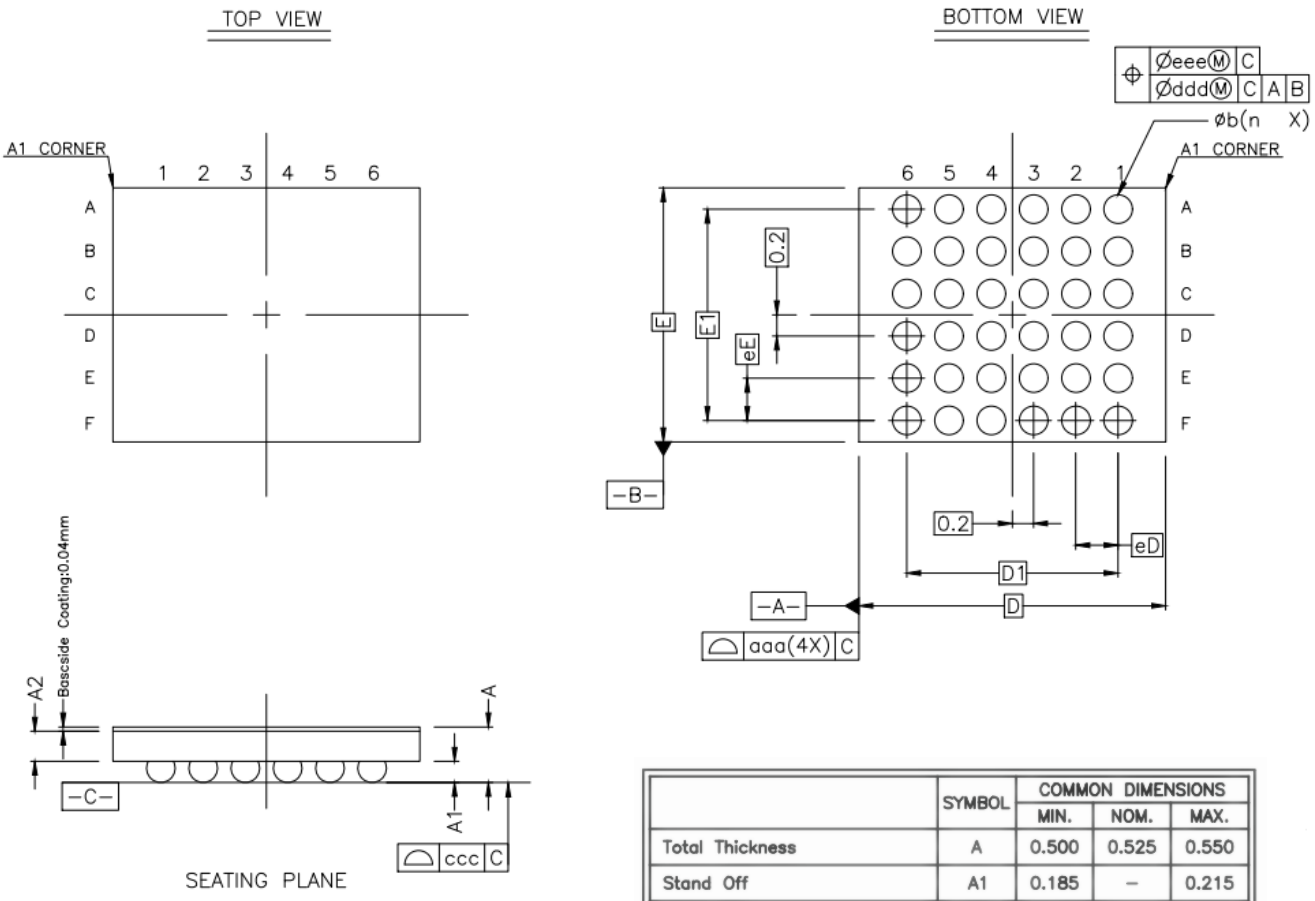
compatible with HR03 device, but the definition of other pins can be according to pinlist file.

4) The compatibility design of HR01/02 and HR03 QFN32 package device can refer to the file of “HR_FPGA_Application_Note.pdf”.

5) For HR02PN3Q32 device: pin IO00_SDO_2 and FLS_DO, IO03_SS_2 and FLS_CSB must be connected together on pcb board.

Package Information

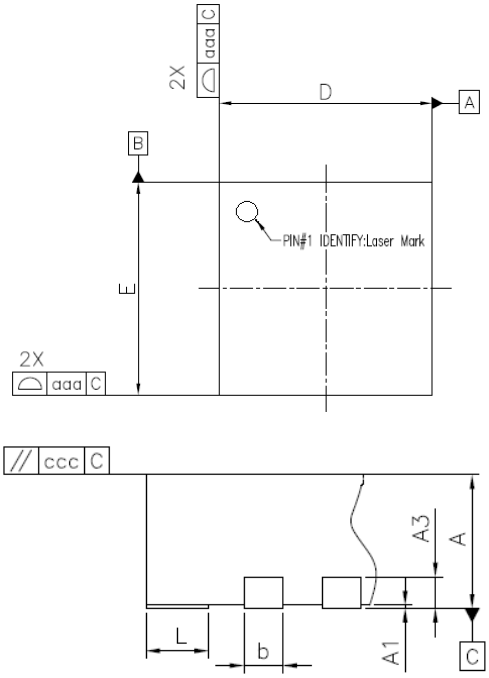
36-Ball WLCS Package



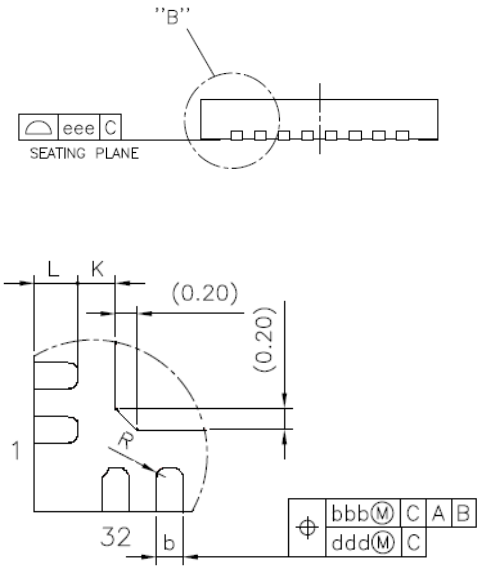
Dimensions in Millimeters

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
Total Thickness	A	0.500	0.525	0.550
Stand Off	A1	0.185	–	0.215
Wafer Thickness (Molding)	A2	0.285 ± 0.020		
SI Die Thickness	~~A3~~	0.285 REF		
Body Size	D	2.903 BSC		
	E	2.404 BSC		
Ball Diameter (Size)		0.250		
Ball/Bump Width	b	0.240	0.270	0.300
Ball/Bump Pitch	eD	0.400		
	eE	0.400		
Ball/Bump Count	n	36		
Edge Ball Center to Center	D1	2.000 BSC		
	E1	2.000 BSC		
Package Edge Tolerance	aaa	0.035		
Coplanarity ~~(whole wafer)~~	ccc	0.030		
Ball/Bump Offset (Package)	ddd	0.150		
Ball/Bump Offset (Ball)	eee	0.080		

QFN32 Package (5mmx5mm)



DETAIL : "B"



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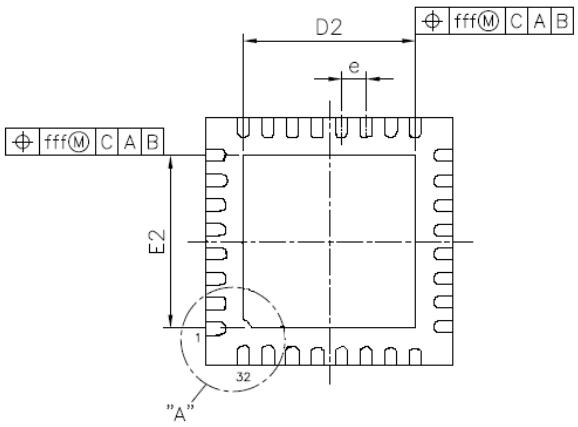
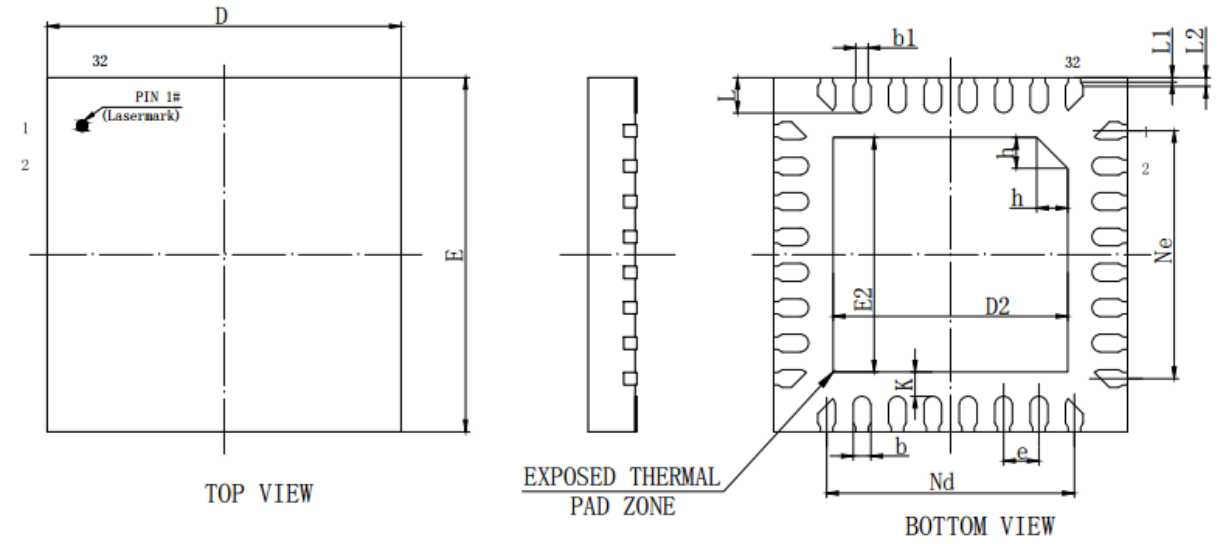
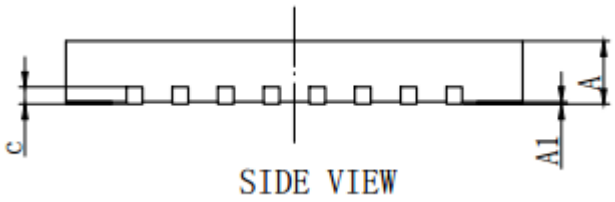


Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	5.00 BSC			0.197 BSC		
D2/E2	3.35	3.50	3.65	0.132	0.138	0.144
e	0.50 BSC			0.020 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
K	0.20	---	---	0.008	---	---
R	0.09	---	---	0.004	---	---
aaa	0.15			0.006		
bbb	0.10			0.004		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

Dimensions in Millimeters

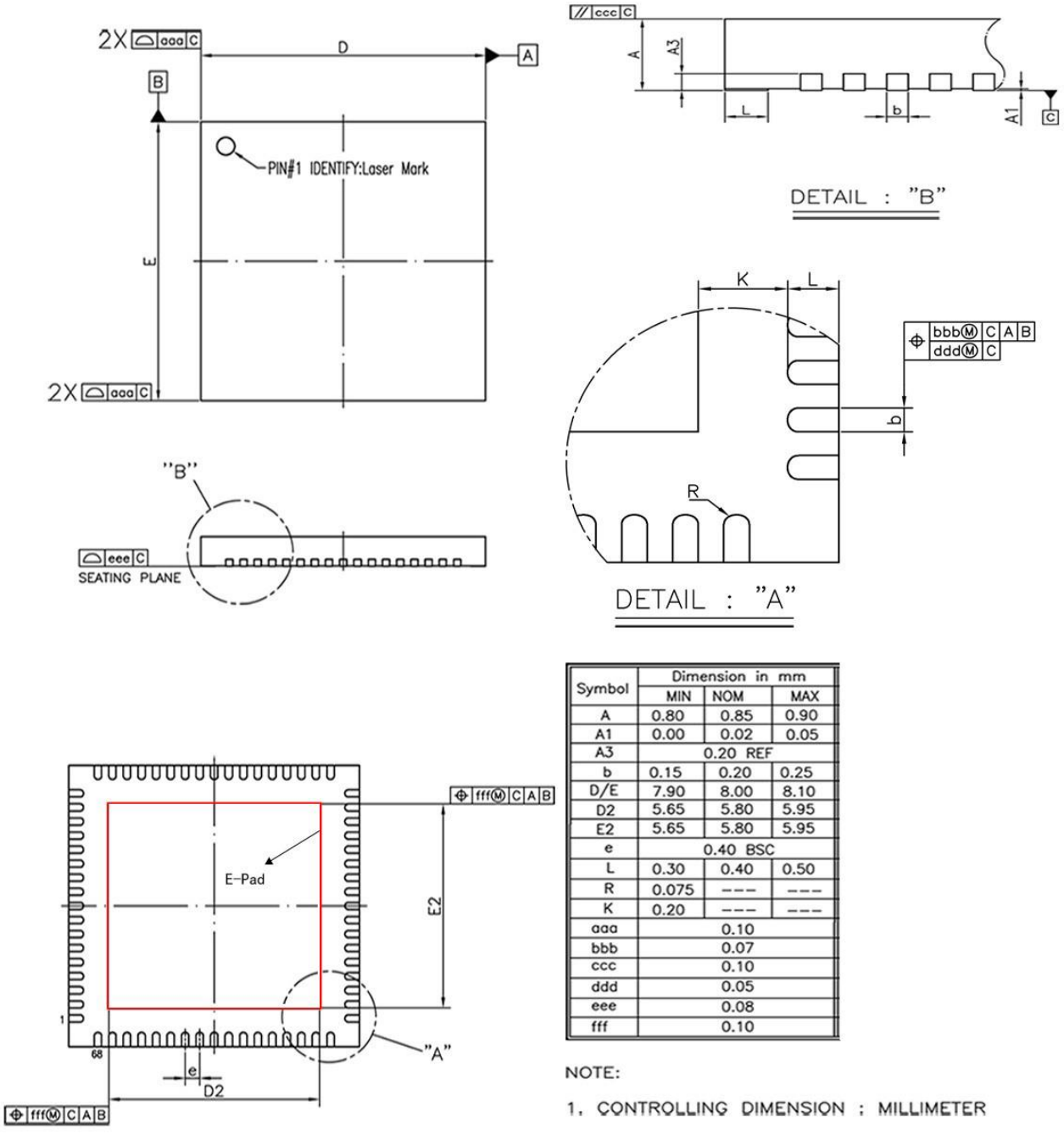
QFN32 Package (4mmx4mm)





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1		0.14REF	
c	0.10	0.15	0.20
D	3.90	4.00	4.10
D2	2.55	2.65	2.75
e		0.40BSC	
Nd		2.80BSC	
E	3.90	4.00	4.10
E2	2.55	2.65	2.75
Ne		2.80BSC	
L	0.35	0.40	0.45
L1	0	0.05	0.10
L2	0.05	0.10	0.15
h	0.30	0.35	0.40
K	0.20	-	-
L/F载体尺寸		2.85x2.85	

QFN68 Package



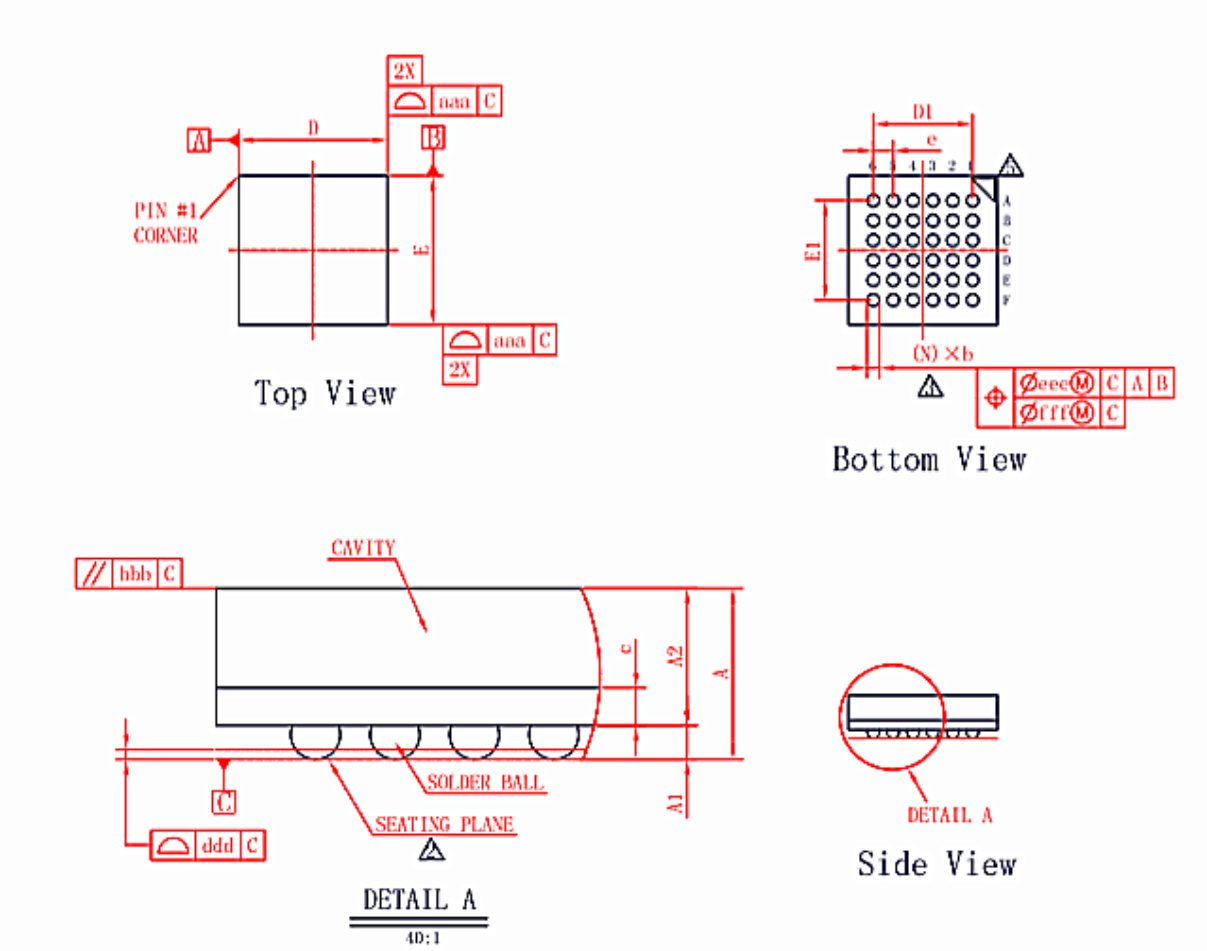
Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D/E	7.90	8.00	8.10
D2	5.65	5.80	5.95
E2	5.65	5.80	5.95
e		0.40 BSC	
L	0.30	0.40	0.50
R	0.075	---	---
K	0.20	---	---
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

Dimensions in Millimeters

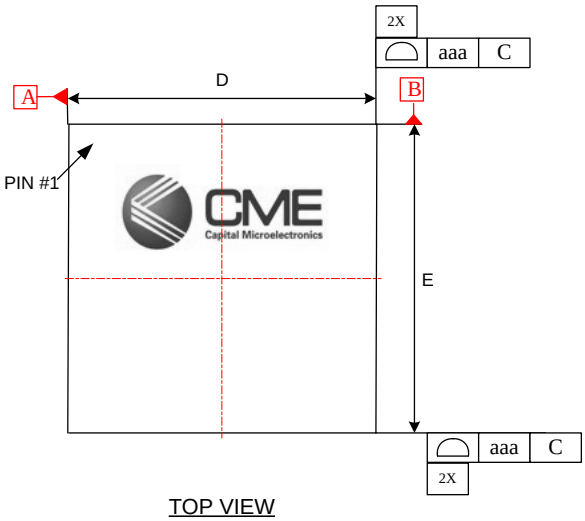
ucBGA36 Package



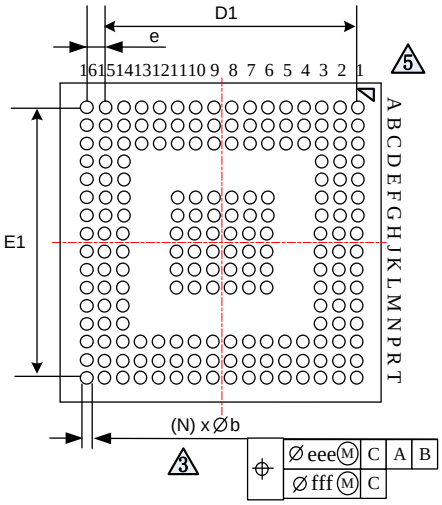
symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	0.960	---	---	0.038
A1	0.120	0.170	0.220	0.005	0.007	0.009
A2	0.640	0.690	0.740	0.025	0.027	0.029
c	0.160	0.190	0.220	0.006	0.007	0.009
D	2.900	3.000	3.100	0.114	0.118	0.122
E	2.900	3.000	3.100	0.114	0.118	0.122
D1	---	2.000	---	---	0.079	---
E1	---	2.000	---	---	0.079	---
e	---	0.400	---	---	0.016	---
b	0.200	0.250	0.300	0.008	0.010	0.012
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.050			0.002		
Ball Diam	0.250			0.010		
N	36			36		
MD/ME	6/6			6/6		

Dimensions in Millimeters

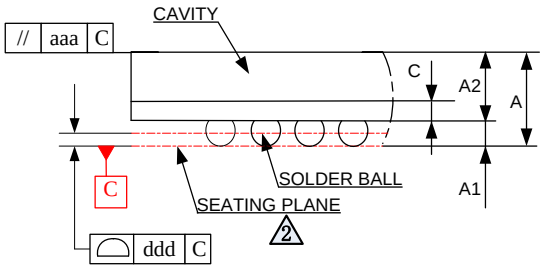
csBGA192 Package



TOP VIEW

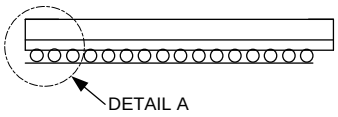


BOTTOM VIEW



DETAIL A

20:1



Side View

TECHNOLOGY SPECIFICATION

1.BALL PAD OPENING: 0.270mm;

2 PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS;

3 DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER,PARALLEL TO PRIMARY DATUM C;

4.SPECIAL CHARACTERISTICS C CLASS: bbb,ddd;

5 THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY;

6.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING;

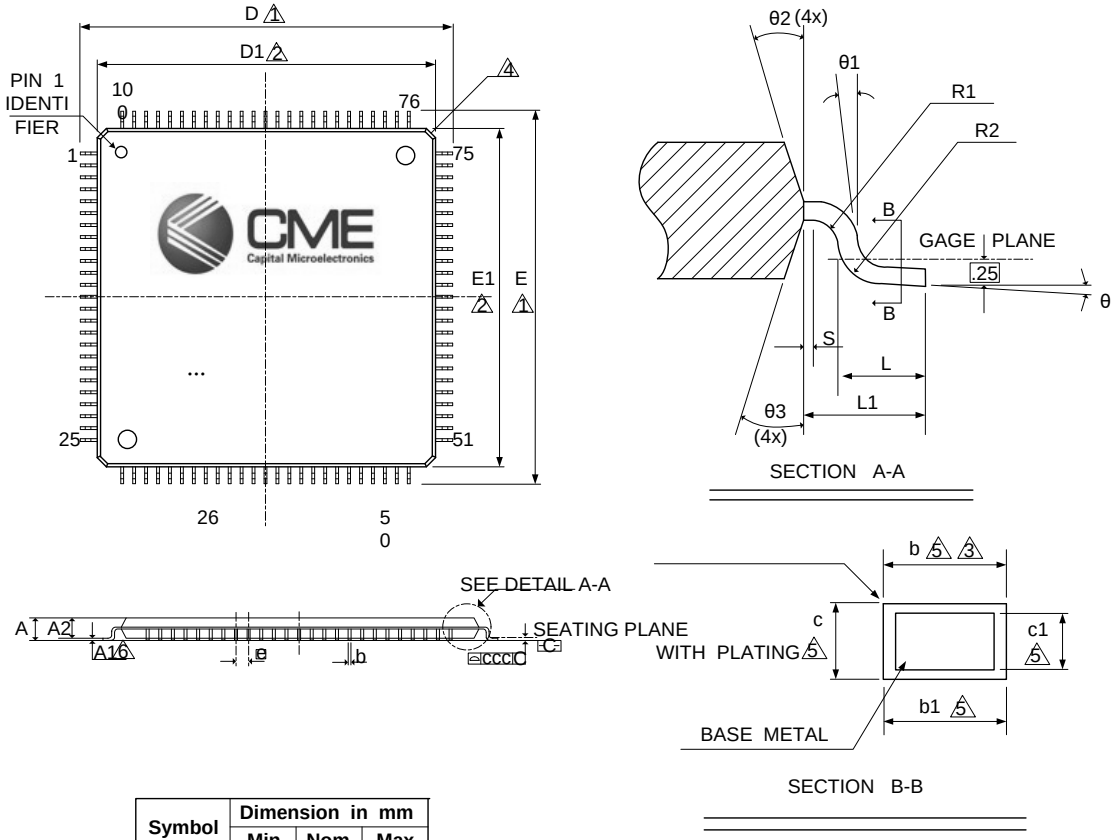
7.ALL UNITS ARE IN MILLIMETER;

8.THE DERECTION OF VIEW  。

Symbol	Dimension in mm		
	Min	Nom	Max
A	——	——	1.000
A1	0.160	0.210	0.260
A2	0.640	0.690	0.740
c	0.160	0.190	0.220
D	8.900	9.000	9.100
E	8.900	9.000	9.100
D1	——	7.500	——
E1	——	7.500	——
e	——	0.500	——
b	0.250	0.300	0.350
aaa	0.150		
bbb	0.200		
ddd	0.080		
eee	0.150		
fff	0.050		
N	192		
MD/ME	16/16		

Dimensions in Millimeters

TQFP100 Thin Quad Flat-Pack Package

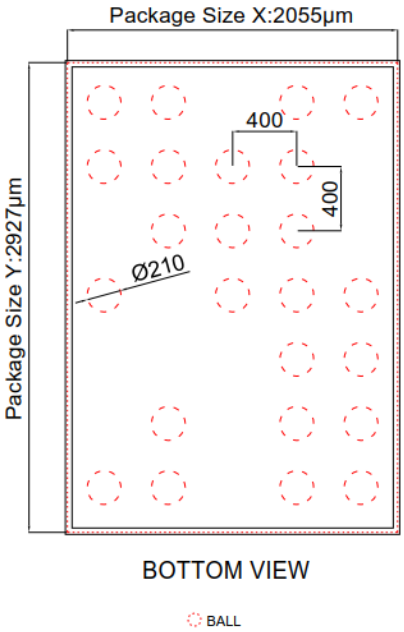


Symbol	Dimension in mm		
	Min	Nom	Max
A	——	——	1.20
A1	0.05	——	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	——	0.20
c1	0.09	——	0.16
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	0.15 REF		
R	0.08	——	——
R1	0.08	——	0.20
S	0.20	——	——
θ	0°	3.5°	7°
θ1	0°	——	——
θ2	11°	12°	13°
θ3	11°	12°	13°
ccc	0.08		

1. TO BE DETERMINED AT SEATING PLANE -C-
   DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION
   D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION
2. INCLUDING MOLD MISMATCH.
   DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION
3. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THEFOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
   THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD
5. BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE
7. CONTROLLING DIMENSION : MILLIMETER.
   TO THE LOWEST POINT OF THE PACKAGE BODY.
8. REFERENCE DOCUMENT : JEDEC MS - 026 , BFB
9. SPECIAL CHARACTERISTICS C CLASS : ccc

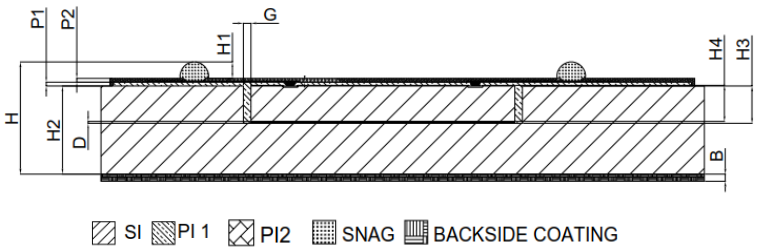
Dimensions in Millimeters

24-Ball WLCS Package



BOTTOM VIEW

BALL



SI PI 1 PI2 SNAG BACKSIDE COATING

CROSS SECTION

ITEM	DATA(UM)
PACKAGE SIZE X*Y	2055*2927±25
BALL DIAMETER	210±25
MIN BALL PITCH	400/400
TOTAL PAD Q'TY	160
PAD Q'TY TO BE BALLED	47
BALL COUNT	24
SCRIBE LINE	80

SYMBOL	ITEM	DATA(UM)
H	PACKAGE HEIGHT	500±50
H1	BALL HEIGHT	150±25
H2	SI THICKNESS	300±10
H3	CAVITY DEPTH	100±5
H4	IC DIE THICKNESS	90±5
P1	PI1 THICKNESS	17±3
P2	PI2 THICKNESS	10±3
G	CAVITY GAP	30/40±5
D	DAF THICKNESS	10±2
B	BACKSIDE COATING THICKNESS	20±10

This appendix describes the ordering information about HR family. You may go to the Selection Guide for the details.

Ordering Information

All part numbers have the following conventions:

Table 41 Part number conventions

Vendor	Product Family	LUT Density	Device Type	Flash	Package Type	Temperature	Speed Grade
HME-	HR	01	P	N0	Q32	C	7

PRODUCT FAMILY:

HR

Device Type

- P FPGA

LUT DENSITY:

- 01: 768 LUTs
- 02: 1536 LUTs
- 03: 3072 LUTs

FLASH:

- N0: NO FLASH
- N3: 4Mbit FLASH

Package Type: <type><#>

- Q Quad Flat No-Lead Package (QFN)
- W Wafer Level Chip Scale (WLCSP)
- U Ultra Chip Scale BGA (ucBGA) 0.4mm
- C Chip Scale BGA (csBGA) 0.5mm
- T Thin Quad Flat Pack (TQFP)

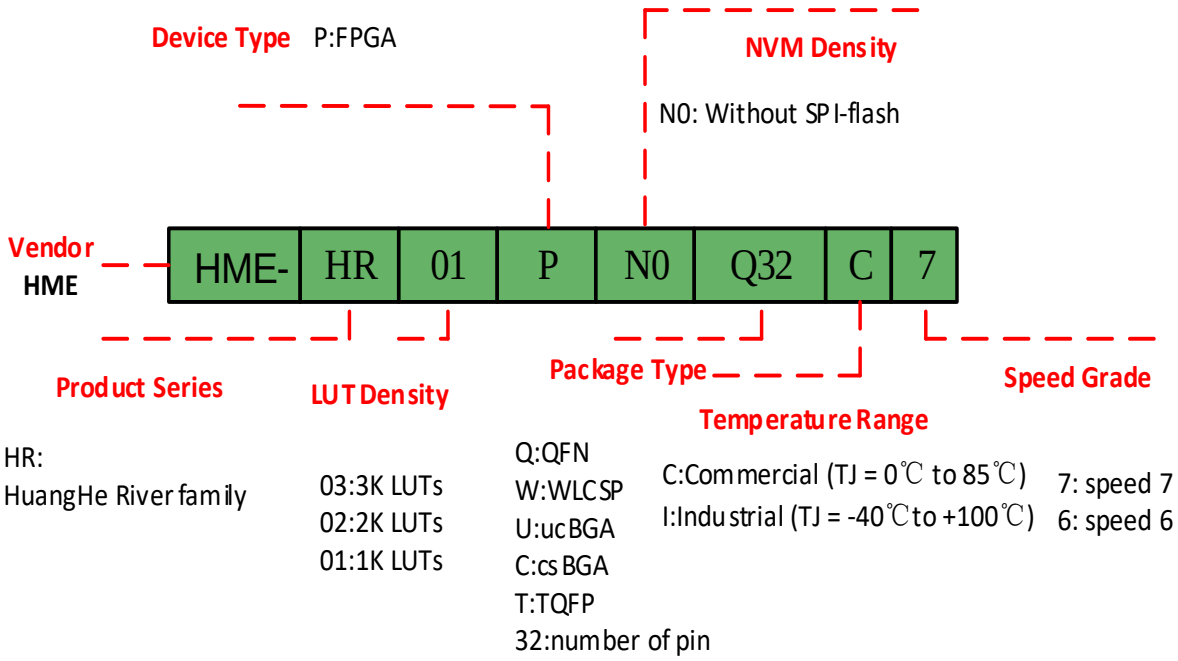
Temperature Range

- C Commercial (TJ = 0℃ to 85℃)
- I Industrial (TJ = -40℃to +100℃)

Speed Grade

- # Speed (7 for speed 7, 6 for speed 6, …)

Example: **HME-HR01PN0Q32C7**



Revision History

The table below shows the revision history for this document.

Release Date	Doc Version	Revision
Sept. 2017	HME-HRDSE01	Initial release.
April 2018	HME-HRDSE02	Modify pin VDD2V5 description Add caution information Modify W36 package information Update U36 package information Modify VDD_CORE voltage value, delete 1.2V
July 2018	HME-HRDSE03	Modify Figure27
Sept.2018	HME-HRDSE04	Add W24 package information Add Q32(with flash) package information