TPA2005D1 1.4-W MONO Filter-Free Class-D Audio Power Amplifier

1 Features

- 1.4 W Into 8 Ω From a 5 V Supply at THD = 10% (Typ)
- Maximum Battery Life and Minimum Heat
  - Efficiency With an 8-Ω Speaker:
    - 84% at 400 mW
    - 79% at 100 mW
  - 2.8-mA Quiescent Current
  - 0.5-μA Shutdown Current
- Capable of Driving an 8-Ω Speaker (2.5 V ≤ V_{DD} ≤ 5.5 V) and a 4-Ω Speaker (2.5 V ≤ V_{DD} ≤ 4.2 V)
- Only Three External Components
  - Optimized PWM Output Stage Eliminates LC Output Filter
  - Internally Generated 250-kHz Switching Frequency Eliminates Capacitor & Resistor
  - Improved PSRR (–71 dB at 217 Hz) and Wide Supply Voltage (2.5 V to 5.5 V) Eliminates Need for a Voltage Regulator
  - Fully Differential Design Reduces RF Rectification & Eliminates Bypass Capacitor
  - Improved CMRR Eliminates Two Input Coupling Capacitors
- Space Saving Package
  - 3 mm × 3 mm QFN package (DRB)
  - 2.5 mm × 2.5 mm MicroStar Junior™ BGA Package (ZQY)
  - 3 mm x 5 mm MSOP PowerPAD™ Package (DGN)
- Use TPA2006D1 for 1.8 V Logic Compatibility on Shutdown Pin

2 Applications

Ideal for Wireless or Cellular Handsets and PDAs

3 Description

The TPA2005D1 is a 1.4-W high efficiency filter-free class-D audio power amplifier in a MicroStar Junior™ BGA, QFN, or MSOP package that requires only three external components.

Features like 84% efficiency, –71-dB PSRR at 217 Hz, improved RF-rectification immunity, and 15 mm^2 total PCB area make the TPA2005D1 ideal for cellular handsets. A fast start-up time of 9 ms with minimal pop makes the TPA2005D1 ideal for PDA applications.

In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the TPA2005D1. The device allows independent gain control by summing the signals from each function while minimizing noise to only 48 μV_{RMS}.

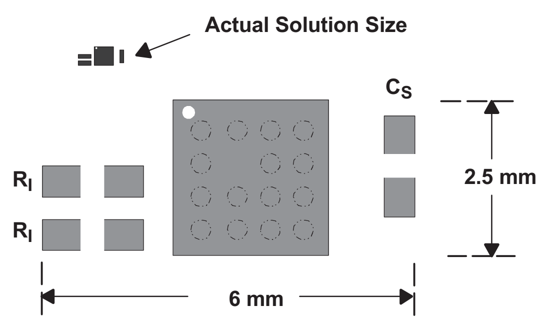
The TPA2005D1 has short-circuit and thermal protection.

Device Information[1]

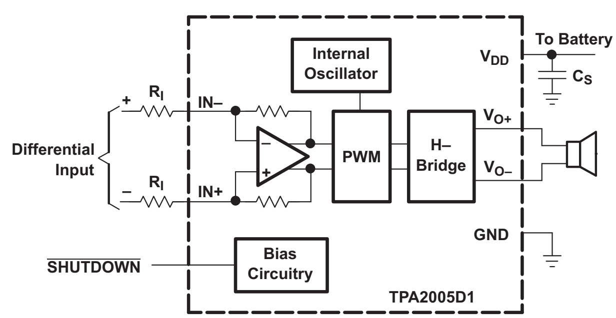
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA2005D1	HVSSOP (8)	3.00 mm × 3.00 mm
	VSON (8)	3.00 mm x 3.00 mm
	BGA MICROSTAR JUNIOR (15)	2.50 mm x 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Device Layout and Size



Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (July 2008) to Revision G	Page
• Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

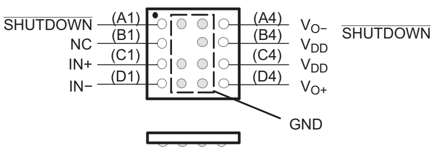
Changes from Revision E (July 2008) to Revision F	Page
• Added Capable of Driving an 8-Ω Speaker and a 4-Ω Speaker	1
• Added Use TPA2006D1 for 1.8 V Logic Compatibility on Shutdown Pin	1
• Added to Description: The TPA2005D1 has short-circuit and thermal protection.	1
• Changed Storage temperature From: -40°C to 85°C To: -40°C to 150°C	4
• Added R_L Load resistance, to the Abs Max Ratings Table	4
• Added New graph, Figure 3	6
• Changed graph, Figure 4	6
• Added graph, Figure 10	6
• Changed graph, Figure 11	6
• Changed graph, Figure 12	6
• Added graph, Figure 13	7
• Added graph, Figure 20	8
• Added graph, Figure 21	8
• Added graph, Figure 22	8
• Added Any capacitor in the audio path should have a rating of X7R or better.	23
• Deleted Section: 8-Pin QFN 9DRB) Layout	26

5 Device Comparison Table

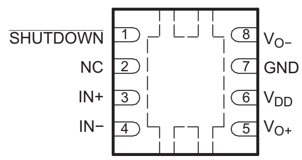
DEVICE NUMBER	SPEAKER CHANNELS	SPEAKER AMP TYPE	OUTPUT POWER (W)	PSRR (dB)	SUPPLY MIN (V)	SUPPLY MAX (V)	PACKAGE FAMILY
TPA2005D1	Mono	Class D	1.4	75	2.5	5.5	BGA MICROSTAR JUNIOR
							HVSSOP
							VSON
TPA2006D1	Mono	Class D	1.45	75	2.5	5.5	VSON

6 Pin Configuration and Functions

GQY and ZQY Packages
15-Pin MicroStar Junior™
Top and Side Views

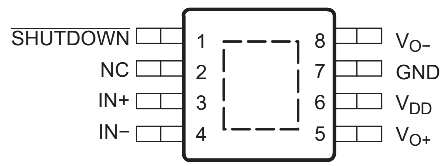


DRB Package
8-Pin VSON
Top View



NC − No internal connection

DGN Package
8-Pin HVSSOP
Top View



A. The shaded terminals are used for electrical and thermal connections to the ground plane. All the shaded terminals need to be electrically connected to ground. No connect (NC) terminals still need a pad and trace.

B. The thermal pad of the DRB and DGN packages must be electrically and thermally connected to a ground plane.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	GQY, ZQY	DRB, DGN		
GND	A2, A3, B3, C2, C3, D2, D3	7	I	High-current ground
IN-	D1	4	I	Negative differential input
IN+	C1	3	I	Positive differential input
NC	B1	2		No internal connection
SHUTDOWN	A1	1	I	Shutdown terminal (active low logic)
Thermal Pad				Must be soldered to a grounded pad on the PCB.
V_{DD}	B4, C4	6	I	Power supply
V_{O-}	A4	8	O	Negative BTL output
V_{O+}	D4	5	O	Positive BTL output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{DD}	Supply voltage[2]	In active mode	–0.3	6	V
		In SHUTDOWN mode	–0.3	7	V
V_I	Input voltage		–0.3	V_{DD} + 0.3 V	V
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature		–40	85	°C
T_{stg}	Storage temperature		–65	150	°C
R_L	Load resistance	$2.5 \le V_{DD} \le 4.2$ V	3.2 (Minimum)		Ω
		$4.2 < V_{DD} \le 6$ V	6.4 (Minimum)		Ω

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For the MSOP (DGN) package option, the maximum V_{DD} should be limited to 5 V if short-circuit protection is desired.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		2.5		5.5	V
V_{IH}	High-level input voltage	SHUTDOWN	2		V_{DD}	V
V_{IL}	Low-level input voltage	SHUTDOWN	0		0.8	V
R_I	Input resistor	Gain ≤ 20 V/V (26 dB)	15			kΩ
V_{IC}	Common mode input voltage range	V_{DD} = 2.5 V, 5.5 V, CMRR ≤ –49 dB	0.5		V_{DD}-0.8	V
T_A	Operating free-air temperature		–40		85	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPA2005D1				UNIT
		ZQY (MicroStar Junior)	GQY (MicroStar Junior)	DRB (VSON)	DGN (MSOP PowerPAD)	
		15 PINS	15 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.7	92.7	50.9	57.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	120.5	120.5	66.2	53.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	104	104	25.9	33.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.1	3.1	1.4	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.8	44.8	26	33.47	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	7	6.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_A = 25°C, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Output offset voltage (measured differentially)	V_I = 0 V, A_V = 2 V/V, V_{DD} = 2.5 V to 5.5 V			25	mV
PSRR	Power supply rejection ratio	V_{DD} = 2.5 V to 5.5 V		–75	–55	dB
CMRR	Common mode rejection ratio	V_{DD} = 2.5 V to 5.5 V, V_{IC}= V_{DD}/2 to 0.5 V, V_{IC}= V_{DD}/2 to V_{DD}- 0.8 V		–68	–49	dB
$\lvert I_{IH} \rvert$	High-level input current	V_{DD} = 5.5 V, V_I = 5.8 V			50	µA
$\lvert I_{IL} \rvert$	Low-level input current	V_{DD} = 5.5 V, V_I = 0.3 V			1	µA
$I_{(Q)}$	Quiescent current	V_{DD} = 5.5 V, no load		3.4	4.5	mA
		V_{DD} = 3.6 V, no load		2.8		
		V_{DD} = 2.5 V, no load		2.2	3.2	
$I_{(SD)}$	Shutdown current	$V_{\overline{(SHUTDOWN)}}$ = 0.8 V, V_{DD} = 2.5 V to 5.5 V		0.5	2	µA
$r_{DS(on)}$	Static drain-source on-state resistance	V_{DD} = 2.5 V		770		mΩ
		V_{DD} = 3.6 V		590		
		V_{DD} = 5.5 V		500		
	Output impedance in $\overline{\text{SHUTDOWN}}$	$V_{\overline{(SHUTDOWN)}}$ = 0.8 V		>1		kΩ
$f_{(sw)}$	Switching frequency	V_{DD} = 2.5 V to 5.5 V	200	250	300	kHz
	Gain		$2 \times \frac{142\ k\Omega}{R_I}$	$2 \times \frac{150\ k\Omega}{R_I}$	$2 \times \frac{158\ k\Omega}{R_I}$	$\frac{V}{V}$

7.6 Operating Characteristics

T_A = 25°C, Gain = 2 V/V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD + N= 1%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		1.18		W
			V_{DD} = 3.6 V		0.58		
			V_{DD} = 2.5 V		0.26		
		THD + N= 10%, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		1.45		W
			V_{DD} = 3.6 V		0.75		
			V_{DD} = 2.5 V		0.35		
THD+N	Total harmonic distortion plus noise	P_O = 1 W, f = 1 kHz, R_L = 8 Ω	V_{DD} = 5 V		0.18%		
		P_O = 0.5 W, f = 1 kHz, R_L = 8 Ω	V_{DD} = 3.6 V		0.19%		
		P_O = 200 mW, f = 1 kHz, R_L = 8 Ω	V_{DD} = 2.5 V		0.20%		
k_{SVR}	Supply ripple rejection ratio	f = 217 Hz, $V_{(RIPPLE)}$ = 200 mV_{pp} Inputs ac-grounded with C_i = 2 µF	V_{DD} = 3.6 V		–71		dB
SNR	Signal-to-noise ratio	P_O= 1 W, R_L = 8 Ω	V_{DD} = 5 V		97		dB
V_n	Output voltage noise	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, Inputs ac-grounded with C_i = 2 µF	No weighting		48		μV_{RMS}
			A weighting		36		
CMRR	Common mode rejection ratio	V_{IC} = 1 V_{pp} , f = 217 Hz	V_{DD} = 3.6 V		–63		dB
Z_I	Input impedance			142	150	158	kΩ
	Start-up time from shutdown	V_{DD} = 3.6 V			9		ms

7.7 Typical Characteristics

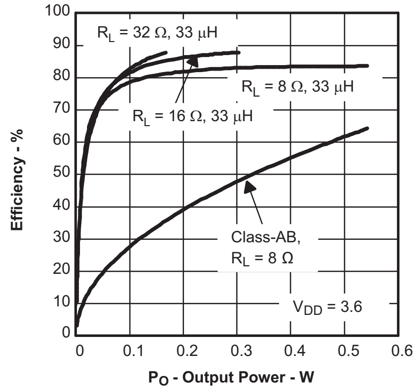


Figure 1. Efficiency vs Output Power

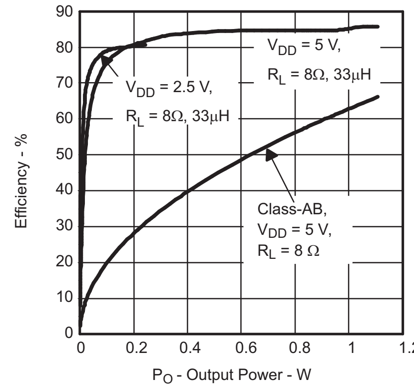


Figure 2. Efficiency vs Output Power

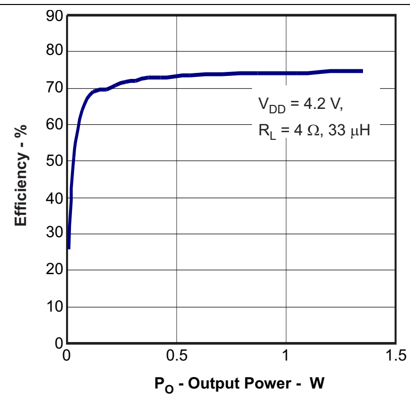


Figure 3. Efficiency vs Output Power

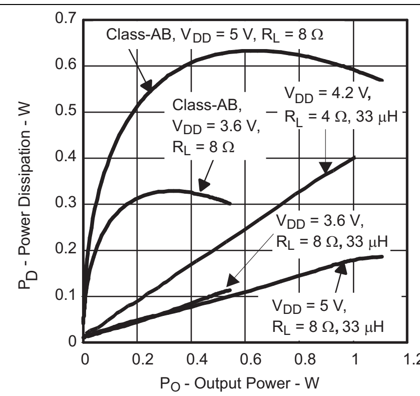


Figure 4. Power Dissipation vs Output Power

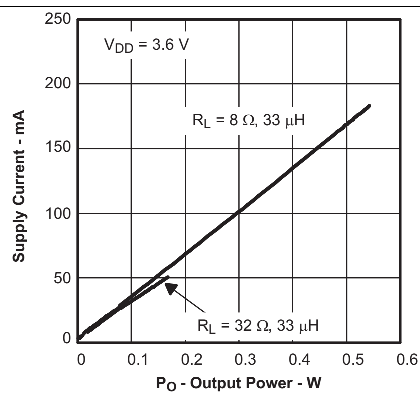


Figure 5. Supply Current vs Output Power

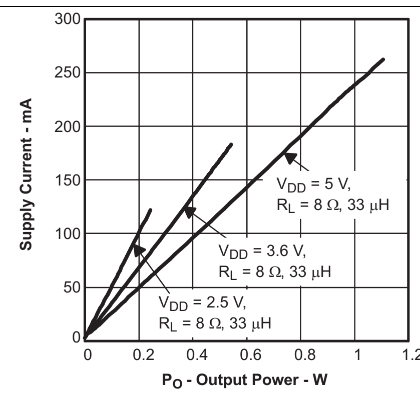


Figure 6. Supply Current vs Output Power

Typical Characteristics (continued)

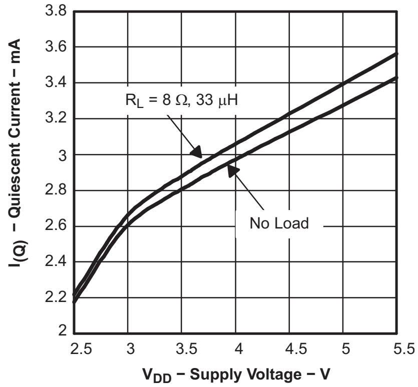


Figure 7. Quiescent Current vs Supply Voltage

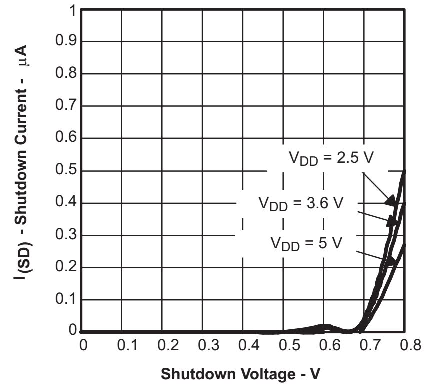


Figure 8. Shutdown Current vs Shutdown Voltage

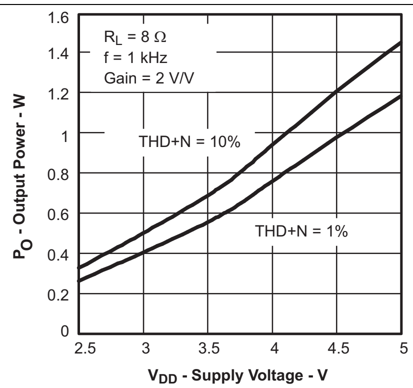


Figure 9. Output Power vs Supply Voltage

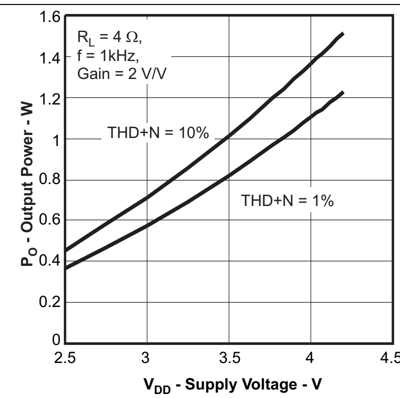


Figure 10. Output Power vs Supply Voltage

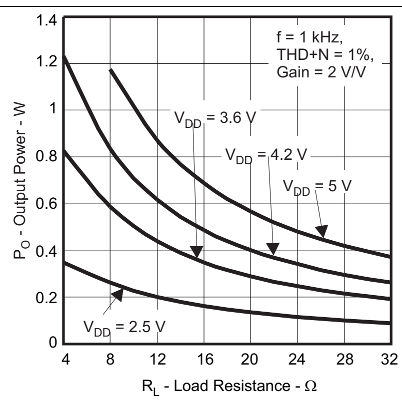


Figure 11. Output Power vs Load Resistance

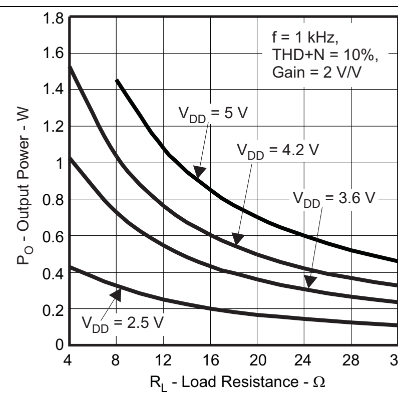


Figure 12. Output Power vs Load Resistance

Typical Characteristics (continued)

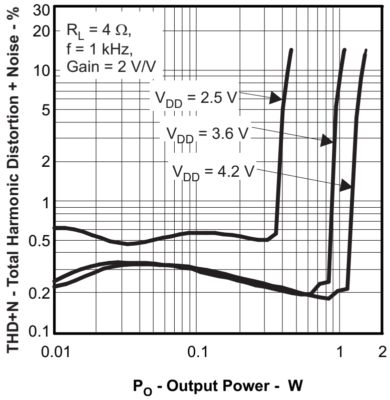


Figure 13. Total Harmonic Distortion + Noise vs Output Power

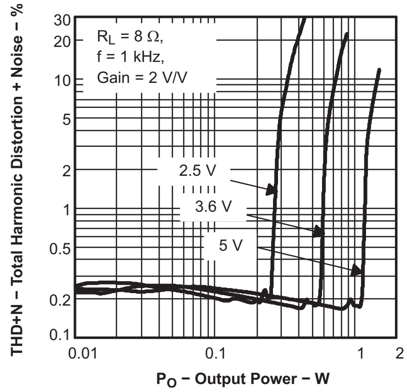


Figure 14. Total Harmonic Distortion + Noise vs Output Power

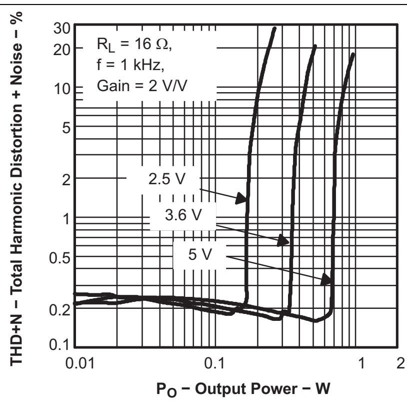


Figure 15. Total Harmonic Distortion + Noise vs Output Power

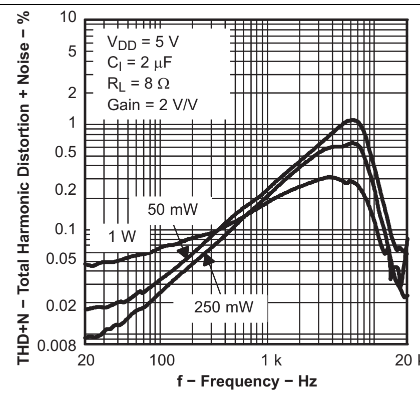


Figure 16. Total Harmonic Distortion + Noise vs Frequency

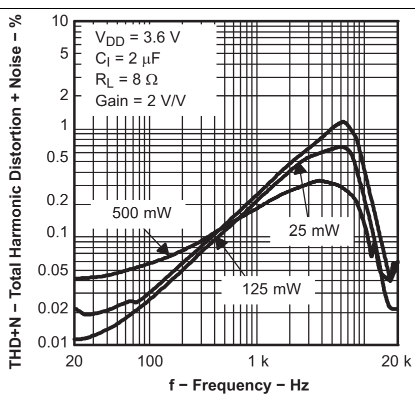


Figure 17. Total Harmonic Distortion + Noise vs Frequency

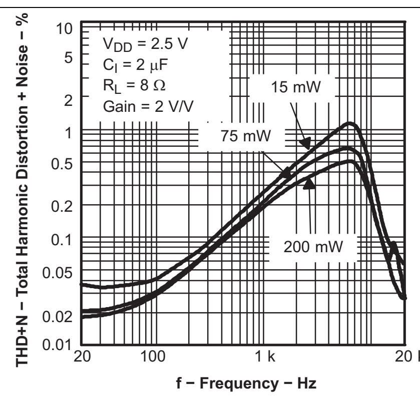


Figure 18. Total Harmonic Distortion + Noise vs Frequency

Typical Characteristics (continued)

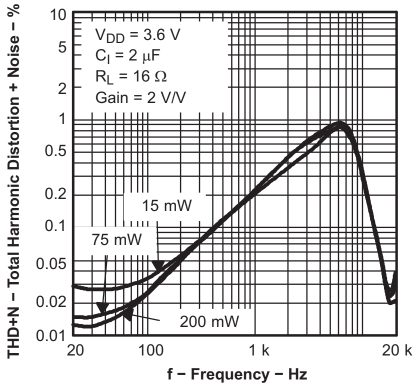


Figure 19. Total Harmonic Distortion + Noise vs Frequency

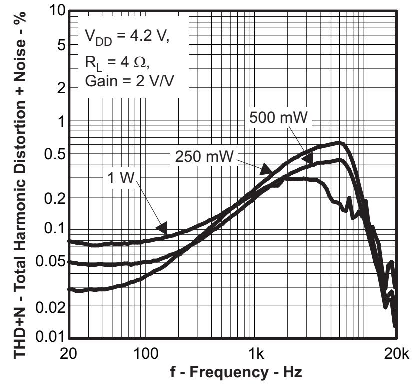


Figure 20. Total Harmonic Distortion + Noise vs Frequency

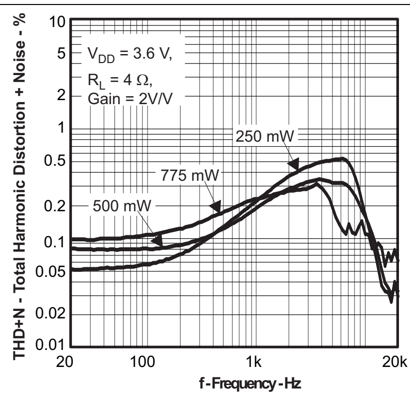


Figure 21. Total Harmonic Distortion + Noise vs Frequency

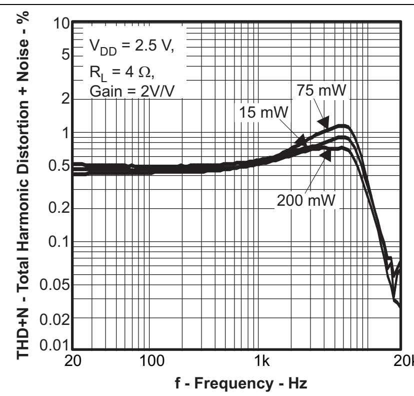


Figure 22. Total Harmonic Distortion + Noise vs Frequency

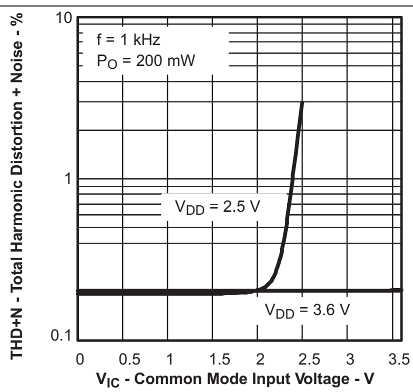


Figure 23. Total Harmonic Distortion + Noise vs Common Mode Input Voltage

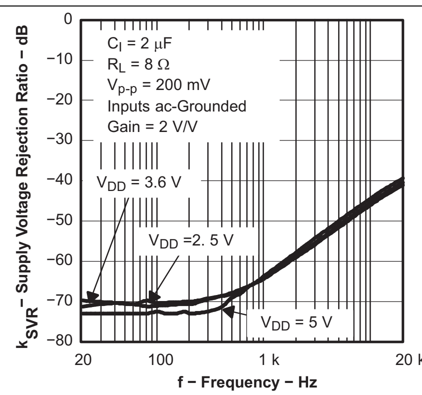


Figure 24. Supply Voltage Rejection Ratio vs Frequency

Typical Characteristics (continued)

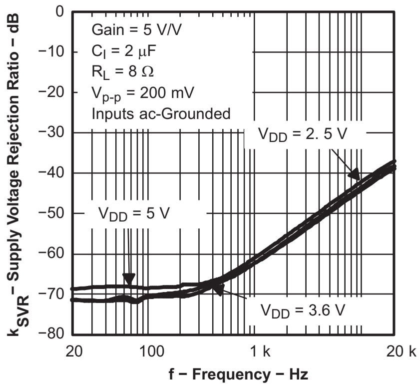


Figure 25. Supply Voltage Rejection Ratio vs Frequency 25

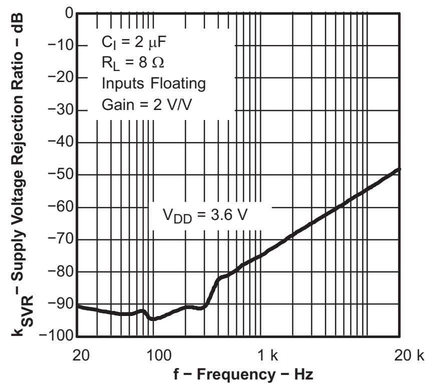


Figure 26. Supply Voltage Rejection Ratio vs Frequency

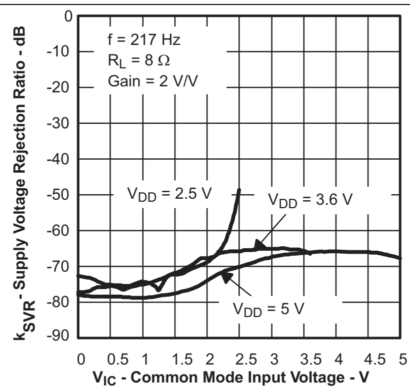


Figure 27. Supply Voltage Rejection Ratio vs Common-mode Input Voltage

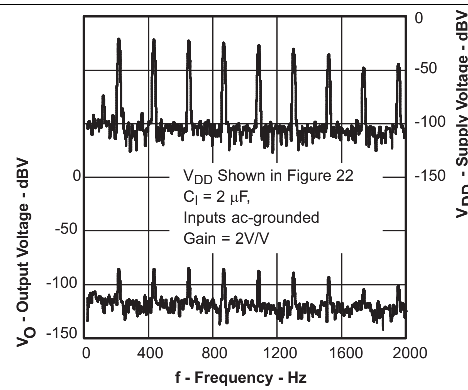


Figure 28. GSM Power Supply Rejection vs Time

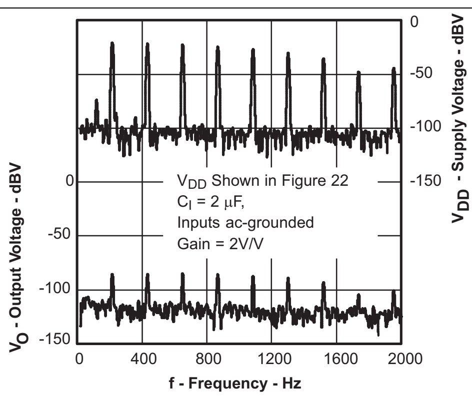


Figure 29. GSM Power Supply Rejection vs Frequency

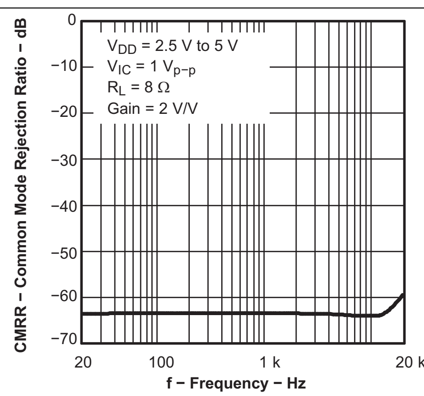


Figure 30. Common-mode Rejection Ratio vs Frequency

Typical Characteristics (continued)

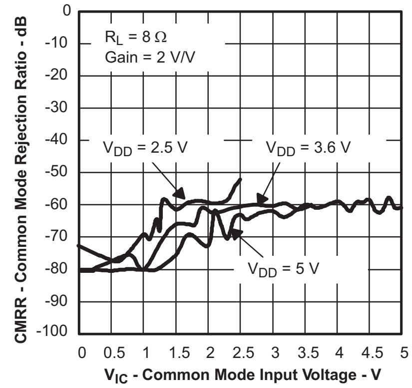
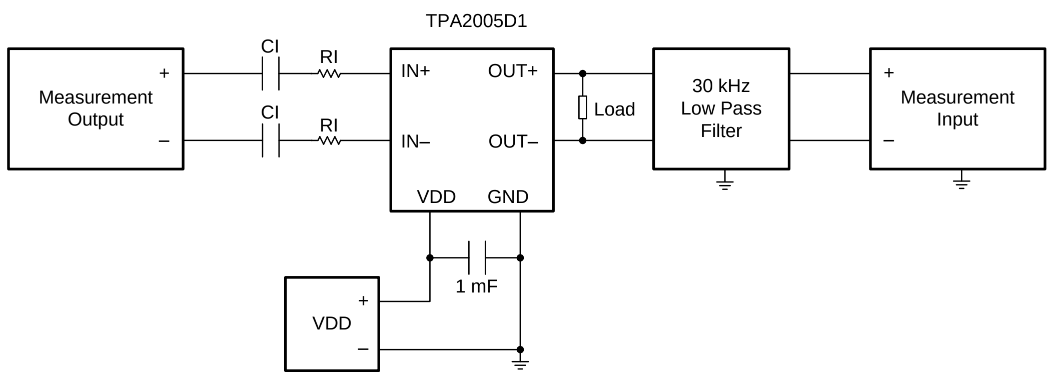


Figure 31. Common-mode Rejection Ratio vs Common-mode Input Voltage

8 Parameter Measurement Information



(1) CI was Shorted for any Common-Mode input voltage measurement .

(2) A 33-mH inductor was placed in series with the load resistor to emulate a small speaker for efficiency measurements.

(3) The 30-kHz low-pass filter is required even if the analyzer has a low-pass filter. An RC filter (100 W, 47 nF) is used on each output for the data sheet graphs.

Figure 32. Test Set-up for Graphs

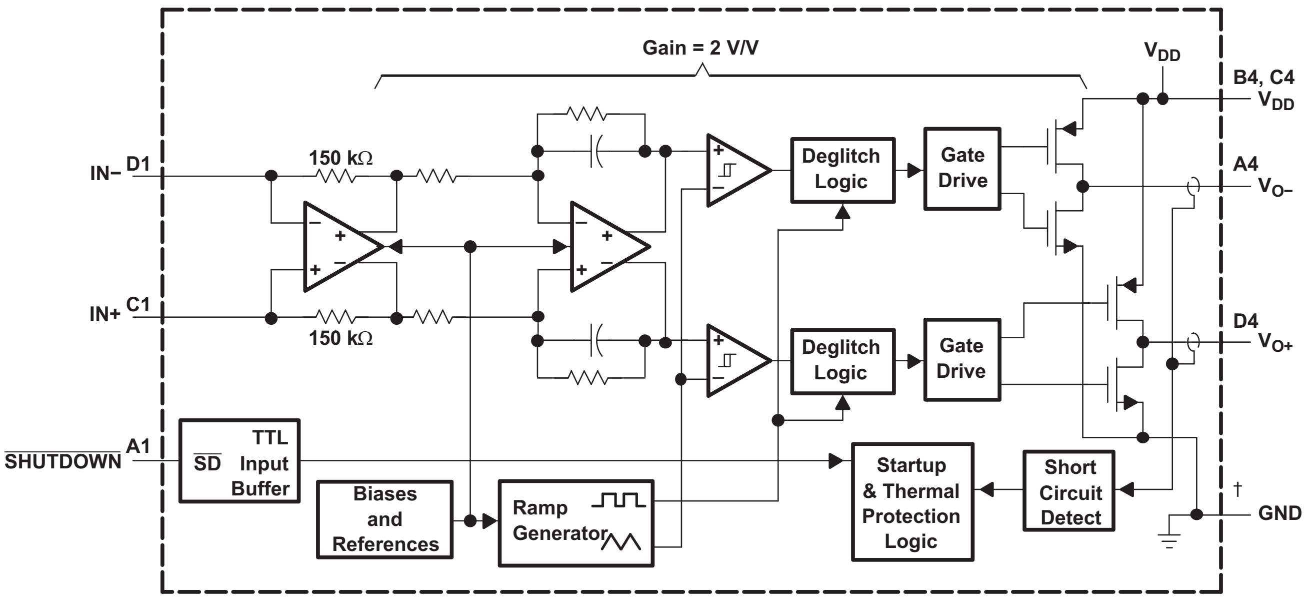
9 Detailed Description

9.1 Overview

The TPA2005D1 is a high-efficiency filter-free Class-D audio amplifier capable of delivering up to 1.4 W into 8-Ω loads with 5-V power supply. The fully-differential design of this amplifier avoids the usage of bypass capacitors and the improved CMRR eliminates the usage of input-coupling capacitors. This makes the device size a perfect choice for small, portable applications as only three external components are required.

The advanced modulation used in the TPA2005D1 PWM output stage eliminates the need for an output filter.

9.2 Functional Block Diagram



† A2, A3, B3, C2, C3, D2, D3
(terminal labels for MicroStar Junior™ package)

9.3 Feature Description

9.3.1 Fully Differential Amplifier

The TPA2005D1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common-mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage on the output that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common-mode voltage at the input. The fully differential TPA2005D1 can still be used with a single-ended input; however, the TPA2005D1 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Feature Description (continued)

9.3.1.1 Advantages of Fully Differential Amplifiers

- Input-coupling capacitors not required:
  – The fully differential amplifier allows the inputs to be biased at voltage other than mid-supply. For example, if a codec has a midsupply lower than the midsupply of the TPA2005D1, the common-mode feedback circuit will adjust, and the TPA2005D1 outputs will still be biased at midsupply of the TPA2005D1. The inputs of the TPA2005D1 can be biased from 0.5 V to V_{DD} - 0.8 V. If the inputs are biased outside of that range, input-coupling capacitors are required.
- Midsupply bypass capacitor, $C_{(BYPASS)}$, not required:
  – The fully differential amplifier does not require a bypass capacitor. This is because any shift in the midsupply affects both positive and negative channels equally and cancels at the differential output.
- Better RF-immunity:
  – GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

9.3.2 Efficiency and Thermal Information

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the 2,5-mm x 2,5-mm MicroStar Junior package is shown in the dissipation rating table. Converting this to θ_{JA}:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.016} = 62.5°\text{C/W} \quad (1)$$

Given θ_{JA} of 62.5°C/W, the maximum allowable junction temperature of 150°C, and the maximum internal dissipation of 0.2 W (worst case 5-V supply), the maximum ambient temperature can be calculated with equation Equation 2.

$$T_A\text{Max} = T_J\text{Max} - \theta_{JA}P_{Dmax} = 150 - 62.5\,(0.2) = 137.5°\text{C} \quad (2)$$

Equation Equation 2 shows that the calculated maximum ambient temperature is 137.5°C at maximum power dissipation with a 5-V supply; however, the maximum ambient temperature of the package is limited to 85°C. Because of the efficiency of the TPA2005D1, it can be operated under all conditions to an ambient temperature of 85°C. The TPA2005D1 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Also, using speakers more resistive than 8-Ω dramatically increases the thermal performance by reducing the output current and increasing the efficiency of the amplifier.

9.3.3 Eliminating the Output Filter with the TPA2005D1

This section focuses on why the user can eliminate the output filter with the TPA2005D1.

9.3.3.1 Effect on Audio

The class-D amplifier outputs a pulse-width modulated (PWM) square wave, which is the sum of the switching waveform and the amplified input audio signal. The human ear acts as a band-pass filter such that only the frequencies between approximately 20 Hz and 20 kHz are passed. The switching frequency components are much greater than 20 kHz, so the only signal heard is the amplified input audio signal.

9.3.3.2 Traditional Class-D Modulation Scheme

The traditional class-D modulation scheme, which is used in the TPA005Dxx family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, V_{DD}. Therefore, the differential pre-filtered output varies between positive and negative V_{DD}, where filtered 50% duty cycle yields 0 volts across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 33. Note that even at an average of 0 volts across the load (50% duty cycle), the current to the load is high causing a high loss and thus causing a high supply current.

Feature Description (continued)

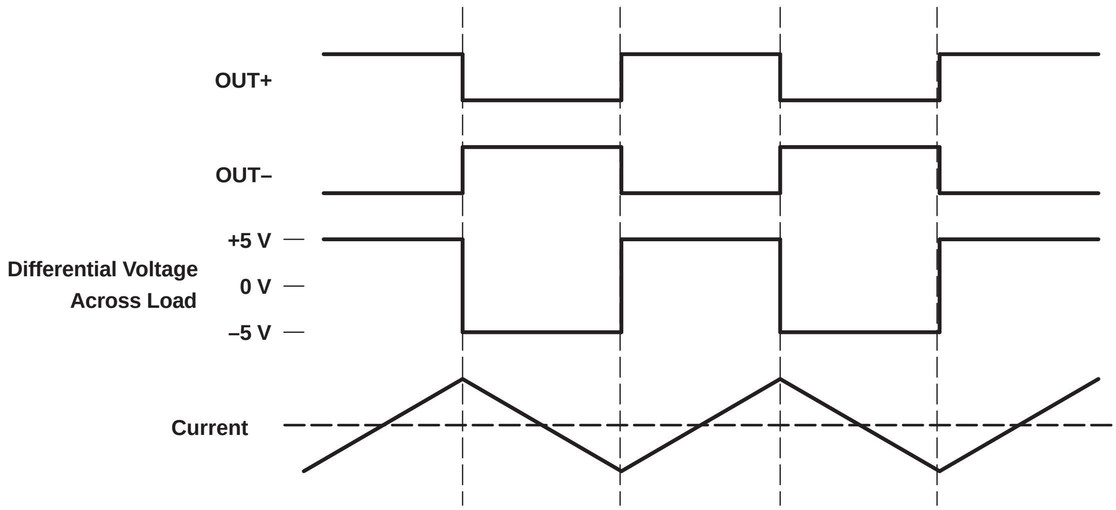


Figure 33. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms Into an Inductive Load With no Input

9.3.3.3 TPA2005D1 Modulation Scheme

The TPA2005D1 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUT+ and OUT- are now in phase with each other with no input. The duty cycle of OUT+ is greater than 50% and OUT- is less than 50% for positive voltages. The duty cycle of OUT+ is less than 50% and OUT- is greater than 50% for negative voltages. The voltage across the load sits at 0 volts throughout most of the switching period greatly reducing the switching current, which reduces any I^2R losses in the load.

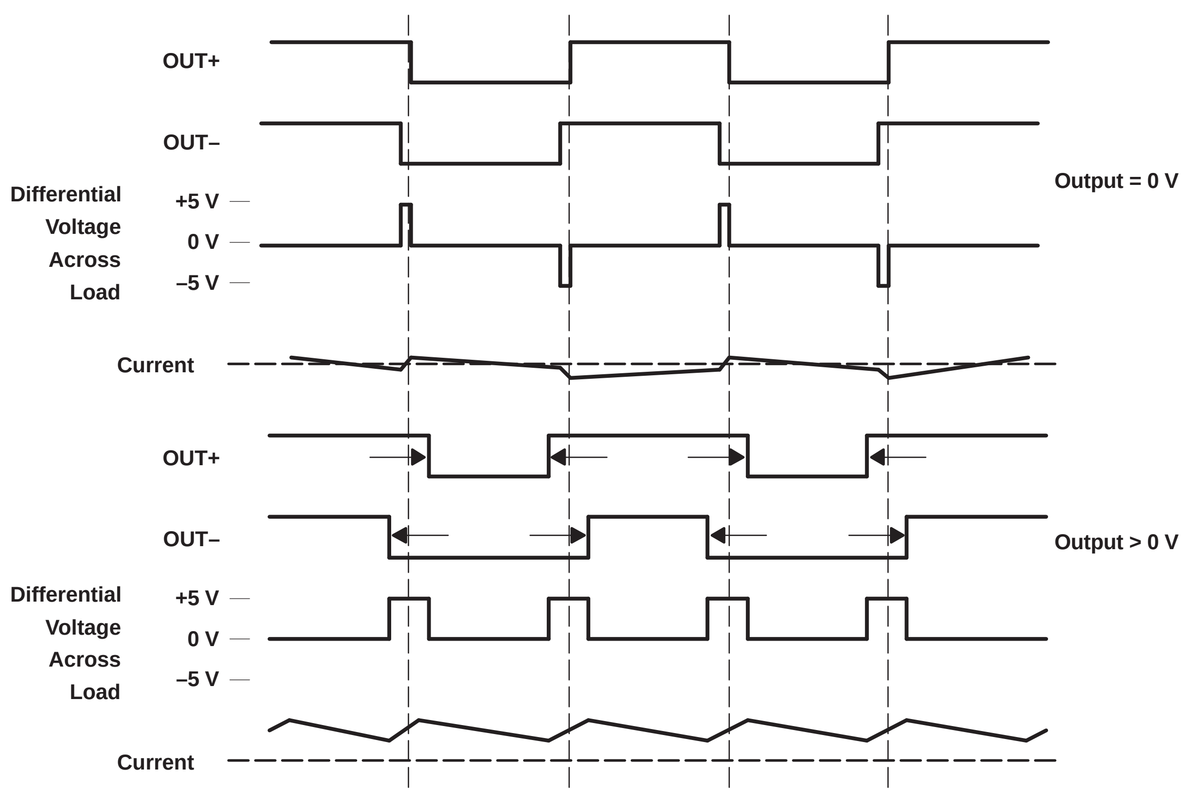


Figure 34. The TPA2005D1 Output Voltage and Current Waveforms Into an Inductive Load

Feature Description (continued)

9.3.3.4 Efficiency: Why You Must Use a Filter With the Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2 × V_{DD} and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA2005D1 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{DD} instead of 2 × V_{DD}. As the output power increases, the pulses widen making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance than the speaker that results in less power dissipated, which increases efficiency.

9.3.3.5 Effects of Applying a Square Wave Into a Speaker

If the amplitude of a square wave is high enough and the frequency of the square wave is within the bandwidth of the speaker, a square wave could cause the voice coil to jump out of the air gap and/or scar the voice coil. A 250-kHz switching frequency, however, is not significant because the speaker cone movement is proportional to $1/f^2$ for frequencies beyond the audio band. Therefore, the amount of cone movement at the switching frequency is small. However, damage could occur to the speaker if the voice coil is not designed to handle the additional power. To size the speaker for added power, the ripple current dissipated in the load needs to be calculated by subtracting the theoretical supplied power, $P_{SUP\ THEORETICAL}$, from the actual supply power, P_{SUP}, at maximum output power, P_{OUT}. The switching power dissipated in the speaker is the inverse of the measured efficiency,$\eta_{MEASURED}$, minus the theoretical efficiency,$\eta_{THEORETICAL}$.

$$P_{SPKR} = P_{SUP} - P_{SUP\ THEORETICAL} \text{ (at max output power)} \quad (3)$$

$$P_{SPKR} = \frac{P_{SUP}}{P_{OUT}} - \frac{P_{SUP\ THEORETICAL}}{P_{OUT}} \text{ (at max output power)} \quad (4)$$

$$P_{SPKR} = P_{OUT}\left(\frac{1}{\eta_{MEASURED}} - \frac{1}{\eta_{THEORETICAL}}\right) \text{ (at max output power)} \quad (5)$$

$$\eta_{THEORETICAL} = \frac{R_L}{R_L + 2r_{DS(on)}} \text{ (at max output power)} \quad (6)$$

The maximum efficiency of the TPA2005D1 with a 3.6 V supply and an 8-Ω load is 86% from equation Equation 6. Using equation Equation 5 with the efficiency at maximum power (84%), we see that there is an additional 17 mW dissipated in the speaker. The added power dissipated in the speaker is not an issue as long as it is taken into account when choosing the speaker.

9.3.3.6 When to Use an Output Filter

Design the TPA2005D1 without an output filter if the traces from amplifier to speaker are short. The TPA2005D1 passed FCC and CE radiated emissions with no shielding with speaker trace wires 100 mm long or less. Wireless handsets and PDAs are great applications for class-D without a filter.

A ferrite bead filter can often be used if the design is failing radiated emissions without an LC filter, and the frequency sensitive circuit is greater than 1 MHz. This is good for circuits that just have to pass FCC and CE because FCC and CE only test radiated emissions greater than 30 MHz. If choosing a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low frequency (< 1 MHz) EMI sensitive circuits and/or there are long leads from amplifier to speaker.

Figure 35 and Figure 36 show typical ferrite bead and LC output filters.

Feature Description (continued)

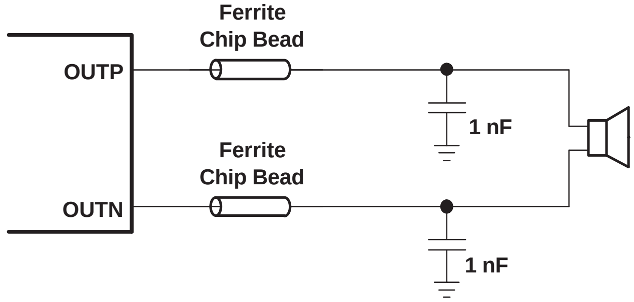


Figure 35. Typical Ferrite Chip Bead Filter (Chip bead example: NEC/Tokin: N2012ZPS121)

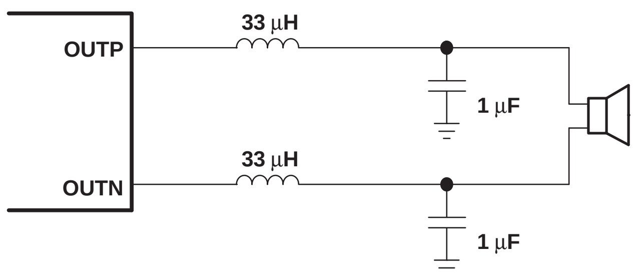


Figure 36. Typical LC Output Filter, Cutoff Frequency of 27 kHz

9.3.4 Thermal and Short-Circuit Protection

The TPA2005D1 features thermal and short-circuit protection. When the protection circuit is triggered, the device will enter in shutdown mode, setting the outputs of the device into high impedance. Thermal protection turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC.

9.4 Device Functional Modes

9.4.1 Summing Input Signals with the TPA2005D1

Most wireless phones or PDAs need to sum signals at the audio power amplifier or just have two signal sources that need separate gain. The TPA2005D1 makes it easy to sum signals or use separate signal sources with different gains. Many phones now use the same speaker for the earpiece and ringer, where the wireless phone would require a much lower gain for the phone earpiece than for the ringer. PDAs and phones that have stereo headphones require summing of the right and left channels to output the stereo signal to the mono speaker.

9.4.1.1 Summing Two Differential Input Signals

Two extra resistors are needed for summing differential signals (a total of 5 components). The gain for each input source can be set independently (see equations Equation 7 and Equation 8, and Figure 37).

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = 2 \times \frac{150\text{ k}}{R_{I1}}\left(\frac{V}{V}\right) \tag{7}$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = 2 \times \frac{150\text{ k}}{R_{I2}}\left(\frac{V}{V}\right) \tag{8}$$

If summing left and right inputs with a gain of 1 V/V, use $R_{I1} = R_{I2} = 300\ k\Omega$.

This configuration will use resistor values of $R_{I1} = 3\ M\Omega$, and $R_{I2} = 150\ k\Omega$

Device Functional Modes (continued)

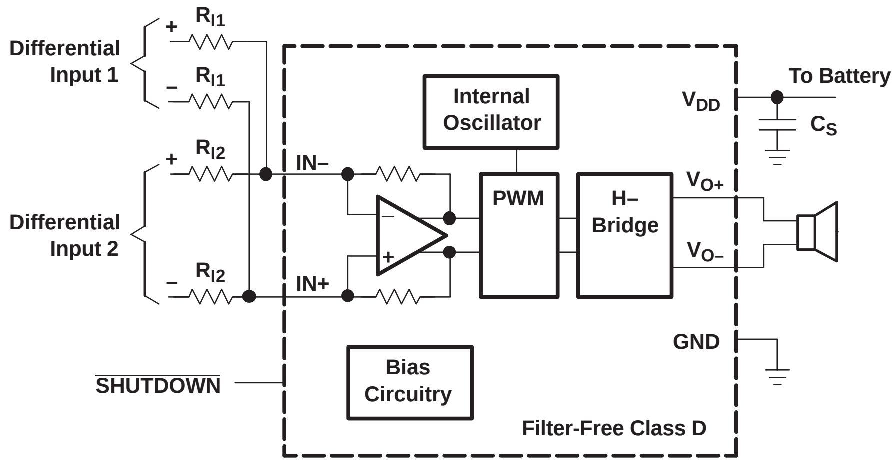


Figure 37. Application Schematic With TPA2005D1 Summing Two Differential Inputs

9.4.1.2 Summing a Differential Input Signal and a Single-Ended Input Signal

Figure 38 shows how to sum a differential input signal and a single-ended input signal. Ground noise can couple in through IN+ with this method. It is better to use differential inputs. The corner frequency of the single-ended input is set by C_{I2}, shown in equation Equation 11. To assure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use.

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = 2 \times \frac{150\text{ k}}{R_{I1}} \left(\frac{V}{V}\right) \tag{9}$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = 2 \times \frac{150\text{ k}}{R_{I2}} \left(\frac{V}{V}\right) \tag{10}$$

$$C_{I2} = \frac{1}{\left(2\pi \times R_{I2} \times f_{c2}\right)} \tag{11}$$

Device Functional Modes (continued)

If summing a ring tone and a phone signal, the phone signal should use a differential input signal while the ring tone might be limited to a single-ended signal. Phone gain is set at gain 1 = 0.1 V/V, and the ring-tone gain is set to gain 2 = 2 V/V, The resistor values are R_{I1} = 3 MΩ and R_{I2} = 150 kΩ.

The high pass corner frequency of the single-ended input is set by C_{I2}. If the desired corner frequency is less than 20 Hz.

$$C_{I2} > \frac{1}{(2\pi \times 150k\Omega \times 20Hz)} \quad (12)$$

$$C_{I2} > 53nF \quad (13)$$

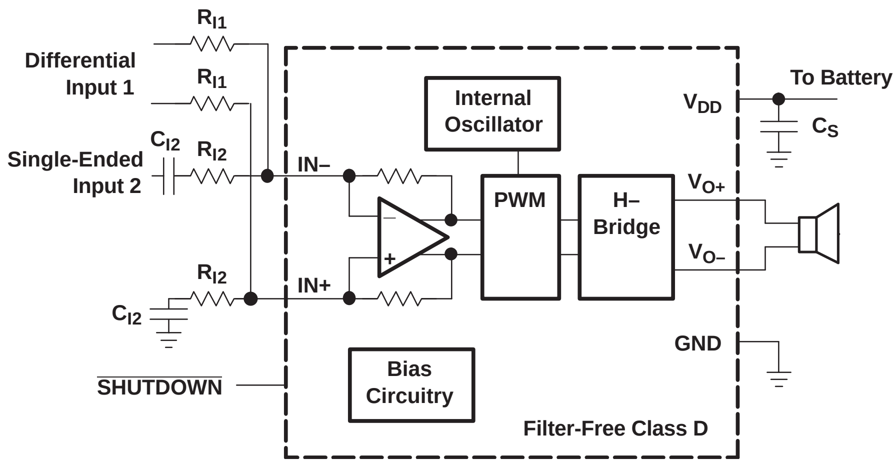


Figure 38. Application Schematic With TPA2005D1 Summing Differential Input and Single-Ended Input Signals

9.4.1.3 Summing Two Single-Ended Input Signals

Four resistors and three capacitors are needed for summing single-ended input signals. The gain and corner frequencies (f_{c1} and f_{c2}) for each input source can be set independently (see equations through Equation 17, and Figure 39). Resistor, R_P, and capacitor, C_P, are needed on the IN+ terminal to match the impedance on the IN- terminal. The single-ended inputs must be driven by low impedance sources even if one of the inputs is not outputting an ac signal.

$$\text{Gain 1} = \frac{V_O}{V_{I1}} = 2 \times \frac{150\text{ k}}{R_{I1}}\left(\frac{V}{V}\right) \quad (14)$$

$$\text{Gain 2} = \frac{V_O}{V_{I2}} = 2 \times \frac{150\text{ k}}{R_{I2}}\left(\frac{V}{V}\right) \quad (15)$$

$$C_{I1} = \frac{1}{(2\pi \times R_{I1} \times f_{c1})} \quad (16)$$

$$C2 = \frac{1}{(2\pi \times R_{I2} \times f_{c2})} \quad (17)$$

$$C_P = C_{I1} + C_{I2} \quad (18)$$

$$R_P = \frac{R_{I1} \times R_{I2}}{(R_{I1} + R_{I2})} \quad (19)$$

Device Functional Modes (continued)

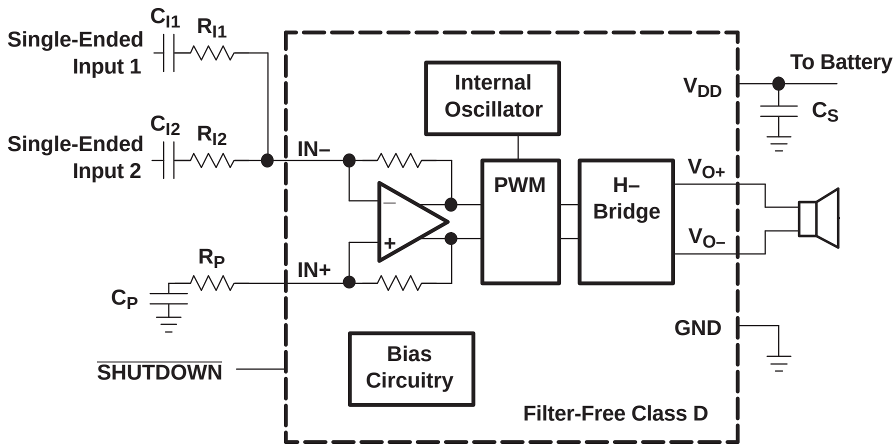


Figure 39. Application Schematic With TPA2005D1 Summing Two Single-Ended Inputs

9.4.2 Shutdown Mode

The TPA2005D1 can be put in shutdown mode when asserting SHUTDOWN pin to a logic LOW. While in shutdown mode, the device output stage is turned off and set into high impedance, making the current consumption very low. The device exits shutdown mode when a HIGH logic level is applied to SHUTDOWN pin.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

These typical connection diagrams highlight the required external components and system level connections for proper operation of the device in several popular use cases.

Each of these configurations can be realized using the Evaluation Modules (EVMs) for the device. These flexible modules allow full evaluation of the device in the most common modes of operation. Any design variation can be supported by TI through schematic and layout reviews. Visit http://e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information.

10.2 Typical Applications

These application circuits detail the recommended component selection and board configurations for the TPA2005D1 device.

10.2.1 TPA2005D1 with Differential Input

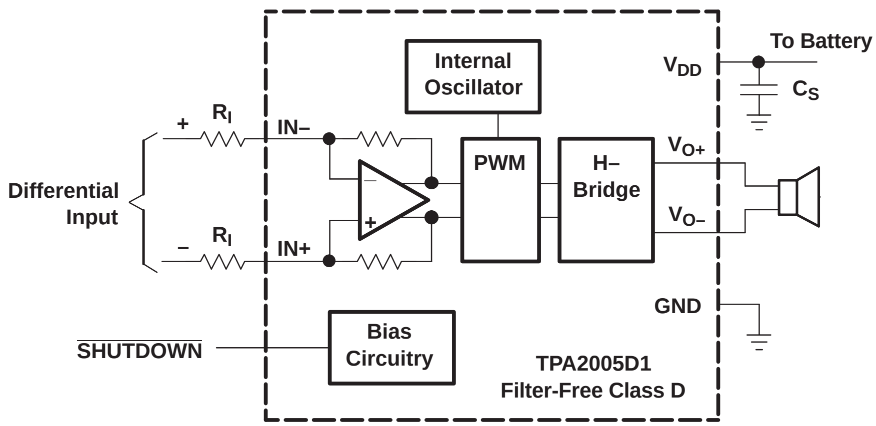


Figure 40. Typical TPA2005D1 Differential Input for a Wireless Phone

10.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Requirements

PARAMETER	EXAMPLE
Power Supply	5 V
Shutdown Input	High > 2 V
	Low < 0.8 V
Speaker	8 Ω

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Component Selection

Figure 40 shows the TPA2005D1 typical schematic with differential inputs and Figure 42 shows the TPA2005D1 with differential inputs and input capacitors, and Figure 43 shows the TPA2005D1 with single-ended inputs. Differential inputs should be used whenever possible because the single-ended inputs are much more susceptible to noise.

Table 2. Typical Component Values

REF DES	VALUE	EIA SIZE	MANUFACTURER	PART NUMBER
R_I	150 kΩ (±0.5%)	0402	Panasonic	ERJ2RHD154V
C_S	1 μF (+22%, -80%)	0402	Murata	GRP155F50J105Z
C_I (1)	3.3 nF (±10%)	0201	Murata	GRP033B10J332K

(1) C_I is only needed for single-ended input or if V_{ICM} is not between 0.5 V and V_{DD} - 0.8 V. C_I = 3.3 nF (with R_I = 150 kΩ) gives a high-pass corner frequency of 321 Hz.

10.2.1.2.2 Input Resistors (R_I)

The input resistors (R_I) set the gain of the amplifier according to equation Equation 20.

$$\text{Gain} = 2 \times \frac{150\text{ k}}{R_I} \tag{20}$$

Resistor matching is important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

Place the input resistors close to the TPA2005D1 to limit noise injection on the high-impedance nodes.

For optimal performance the gain should be set to 2 V/V or lower. Lower gain allows the TPA2005D1 to operate at its best, and keeps a high voltage at the input making the inputs less susceptible to noise.

10.2.1.2.3 Decoupling Capacitor (C_S)

The TPA2005D1 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 μF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the TPA2005D1 is important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10 μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

10.2.1.3 Application Curves

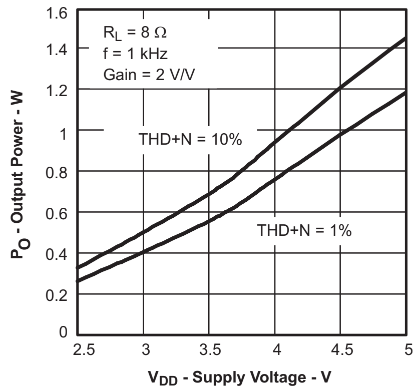


Figure 41. Output Power vs Supply Voltage

10.2.2 TPA2005D1 with Differential Input and Input Capacitors

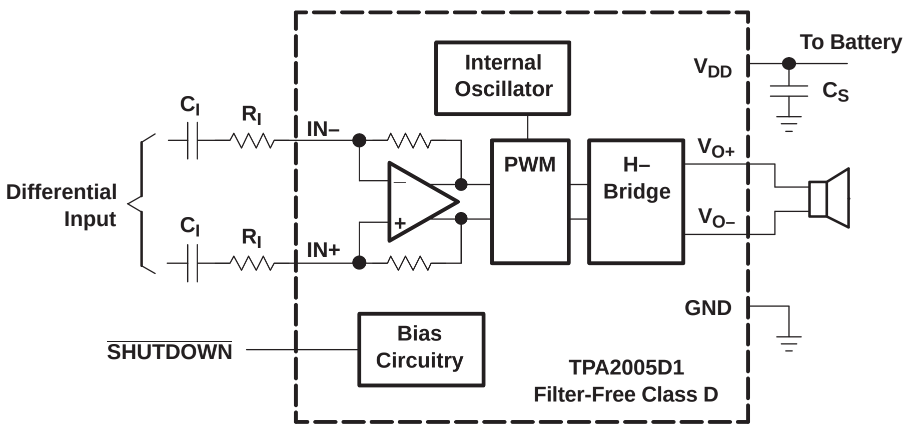


Figure 42. TPA2005D1 Differential Input and Input Capacitors

10.2.2.1 Design Requirements

Please see *Design Requirements*.

10.2.2.2 Detailed Design Procedure

Please see *Detailed Design Procedure*.

10.2.2.2.1 Input Capacitors (C_I)

The TPA2005D1 does not require input coupling capacitors if the design uses a differential source that is biased from 0.5 V to V_{DD} - 0.8 V (shown in Figure 40). If the input signal is not biased within the recommended common-mode input range, if needing to use the input as a high pass filter (shown in Figure 42), or if using a single-ended source (shown in Figure 43), input coupling capacitors are required.

The input capacitors and input resistors form a high-pass filter with the corner frequency, f_c, determined in equation Equation 21.

$$f_c = \frac{1}{(2\pi \times R_I \times C_I)} \tag{21}$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application.

Equation Equation 22 is reconfigured to solve for the input coupling capacitance.

$$C_I = \frac{1}{(2\pi \times R_I \times f_c)} \tag{22}$$

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below, and causes pop. Any capacitor in the audio path should have a rating of X7R or better.

For a flat low-frequency response, use large input coupling capacitors (1 μF). However, in a GSM phone the ground signal is fluctuating at 217 Hz, but the signal from the codec does not have the same 217 Hz fluctuation. The difference between the two signals is amplified, sent to the speaker, and heard as a 217 Hz hum.

10.2.3 TPA2005D1 with Single-Ended Input

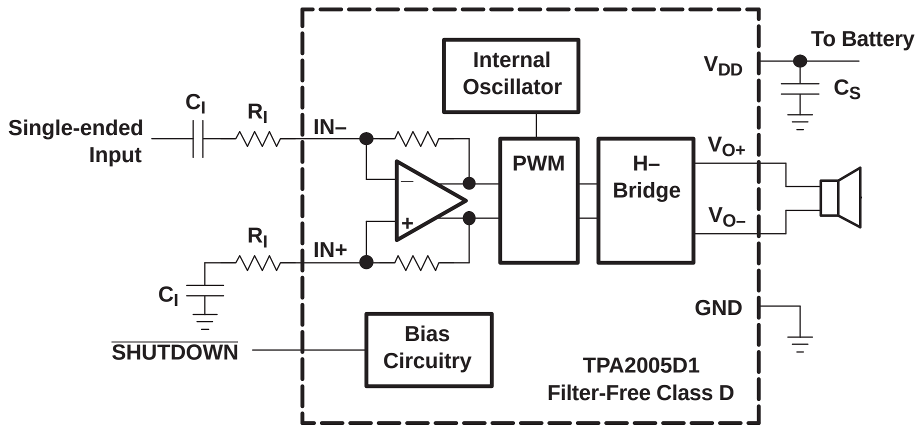


Figure 43. TPA2005D1 Single-Ended Input

10.2.3.1 Design Requirements

Please see *Design Requirements*.

10.2.3.2 Detailed Design Procedure

Please see *Detailed Design Procedure*.

11 Power Supply Recommendations

The TPA2005D1 is designed to operate from an input voltage supply range between 2.5-V and 5.2-V. Therefore, the output voltage range of power supply should be within this range and well regulated. The current capability of upper power should not exceed the maximum current limit of the power switch.

11.1 Power Supply Decoupling Capacitors

The TPA2005D1 requires adequate power supply decoupling to ensure a high efficiency operation with low total harmonic distortion (THD). Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, within 2 mm of the V_{DD} pin. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. In addition to the 0.1 µF ceramic capacitor, is recommended to place a 2.2 µF to 10 µF capacitor on the VDD supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

12 Layout

12.1 Layout Guidelines

12.1.1 Component Location

Place all the external components close to the TPA2005D1. The input resistors need to be close to the TPA2005D1 input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the TPA2005D1. Placing the decoupling capacitor, C_S, close to the TPA2005D1 is important for the efficiency of the class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

12.1.2 Trace Width

Make the high current traces going to pins VDD, GND, V_{O+} and V_{O-} of the TPA2005D1 have a minimum width of 0,7 mm. If these traces are too thin, the TPA2005D1's performance and output power will decrease. The input traces do not need to be wide, but do need to run side-by-side to enable common-mode noise cancellation.

12.1.3 MicroStar Junior™ BGA Specifications

Use the following MicroStar Junior BGA ball diameters:

- 0,25 mm diameter solder mask
- 0,28 mm diameter solder paste mask/stencil
- 0,38 mm diameter copper trace

Figure 44 shows how to lay out a board for the TPA2005D1 MicroStar Junior BGA.

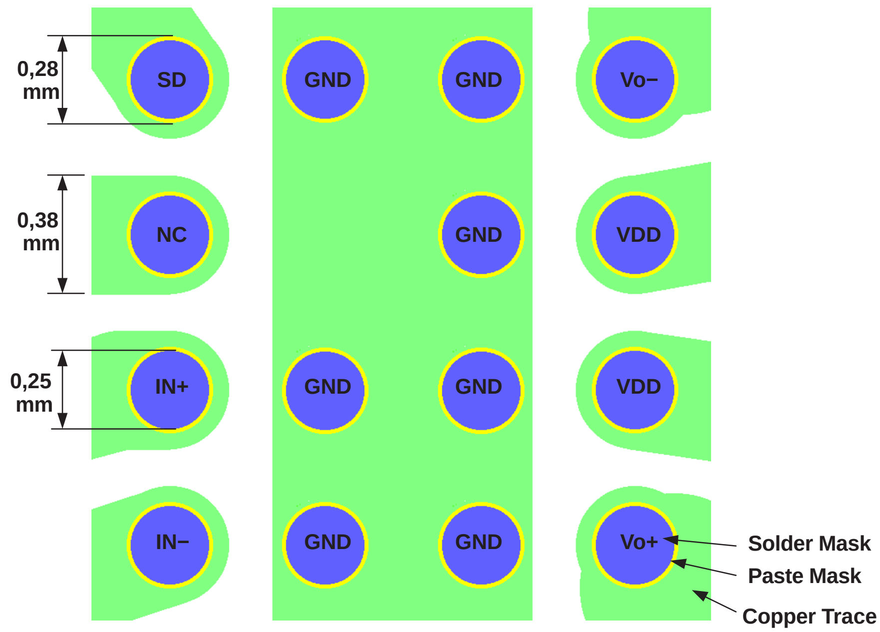


Figure 44. TPA2005D1 MicroStar Junior BGA Board Layout (Top View)

12.2 Layout Examples

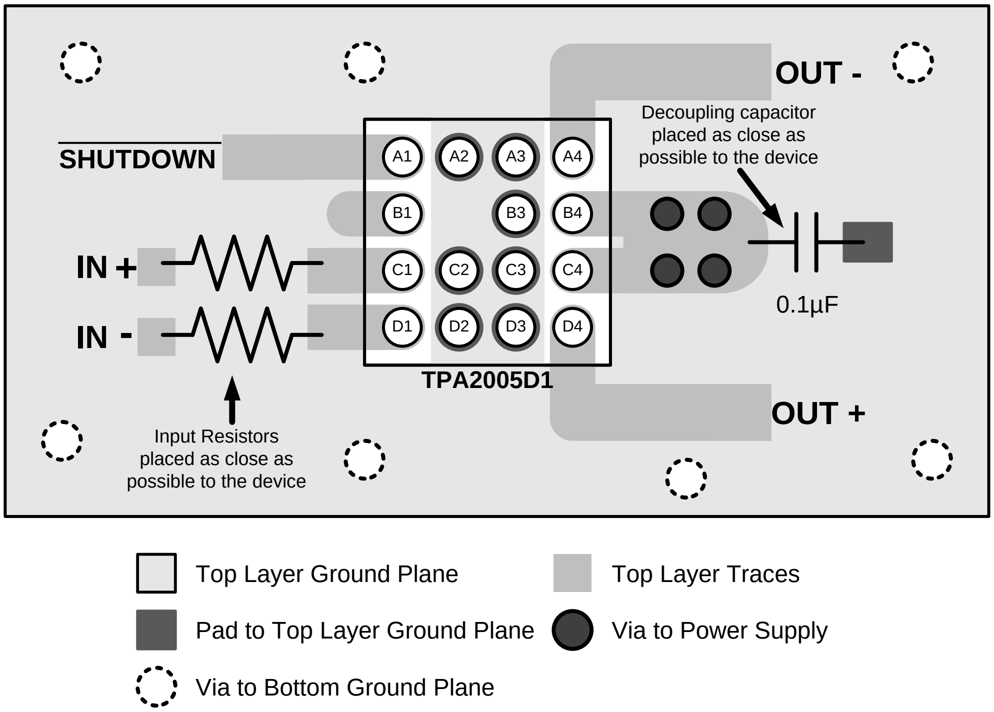


Figure 45. TPA2005D1 MicroStar Junior™ BGA Package Layout Example

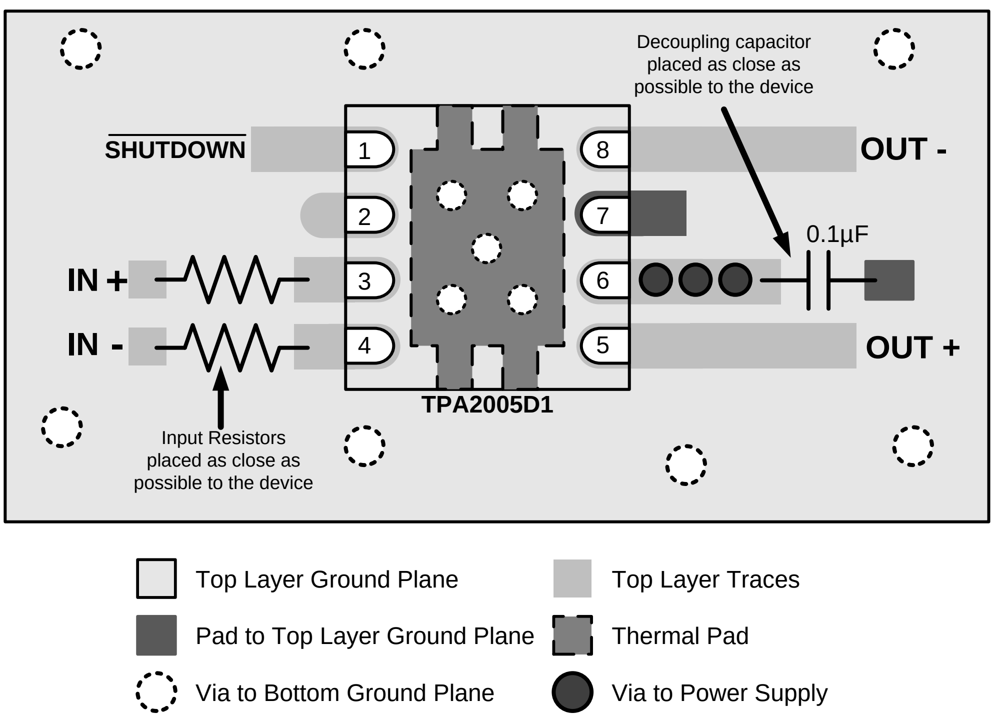


Figure 46. TPA2005D1 DRB Package Layout Example

Layout Examples (continued)

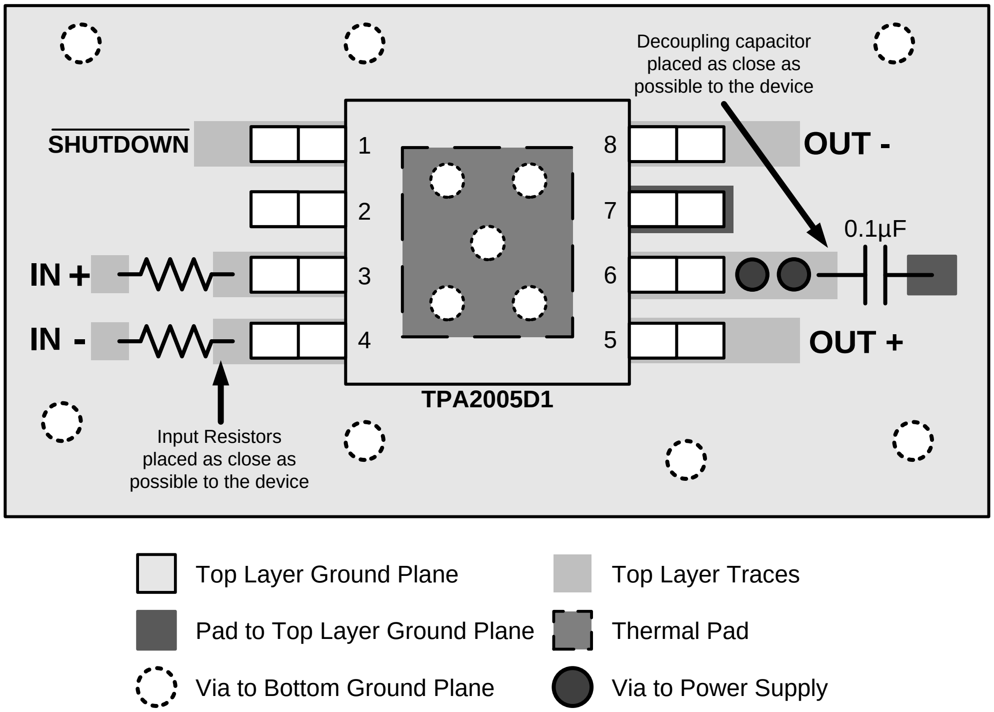


Figure 47. TPA2005D1 DGN Package Layout Example

13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

MicroStar Junior, PowerPAD, E2E are trademarks of Texas Instruments.
is a trademark of ~ Texas Instruments Incorporated.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA2005D1DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BAL	Samples
TPA2005D1DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BAL	Samples
TPA2005D1DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BAL	Samples
TPA2005D1DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIQ	Samples
TPA2005D1DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BIQ	Samples
TPA2005D1GQYR	ACTIVE	BGA MICROSTAR JUNIOR	GQY	15	2500	TBD	SNPB	Level-2-235C-1 YEAR	-40 to 85	PB051	Samples
TPA2005D1ZQYR	ACTIVE	BGA MICROSTAR JUNIOR	ZQY	15	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	AAFI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPA2005D1 :

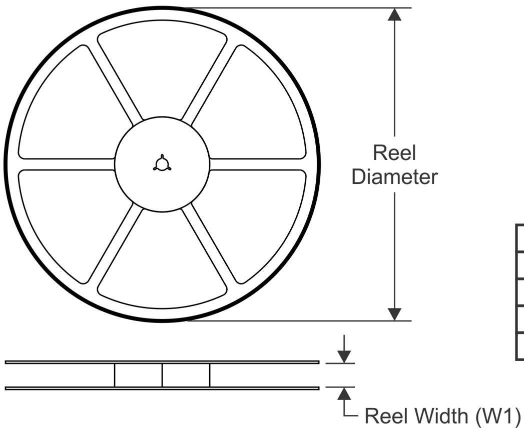
- Automotive: TPA2005D1-Q1

NOTE: Qualified Version Definitions:

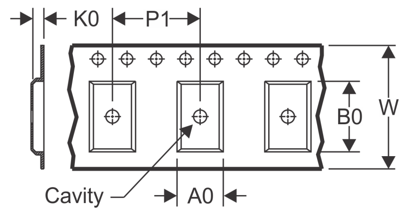
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

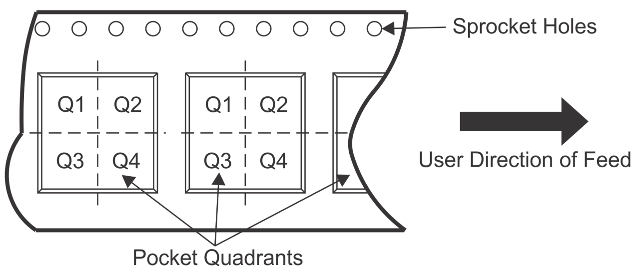


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

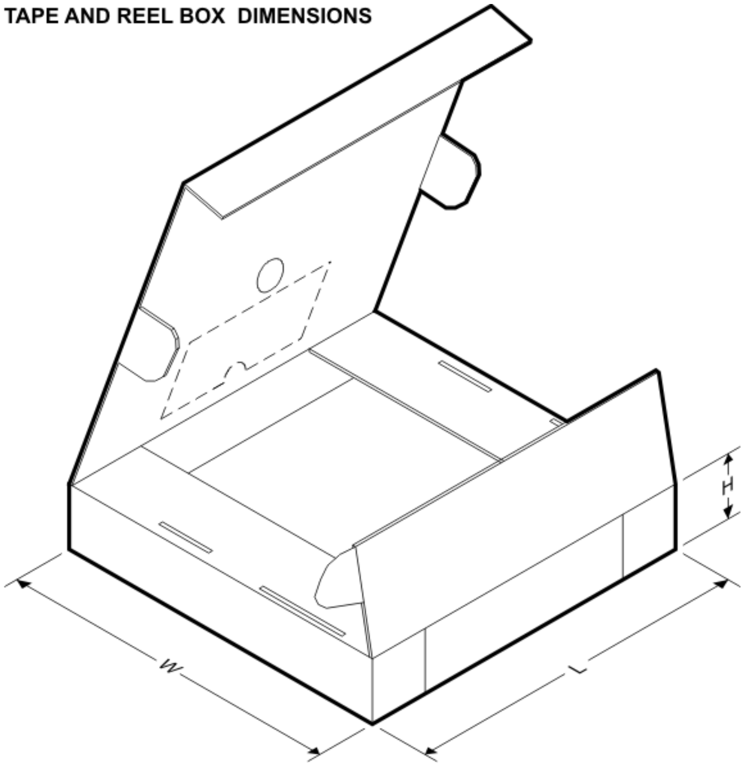
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA2005D1DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA2005D1DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA2005D1DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA2005D1GQYR	BGA MI CROSTA R JUNI OR	GQY	15	2500	330.0	8.4	2.8	2.8	1.25	4.0	8.0	Q1
TPA2005D1ZQYR	BGA MI CROSTA R JUNI OR	ZQY	15	2500	330.0	8.4	2.8	2.8	1.25	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA2005D1DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
TPA2005D1DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPA2005D1DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPA2005D1GQYR	BGA MICROSTAR JUNIOR	GQY	15	2500	338.1	338.1	20.6
TPA2005D1ZQYR	BGA MICROSTAR JUNIOR	ZQY	15	2500	338.1	338.1	20.6

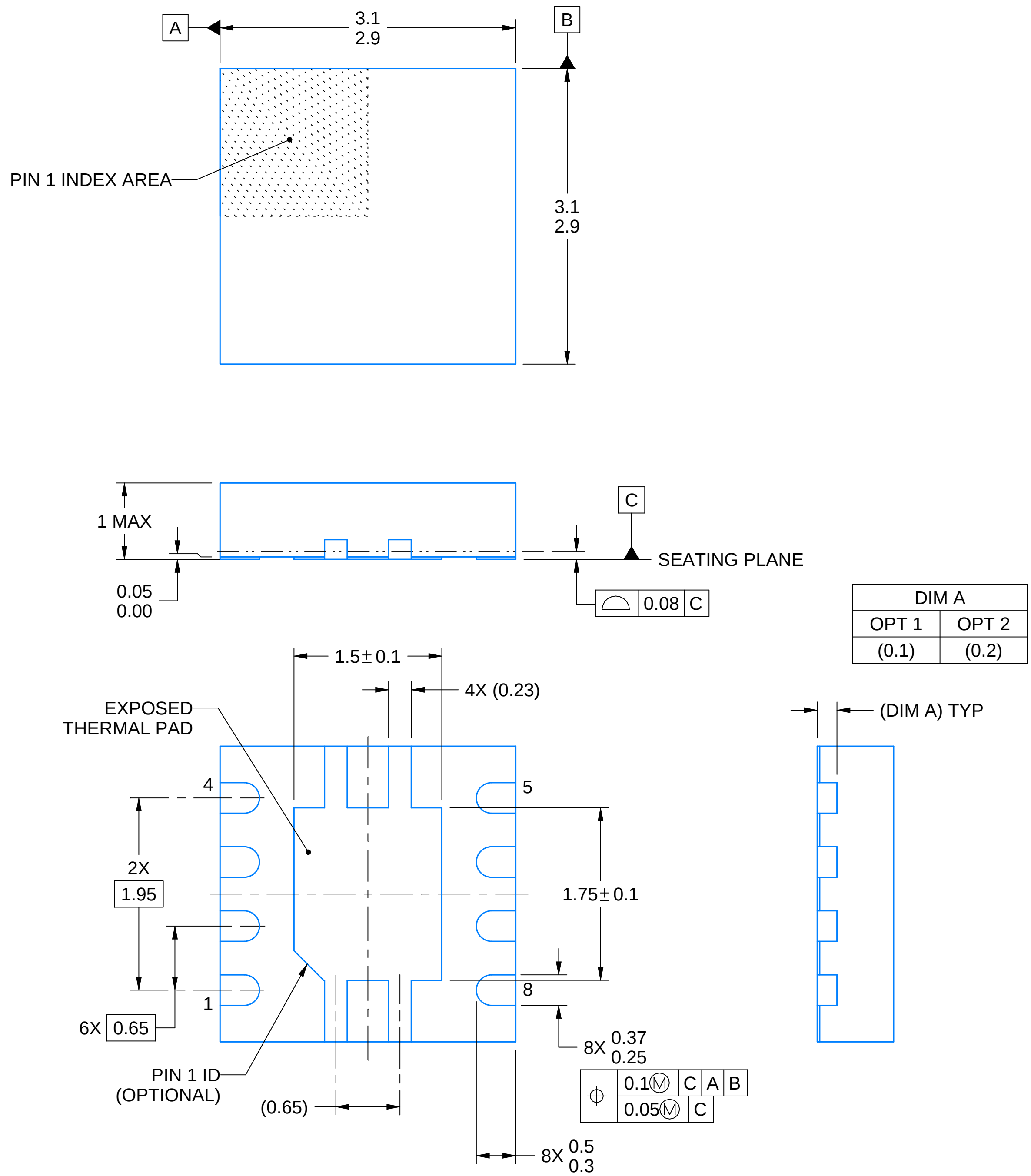
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

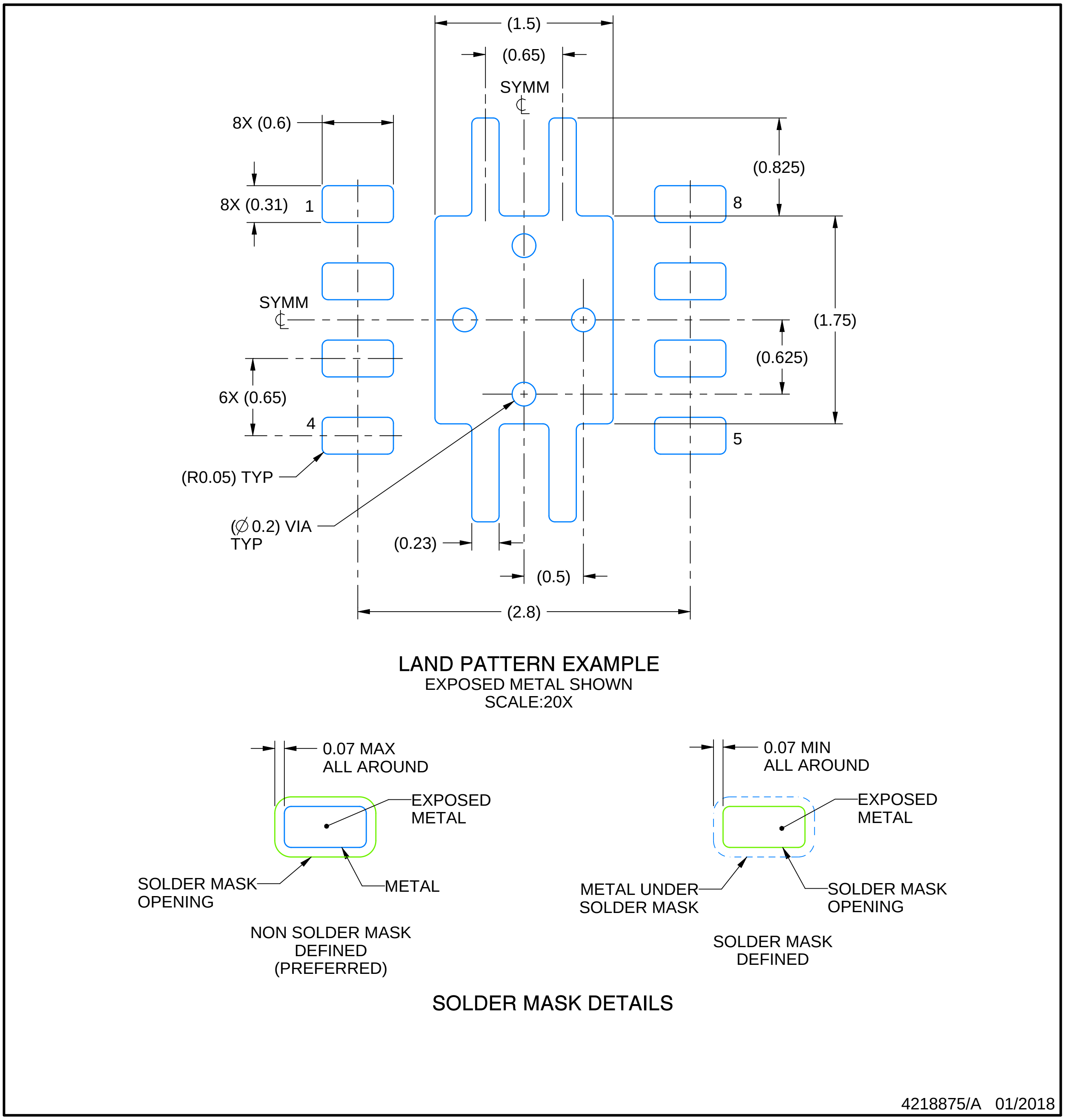
PLASTIC SMALL OUTLINE - NO LEAD



4218875/A 01/2018

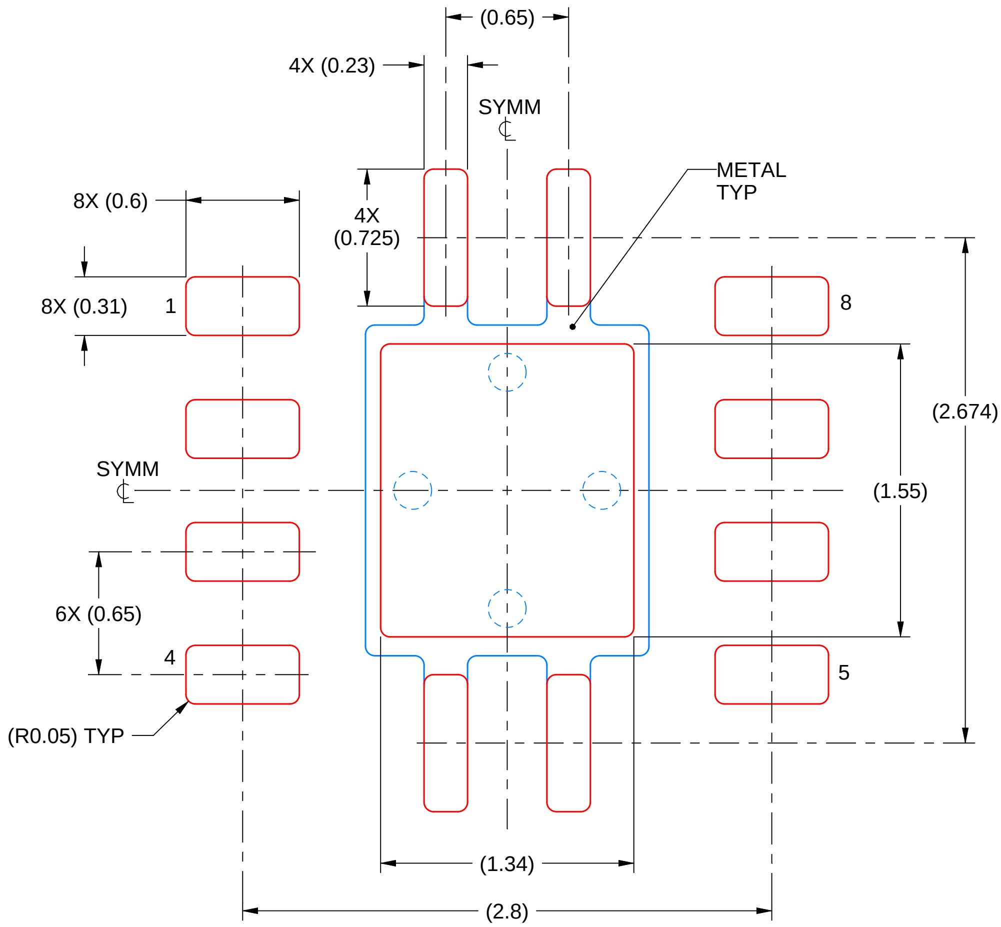
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

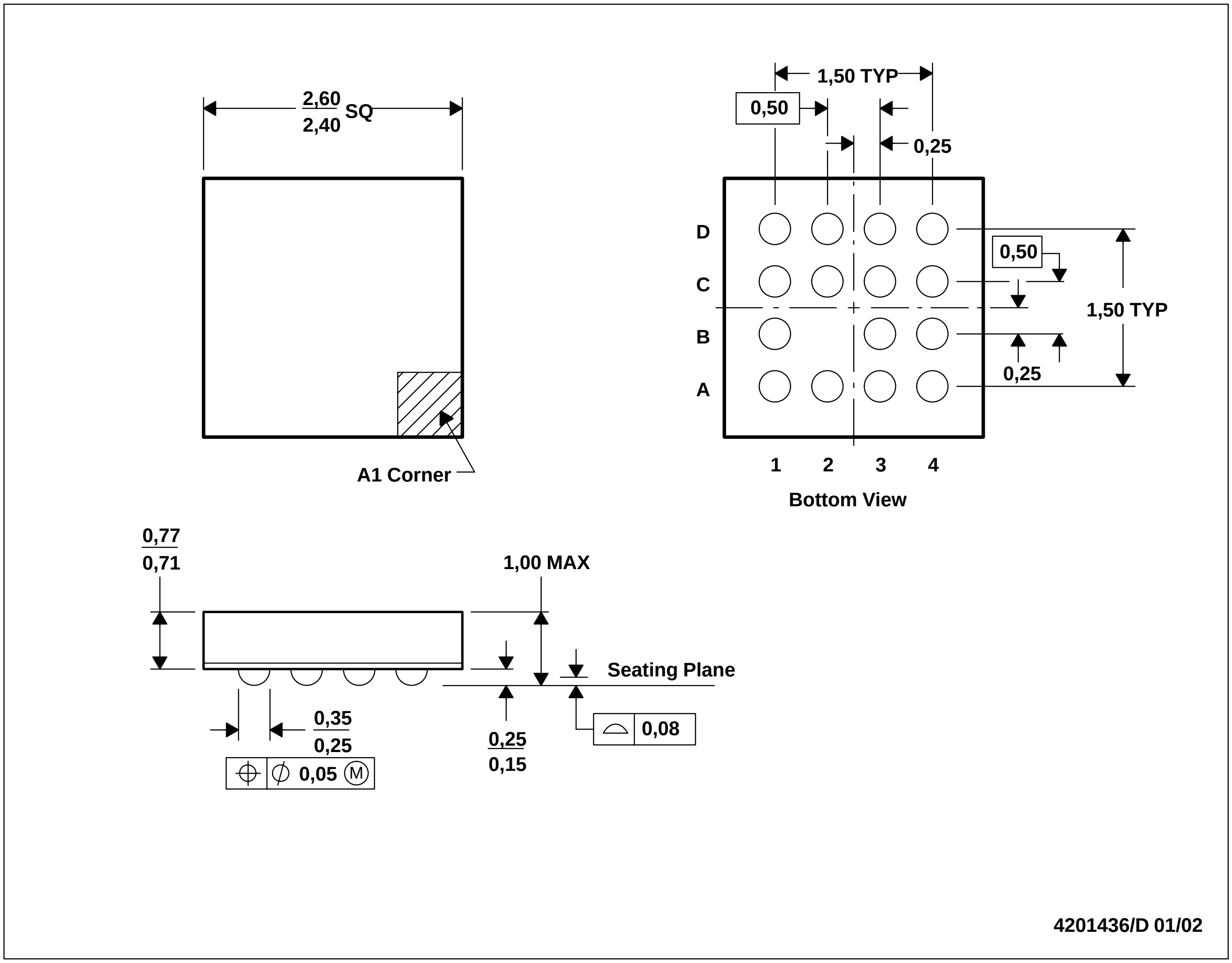
EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

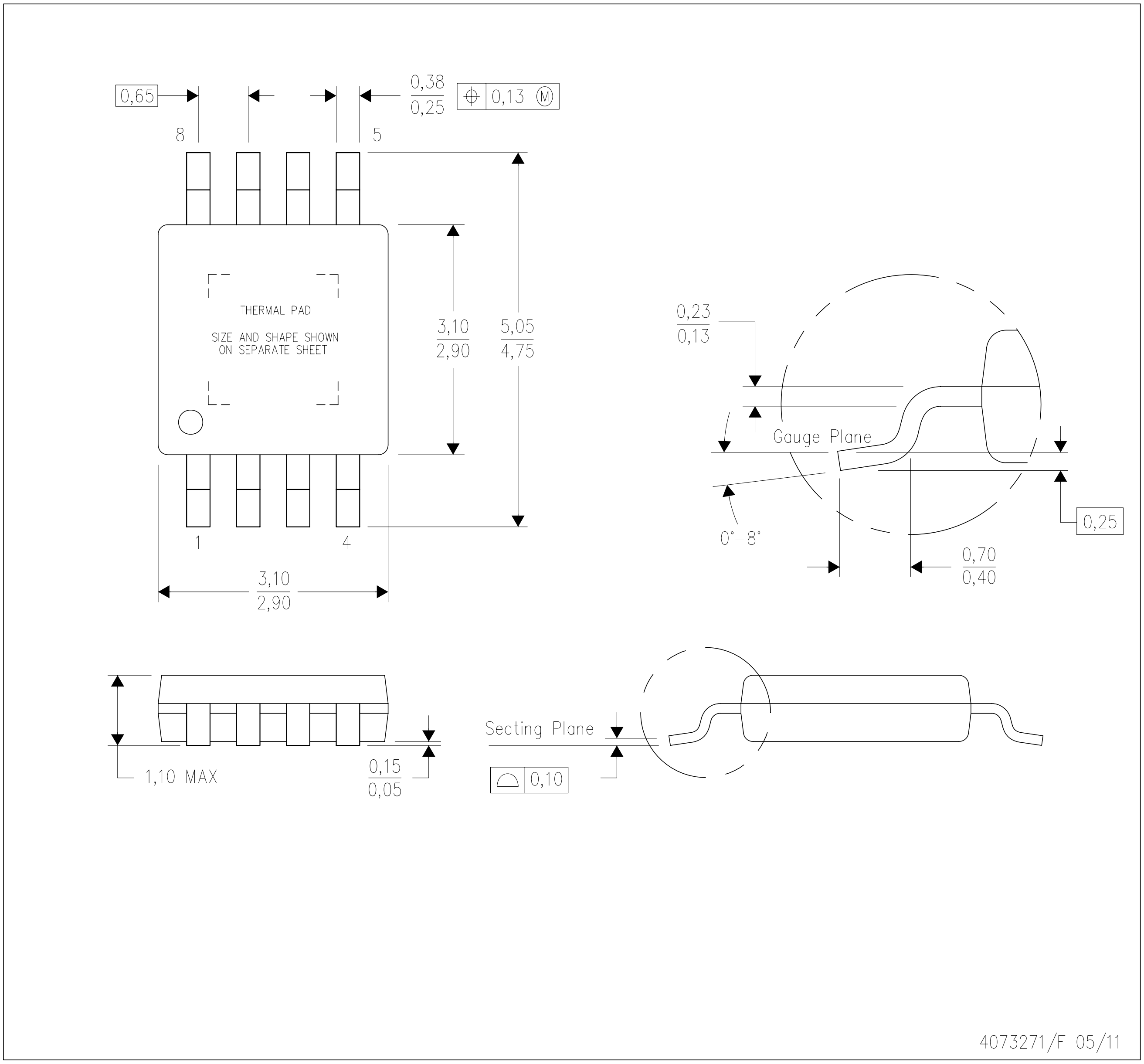
GQY (S-PBGA-N15) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ configuration
D. Falls within JEDEC MO-225

MicroStar Junior is a trademark of Texas Instruments.

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-187 variation AA-T

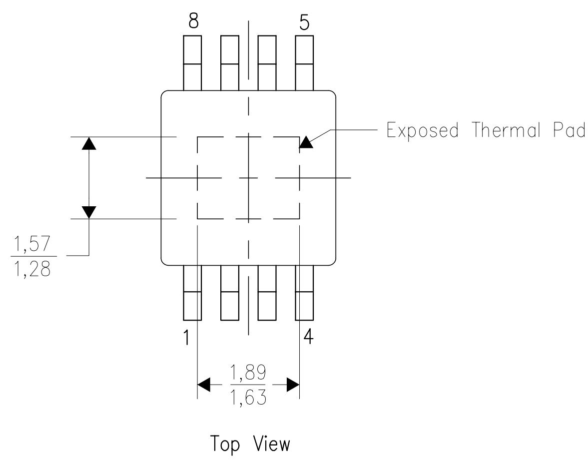
DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



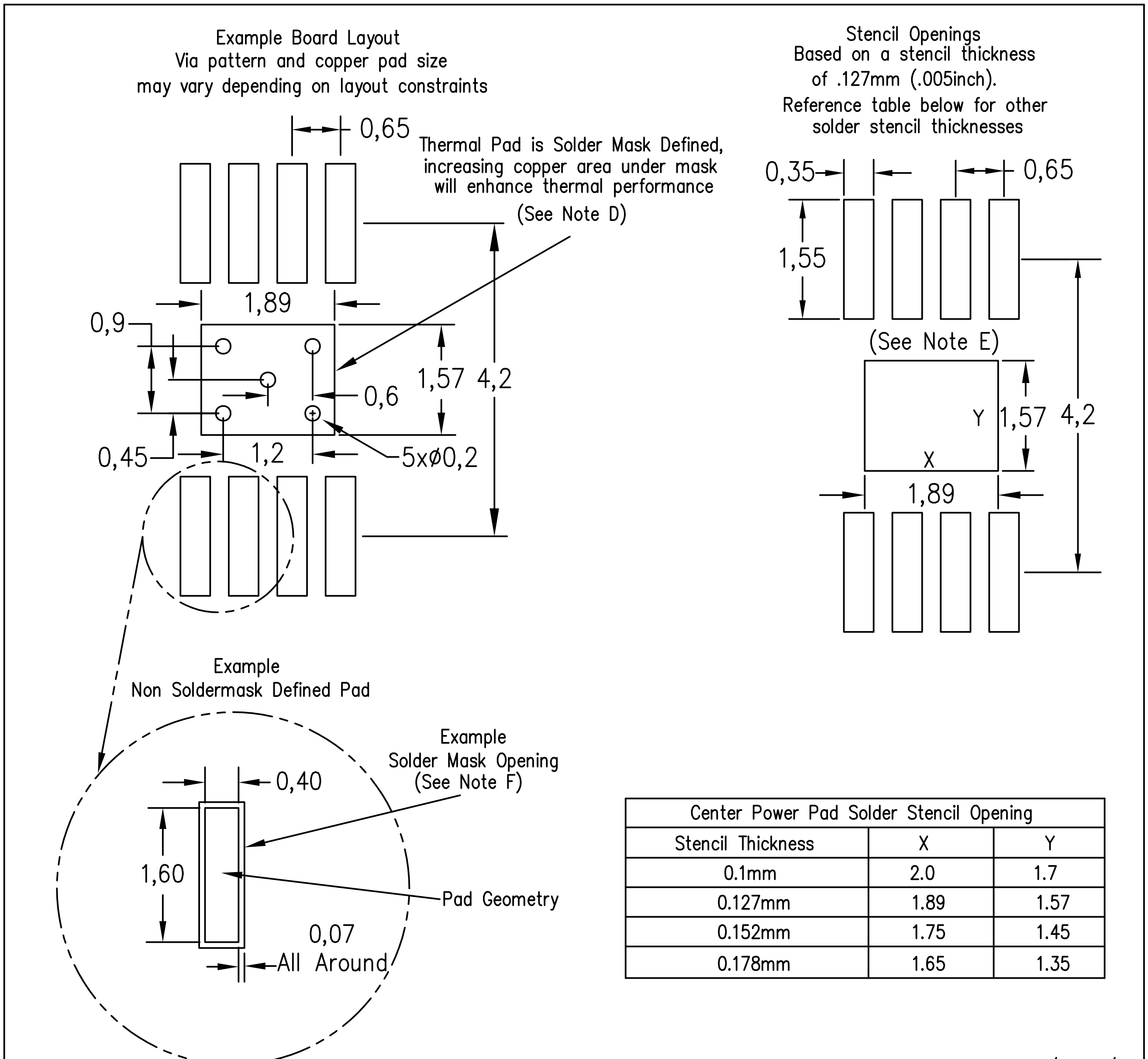
Exposed Thermal Pad Dimensions

4206323-2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

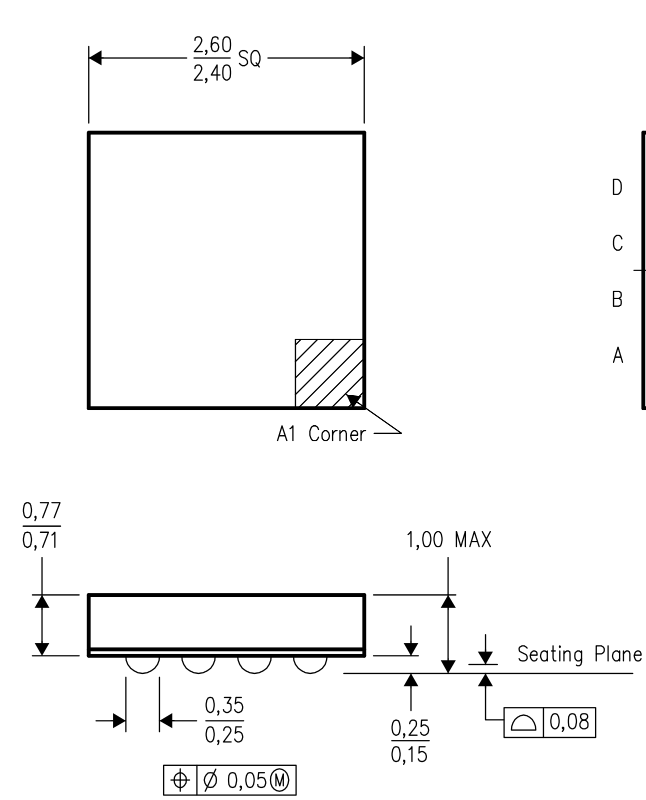


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

ZQY (S–PBGA–N15) **PLASTIC BALL GRID ARRAY**



4205130/A 05/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior configuration
D. Falls within JEDEC MO–225
E. This package is lead–free.

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