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FAIRCHILD SEMICONDUCTOR®

March 2008

NC7S08
TinyLogic® HS 2-Input AND Gate

Features

- Space saving SOT23 or SC70 5-lead package
- Ultra small MicroPak™ Pb-Free leadless package
- High Speed; t_{PD} 3.5ns typ
- Low Quiescent Power; I_{CC} < 1µA
- Balanced Output Drive; 2mA I_{OL}, –2mA I_{OH}
- Broad V_{CC} Operating Range; 2V–6V
- Balanced Propagation Delays
- Specified for 3V operation

General Description

The NC7S08 is a single 2-Input high performance CMOS AND Gate. Advanced Silicon Gate CMOS fabrication assures high speed and low power circuit operation over a broad V_{CC} range. ESD protection diodes inherently guard both inputs and output with respect to the V_{CC} and GND rails. Three stages of gain between inputs and outputs assures high noise immunity and reduced sensitivity to input edge rate.

Ordering Information

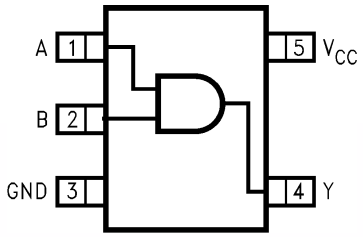
Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7S08M5X	MA05B	7S08	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7S08P5X	MAA05A	S08	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel
NC7S08L6X	MAC06A	PP	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

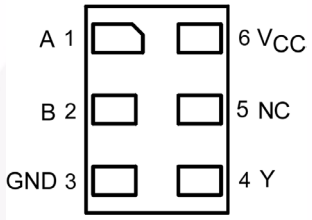
Connection Diagram

Pin Assignments for SC70 and SOT23



(Top View)

Pad Assignments for MicroPak



(Top Thru View)

Pin Description

Pin Names	Description
A, B	Inputs
Y	Output
NC	No Connect

Logic Symbol

IEEE/IEC

Function Table

Y = AB

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level

L = LOW Logic Level

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
I_{IK}	DC Input Diode Current @ $V_{IN} \le -0.5V$ @ $V_{IN} \ge V_{CC} +0.5V$	 –20mA +20mA
V_{IN}	DC Input Voltage	–0.5V to V_{CC}+0.5V
I_{OK}	DC Output Diode Current @ $V_{OUT} < -0.5V$ @ $V_{OUT} > V_{CC} +0.5V$	 –20mA +20mA
V_{OUT}	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_{OUT}	DC Output Sourceor Sink Current	±12.5mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±25mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_J	Junction Temperature	150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C
P_D	Power Dissipation @ +85°C SOT23-5 SC70-5	 200mW 150mW

Recommended Operating Conditions[1]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to 6.0V
V_{IN}	Input Voltage	0V to V_{CC}
V_{OUT}	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C
t_r, t_f	Input Rise and Fall Time V_{CC} @ 2.0V V_{CC} @ 3.0V V_{CC} @ 4.5V V_{CC} @ 6.0V	 0ns to 1000ns 0ns to 750ns 0ns to 500ns 0ns to 400ns
θ_{JA}	Thermal Resistance SOT23-5 SC70-5	 300°C/W 425°C/W

Notes:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = –40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	2.0		1.50			1.50		V
		3.0-6.0		0.7 x V_{CC}			0.7 x V_{CC}		
V_{IL}	LOW Level Input Voltage	2.0				0.50		0.50	V
		3.0-6.0				0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	2.0	I_{OH} = –20µA, V_{IN} = V_{IH}	1.90	2.0		1.90		V
		3.0		2.90	3.0		2.90		
		4.5		4.40	4.5		4.40		
		6.0		5.90	6.0		5.90		
		3.0	V_{IN} = V_{IH}, I_{OH} = –1.3mA	2.68	2.85		2.63		
		4.5	V_{IN} = V_{IH}, I_{OH} = –2mA	4.18	4.35		4.13		
		6.0	V_{IN} = V_{IH}, I_{OH} = –2.6mA	5.68	5.85		5.63		
V_{OL}	LOW Level Output Voltage	2.0	I_{OL} = 20µA V_{IN} = V_{IL}		0.0	0.10		0.10	V
		3.0			0.0	0.10		0.10	
		4.5			0.0	0.10		0.10	
		6.0			0.0	0.10		0.10	
		3.0	V_{IN} = V_{IH} or V_{IL}, I_{OH} = 1.3mA		0.1	0.26		0.33	
		4.5	V_{IN} = V_{IH} or V_{IL}, I_{OL} = 2mA		0.1	0.26		0.33	
		6.0	V_{IN} = V_{IH} or V_{IL}, I_{OL} = 2.6mA		0.1	0.26		0.33	
I_{IN}	Input Leakage Current	6.0	V_{IN} = V_{CC}, GND			±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	6.0	V_{IN} = V_{CC}, GND			1.0		10.0	µA

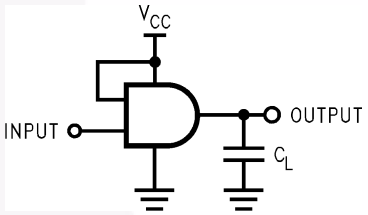
AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = –40°C to +85°C		Units	Figure Number
				Min.	Typ.	Max.	Min.	Max.		
t_{PLH}, t_{PHL}	Propagation Delay	5.0	C_L = 15pF		3.5	15			ns	Figure 1 Figure 3
		2.0	C_L = 50pF		20	100		125		
		3.0			11	27		35		
		4.5			8	20		25		
		6.0			7	17		21		
t_{TLH}, t_{THL}	Output Transition Time	5.0	C_L = 15pF		3.0	10			ns	Figure 1 Figure 3
		2.0	C_L = 50pF		25	125		155		
		3.0			16	35		45		
		4.5			11	25		31		
		6.0			9	21		26		
C_{IN}	Input Capacitance	Open			2	10		10	pF	
C_{PD}	Power Dissipation Capacitance	5.0	(2)		6				pF	Figure 2

Note:

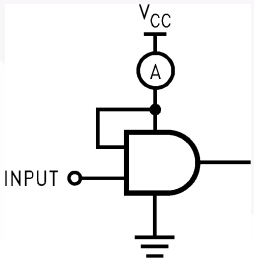
2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}static)$.

AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR = 1.0 MHz; t_W = 500 ns

Figure 1. AC Test Circuit



Input = AC Waveform;
PRR = variable; Duty Cycle = 50%

Figure 2. I_{CCD} Test Circuit

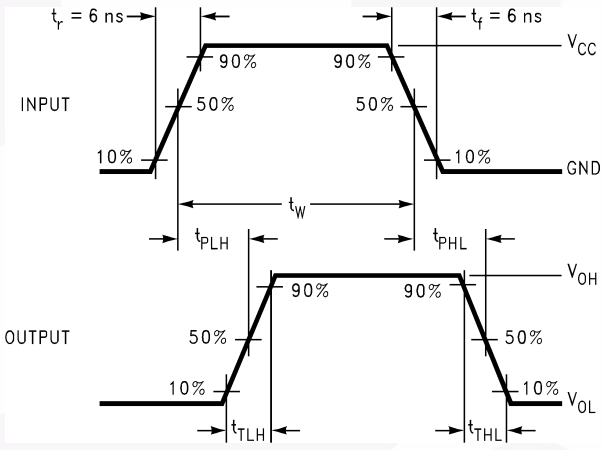


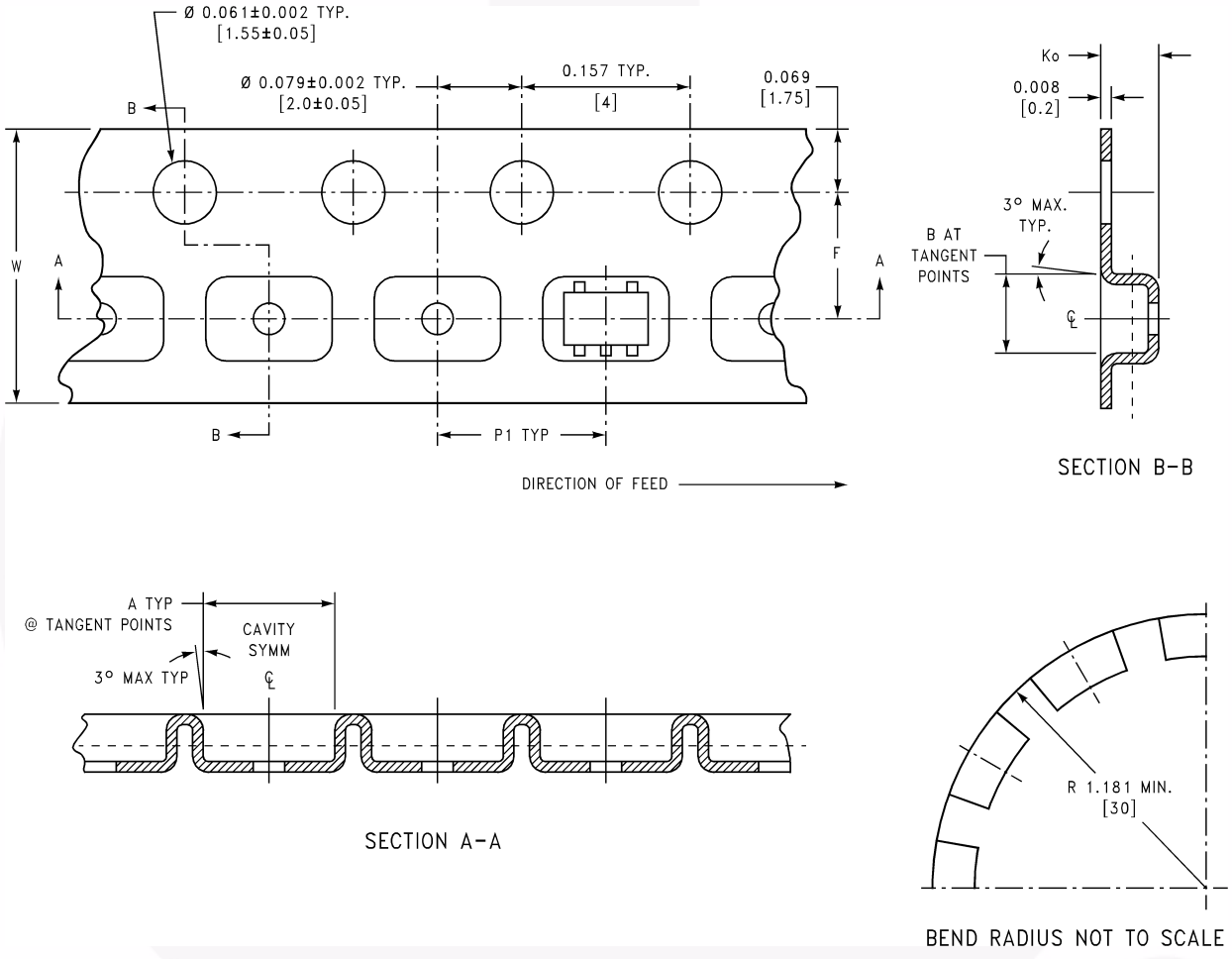
Figure 3. AC Waveforms

Tape and Reel Specifications

Tape Format for SC70 and SOT23

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
M5X, P5X	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

Tape Dimensions inches (millimeters)

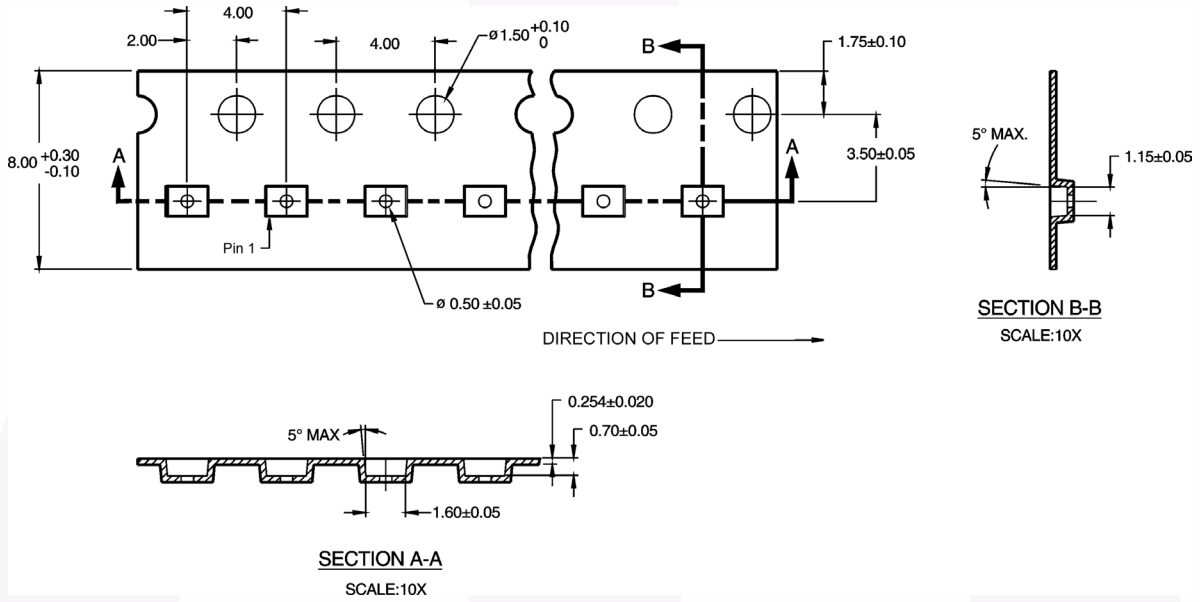


Package	Tape Size	Dim A	Dim B	Dim F	Dim K_o	Dim P1	Dim W
SC70-5	8mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)
SOT23-5	8mm	0.130 (3.3)	0.130 (3.3)	0.138 ± 0.002 (3.5 ± 0.05)	0.055 ± 0.004 (1.4 ± 0.11)	0.157 (4)	0.315 ± 0.012 (8 ± 0.3)

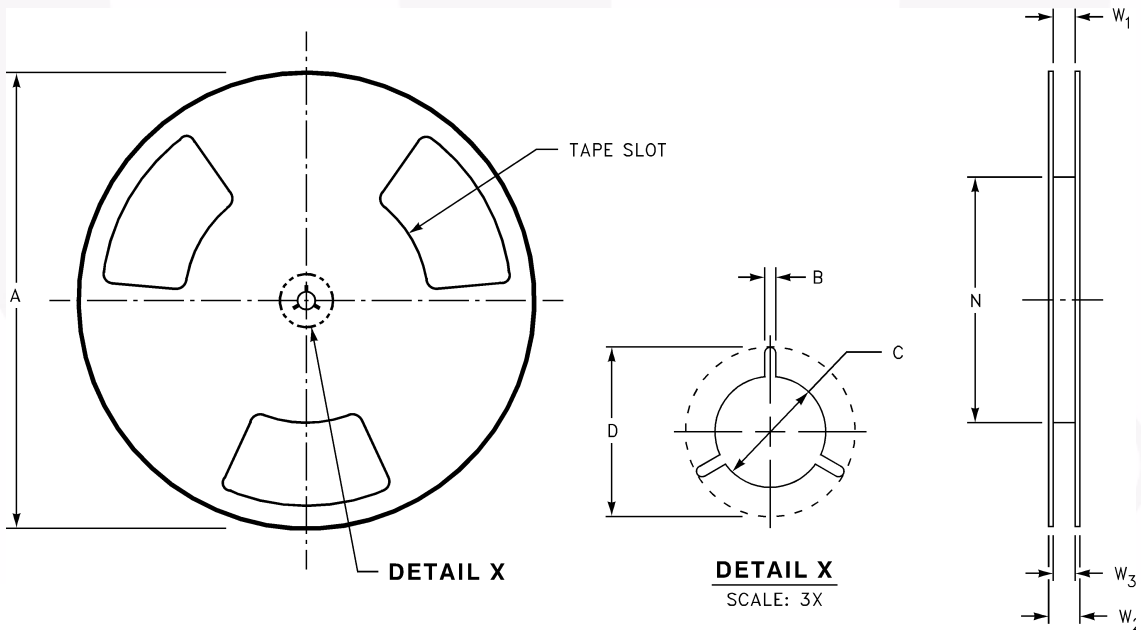
Tape and Reel Specifications (Continued)

Tape Format for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

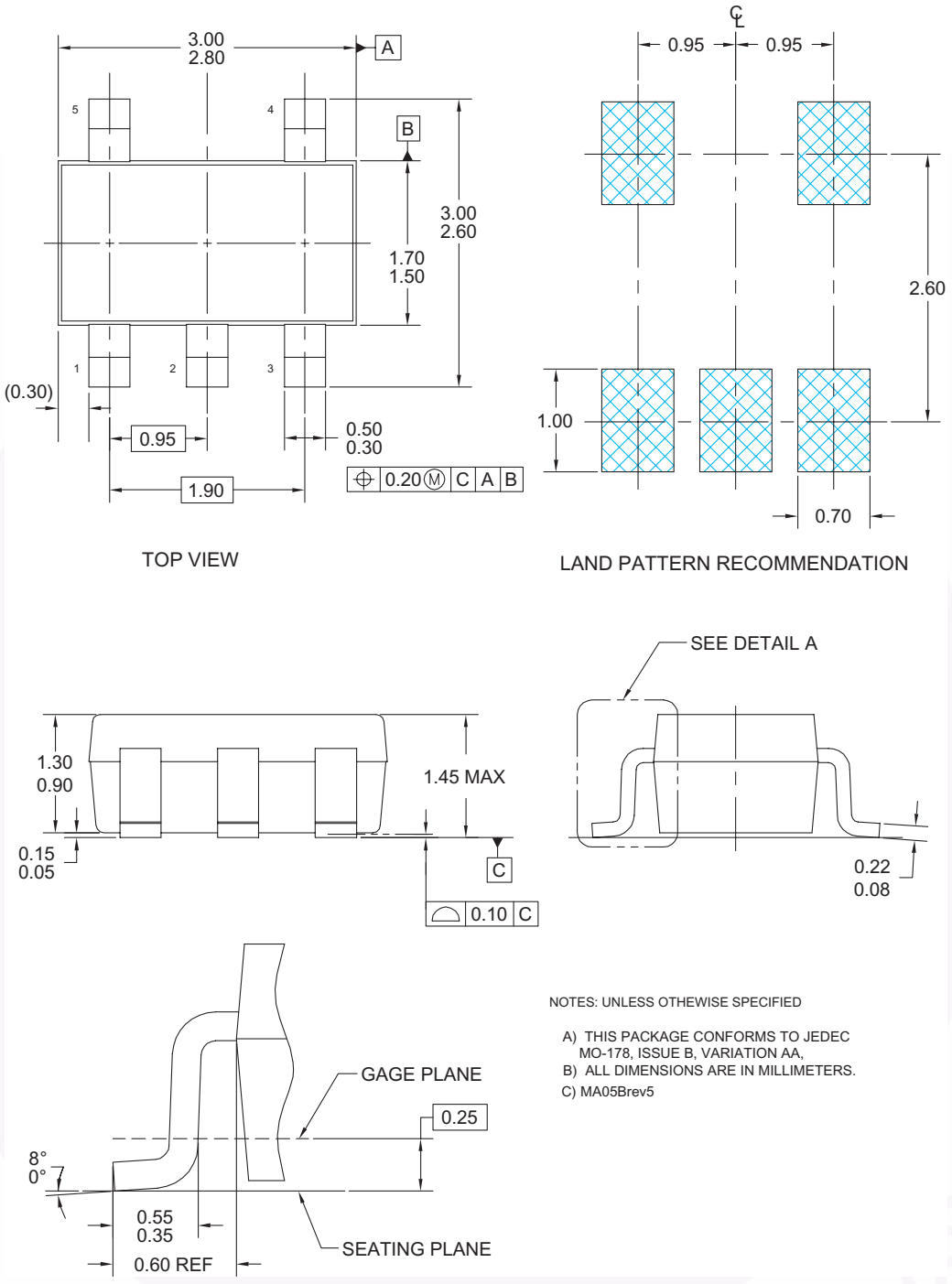


Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

Physical Dimensions



NOTES: UNLESS OTHEWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MO-178, ISSUE B, VARIATION AA,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) MA05Brev5

Figure 4. 5-Lead SOT23, JEDEC MO-178, 1.6mm

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Physical Dimensions (Continued)

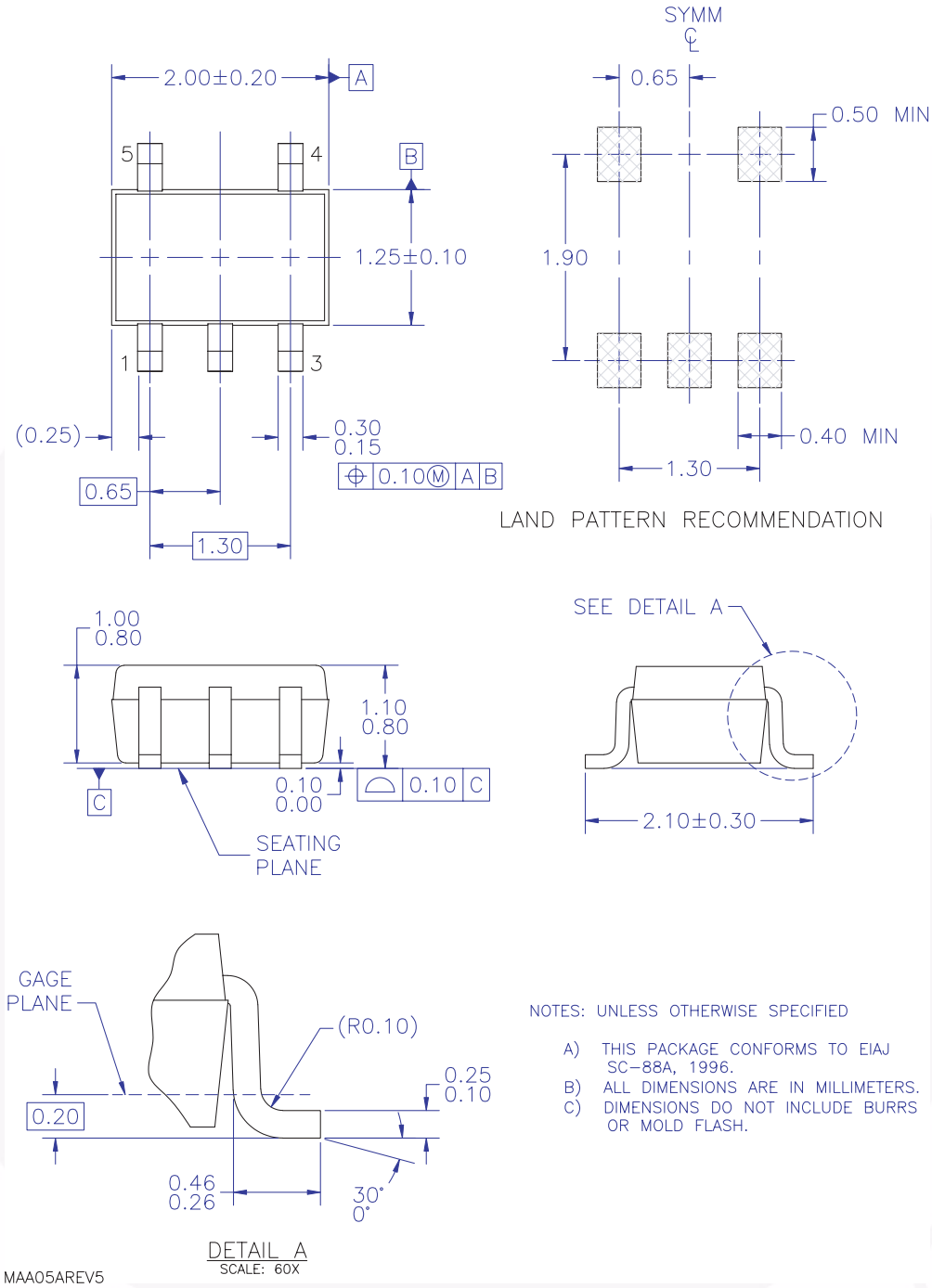

Figure 5. 5-Lead SC70, EIAJ SC-88a, 1.25mm Wide

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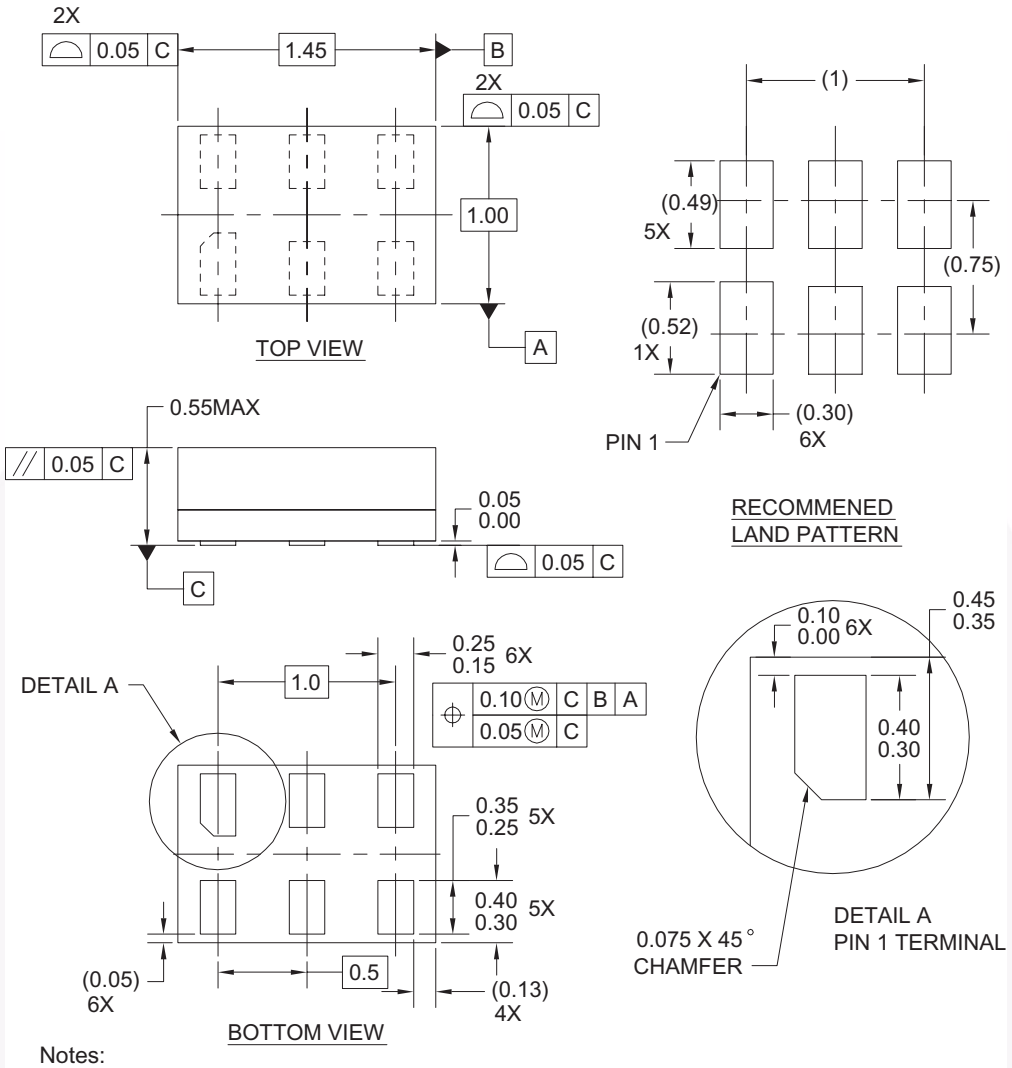
Physical Dimensions (Continued)



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06AREVC

Figure 6. 6-Lead MicroPak, 1.0mm Wide

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Rev. I33

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