



# MIC23451

## 3MHz, 2A Triple Synchronous Buck Regulator with HyperLight Load<sup>®</sup> and Power Good

### General Description

The MIC23451 is a high-efficiency, 3MHz, triple 2A, synchronous buck regulator with HyperLight Load<sup>®</sup> mode. HyperLight Load provides very-high efficiency at light loads and ultra-fast transient response, which is ideal for supplying processor core voltages. An additional benefit of this proprietary architecture is very low output ripple voltage throughout the entire load range with the use of small output capacitors. The 4mm x 4mm QFN package saves board space and requires only five external components for each channel.

The MIC23451 is designed for use with a very small inductor, down to 0.47 $\mu$ H, and an output capacitor as small as 2.2 $\mu$ F that enables a total solution size that is less than 1mm height.

The MIC23451 has a very-low quiescent current of 24 $\mu$ A each channel and achieves as high as 81% efficiency at 1mA. At higher loads, the MIC23451 provides a constant switching frequency around 3MHz while achieving peak efficiencies up to 93%.

The MIC23451 is available in a 26-pin 4mm x 4mm QFN package with an operating junction temperature range from -40°C to +125°C.

Datasheets and support documentation are available on Micrel's web site at: [www.micrel.com](http://www.micrel.com).

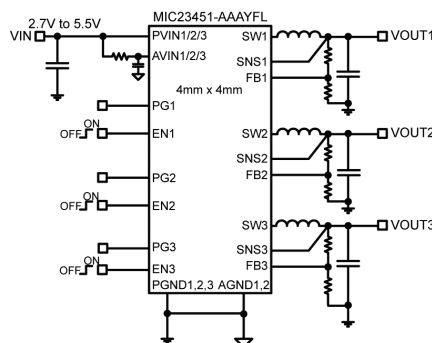
### Features

- 2.7V to 5.5V input voltage
- Three independent 2A outputs
- Up to 93% peak efficiency
- 81% typical efficiency at 1mA
- Three independent power good indicators
- 24 $\mu$ A typical quiescent current (per channel)
- 3MHz PWM operation in continuous mode
- Ultra-fast transient response
- Low voltage output ripple
  - 30mV<sub>PP</sub> ripple in HyperLight Load mode
  - 5mV output voltage ripple in full PWM mode
- Fully integrated MOSFET switches
- 0.1 $\mu$ A shutdown current (per channel)
- Thermal-shutdown and current-limit protection
- Output voltage as low as 1V
- 26-pin 4mm x 4mm QFN
- -40°C to +125°C junction temperature range

### Applications

- Solid state drives (SSD)
- $\mu$ C/ $\mu$ P, FPGA, and DSP power
- Test and measurement systems
- Set-top boxes and DTV
- High-performance servers
- Security/surveillance cameras
- 5V POL applications

### Typical Application



HyperLight Load is a registered trademark of Micrel, Inc.

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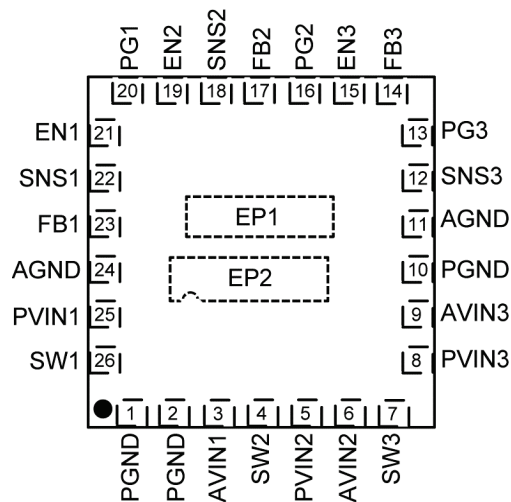
## Ordering Information

Part Number	Marking	Nominal Output Voltage	Junction Temperature Range <sup>(1)</sup>	Package <sup>(2,3)</sup>	Lead Finish
MIC23451-AAAYFL	AAA	Adj./Adj./Adj.	-40°C to +125°C	26-Pin 4mm × 4mm QFN	Pb-Free

### Notes:

- Other options are available. Contact Micrel for details.
- QFN is a Green, RoHS-compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.
- QFN • = Pin 1 identifier

## Pin Configuration



26-Pin 4mm × 4mm QFN (FL) – Adjustable  
(Top View)

## Pin Description

Pin Number	Pin Name	Pin Function
26, 4, 7	SW1, 2, 3	Switch (Output). Internal power MOSFET output switches for output 1/2/3.
21, 19, 15	EN1, 2, 3	Enable (Input). Logic high enables operation of regulator 1/2/3. Logic low will shut down the device. Do not leave floating.
22, 18, 12	SNS1, 2, 3	Sense. Connect to $V_{OUT1,2,3}$ as close to output capacitor as possible to sense output voltage.
23, 17, 14	FB1, 2, 3	Feedback. Connect a resistor divider from output 1/2/3 to ground to set the output voltage.
20, 16, 13	PG1, 2, 3	Power Good. Open-drain output for the power good indicator for output 1/2/3. Place a resistor between this pin and a voltage source to detect a power good condition.
EP1, 24, 11	AGND	Analog Ground. Connect to quiet ground point away from high-current paths, for example, $C_{OUT}$ , for best operation. Must be connected externally to PGND.
25, 5, 8	PVIN1, 2, 3	Power Input Voltage. Connect a capacitor to PGND to localize loop currents and decouple switching noise.
3, 6, 9	AVIN1, 2, 3	Analog Input Voltage. Connect a capacitor to AGND to decouple noise.
EP2, 10, 2, 1	PGND	Power Ground.

### Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage ( $PV_{IN}, AV_{IN}$ )	-0.3 to 6V
Sense ( $V_{SNS1}, V_{SNS2}, V_{SNS3}$ )	-0.3 to 6V
Power Good (PG1, PG2, PG3)	-0.3 to 6V
Output Switch Voltage ( $V_{SW1}, V_{SW2}, V_{SW3}$ )	-0.3V to 6V
Enable Input Voltage ( $V_{EN1}, V_{EN2}, V_{EN3}$ )	-0.3V to $V_{IN}$
Storage Temperature Range	-65°C to +150°C
ESD Rating <sup>(3)</sup>	ESD Sensitive

### Operating Ratings<sup>(2)</sup>

Supply Voltage ( $V_{IN}$ )	+2.7V to +5.5V
Enable Input Voltage ( $V_{EN1}, V_{EN2}, V_{EN3}$ )	0V to $V_{IN}$
Output Voltage Range ( $V_{SNS1}, V_{SNS2}, V_{SNS3}$ )	+1V to +3.3V
Junction Voltage Range ( $T_J$ )	-40°C ≤ $T_J$ ≤ +125°C
Thermal Resistance	
26-Pin 4mm × 4mm QFN ( $\theta_{JA}$ )	+20°C/W
26-Pin 4mm × 4mm QFN ( $\theta_{JC}$ )	+10°C/W

### Electrical Characteristics<sup>(4)</sup>

$T_A = +25^\circ\text{C}$ ;  $V_{IN} = V_{EN1}, V_{EN2}, V_{EN3} = 3.6\text{V}$ ;  $L1 = L2 = L3 = 1\mu\text{H}$ ;  $C_{OUT1}, C_{OUT2}, C_{OUT3} = 4.7\mu\text{F}$ , unless otherwise specified.

**Bold** values indicate  $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ , unless noted.

Parameter	Condition	Min.	Typ.	Max.	Units
Supply Voltage Range		<b>2.7</b>		<b>5.5</b>	V
Undervoltage Lockout Threshold	Turn-On	<b>2.45</b>	2.55	<b>2.65</b>	V
Undervoltage Lockout Hysteresis			75		mV
Quiescent Current	$I_{OUT} = 0\text{mA}$ , $SNS > 1.2 \times V_{OUTNOM}$		65	<b>120</b>	$\mu\text{A}$
Per Channel Shutdown Current	$V_{EN1}, V_{EN2}, V_{EN3} = 0\text{V}$ ; $V_{IN} = 5.5\text{V}$		0.1	<b>5</b>	$\mu\text{A}$
Output Voltage Accuracy	$V_{IN} = 3.6\text{V}$ if $V_{OUT(NOM)} < 2.5\text{V}$ , $I_{LOAD} = 20\text{mA}$	<b>-2.5</b>		<b>+2.5</b>	%
	$V_{IN} = 4.5\text{V}$ if $V_{OUT(NOM)} \geq 2.5\text{V}$ , $I_{LOAD} = 20\text{mA}$				
Feedback Voltage ( $V_{FB1}, V_{FB2}, V_{FB3}$ )		<b>0.604</b>	0.62	<b>0.635</b>	V
Peak Current Limit	$I_{OUT1}, I_{OUT2}, I_{OUT3}$ $SNS1, SNS2, SNS3 = 0.9 \times V_{OUTNOM}$	<b>2.2</b>	4.1		A
Foldback Current Limit			2.3		A
Output Voltage Line Regulation ( $V_{OUT1}, V_{OUT2}, V_{OUT3}$ )	$V_{IN} = 3.6\text{V to } 5.5\text{V}$ if $V_{OUTNOM1, 2, 3} < 2.5\text{V}$ , $I_{LOAD} = 20\text{mA}$		0.3		%/V
	$V_{IN} = 4.5\text{V to } 5.5\text{V}$ if $V_{OUTNOM1, 2, 3} \geq 2.5\text{V}$ , $I_{LOAD} = 20\text{mA}$				
Output Voltage Load Regulation ( $V_{OUT1}, V_{OUT2}, V_{OUT3}$ )	DCM: $20\text{mA} < I_{LOAD} < 130\text{mA}$ , $V_{IN} = 3.6\text{V}$ if $V_{OUTNOM} < 2.5\text{V}$		0.2		%
	DCM: $20\text{mA} < I_{LOAD} < 130\text{mA}$ , $V_{IN} = 5.0\text{V}$ if $V_{OUTNOM} > 2.5\text{V}$		0.4		
	CCM: $200\text{mA} < I_{LOAD} < 500\text{mA}$ , $V_{IN} = 3.6\text{V}$ if $V_{OUTNOM} < 2.5\text{V}$		0.6		
	CCM: $200\text{mA} < I_{LOAD} < 1\text{A}$ , $V_{IN} = 5.0\text{V}$ if $V_{OUTNOM} > 2.5\text{V}$		0.3		
PWM Switch ON-Resistance ( $R_{SW1}, R_{SW2}, R_{SW3}$ )	$I_{SW1}, I_{SW2}, I_{SW3} = +100\text{mA}$ (PMOS)		0.217		$\Omega$
Maximum Frequency	$I_{OUT1}, I_{OUT2}, I_{OUT3} = 120\text{mA}$		3		MHz
Soft-Start Time	$V_{OUT1}, V_{OUT2}, V_{OUT3} = 90\%$		150		$\mu\text{s}$
Power Good Threshold	% of $V_{NOM}$	83	90	96	%
Power Good Hysteresis			10		%
Power Good Pull Down	$V_{SNS} = 90\% V_{NOM}$ , $I_{PG} = 1\text{mA}$			200	mV

**Notes:**

- Exceeding the absolute maximum ratings may damage the device.
- The device is not guaranteed to function outside its operating ratings.
- Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5k $\Omega$  in series with 100pF.
- Specification for packaged product only.

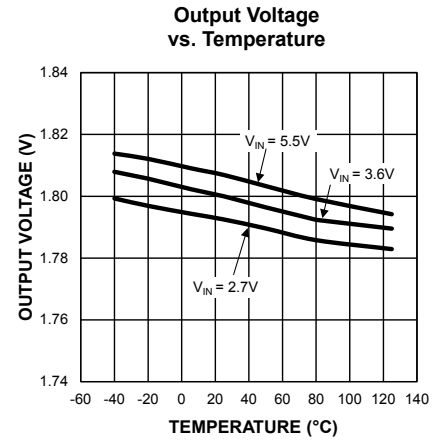
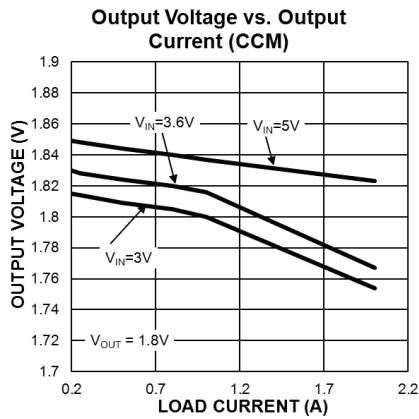
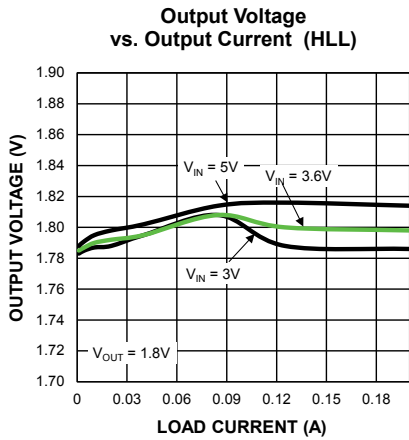
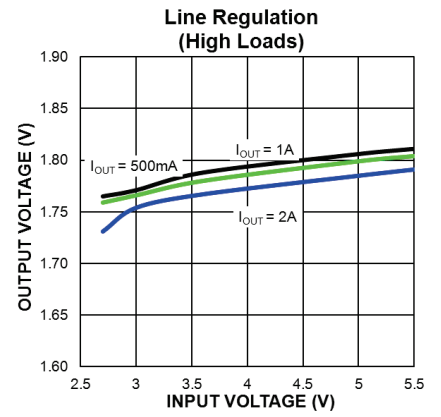
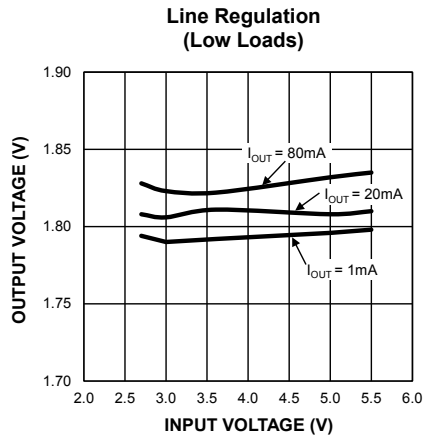
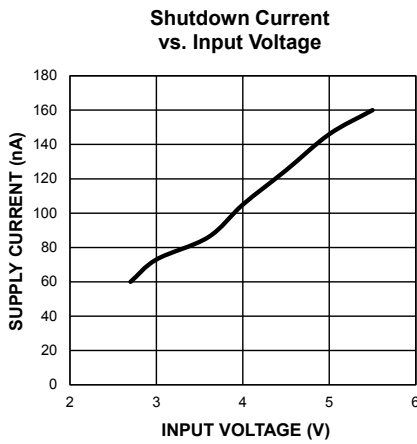
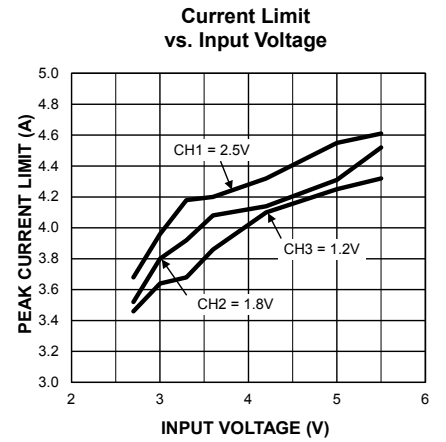
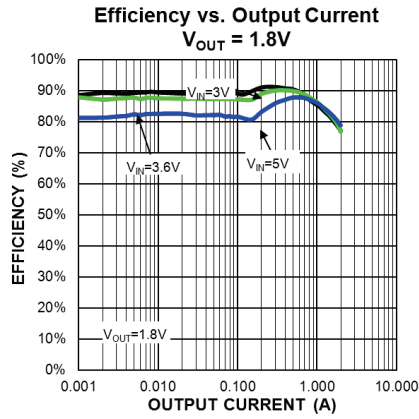
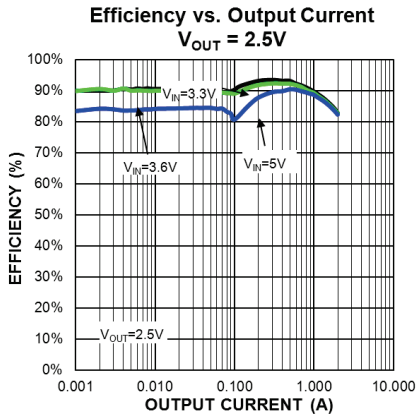
**Electrical Characteristics<sup>(4)</sup> (Continued)**

$T_A = +25^\circ\text{C}$ ;  $V_{IN} = V_{EN1}, V_{EN2}, V_{EN3} = 3.6\text{V}$ ;  $L1 = L2 = L3 = 1\mu\text{H}$ ;  $C_{OUT1}, C_{OUT2}, C_{OUT3} = 4.7\mu\text{F}$ , unless otherwise specified.

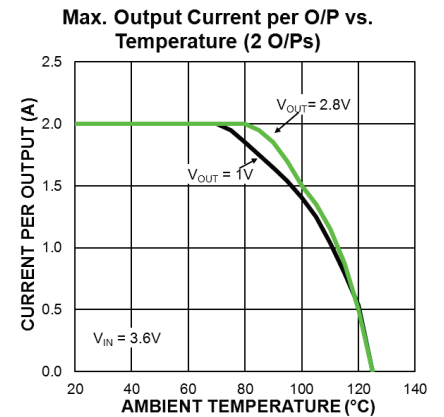
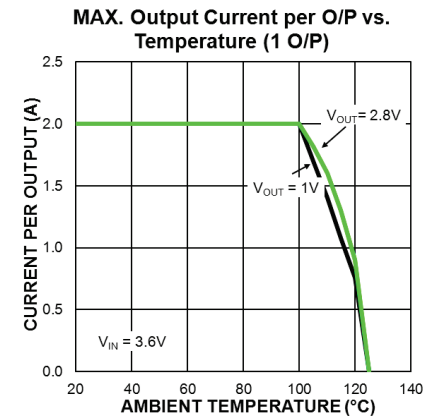
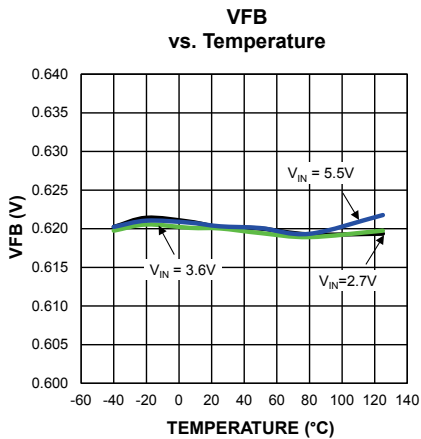
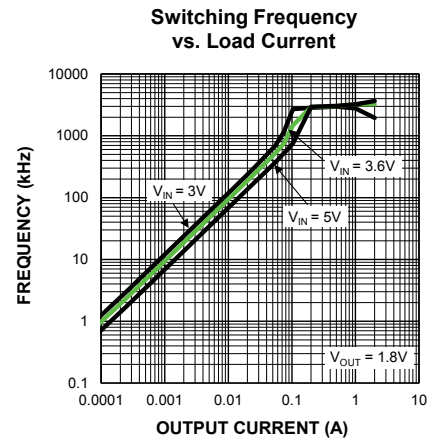
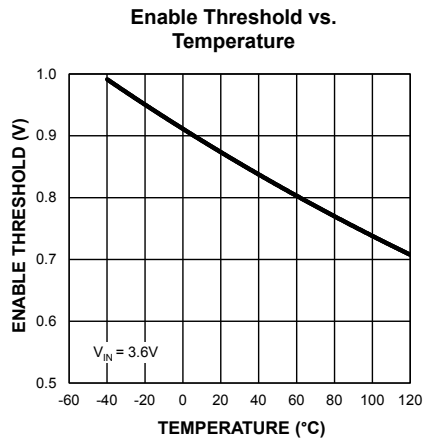
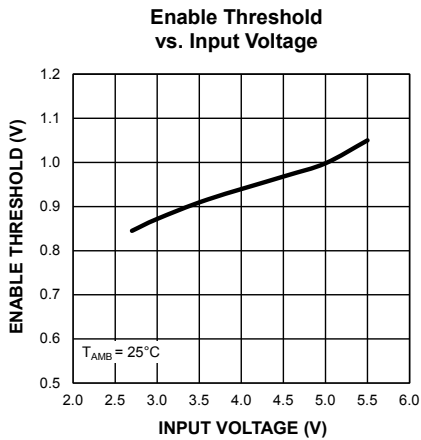
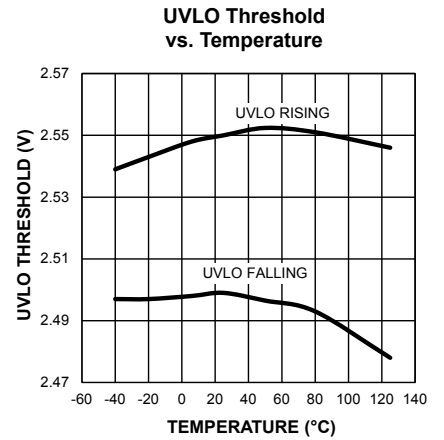
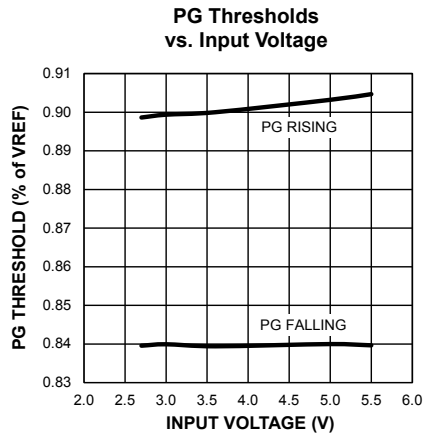
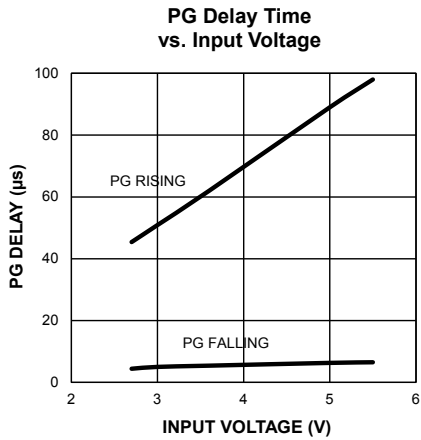
**Bold** values indicate  $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ , unless noted.

Parameter	Condition	Min.	Typ.	Max.	Units
Enable Threshold	Turn-On	<b>0.5</b>	0.9	<b>1.2</b>	V
Enable Input Current			0.1	<b>1</b>	$\mu\text{A}$
Overtemperature Shutdown			160		$^\circ\text{C}$
Overtemperature Shutdown Hysteresis			20		$^\circ\text{C}$

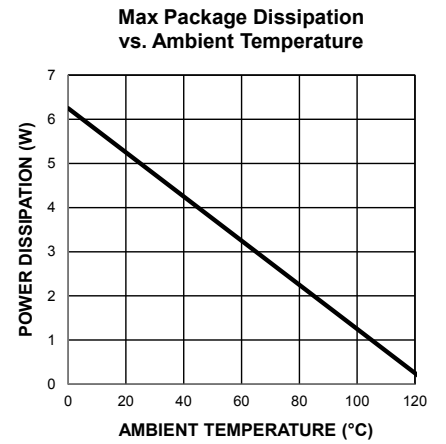
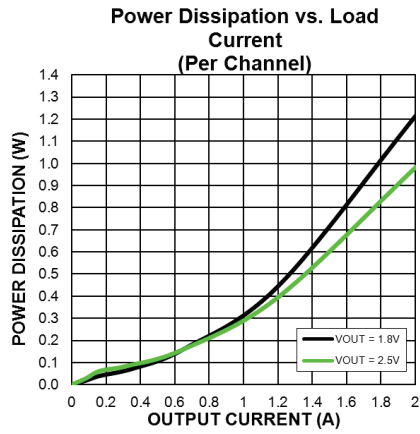
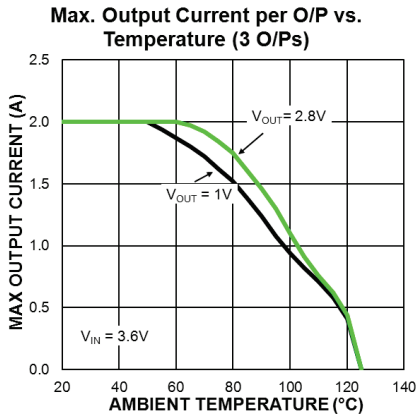
# Typical Characteristics



### Typical Characteristics (Continued)

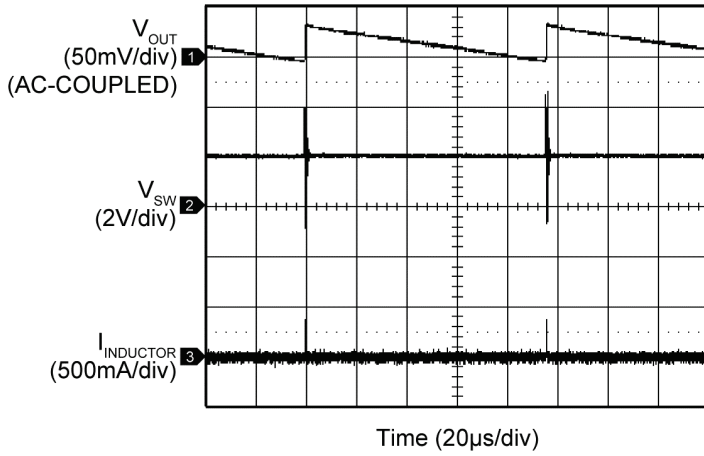


### Typical Characteristics (Continued)

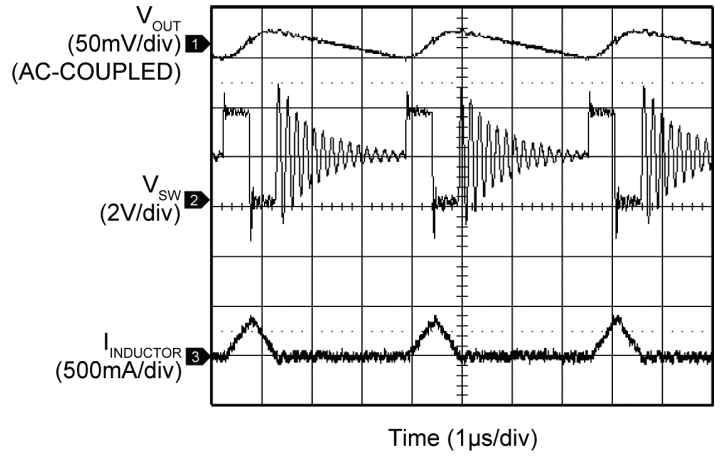


## Functional Characteristics

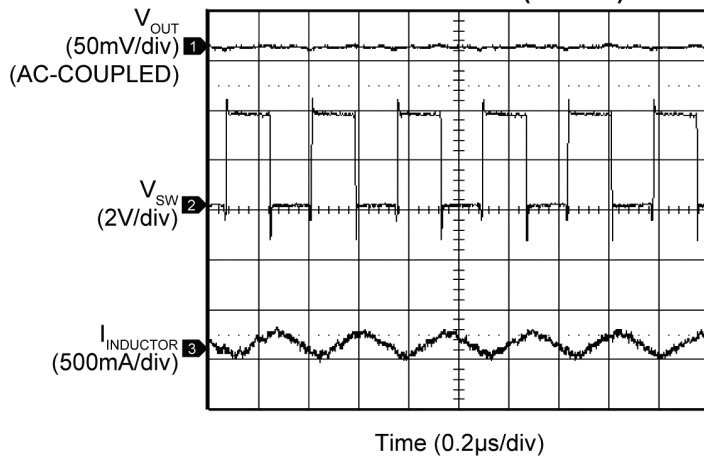
**Switching Waveform  
Discontinuous Mode (1mA)**



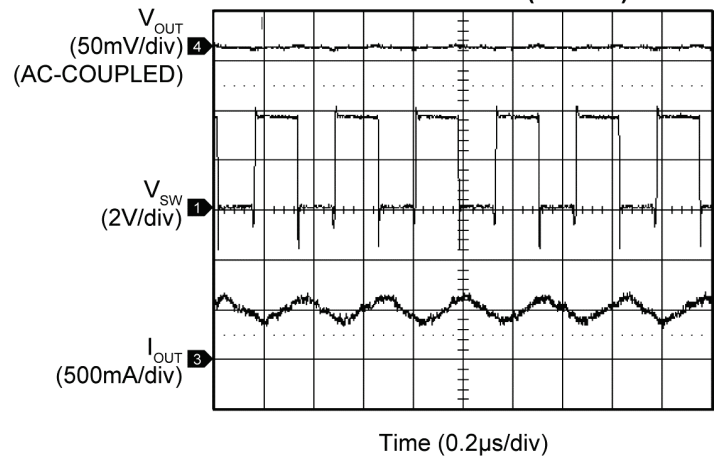
**Switching Waveform  
Discontinuous Mode (50mA)**



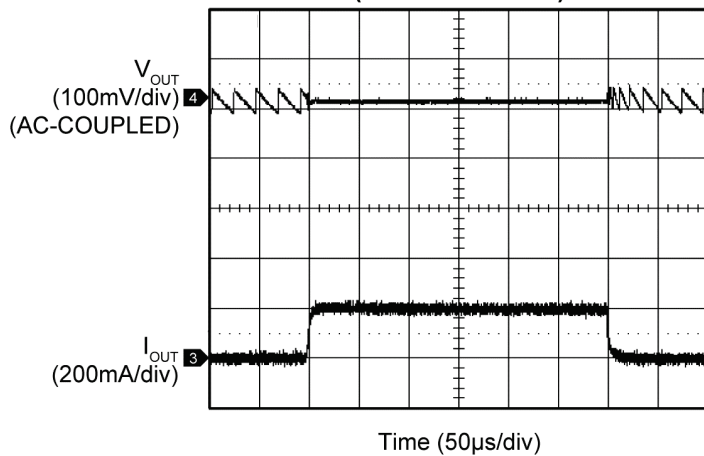
**Switching Waveform  
Continuous Mode (150mA)**



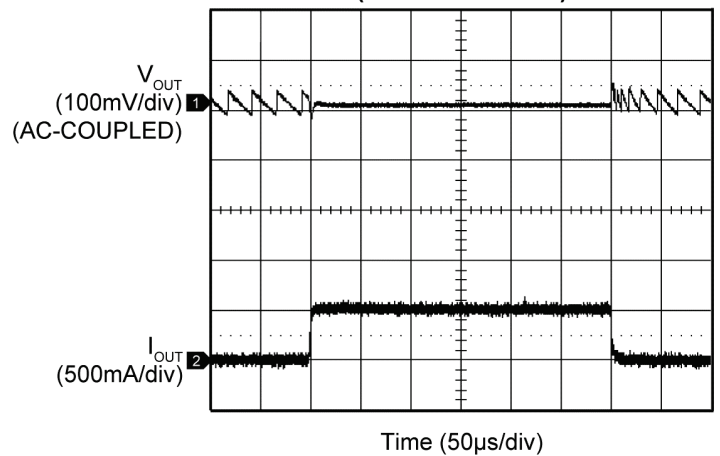
**Switching Waveform  
Continuous Mode (500mA)**



**Load Transient  
(10mA to 200mA)**



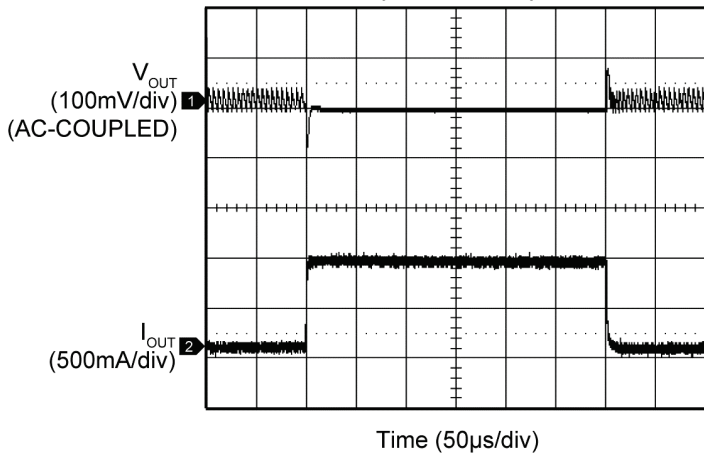
**Load Transient  
(10mA to 500mA)**



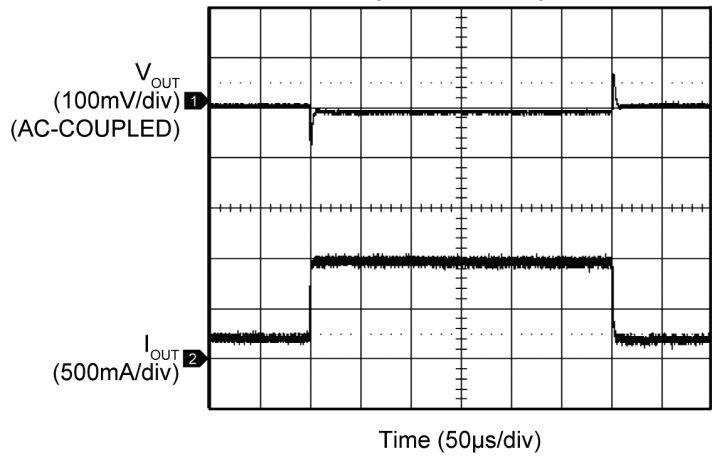


### Functional Characteristics (Continued)

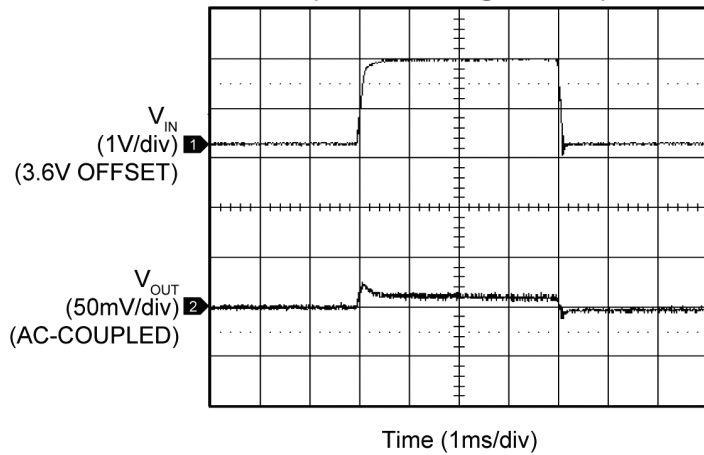
**Load Transient  
(50mA to 1A)**



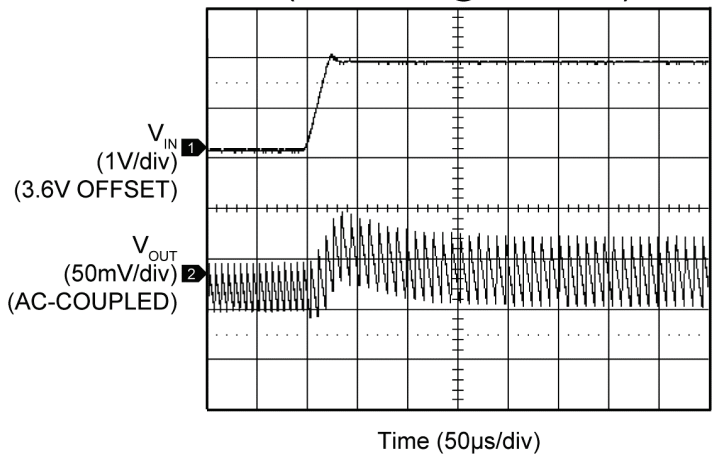
**Load Transient  
(200mA to 1A)**



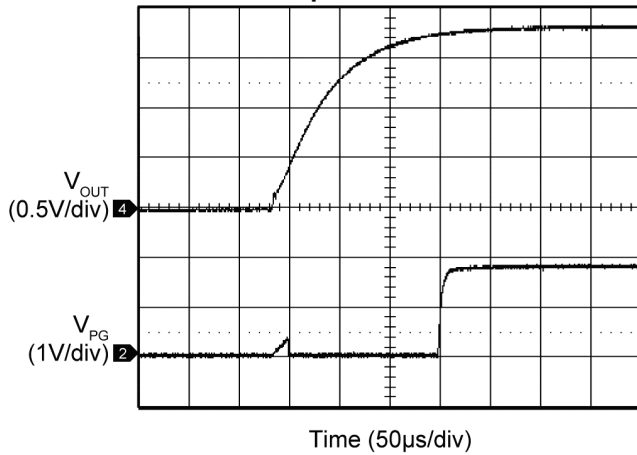
**Line Transient  
(3.6V to 5.5V @1A Load)**



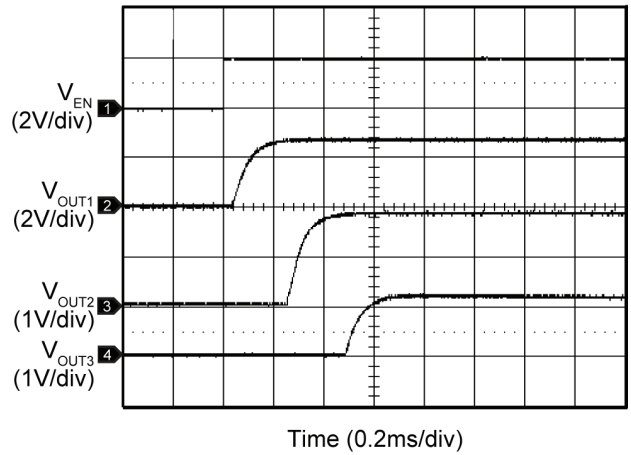
**Line Transient  
(3.6V to 5.5V @ 20mA Load)**



**Start-Up and PG Waveform**

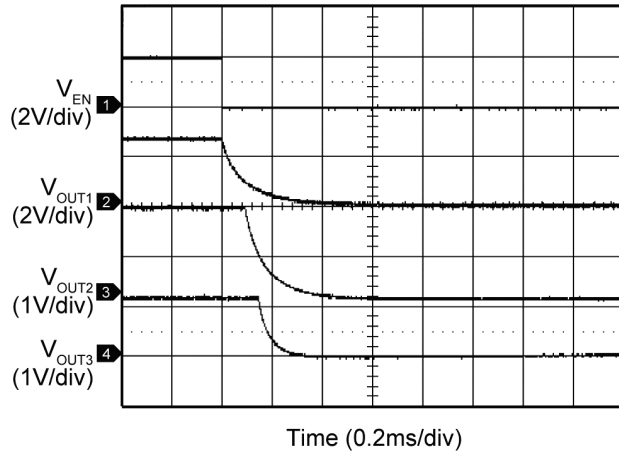


**Start-Up and PG Waveform – Sequenced  
(EN = EN1, PG1 = EN2, PG2 = EN3)**

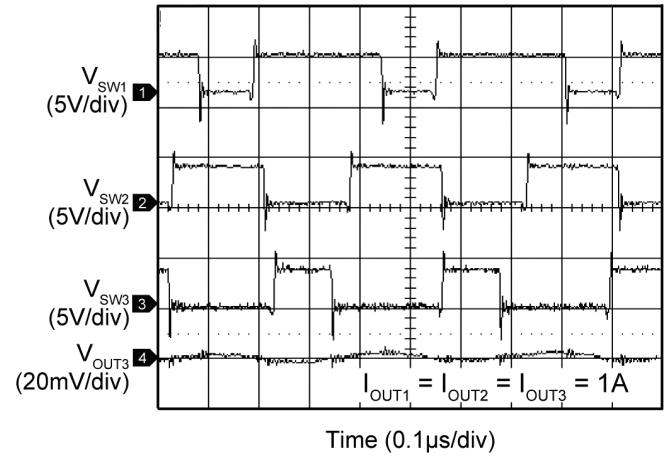


## Functional Characteristics (Continued)

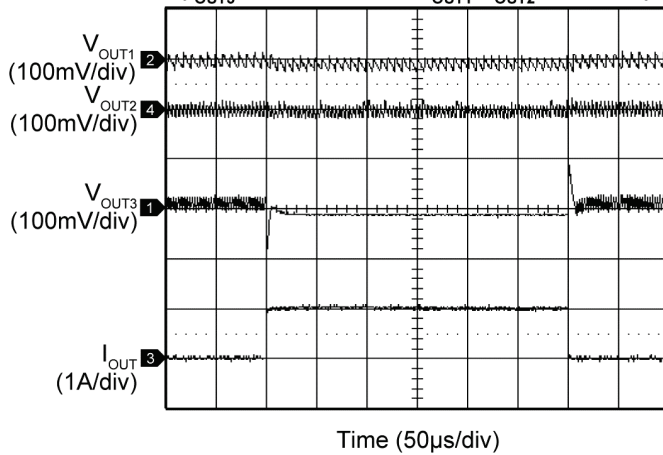
**Shutdown and PG Waveform – Sequenced**  
(EN = EN1, PG1 = EN2, PG2 = EN3)



**Switching Waveform**  
(All Channels in Continuous Mode)



**Transient Cross Regulation**  
( $I_{OUT3} = 20\text{mA to } 1\text{A}$ ;  $I_{OUT1}, I_{OUT2} = 20\text{ mA}$ )



## Functional Diagram

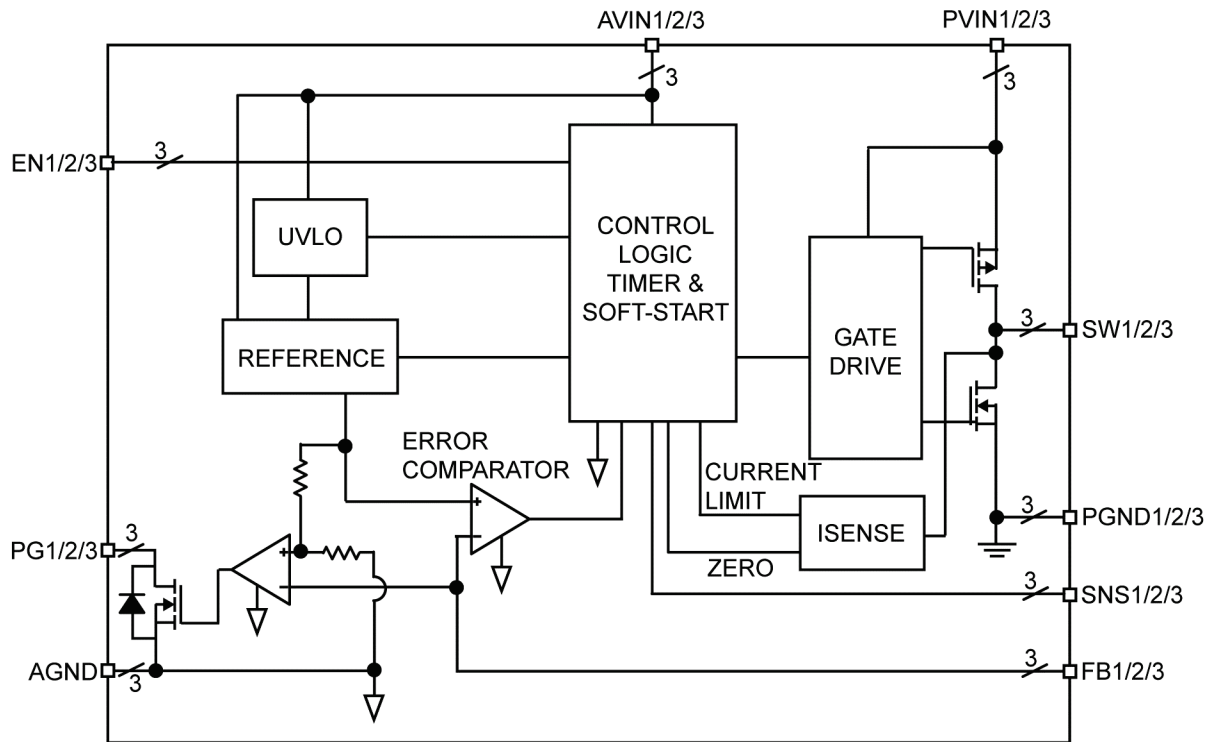


Figure 1. Simplified MIC23451 Adjustable Functional Block Diagram

## Functional Description

### PVIN

The input supply (PVIN) provides power to the internal MOSFETs for the switch mode regulator. The  $V_{IN}$  operating range is 2.7V to 5.5V, so an input capacitor, with a minimum voltage rating of 6.3V is recommended. Because of the high di/dt switching speeds, a minimum 2.2 $\mu$ F or 4.7 $\mu$ F recommended bypass capacitor, placed close to PVIN and the power ground (PGND) pin, is required. Refer to the “[PCB Layout Recommendations](#)” section for details.

### AVIN

The input supply (AVIN) provides power to the internal control circuitry. Because the high di/dt switching speeds on PVIN cause small voltage spikes, a 50 $\Omega$  RC filter and a minimum 100nF decoupling capacitor, placed close to the AVIN and signal ground (AGND) pin, is required.

### EN

A logic high signal on the enable pin (EN) activates the output voltage of the device. A logic low signal on the enable pin deactivates the output and reduces supply current to 0.01 $\mu$ A. The MIC23451 features internal soft-start circuitry that reduces inrush current and prevents the output voltage from overshooting at start-up. Do not leave the EN pin floating.

### SW

The switch (SW) connects directly to one end of the inductor and provides the current path during switching cycles. The other end of the inductor is connected to the load, SNS pin, and output capacitor. Because of the high-speed switching on this pin, the switch node should be routed away from sensitive nodes.

### SNS

The sense (SNS) pin is connected to the output of the device to provide feedback to the control circuitry. The SNS connection should be placed close to the output capacitor. Refer to the “[PCB Layout Recommendations](#)” section for more details.

### AGND

The analog ground (AGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the power ground (PGND) loop. Refer to the “[PCB Layout Recommendations](#)” section for more details.

### PGND

The power ground pin is the ground path for the high current in PWM mode. The current loop for the power ground should be as short and wide as possible and separate from the analog ground (AGND) loop as applicable. Refer to the “[PCB Layout Recommendations](#)” section for more details.

### PG

The power good (PG) pin is an open-drain output that indicates logic high when the output voltage is typically above 90% of its steady state voltage. A pull-up resistor of more than 5k $\Omega$  should be connected from PG to  $V_{OUT}$ .

### FB

The feedback (FB) pin is the control input for programming the output voltage. A resistor divider network is connected to this pin from the output and is compared to the internal 0.62V reference within the regulation loop.

The output voltage can be programmed between 1V and 3.3V using Equation 1:

$$V_{OUT} = V_{REF} \times \left( 1 + \frac{R1}{R2} \right) \quad \text{Eq. 1}$$

where:

R1 is the top,  $V_{OUT}$  connected resistor

R2 is the bottom, AGND connected resistor

[Table 1](#) shows example feedback resistor values.

**Table 1. Feedback Resistor Values**

$V_{OUT}$	R1	R2
1.2V	274k	294k
1.5V	316k	221k
1.8V	301k	158k
2.5V	324k	107k
3.3V	309k	71.5k

## Application Information

The MIC23451 is a triple high performance DC-to-DC step down regulator offering a small solution size. Supporting three outputs with currents up to 2A inside a 4mm × 4mm QFN package, the IC requires only five external components per channel while meeting today's miniature portable electronic device needs. Using the HyperLight Load switching scheme, the MIC23451 can maintain high efficiency throughout the entire load range while providing ultra-fast load transient response. The following sections provide additional device application information.

### Input Capacitor

A 2.2μF or greater ceramic capacitor should be placed close to the PVIN pin for each channel and its corresponding PGND pin for bypassing. For example, the Murata GRM188R60J475ME19D, size 0603, 4.7μF ceramic capacitor is ideal, based on performance, size, and cost. An X5R or X7R temperature rating is recommended for the input capacitor. Y5V temperature rating capacitors, in addition to losing most of their capacitance over temperature, can also become resistive at high frequencies. This reduces their ability to filter out high-frequency noise.

### Output Capacitor

The MIC23451 is designed for use with a 2.2μF or greater ceramic output capacitor. Increasing the output capacitance lowers output ripple and improves load transient response, but could also increase solution size or cost. A low equivalent series resistance (ESR) ceramic output capacitor, such as the Murata GRM188R60J475ME84D, size 0603, 4.7μF ceramic capacitor, is recommended based on performance, size, and cost. Both the X7R or X5R temperature rating capacitors are recommended. The Y5V and Z5U temperature rating capacitors are not recommended due to their wide variation in capacitance over temperature and increased resistance at high frequencies.

### Inductor Selection

When selecting an inductor, it is important to consider the following factors (not necessarily in order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC23451 is designed for use with a 0.47μH to 2.2μH inductor. For faster transient response, a 0.47μH inductor yields the best result. On the other hand, a 2.2μH inductor yields lower output voltage ripple. For the best compromise of these, a 1μH is generally recommended.

Maximum current ratings of the inductor are generally given in two forms: permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Make sure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin, so that the peak current does not cause the inductor to saturate. Peak current can be calculated as shown in Equation 2:

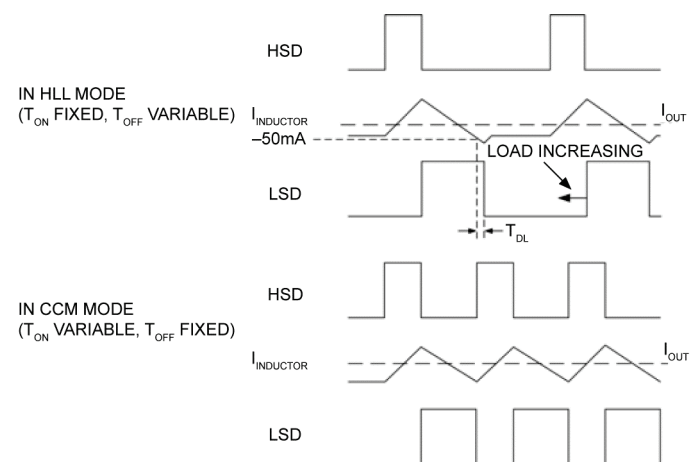
$$I_{PEAK} = \left[ I_{OUT} + V_{OUT} \left( \frac{1 - V_{OUT}/V_{IN}}{2 \times f \times L} \right) \right] \quad \text{Eq. 2}$$

As Equation 2 shows, the peak inductor current is inversely proportional to the switching frequency and the inductance; the lower the switching frequency or the inductance the higher the peak current. As input voltage increases, the peak current also increases.

The size of the inductor depends on the requirements of the application. Refer to the “[Typical Application Schematic](#)” and “[Bill of Materials](#)” sections for details.

DC resistance (DCR) is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the “[Efficiency Considerations](#)” section.

The transition between high loads (CCM) to HyperLight Load (HLL) mode is determined by the inductor ripple current and the load current, as shown in [Figure 2](#).



**Figure 2. Transition between CCM Mode and HLL Mode**

The diagram shows the signals for high-side switch drive (HSD) for  $T_{ON}$  control, the inductor current, and the low-side switch drive (LSD) for  $T_{OFF}$  control.

In HLL mode, the inductor is charged with a fixed  $T_{ON}$  pulse on the high-side switch (HSD). After this, the LSD is switched on and current falls at a rate of  $V_{OUT}/L$ . The controller remains in HLL mode while the inductor falling

current is detected to cross approximately  $-50\text{mA}$ . When the LSD (or  $T_{\text{OFF}}$ ) time reaches its minimum and the inductor falling current is no longer able to reach this  $-50\text{mA}$  threshold, the part is in CCM mode and switching at a virtually constant frequency.

Once in CCM mode, the  $T_{\text{OFF}}$  time does not vary. Therefore, it is important to note that if L is large enough, the HLL transition level will not be triggered.

That inductor is:

$$L_{\text{MAX}} = \frac{V_{\text{OUT}} \times 135\text{ns}}{2 \times 50\text{mA}} \quad \text{Eq. 3}$$

### Compensation

The MIC23451 is designed to be stable with a  $0.47\mu\text{H}$  to  $2.2\mu\text{H}$  inductor with a  $4.7\mu\text{F}$  ceramic (X5R) output capacitor.

### Duty Cycle

The typical maximum duty cycle of the MIC23451 is 80%.

### Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied.

$$\text{Efficiency \%} = \left( \frac{V_{\text{OUT}} \times I_{\text{OUT}}}{V_{\text{IN}} \times I_{\text{IN}}} \right) \times 100 \quad \text{Eq. 4}$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations, and it reduces current consumption for battery-powered applications. Reduced current draw from a battery increases the device's operating time and is critical in hand-held devices.

There are two types of losses in switching converters: DC losses and switching losses. DC losses are the power dissipation of  $I^2R$ . Power is dissipated in the high-side switch during the on cycle. Power loss is equal to the high-side MOSFET  $R_{\text{DS(ON)}}$  multiplied by the switch current squared. During the off cycle, the low-side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage represents another DC loss. The current required to drive the gates on and off at a constant 4MHz frequency, and the switching transitions, make up the switching losses.

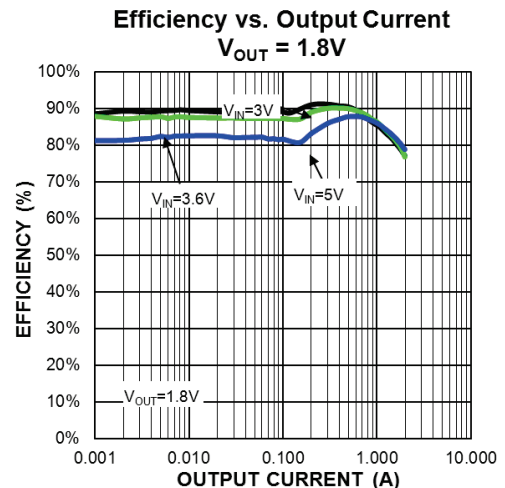


Figure 3. Efficiency under Load

Figure 3 shows an efficiency curve. From no load to 100mA, efficiency losses are dominated by quiescent current losses, gate drive, and transition losses. By using the HyperLight Load mode, the MIC23451 can maintain high efficiency at low output currents.

Over 100mA, efficiency loss is dominated by MOSFET  $R_{\text{DS(ON)}}$  and inductor losses. Higher input supply voltages will increase the gate-to-source voltage on the internal MOSFETs, thereby reducing the internal  $R_{\text{DS(ON)}}$ . This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. Because of this, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become very significant. The DCR losses can be calculated as shown in Equation 5.

$$P_{\text{DCR}} = I_{\text{OUT}}^2 \times \text{DCR} \quad \text{Eq. 5}$$

From that, the loss in efficiency caused by inductor resistance can be calculated as shown in Equation 6.

$$\text{Efficiency Loss} = \left[ 1 - \left( \frac{V_{\text{OUT}} \times I_{\text{OUT}}}{V_{\text{OUT}} \times I_{\text{OUT}} + P_{\text{DCR}}} \right) \right] \times 100 \quad \text{Eq. 6}$$

Efficiency loss caused by DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.



## Thermal Considerations

Most applications will not require 2A continuous current from all outputs at all times, so it is useful to know what the thermal limits are for various loading profiles.

The allowable overall package dissipation is limited by the intrinsic thermal resistance of the package ( $R_{\theta(J-C)}$ ) and the area of copper used to spread heat from the package case to the ambient surrounding temperature ( $R_{\theta(C-A)}$ ). The composite of these two thermal resistances is  $R_{\theta(J-A)}$ , which represents the package thermal resistance with at least 1 square inch of copper ground plane. From this figure, which for the MIC23451 is 20°C/W, we can calculate maximum internal power dissipation, as shown in Equation 7:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMB}}{R_{\theta(J-A)}} \quad \text{Eq. 7}$$

where:

$T_{JMAX}$  = Maximum junction temp (125°C)

$T_{AMB}$  = Ambient temperature

$R_{\theta(J-A)}$  = 20°C/W

The allowable dissipation tends towards zero as the ambient temperature increases towards the maximum operating junction temperature.

The graph of  $PD_{MAX}$  vs. ambient temperature could be drawn quite simply using this equation. However, a more useful measure is the maximum output current per regulator vs. ambient temperature. This requires creating an 'exchange rate' between power dissipation per regulator ( $P_{DISS}$ ) and its output current ( $I_{OUT}$ ).

An accurate measure of this function can use the efficiency curve, as illustrated in Equation 8:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \quad \text{Eq. 8}$$

$$P_{LOSS} = \frac{P_{OUT}(1-\eta)}{\eta}$$

where:

$\eta$  = Efficiency

$P_{OUT} = I_{OUT} \cdot V_{OUT}$

To arrive at the internal package dissipation  $P_{DISS}$ , remove the inductor loss  $P_{DCR}$ , which is not dissipated within the package. This does not give a worst case figure because efficiency is typically measured on a nominal part at nominal temperatures. The  $I_{OUT}$  to  $P_{DISS}$  function used in this case is a synthesized  $P_{DISS}$ , which accounts for worst case values at maximum operating temperature, as shown in Equation 9.

$$P_{DISS} = I_{OUT}^2 \left( R_{DS_{ON\_P}} \times \frac{V_{OUT}}{V_{IN}} + R_{DS_{ON\_N}} \times \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \right) \quad \text{Eq. 9}$$

where:

$R_{DS_{ON\_P}}$  = Maximum  $R_{DS_{ON}}$  of the high-side, P-Channel switch at  $T_{JMAX}$

$R_{DS_{ON\_N}}$  = Maximum  $R_{DS_{ON}}$  of the low-side, N-Channel switch at  $T_{JMAX}$

$V_{OUT}$  = Output voltage

$V_{IN}$  = Input voltage

Because ripple current and switching losses are small with respect to resistive losses at maximum output current, they can be considered negligible for the purpose of this method, but could be included if required.

Using the function describing  $P_{DISS}$  in terms of  $I_{OUT}$ , substitute  $P_{DISS}$  with Equation 7 to form the function of maximum output current  $I_{OUTMAX}$  vs. ambient temperature  $T_{AMB}$  (Equation 10):

$$I_{OUTMAX} = \sqrt{\frac{\frac{T_{JMAX} - T_{AMB}}{R_{\theta(J-A)}}}{R_{DS_{ON\_P}} \times \frac{V_{OUT}}{V_{IN}} + R_{DS_{ON\_N}} \times \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)}} \quad \text{Eq. 10}$$

The curves shown in the "Typical Characteristics" section are plots of this function adjusted to account for 1, 2, or 3 regulators running simultaneously.

## HyperLight Load Mode

Each regulator in the MIC23451 uses a minimum on and off time proprietary control loop (patented by Micrel). When the output voltage falls below the regulation threshold, the error comparator begins a switching cycle that turns the PMOS on and keeps it on for the duration of the minimum-on-time. This increases the output voltage. If the output voltage is over the regulation threshold, then the error comparator turns the PMOS off for a minimum-off-time until the output drops below the threshold. The NMOS acts as an ideal rectifier that conducts when the PMOS is off. Using an NMOS switch instead of a diode allows for lower voltage drop across the switching device when it is on. The asynchronous switching combination between the PMOS and the NMOS allows the control loop to work in discontinuous mode for light load operations. In discontinuous mode, the MIC23451 works in pulse-frequency modulation (PFM) to regulate the output. As the output current increases, the off-time decreases, which provides more energy to the output. This switching scheme improves the efficiency of MIC23451 during light load currents by switching only when it is needed. As the load current

increases, the MIC23451 goes into continuous conduction mode (CCM) and switches at a frequency centered at 3MHz. The equation to calculate the load when the MIC23451 goes into continuous conduction mode is approximated in Equation 11.

$$I_{LOAD} > \left( \frac{(V_{IN} - V_{OUT}) \times D}{2L \times f} \right) \quad \text{Eq. 11}$$

As shown in Equation 11, the load at which the MIC23451 transitions from HyperLight Load mode to PWM mode is a function of the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), duty cycle ( $D$ ), inductance ( $L$ ), and frequency ( $f$ ). Figure 4 shows that as the output current increases, the switching frequency also increases until the MIC23451 goes from HyperLight Load mode to PWM mode at approximately 120mA. The MIC23451 will switch at a relatively constant frequency around 3MHz after the output current is over 120mA.

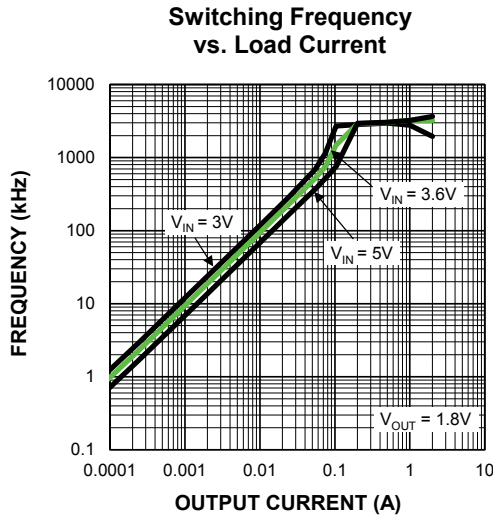


Figure 4. SW Frequency vs. Output Current

**Multiple Sources**

The MIC23451 provides all the pins necessary to operate the three regulators from independent sources. This can be useful in partitioning power within a multi-rail system. For example, two supplies may be available within a system: 3.3V and 5V. The MIC23451 can be connected to use the 3.3V supply to provide two, low-voltage outputs (for example, 1.2V and 1.8V) and use the 5V rail to provide a higher output (for example, 2.5V), resulting in the power blocks shown in Figure 5.

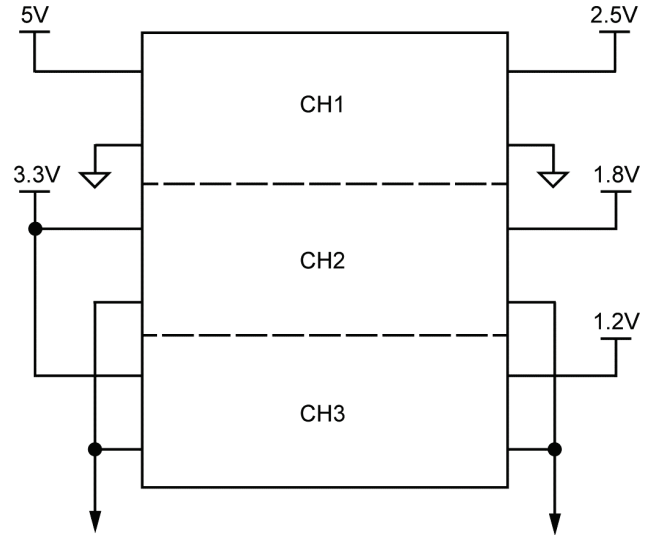
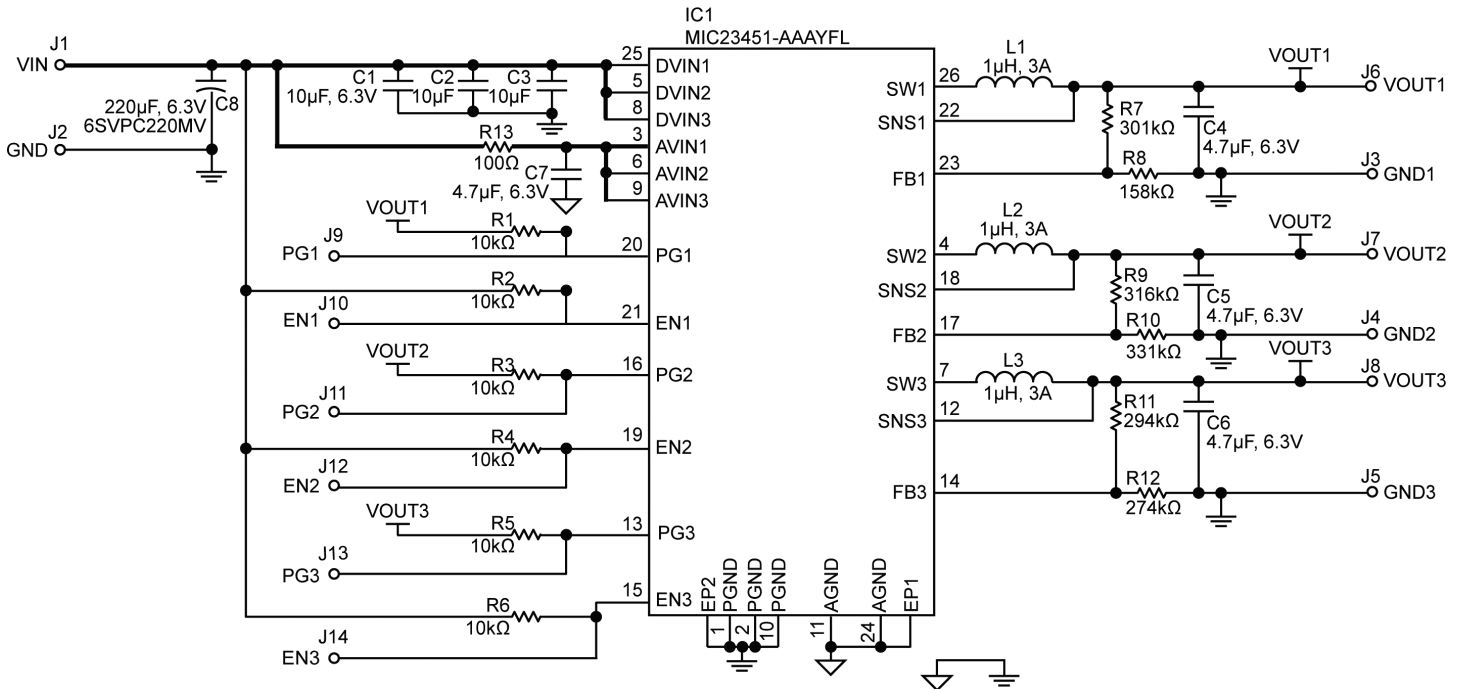


Figure 5. Multi-Source Power Block Diagram



## Typical Application Schematic



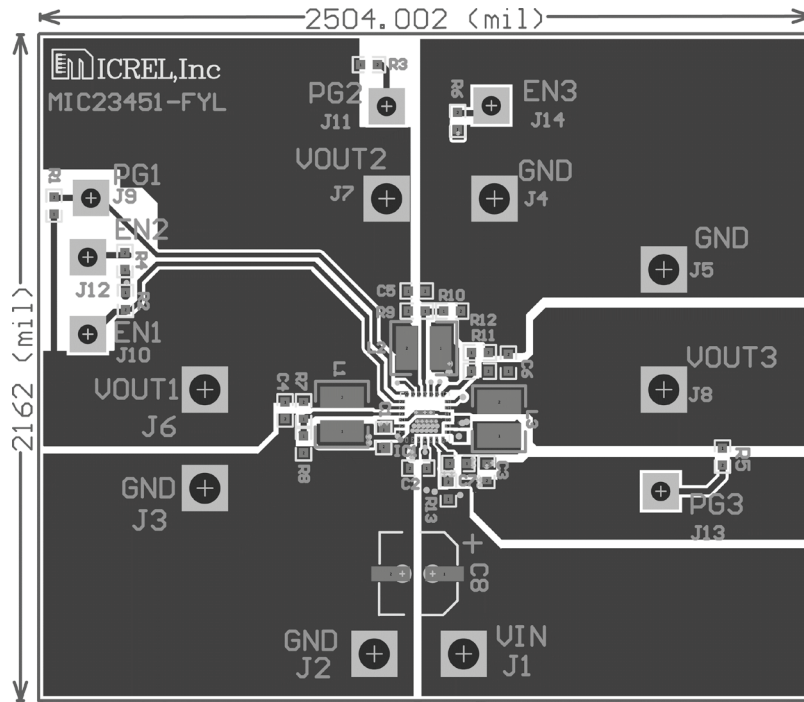
## Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C3	GRM188R60J106KE19D	Murata <sup>(1)</sup>	Capacitor, 10µF, Size 0603	3
C4, C5, C6, C7	C1608X5R0J475K	TDK <sup>(2)</sup>	Capacitor, 4.7µF, Size 0603	4
	GRM188R60J475KE19D	Murata		
C8	EEUFR1A221	Panasonic <sup>(3)</sup>	Electrolytic Capacitor, 220µF, 10V, Size 6.3mm	
R1, R2, R3, R4, R5, R6	CRCW060310K0FKEA	Vishay <sup>(4)</sup>	Resistor, 10KΩ, Size 0603	6
R7	CRCW0603301K0FKEA	Vishay	Resistor, 301KΩ, Size 0603	1
R8	CRCW0603158K0FKEA	Vishay	Resistor, 158KΩ, Size 0603	1
R9	CRCW0603316K0FKEA	Vishay	Resistor, 316Ω, Size 0603	1
R10	CRCW0603331K0FKEA	Vishay	Resistor, 331KΩ, Size 0603	1
R11	CRCW0603294K0FKEA	Vishay	Resistor, 294KΩ, Size 0603	1
R12	CRCW0603274K0FKEA	Vishay	Resistor, 274KΩ, Size 0603	1
L1, L2, L3	VLS3012ST-1R0N1R9	TDK	1µH, 2A, 60mΩ, L3.0mm x W3.0mm x H1.0mm	3
	LQH44PN1R0NJ0	Murata	1µH, 2.8A, 50mΩ, L4.0mm x W4.0mm x H1.2mm	
U1	MIC23451-AAAYFL	Micrel, Inc. <sup>(5)</sup>	3MHz PWM 2A Buck Regulator with HyperLight <sup>®</sup> Load	1

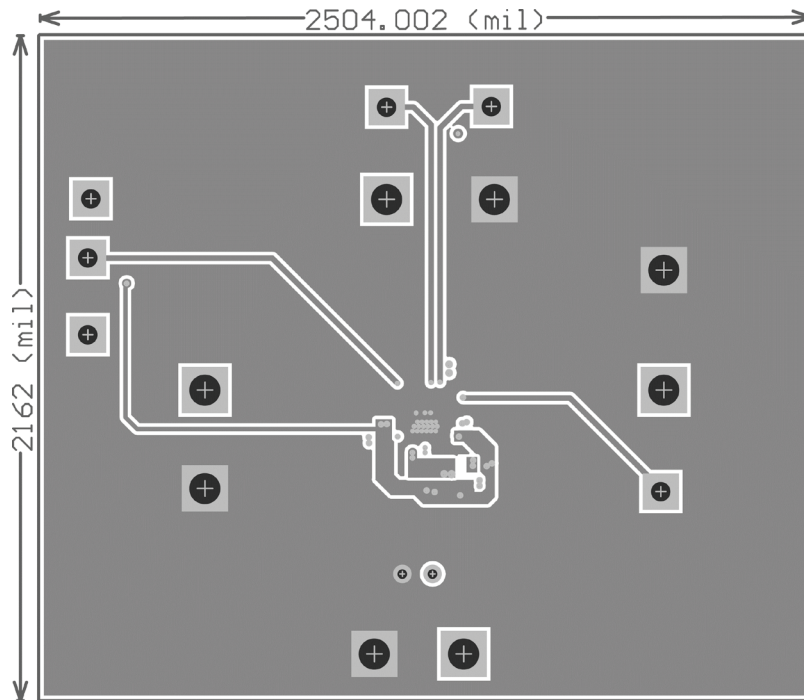
### Notes:

1. TDK: [www.tdk.com](http://www.tdk.com).
2. Murata Tel: [www.murata.com](http://www.murata.com).
3. Panasonic: [www.panasonic.com](http://www.panasonic.com).
4. Vishay Tel: [www.vishay.com](http://www.vishay.com).
5. Micrel, Inc.: [www.micrel.com](http://www.micrel.com).

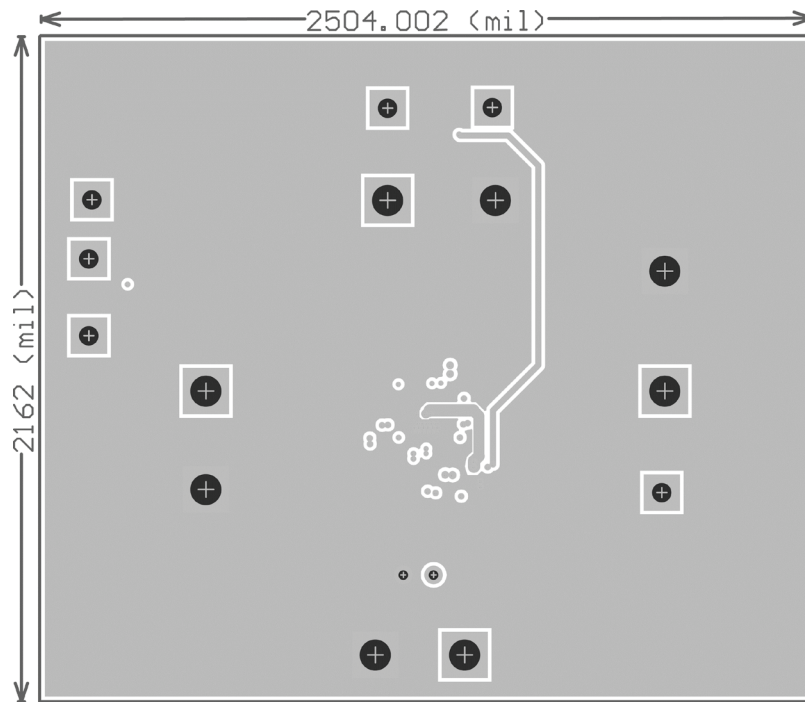
### PCB Layout Recommendations



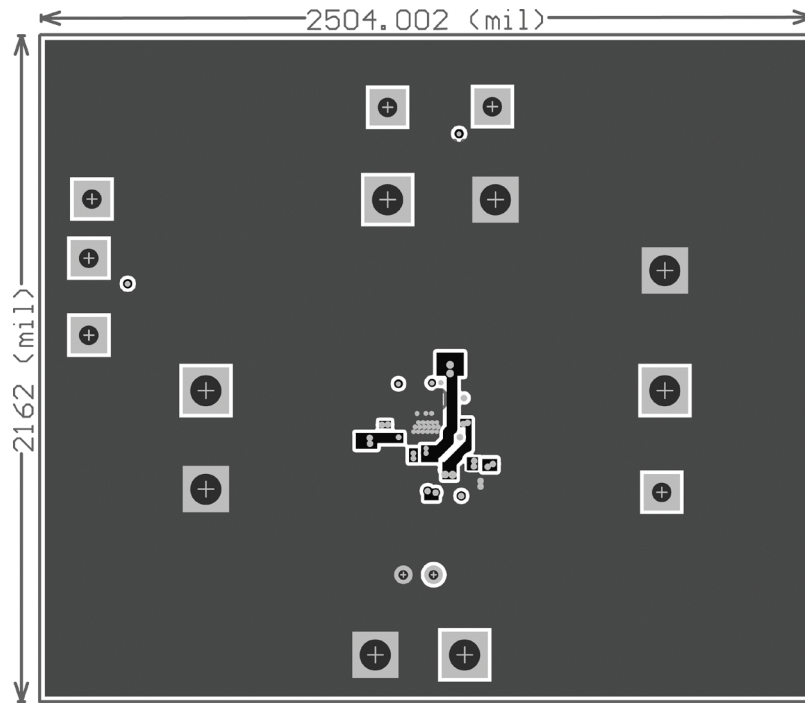
Top Layer



Mid Layer 1

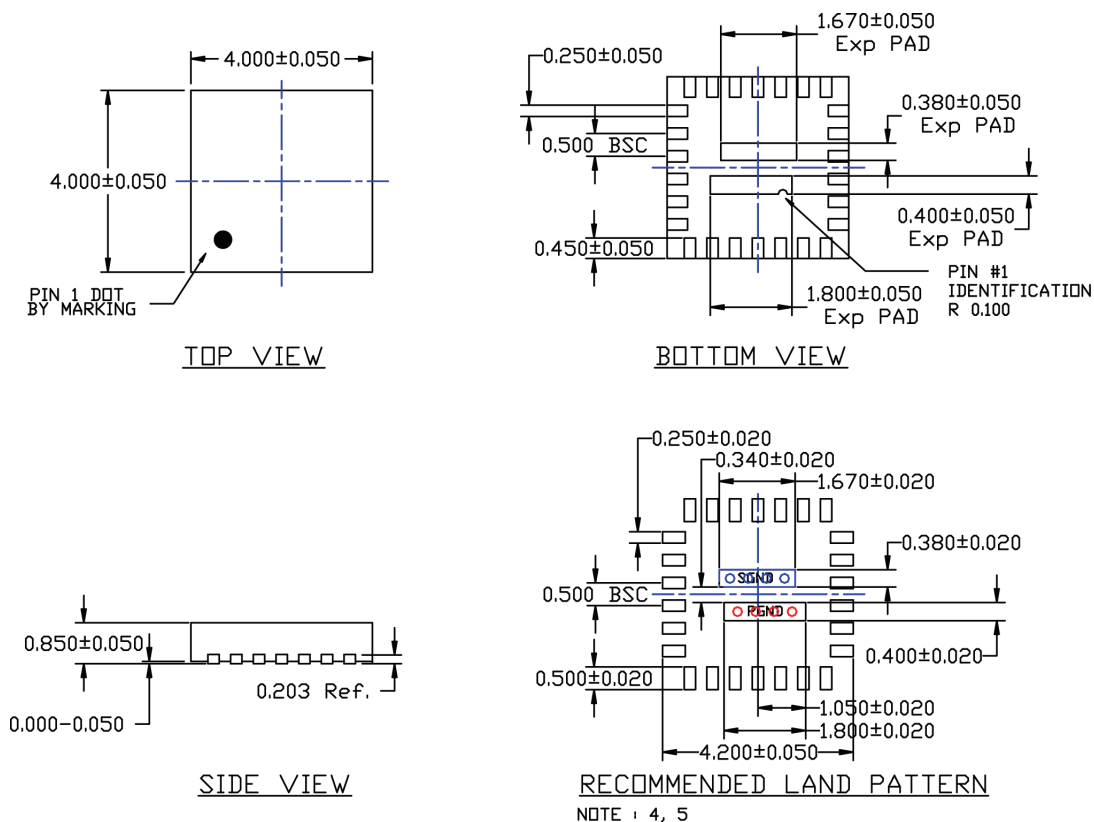


Mid Layer 2



Bottom Layer

**Package Information<sup>(1)</sup>**



**NOTE :**

1. Max package warpage is 0.05mm
2. Max allowable burr is 0.076mm in all directions
3. Pin #1 will be laser marked
4. Red circle in PGND indicate thermal via. Size should be 0.20mm in diameter, 0.40mm pitch and should be connected to GND for max thermal performance.
5. Blue colored pad & circle indicate SGND, do not connect to GND.

**26-Pin 4mm x 4mm QFN (FL)**

**Note:**

1. Package information is correct as of the publication date. For updates and most current information, go to [www.micrel.com](http://www.micrel.com).

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