Description

The 20N06 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

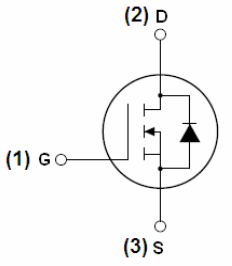
General Features

V_{DSS}	$R_{DS(ON)}$ @4.5V(Typ)	$R_{DS(ON)}$ @10V (Typ)	I_D
60V	53 mΩ	42mΩ	20A

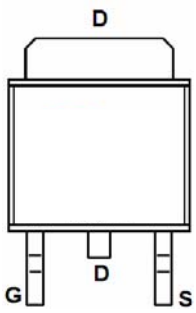
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability
- Totally Lead-Free&Fully RoHS Compliant

Application

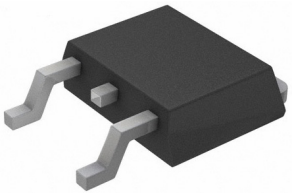
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-252 top view

Ordering Information

Part Number	Marking	Case	Packaging
20N06	20N06	TO-252	2500pcs/Reel

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	20	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	14	A
Pulsed Drain Current	I_{DM}	60	A
Maximum Power Dissipation	P_D	40	W
Derating factor		0.27	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	72	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case (Note 2)	$R_{\theta JC}$	3.7	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

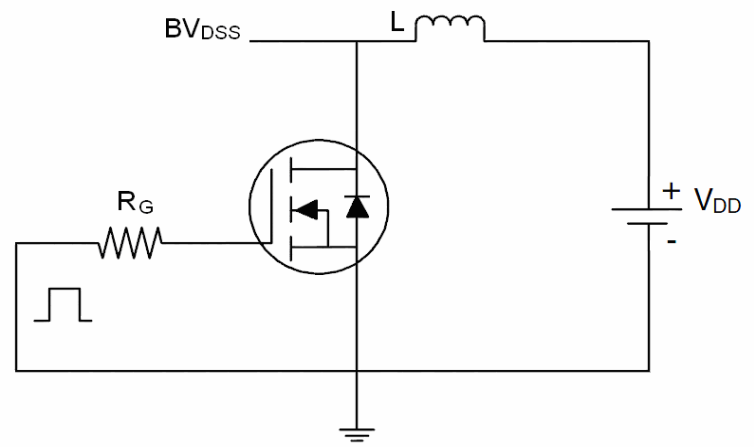
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0	2.0	3.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=10A	-	42	60	mΩ
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=10A	-	53	80	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=4.5A	11	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=30V,V_{GS}=0V, F=1.0MHz	-	500	-	PF
Output Capacitance	C_{oss}		-	60	-	PF
Reverse Transfer Capacitance	C_{rss}		-	25	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V,I_D=2A,R_L=6.7Ω V_{GS}=10V,R_G=3Ω	-	5	-	nS
Turn-on Rise Time	t_r		-	2.6	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	16.1	-	nS
Turn-Off Fall Time	t_f		-	2.3	-	nS
Total Gate Charge	Q_g	V_{DS}=30V,I_D=4.5A, V_{GS}=10V	-	14		nC
Gate-Source Charge	Q_{gs}		-	2.9		nC
Gate-Drain Charge	Q_{gd}		-	5.2		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=20A	-		1.2	V
Diode Forward Current (Note 2)	I_S		-	-	20	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =20A di/dt = 100A/μs (Note3)	-	35	-	nS
Reverse Recovery Charge	Qrr		-	53	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

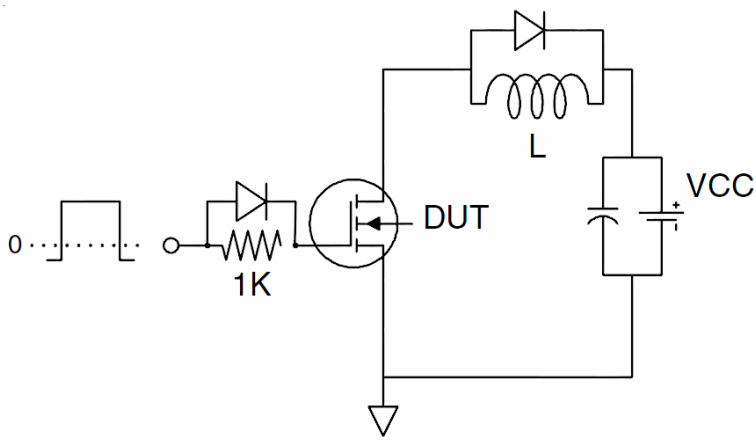
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition:Tj=25℃,VDD=30V,VG=10V,L=0.5mH,Rg=25Ω

Test Circuit

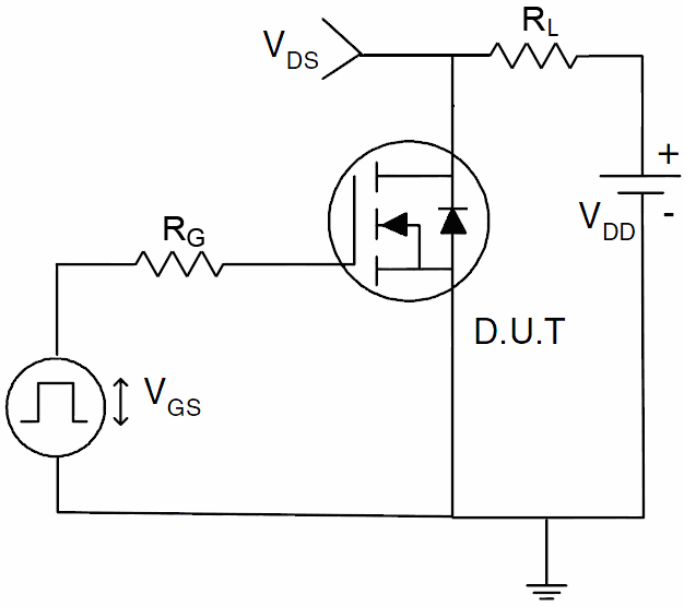
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

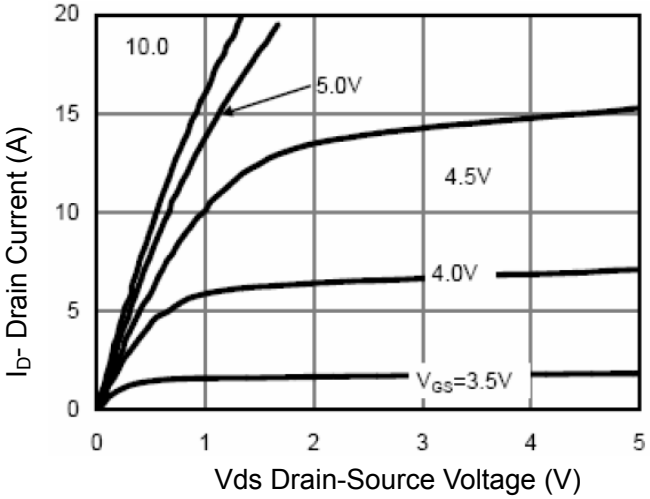


Figure 1 Output Characteristics

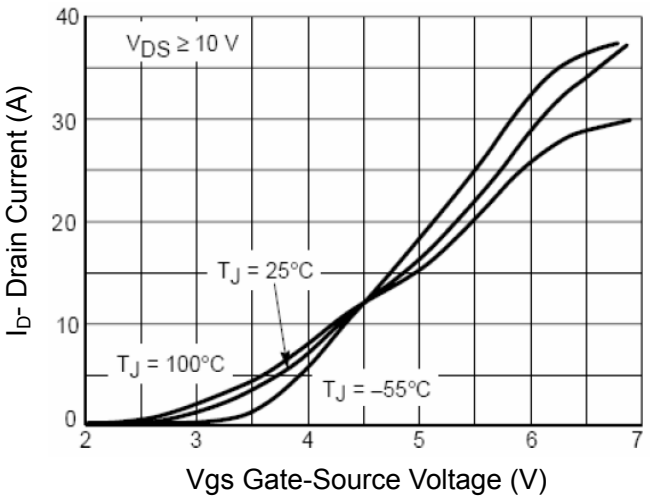


Figure 2 Transfer Characteristics

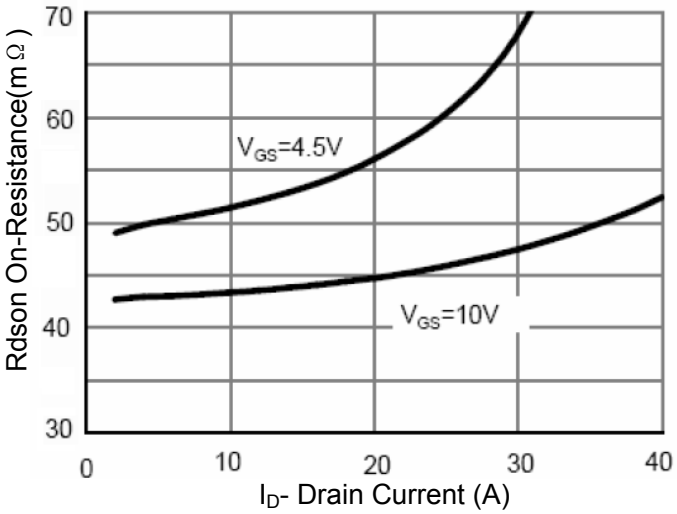


Figure 3 Rdson- Drain Current

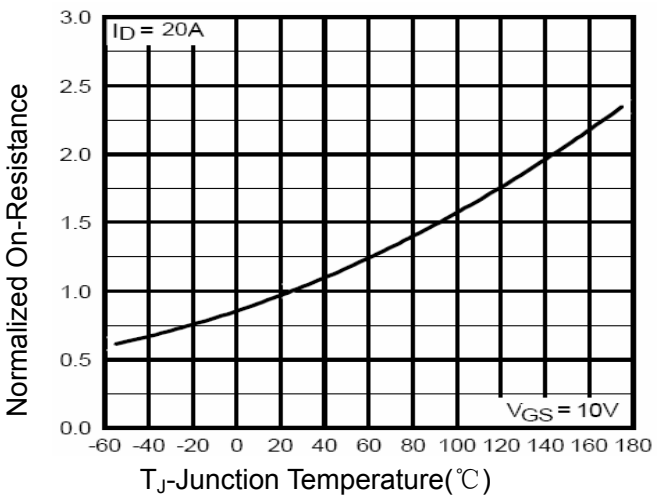


Figure 4 Rdson-Junction Temperature

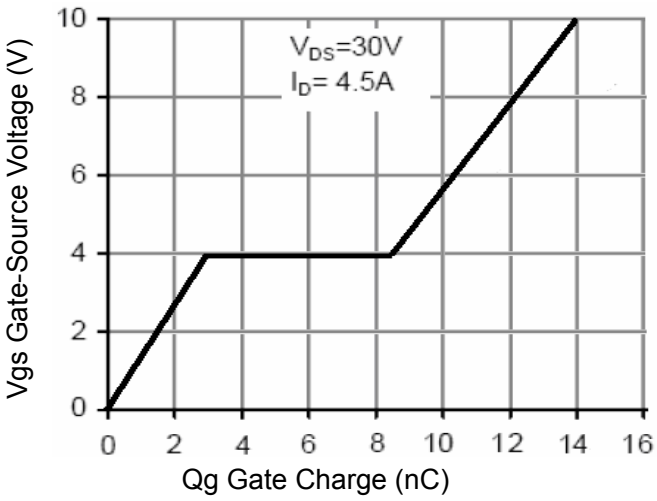


Figure 5 Gate Charge

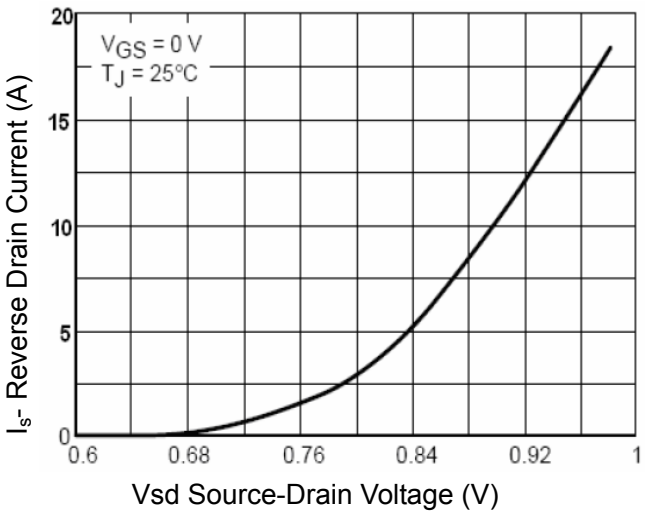


Figure 6 Source- Drain Diode Forward

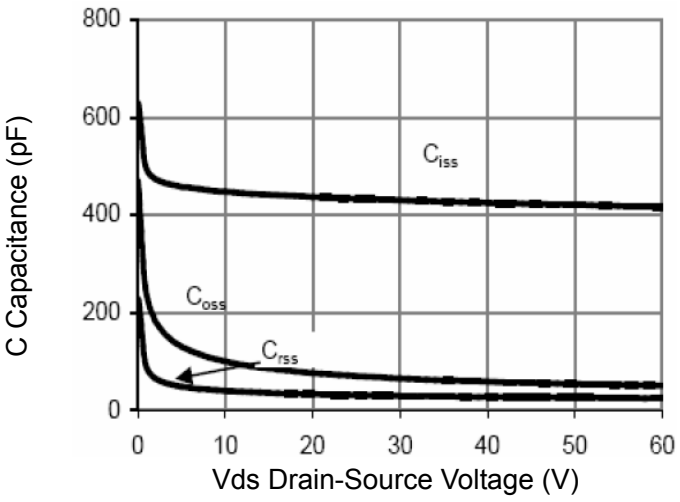


Figure 7 Capacitance vs Vds

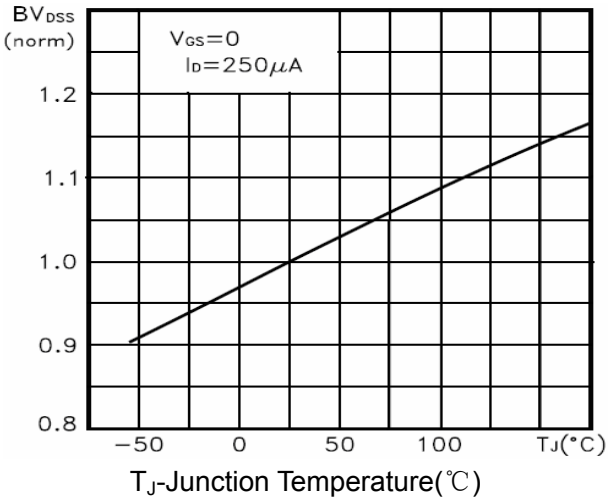


Figure 9 BV_{DSS} vs Junction Temperature

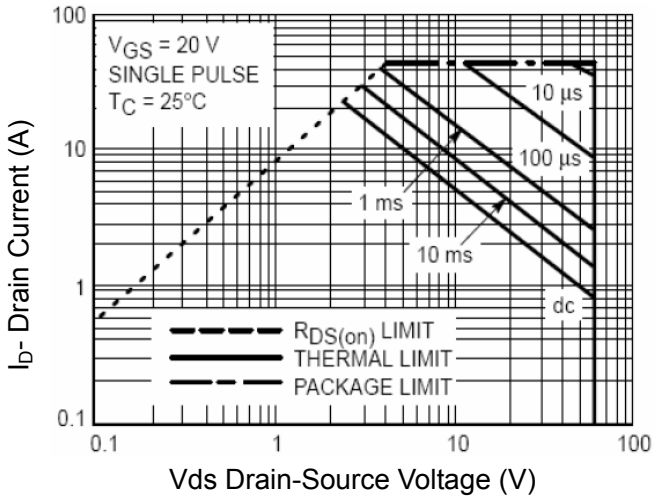


Figure 8 Safe Operation Area

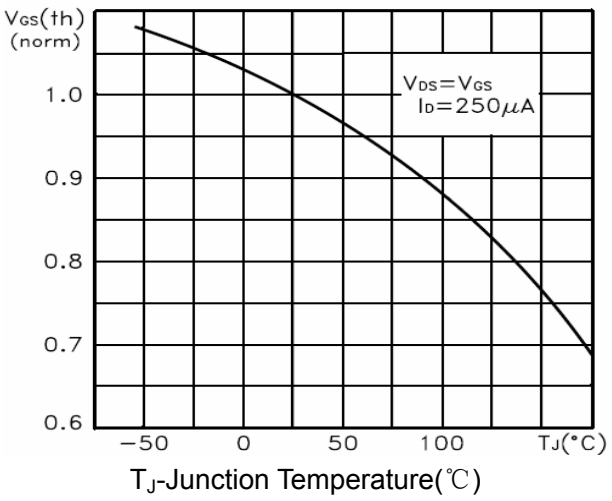


Figure 10 $V_{GS(th)}$ vs Junction Temperature

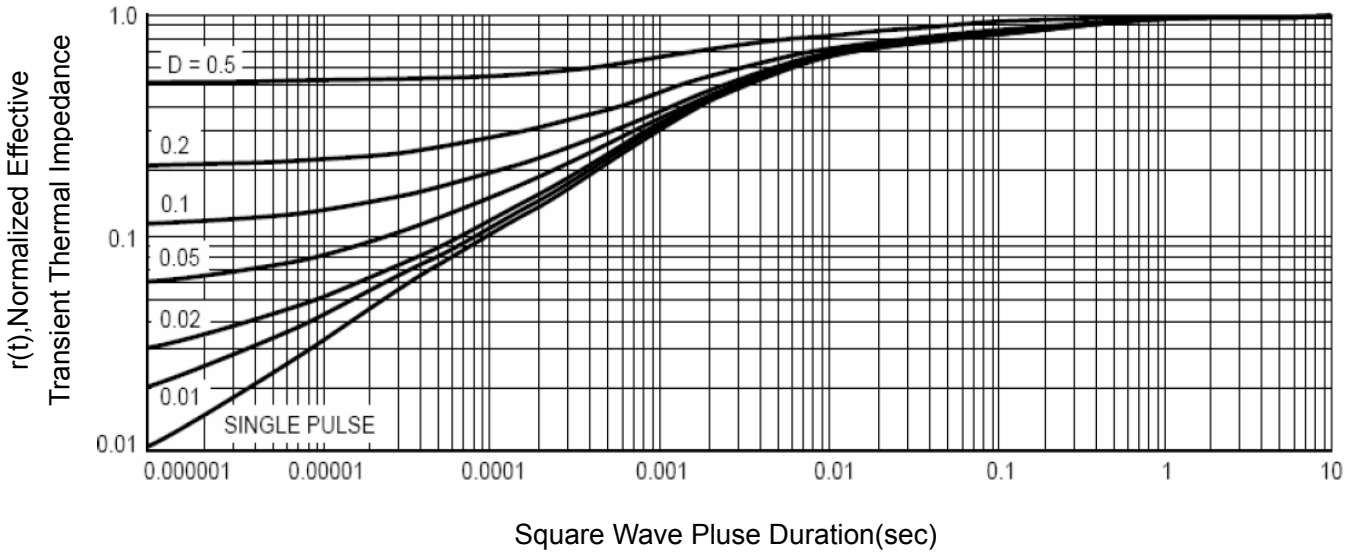
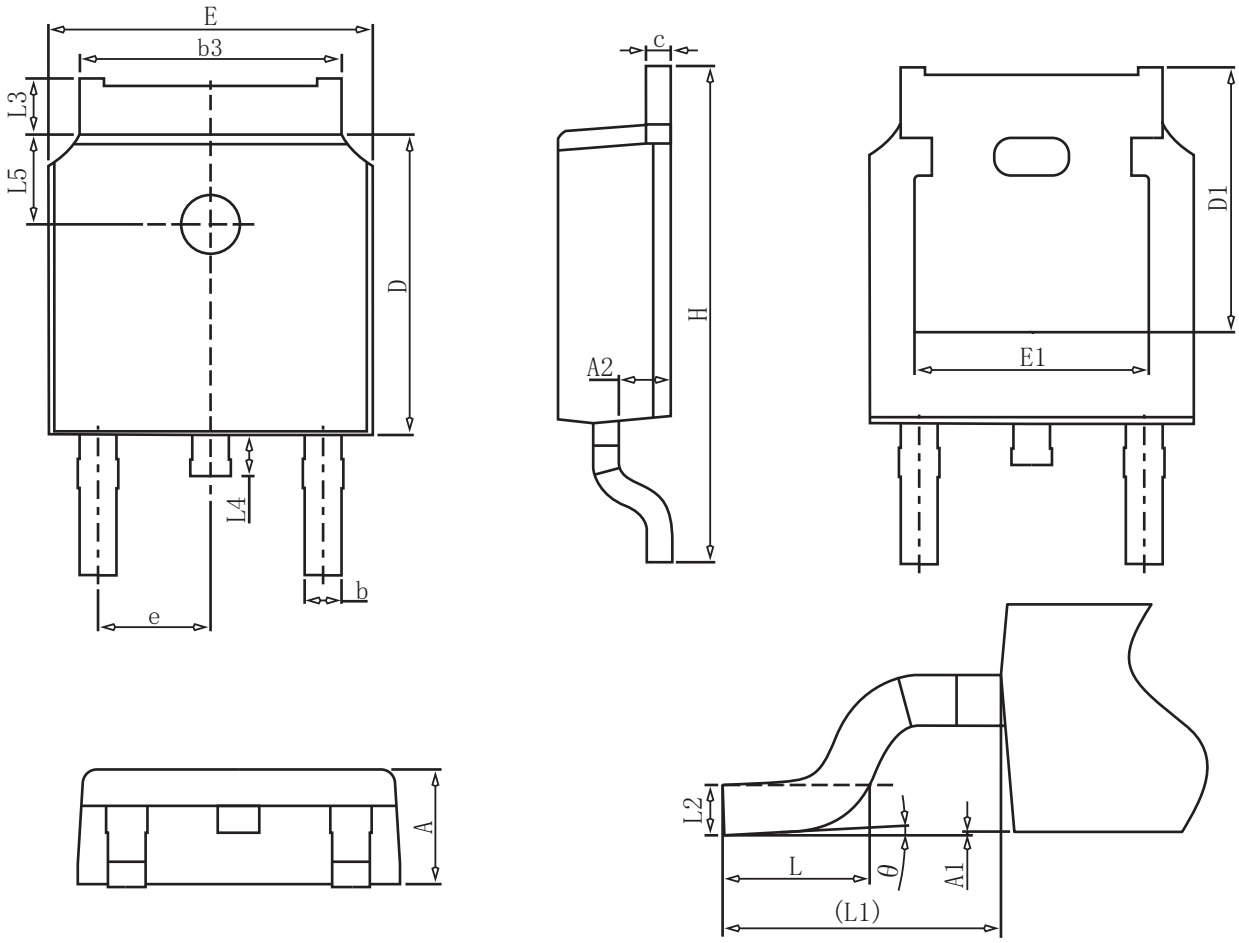


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 package information



COMMON DIMENSIONS

SYMBOL	mm		
	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.00	–	0.20
A2	0.97	1.07	1.17
b	0.68	0.78	0.90
b3	5.20	5.33	5.50
c	0.43	0.53	0.63
D	5.98	6.10	6.22
D1		5.30REF	
E	6.40	6.60	6.80
E1	4.63	–	–
e		2.286BSC	
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1		2.90REF	
L2		0.51BSC	
L3	0.88	–	1.28
L4	0.50	–	1.00
L5	1.65	1.80	1.95
θ	0°	–	8°