

Description

LPN1510C uses advanced FSMOS™ technology to provide low $R_{DS(on)}$, low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness and suitable to use in Synchronous-rectification applications.

◆ $V_{DS,min}$	100V
◆ $I_{D,pulse}$	160A
◆ $R_{DS(ON),max}@V_{GS}=10V$	14m Ω
◆ Q_g	34.4nC

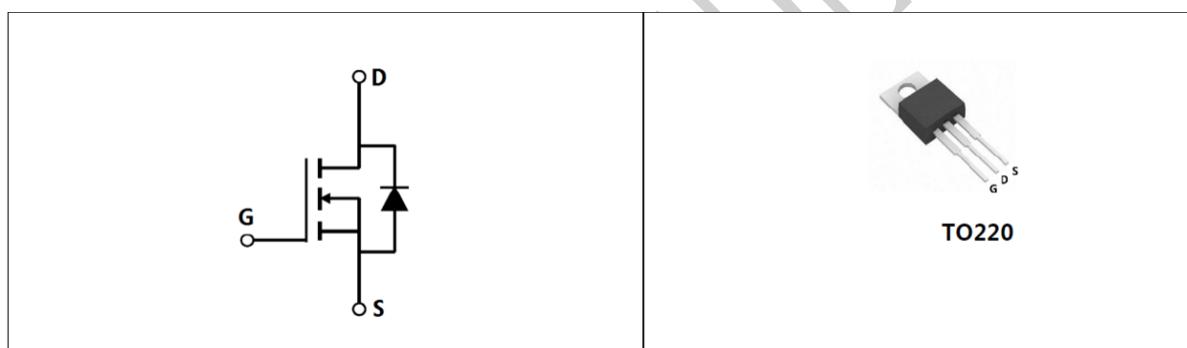
Features

- Low $R_{DS(on)}$ &FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Fast switching and soft recovery

Applications

- Consumer electronic power supply
- Motor control
- Synchronous-rectification
- Isolated DC/DC convertor
- Invertors

Schematic and Package Information



Schematic Diagram

Pin Assignment Top View

Ordering Information

Package	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Box/Carton Box	Units/Carton Box
TO220	50	20	1000	6	6000

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
LPN1510C	TO220	yes	yes	yes

Absolute Maximum Rating at $T_j=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	100	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾	I_D	55	A
Pulsed drain current ²⁾	$I_{D,pulse}$	160	A
Power dissipation ³⁾	P_D	300	W
Single pulsed avalanche energy ⁵⁾	E_{AS}	100	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	$R_{\theta JC}$	0.38	$^\circ\text{C}/\text{W}$
Thermal resistance, junction-ambient ⁴⁾	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$

Electrical Characteristics at $T_j=25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	100			V	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$
Gate threshold voltage	$V_{GS(\text{th})}$	1.5		2.5	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$
Drain-source on-state resistance	$R_{DS(\text{ON})}$		11.0	14.0	$\text{m}\Omega$	$V_{GS}=10\text{V}, I_D=12\text{A}$
Drain-source on-state resistance	$R_{DS(\text{ON})}$		15.0	18.0	$\text{m}\Omega$	$V_{GS}=4.5\text{V}, I_D=9\text{A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20\text{V}$
				-100		$V_{GS}=-20\text{V}$
Drain-source leakage current	I_{DS}			1	μA	$V_{DS}=100\text{V}, V_{GS}=0\text{V}$

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		2145.8		pF	$V_{GS}=0\text{V}, V_{DS}=50\text{V}, f=100\text{kHz}$
Output capacitance	C_{oss}		305.7		pF	
Reverse transfer capacitance	C_{rss}		9.6		pF	
Turn-on delay time	$T_{d(on)}$		19.5		nS	$V_{GS}=10\text{V}, V_{DS}=50\text{V}, R_G=2\Omega, I_D=10\text{A}$
Rise time	t_r		6.2		nS	
Turn-off delay time	$T_{d(off)}$		43.8		nS	
Fall time	t_f		9.3		nS	

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		34.4		nC	$I_D=10\text{A}, V_{DS}=50\text{V}, V_{GS}=10\text{V}$
Gate-source charge	Q_{gs}		5.3		nC	
Gate-drain charge	Q_{gd}		8.0		nC	
Gate plateau voltage	$V_{plateau}$		3.0		V	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward current	I _S			55	A	V _{GS} <V _{th}
Pulsed source current	I _{SP}			160	A	
Diode forward voltage	V _{SD}			1.3	V	I _S =12A, V _{GS} =0V
Reverse recovery time	t _{rr}		59.3		nS	I _S =12A, di/dt=100A/uS
Reverse recovery charge	Q _{rr}		108.7		nC	
Peak reverse recovery current	I _{rrm}		3.0		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) Pd is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of R_{θJA} is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_a=25°C.
- 5) V_{DD}=50V, R_G=25 Ω, L=0.3mH, starting T_j=25°C

Electrical Characteristics Diagrams

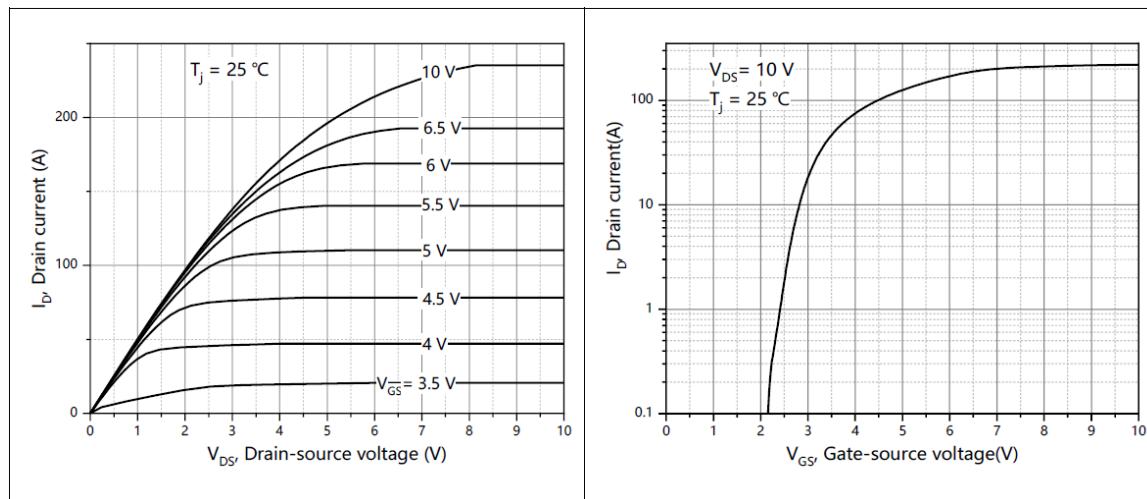


Figure 1, Typ. Output characteristics

Figure 2, Typ. Transfer characteristics

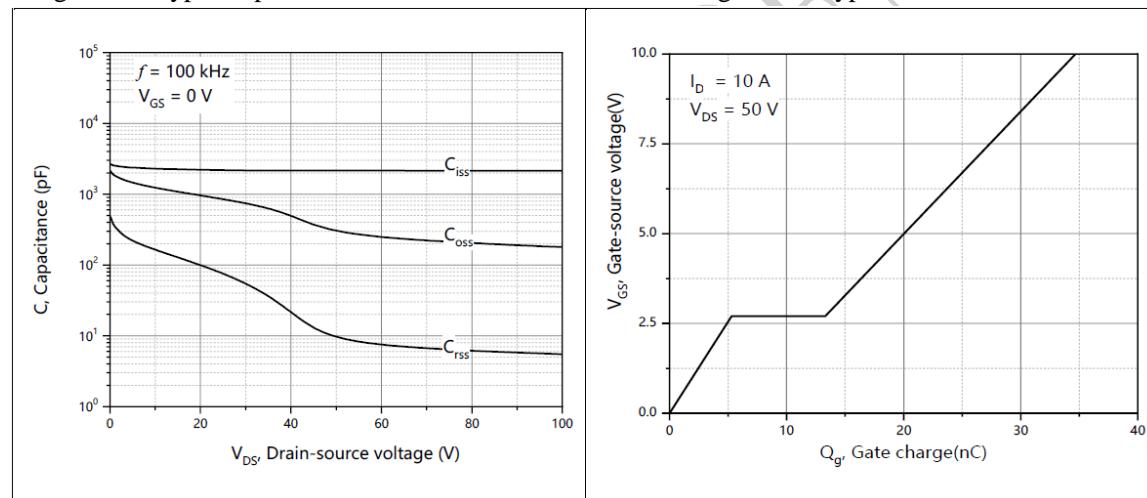


Figure 3, Typ. capacitances

Figure 4, Typ. gate charge

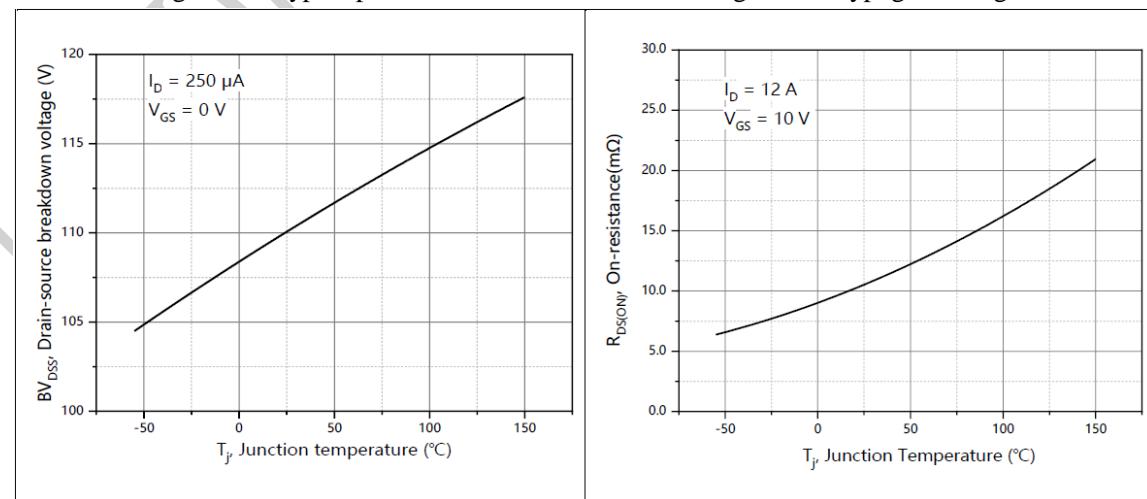


Figure 5, Drain-source breakdown voltage

Figure 6, Drain-source on-state resistance

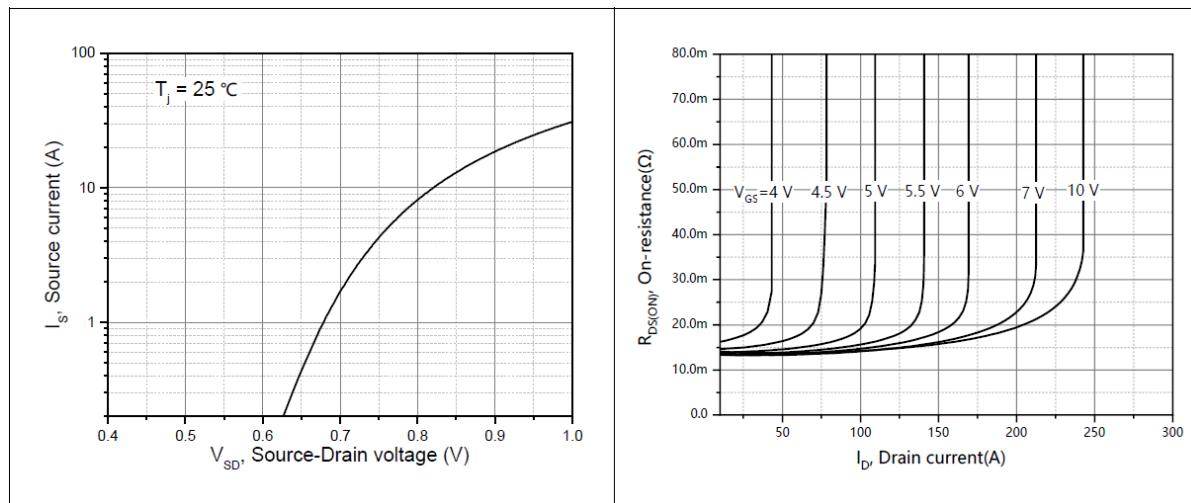


Figure 7, Forward characteristics of body diode

Figure 8, Drain-source on-state resistance

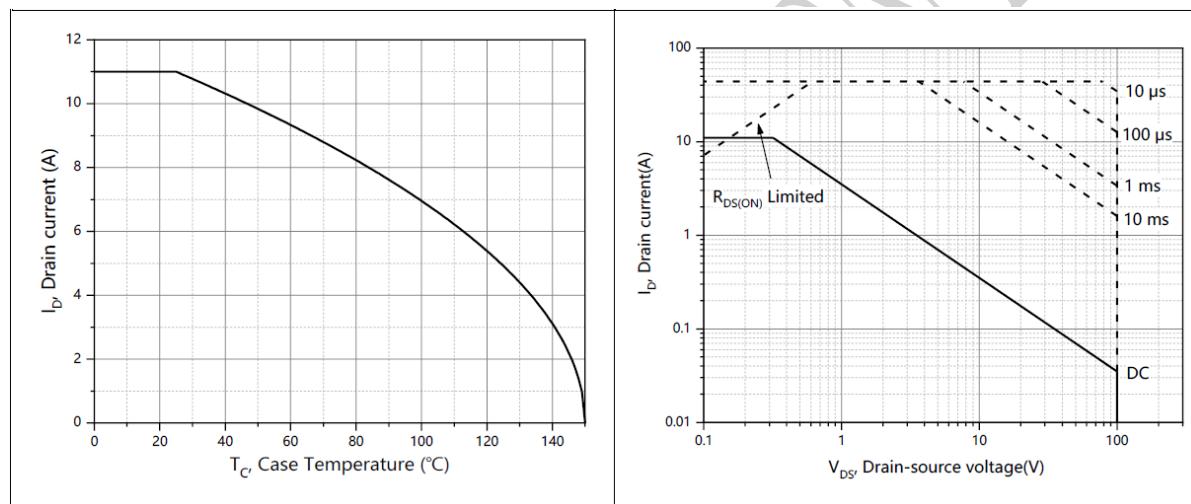


Figure 9, Drain current

Figure 10, Safe operation area $T_C=25^\circ\text{C}$

Test circuits and waveforms

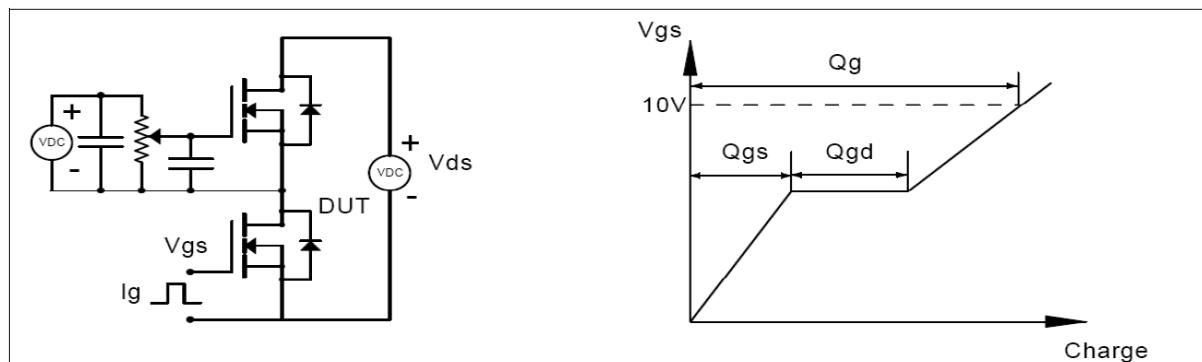


Figure 1, Gate charge test circuit &waveform

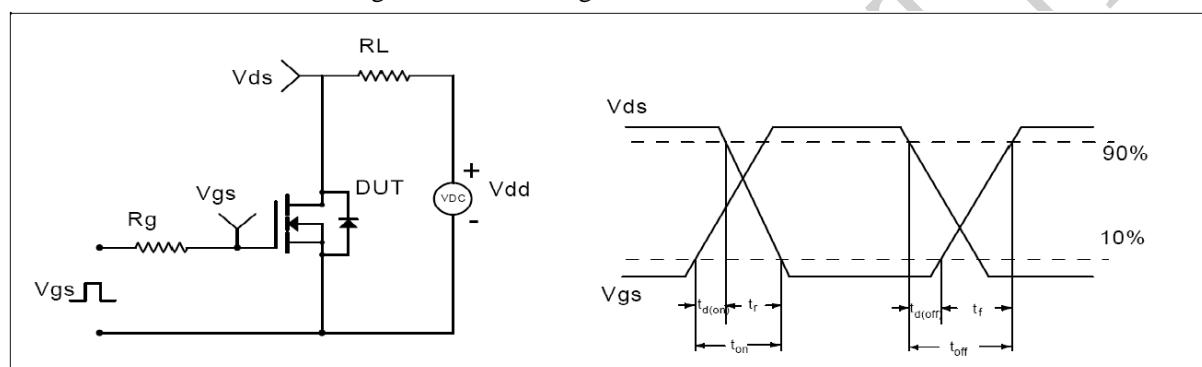


Figure 2, Switching time test circuit & waveforms

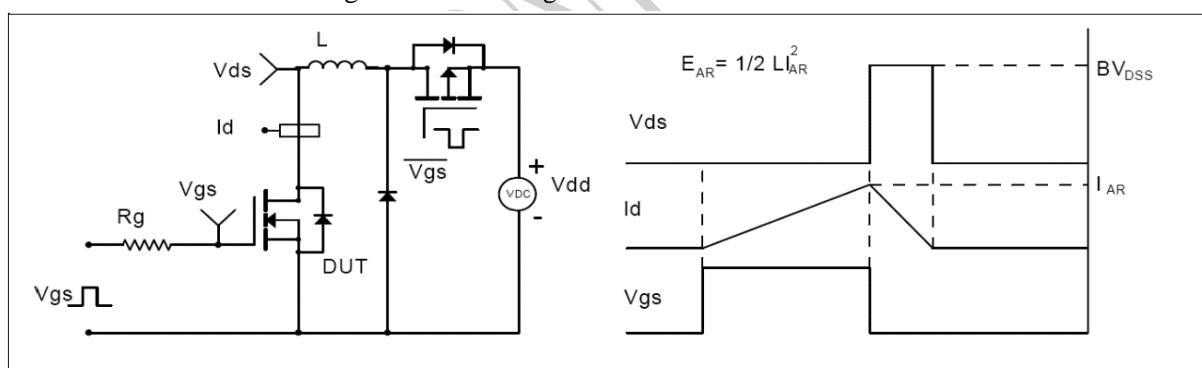


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

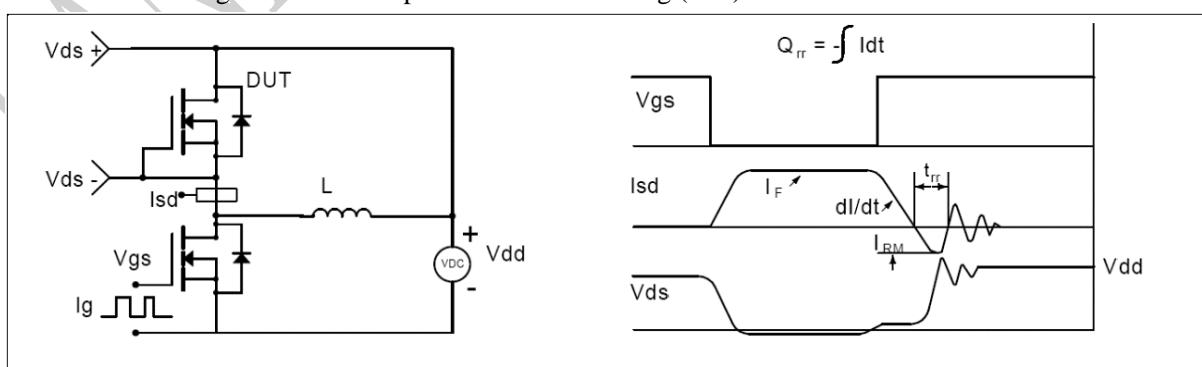
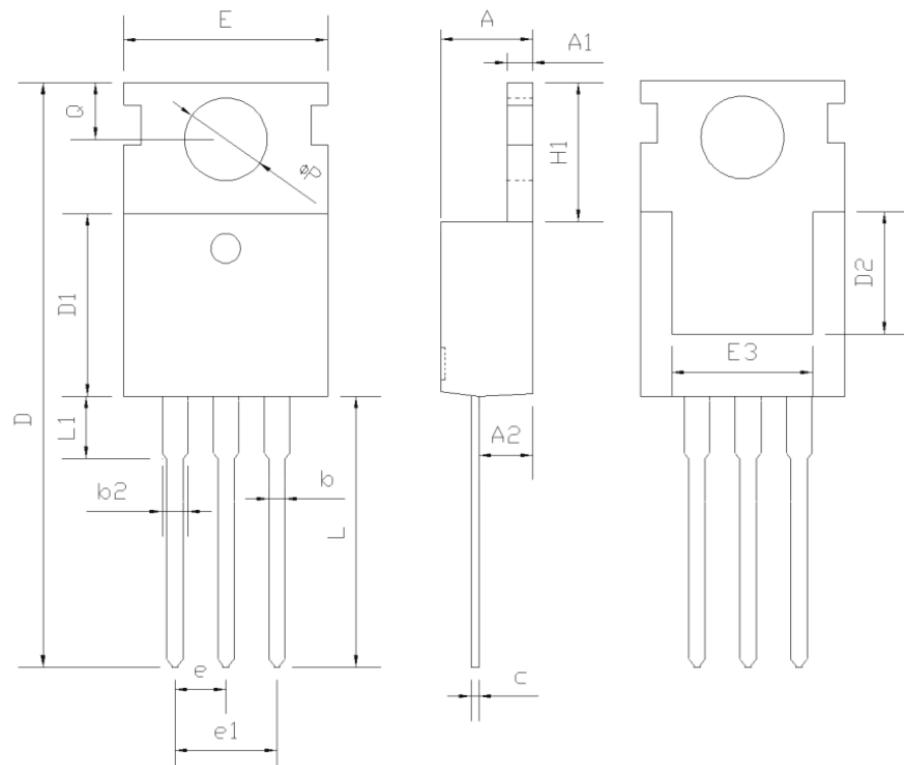


Figure 4, Diode reverse recovery test circuit & waveforms

Package Information



Symbol	Min	Nom	Max
A	4.37	4.57	4.77
A1	1.25	1.30	1.45
A2	2.20	2.40	2.60
b	0.70	0.80	0.95
b2	1.17	1.27	1.47
c	0.40	0.50	0.65
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	-	-
E	9.70	10.00	10.30
E3	7.00	-	-
e	2.54 BSC		
e1	5.08 BSC		
H1	6.25	6.50	6.85
L	12.75	13.50	13.80
L1	-	3.10	3.40
ΦP	3.40	3.60	3.80
Q	2.60	2.80	3.00