LPN1010C

Enhancement Mode N-Channel Power MOSFET

Description

LPN1010C use advanced FSMOS™ technology to provide low $R_{DS(on)}$, low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness and suitable to use in Synchronous-rectification applications.

◆ $V_{DS,min}$	100V
◆ $I_{D,pulse}$	210A
◆ $R_{DS(ON),max}$@V_{GS}=10V	10mΩ
◆ $R_{DS(ON),max}$@V_{GS}=4.5V	14mΩ
◆ Q_g	72nC

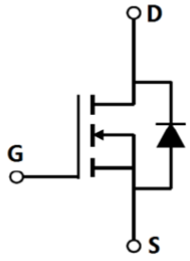
Features

- Low $R_{DS(on)}$&FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Fast switching and soft recovery

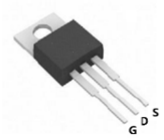
Applications

- Consumer electronic power supply
- Motor control
- Synchronous-rectification
- Isolated DC/DC convertor
- Invertors

Schematic and Package Information



Schematic Diagram



TO220

Pin Assignment Top View

Ordering Information

Package	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Box/Carton Box	Units/Carton Box
TO220	50	20	1000	6	6000

Product Information

Product	Package	Pb Free	RoHS	Halogen Free
LPN1010C	TO220	yes	yes	yes

Absolute Maximum Rating at T_j=25℃ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	100	V
Gate source voltage	V_{GS}	±20	V
Continuous drain current[1)]	I_D	70	A
Pulsed drain current[2)]	$I_{D,puse}$	210	A
Power dissipation[3)]	P_D	330	W
Single pulsed avalanche energy[5)]	E_{AS}	100	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 150	℃

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-case	$R_{\theta JC}$	0.38	℃/W
Thermal resistance, junction-ambient[4)]	$R_{\theta JA}$	62.5	℃/W

Electrical Characteristics at T_j=25℃ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	100			V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{GS(th)}$	1.0		2.5	V	V_{DS}= V_{GS}, I_D=250uA
Drain-source on-state resistance	$R_{DS(ON)}$			10.0	mΩ	V_{GS}=10V, I_D=10A
Drain-source on-state resistance	$R_{DS(ON)}$			14.0	mΩ	V_{GS}=4.5V, I_D=10A
Gate-source leakage current	I_{GSS}			100	nA	V_{GS}=20V
				-100		V_{GS}=-20V
Drain-source leakage current	I_{DSS}			1	uA	V_{DS}=100V, V_{GS}=0V

Dynamic Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Input capacitance	C_{iss}		3888.5		pF	V_{GS}=0V,
Output capacitance	C_{oss}		273.7		pF	V_{DS}=100V,
Reverse transfer capacitance	C_{rss}		5		pF	f=1MHz
Turn-on delay time	$T_{d(on)}$		49.6		nS	V_{GS}=10V,
Rise time	t_r		52.5		nS	V_{DS}=50V,
Turn-off delay time	$T_{d(off)}$		390		nS	R_G=25Ω,
Fall time	t_f		55.2		nS	I_D=12A

Gate Charge Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Total gate charge	Q_g		72		nC	I_D=12A, V_{DS}=50V, V_{GS}=10V
Gate-source charge	Q_{gs}		8.9		nC	
Gate-drain charge	Q_{gd}		18.8		nC	
Gate plateau voltage	$V_{plateau}$		3.2		V	

Body Diode Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Diode forward current	I_S			70	A	V_{GS}<Vth
Pulsed source current	I_{SP}			210	A	
Diode forward voltage	V_{SD}			1.3	V	I_S=20A，V_{GS}=0V
Reverse recovery time	t_{rr}		66.8		nS	I_S=12A，di/dt=100A/uS
Reverse recovery charge	Q_{rr}		139		nC	
Peak reverse recovery current	I_{rrm}		3.5		A	

Note

1） Calculated continuous current based on maximum allowable junction temperature.

2） Repetitive rating；pulse width limited by max. junction temperature.

3） Pd is based on max. junction temperature，using junction-case thermal resistance.

4） The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper，in a still air environment with T_a=25℃.

5） V_{DD}=50V，R_G=25Ω，L=0.3mH，starting T_j=25℃

Electrical Characteristics Diagrams

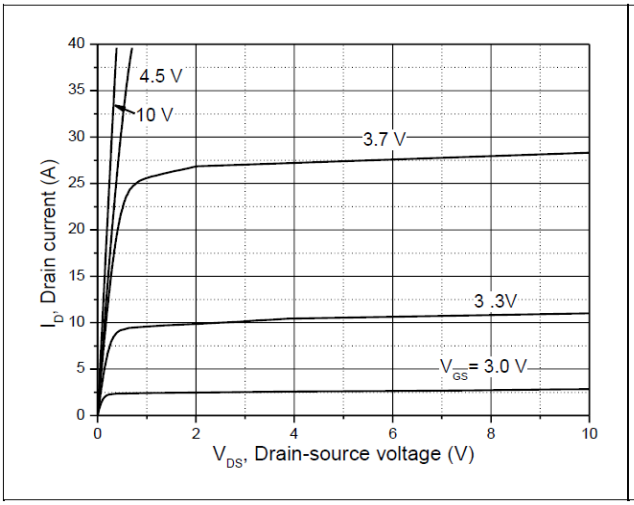


Figure 1， Typ. Output characteristics

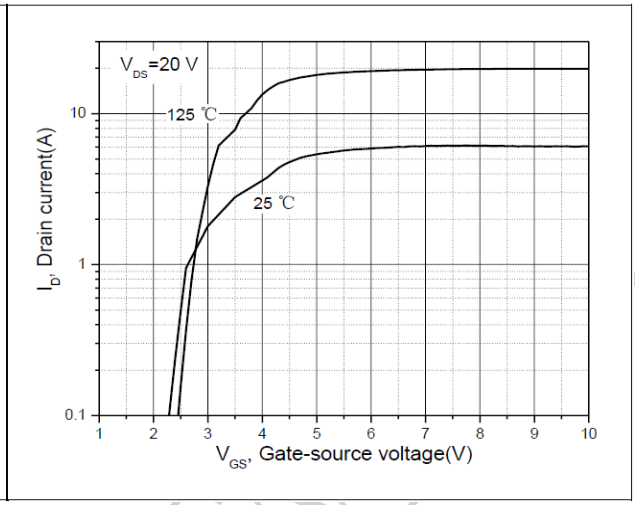


Figure 2， Typ. Transfer characteristics

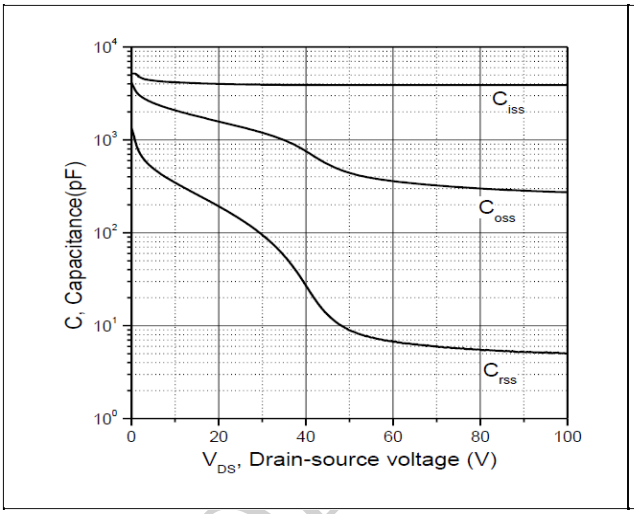


Figure 3， Typ. capacitances

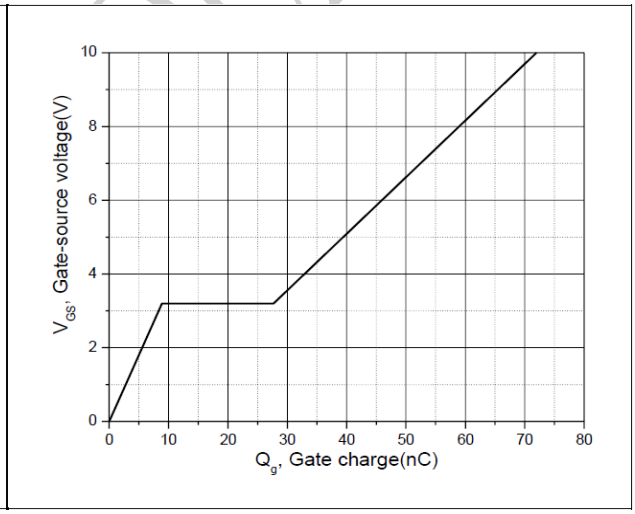


Figure 4， Typ. gate charge

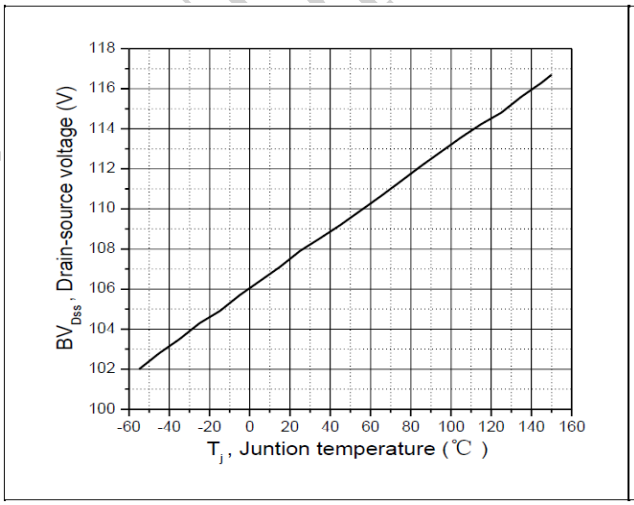


Figure 5， Drain-source breakdown voltage

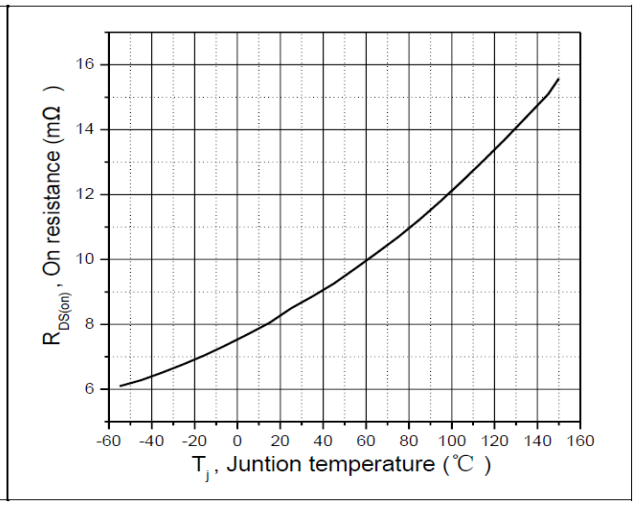


Figure 6， Drain-source on-state resistance

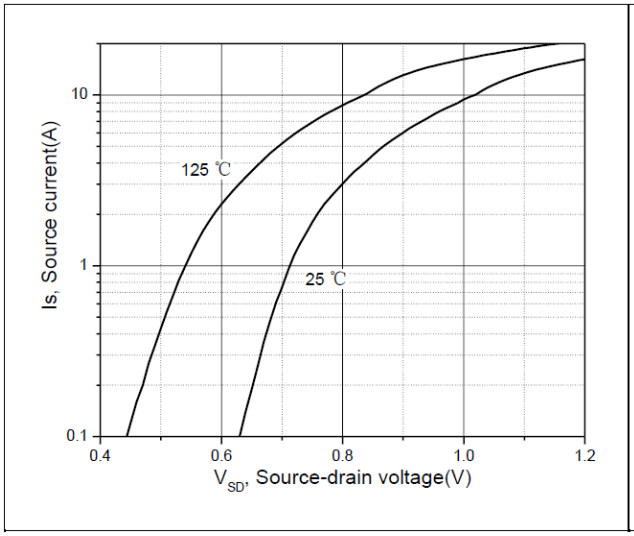


Figure 7，Forward characteristics of body diode

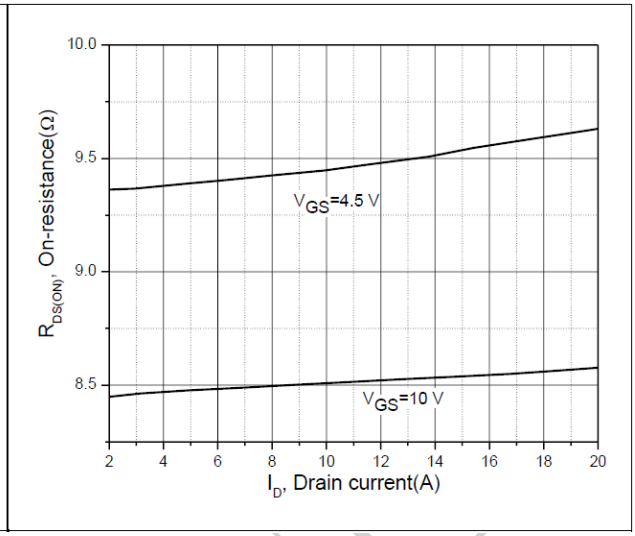


Figure 8，Drain-source on-state resistance

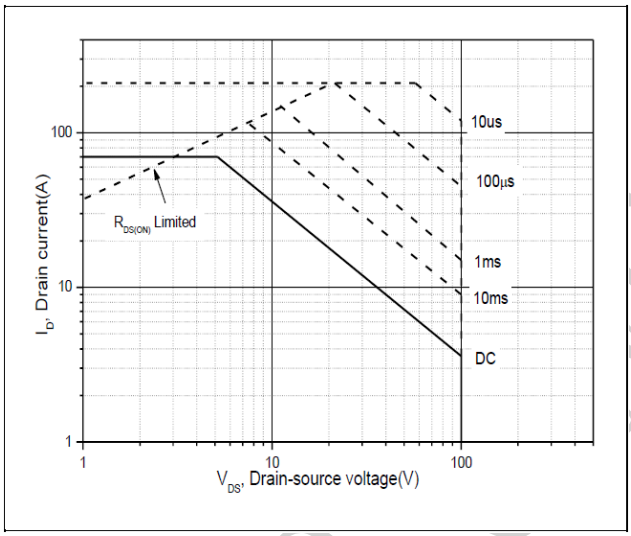


Figure 9，Safe operation area T_C=25℃

Test circuits and waveforms

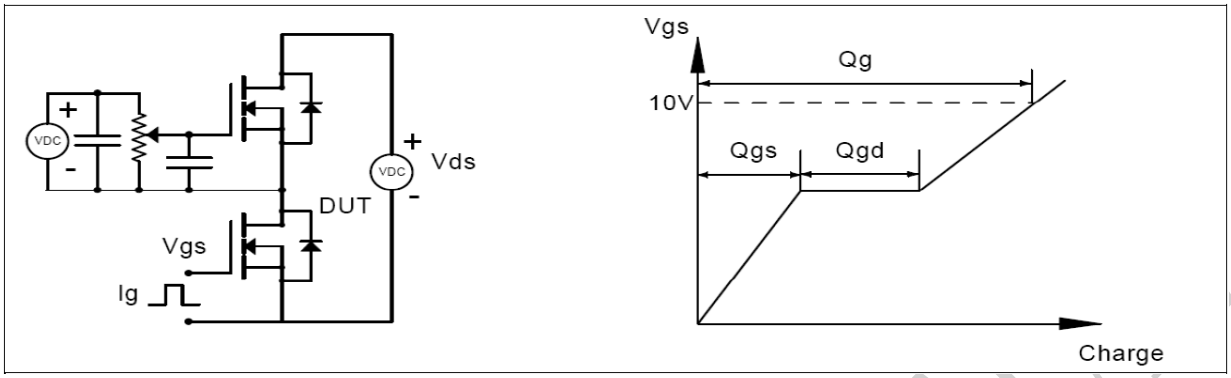


Figure 1，Gate charge test circuit &waveform

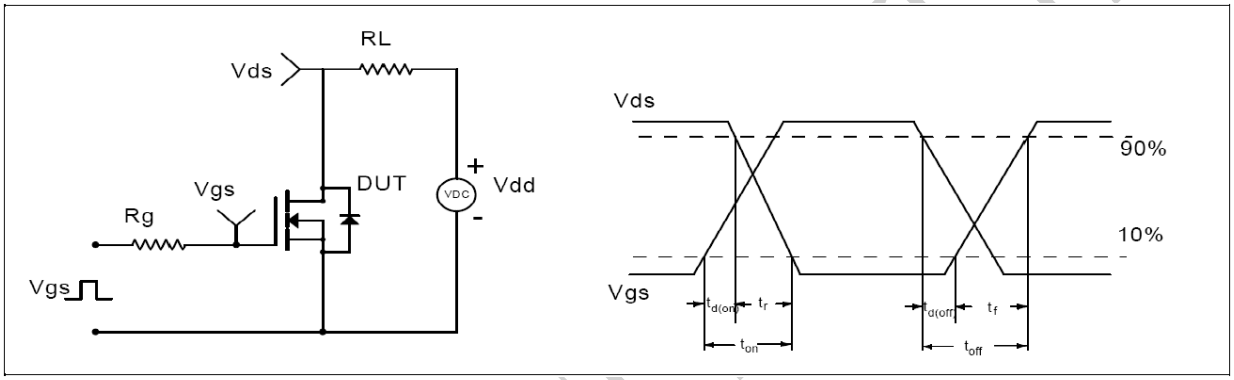


Figure 2，Switching time test circuit & waveforms

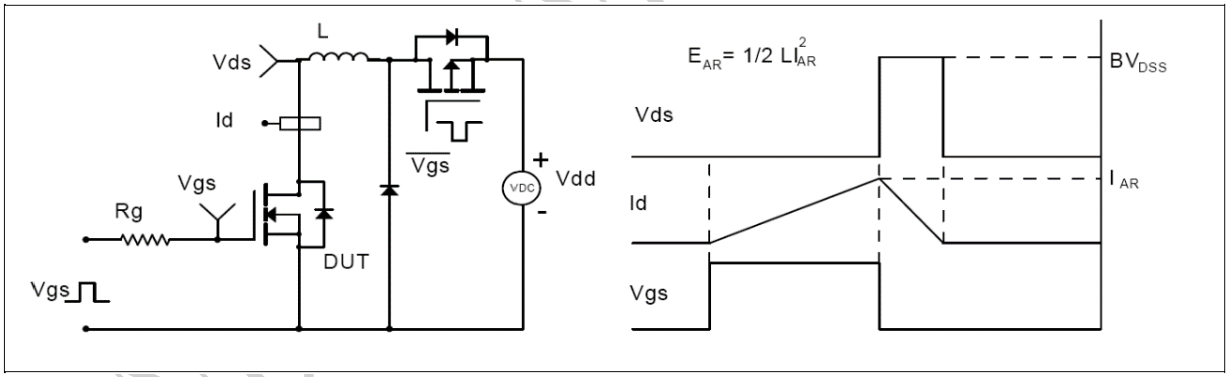


Figure 3，Unclamped inductive switching (UIS) test circuit & waveforms

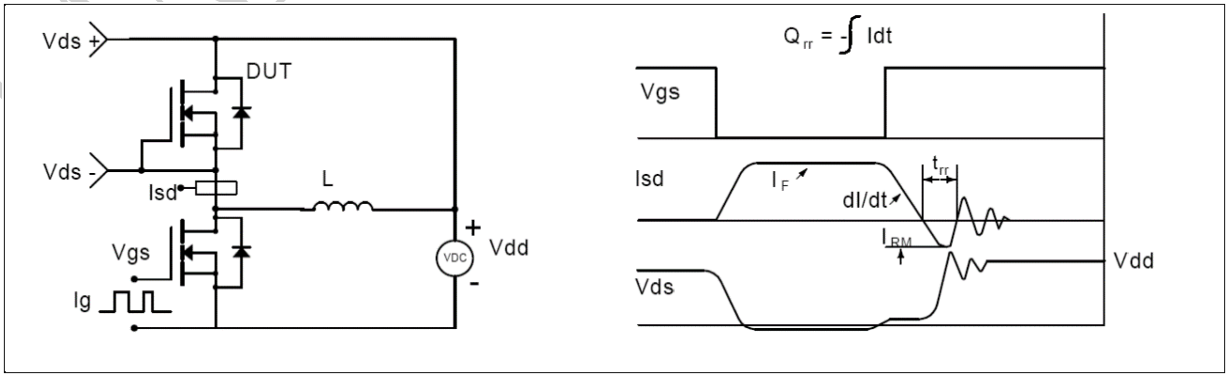
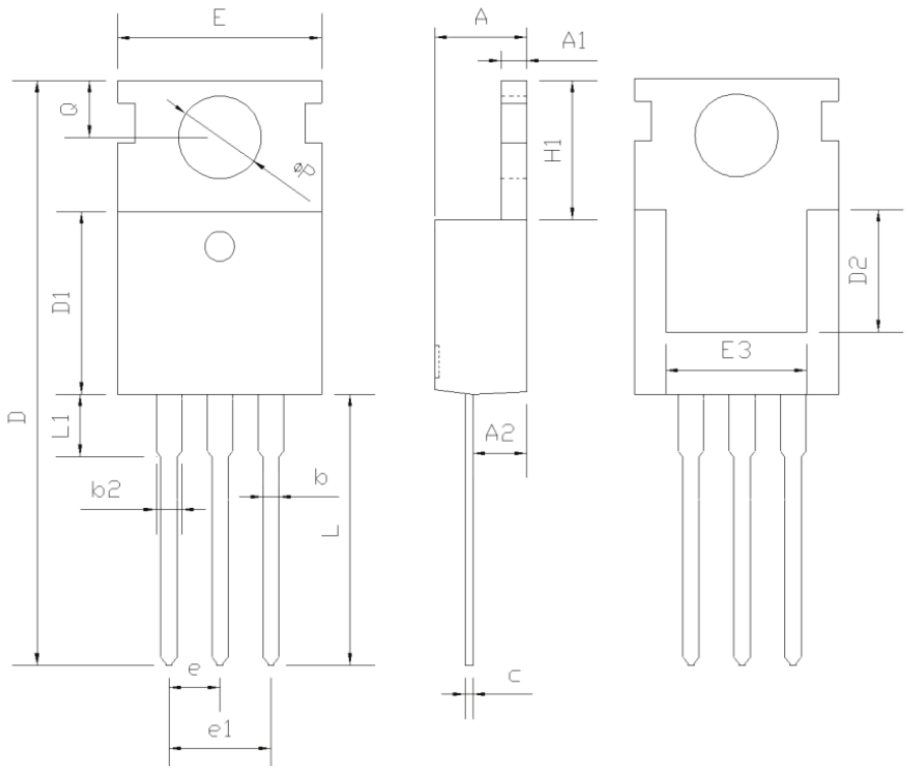


Figure 4，Diode reverse recovery test circuit & waveforms

Package Information



Symbol	Min	Nom	Max
A	4.37	4.57	4.77
A1	1.25	1.30	1.45
A2	2.20	2.40	2.60
b	0.70	0.80	0.95
b2	1.17	1.27	1.47
c	0.40	0.50	0.65
D	15.10	15.60	16.10
D1	8.80	9.10	9.40
D2	5.50	-	-
E	9.70	10.00	10.30
E3	7.00	-	-
e	2.54 BSC		
e1	5.08 BSC		
H1	6.25	6.50	6.85
L	12.75	13.50	13.80
L1	-	3.10	3.40
ΦP	3.40	3.60	3.80
Q	2.60	2.80	3.00