Application Note:AN_SY6935

High Efficiency, 3.5A, Multi-Cell Li-Ion Battery Charger

Preliminary Specification

General Description

SY6935 is a 4-14V input, 3.5A Multi-cell Li-Ion battery step-down charger. The charge current up to 3.5A can be programmed by using the external resistor for different portable applications. It also has a programmable charge timeout and adaptive input power limit for safety battery charge operation. It consists of 16V rating reverse blocking FET and power switching FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

SY6935 along with small QFN3x3 footprint provides small PCB area application.

Ordering Information

SY6935 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6935QDC	QFN3x3-16	

Features

- Integrated Synchronous Buck and Reverse Blocking FET with 16V Rating
- Adaptive Input Power Limit for 4-14V Wide Input Voltage
- Maximum 3.5A Programmable Charge Current
- 4.2V and 4.35V Constant Voltage Selectable
- +/-0.5% Cell Voltage Accuracy
- Support Single-cell or Two-cell Battery Pack
- External Shutdown Function
- Input Voltage UVLO and OVP
- Thermal Fold-back Protection
- Over Temperature Protection
- Battery Short Protection
- Programmable Charge Timeout
- Charge Status Indication
- Low Profile QFN3x3 Package for Portable Applications

Applications

- Power bank
- Cellular Telephones, PDA, MP3 Players, MP4 Players
- PSP Game Players, NDS Game Players
- Notebook

Typical Applications

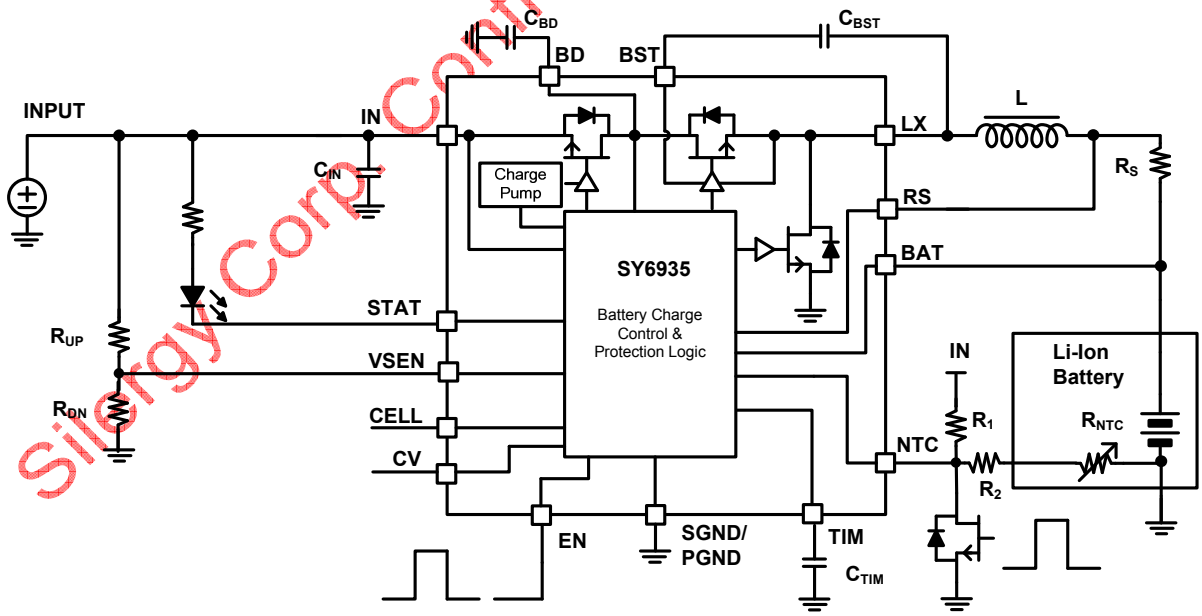
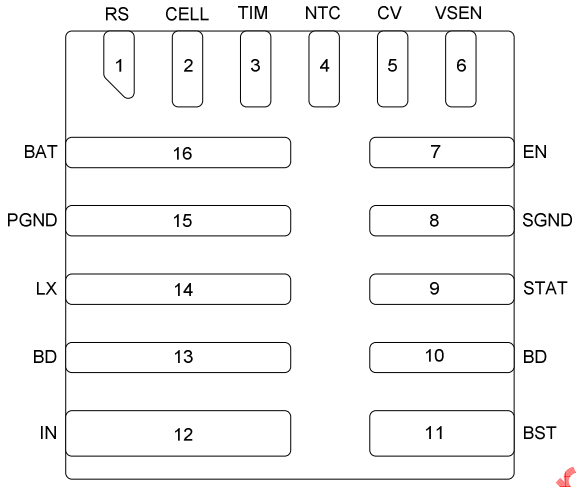


Figure 1. Schematic Diagram

Pinout (top view)



(QFN3x3-16)

Top Mark: **BHF*xyz***, (Device code: BHF, ***x=year code, y=week code, z= lot number code***)

Name	Pin Number	Description
RS	1	Charge current sense resistor positive pin. The sensed voltage drop between RS and BAT is used for charge current regulation and charge termination detection.
CELL	2	Battery voltage selection pin. Floating for two cells battery and grounding for single cell battery. CELL pin can't be pulled high to any bias voltage higher than 3.3V.
TIM	3	Charge time-out programming pin. Connect this pin with a capacitor to ground to program the time-out protection threshold. Internal current source charge the capacitor for TC mode and fast charge (CC&CV) mode's charge time limit. TC charge time limit is about 1/9 of fast charge time.
NTC	4	Battery thermal sense pin. The voltage on the NTC pin is sensed for battery thermal protection. UTP threshold is typical 75%V_{IN} and OTP threshold is typical 45% V_{IN}. NTC pin also can be used for the adaptive input power limit reference refresh. The adaptive input power limit threshold will be refreshed when NTC is pulled low for more than 100ms. SY6935 set the charge current to the trickle value, then IC refreshes the adaptive input power limit threshold according the input voltage. For higher than 6V input, IC clamps the input voltage at V_{IN}-0.6V by regulating the duty cycle of Buck converter. For lower than 6V input, the clamped input voltage is set by VSEN pin.
CV	5	Battery CV voltage selection pin.
VSEN	6	Input voltage sense pin for adaptive input power limit. If the voltage drops to internal 1.19V reference voltage, the V_{IN} will be clamped to setting value and input current will be limited.
EN	7	Enable control pin. High logic for enable on and low logic for enable off.
SGND	8	Signal ground pin.
STAT	9	Charge status indication pin. Open drain pin. Pull high to IN thru a LED to indicate the charge in process. When the charge is done, LED is off.
BD	10, 13	Connect to the Drain of internal Blocking FET. Bypass at least10uF ceramic cap to GND.
BST	11	Boot-Strap pin. Supply Main FET's gate driver. Decouple this pin to LX with 0.1uF ceramic cap.
IN	12	DC power input pin. Connect a MLCC from this pin to ground to decouple high harmonic Noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage area.

LX	14	Switch node pin. Connect to external inductor.
PGND	15	Power ground pin.
BAT	16	Battery voltage sense pin.

Absolute Maximum Ratings

IN, BAT, LX, NTC, STAT, BD, EN, CV, VSEN ---------- 18V
TIM, CELL---------- 4V
BST-LX Voltage ---------- 4V
RS ---------- BAT-0.3~BAT+0.3V
LX Pin current continuous ---------- 5A
Power Dissipation, P_D @ T_A = 25°C, QFN3x3---------- 2.1W
Package Thermal Resistance
θ_{JA} ----------48 °C/W
θ_{JC} ----------4 °C/W
Junction Temperature Range ---------- -40°C to +125°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions

IN ---------- 4V to 14V
BAT, LX, NTC, STAT, BD, EN, CV, VSEN----------0V to16V
TIM, CELL---------- 0V to 3.3V
BST-LX Voltage ---------- 0V to 3.3V
RS ---------- BAT-0.25~BAT+0.25V
LX Pin current continuous ---------- 4.5A
Junction Temperature Range ---------- -40°C to 100°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

T_A=25°C, V_{IN}=5V, GND=0V, C_{IN}=10uF, L=2.2uH, R_S=7.1mΩ, C_{TIM}=330nF, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bias Supply (V_{IN})						
V_{IN}	Supply voltage operation range		4		14	V
V_{UVLO}	Input voltage lockout threshold	V_{IN} rising and measured from IN to ground			4	V
ΔV_{UVLO}	Input voltage lockout hysteresis	Measured from IN to ground		0.2		V
V_{IN_OVP}	Input overvoltage protection	V_{IN} rising and measured from IN to ground	13.5			V
ΔV_{OVP}	Input overvoltage protection hysteresis	Measured from IN to ground		0.5		V
Quiescent Current						
I_{BAT}	Battery discharge current	V_{IN} absent or EN=Low		5	10	uA
I_{IN}	Input quiescent current	Disable Charge		0.8	1.1	mA
Oscillator and PWM						
f_{SW}	Switching frequency			500		kHz
Power MOSFET						
R_{NFET_M}	$R_{DS(ON)}$ of Main N-FET			25		mΩ
R_{NFET_R}	$R_{DS(ON)}$ of Rectified N-FET			45		mΩ
R_{NFET_B}	$R_{DS(ON)}$ of Blocking N-FET			35		mΩ
Voltage Regulation						
V_{BAT}	Battery charge voltage	1-cell battery, Vcv<0.4V	4.179	4.2	4.221	V
		1-cell battery, Vcv>1.5V	4.328	4.35	4.371	
		2-cell battery, Vcv<0.4V	8.358	8.4	8.442	
		2-cell battery, Vcv>1.5V	8.656	8.7	8.744	
ΔV_{RCH}	Recharge threshold refer to V_{BAT}	1-cell battery	50	100	150	mV
		2-cell battery	100	200	300	
V_{TRK}	Trickle charge rising edge threshold	1-cell battery	2.7	2.8	2.9	V
		2-cell battery	5.4	5.6	5.8	
Adaptive input current REF Modify						
V_{NTC}	NTC voltage threshold for adaptive input current reference refresh	NTC falling edge	0.4			V
t_{DET}	NTC low time to enable the adaptive input current refresh	Low pulse width		100		ms
Charge Current						
I_{CC}	Charge current accuracy for Constant Current Mode	I_{CC}=25mV/R_S	-10%		10%	I_{CC}
I_{TC}	Charge current accuracy for Trickle Current Mode	I_{TC}=2.5mV/R_S	-50%		50%	I_{TC}
I_{TERM}	Termination current	I_{TERM}=2.5mV/R_S	-50%		50%	I_{TERM}
Output Voltage OVP						
V_{O_OVP}	Output voltage OVP threshold		105%	110%	115%	V_{CV}
Adaptive Input Power Limit Reference						
V_{SEN}	Reference for adaptive input power limit		1.16	1.19	1.22	V
ΔV_{AICL}	The adaptive input power limit reference is V_{IN}-ΔV_{AICL}	NTC pull low than 100ms and V_{IN} is higher than 6V		600		mV
Timer						
T_{TC}	Trickle current charge timeout		0.36	0.5	0.64	hour
T_{CC}	Constant current charge timeout		3.5	4.5	5.5	hour

T_{MC}	Charge mode change delay time			30		ms
T_{TERM}	Termination delay time			30		ms
T_{RCHG}	Recharge time delay			30		ms
Short Circuit Protection						
V_{SHORT}	Output short protection threshold, falling edge		1.70	2.00	2.30	V
Auto shut down						
ΔV_{ASD}	Auto shutdown voltage threshold	V_{IN} fall, Measured from IN to V_{BAT}	40	90	140	mV
	Auto shutdown voltage threshold hysteresis	Measured from IN to V_{BAT}		65		
Logical Control						
V_{EN}	High level logic for enable control		1.5			V
	Low level logic for enable control				0.4	V
V_{CV}	High level logic for enable control		1.5			V
	Low level logic for enable control				0.4	V
Battery Thermal Protection NTC						
UTP	Under temperature protection		70%	75%	80%	V_{IN}
	Under temperature protection hysteresis	Falling edge		5%		
OTP	Over temperature protection		43%	45%	47%	
	Over temperature protection hysteresis	Rising edge		1.5%		
Thermal fold-back And Thermal shutdown						
T_{Fold}	Thermal fold-back threshold			120		ºC
$T_{FoldHYS}$	Thermal fold-back hysteresis falling edge			20		ºC
I_{Fold}	Thermal fold-back ratio			0.25		I_{CC}
T_{SD}	Thermal shutdown temperature	Rising Threshold		160		ºC
T_{SDHYS}	Thermal shutdown temperature hysteresis			30		ºC

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

General Function Description

SY6935 is a 4V-14V input, 3.5A step-down Multi-cell Li-Ion battery charger, which integrates reverse blocking FET, 500 kHz synchronous buck and full protection functions. The charge current up to 3.5A can be programmed by using the external resistor for different portable applications. It also has a programmable charge timeout and adaptive input power limit for safety battery charge operation. It consists of 16V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

Charging Status Indication Description

STAT is an open drain pin and a pull up resistor is needed for charging status indication. Connect a LED from IN to STAT pin, LED ON means Charge-in-Process, LED OFF means Charge Done, LED Flashing with 1.3Hz means Fault Mode.

1. Charge-In-Process – Pull and keep STAT pin to Low;
2. Charge Done – Pull and keep STAT pin to High;
3. Fault Mode – Output high and low voltage alternatively with 1.3Hz frequency. The faults include input OVP, BAT OVP, BAT short, BAT UTP, BAT OTP, time-out and thermal shutdown.

Switching Mode Buck Charger Basic Operation Description

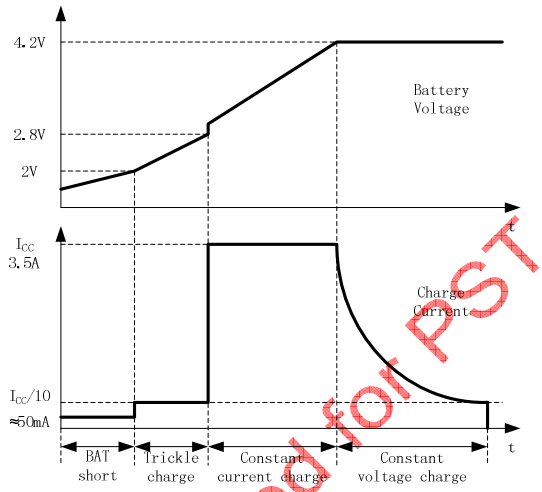
Switching Mode Control Strategy

SY6935 utilizes quasi-fixed frequency control to simplify the internal close-loop compensation design. The quasi-fixed frequency settled at 500 kHz is easy for the size minimization of peripheral circuit design. During the light load operation, the OFF time of the main switch is going to be stretched to achieve frequency fold back.

Operation Principle

SY6935 works as a synchronous Buck mode battery charger when the adapter is present. It utilizes 500 kHz switching frequency to minimize the PCB design.

The charger will operate in battery short mode, trickle charge mode, constant current charge mode and constant voltage charge mode according to the battery voltage. The charge current in every mode is showed in following charge curve. In constant voltage mode, if charge current is lower than termination current, the charger will stop charging until battery voltage drops to recharge voltage.



Basic Adaptive Input Power Limit Principle

SY6935 can limit the input power adaptively and adjust this threshold according the input voltage. It will automatically decrease charge current when IN voltage drops to adaptive input power limit reference Vref.

For typical 5V adapter, Vref is set by VSEN pin, that is calculated as：

$$Vref = 1.19 * \frac{R_{UP} + R_{DN}}{R_{DN}}$$

If IN voltage is higher than 6V, Vref is calculated as:

$$Vref = V_{IN} - \Delta V_{AICL}$$

Where ΔV_{AICL} is 0.6V typically.

V_{IN} is the input voltage when adapter insert. Vref can be modified after a more than 100ms low pulse on NTC pin if the adapter is always present.

When NTC is pulled low, the charge current is set to the trickle value; battery thermal protection and adaptive input power limit function are disabled.

Full Charger Protections Description

In charge mode, SY6935 has full protection to protect the IC and the battery.

Input Over Voltage Protection – SY6935 has IN over voltage protection. It will turn off switching charger when input OVP occurs. IC will auto recover normal operation when fault removes.

BAT Over Voltage Protection – SY6935 will stop charging when BAT OVP occurs. IC will auto recover normal operation when fault removes.

Timeout Protection – The charger can detect a bad battery. It will stop charge and latch off when the charger works over safety time which is set by C_{TIM}. Only recycling the input can release this fault.

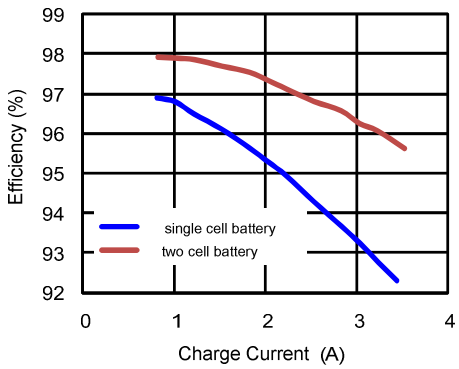
Battery Thermal Protection – When NTC voltage is lower than OTP threshold and higher than 0.4V or higher than UTP threshold, the converter will stop switching. IC will auto recovery when fault removes.

Thermal Shutdown Protection – The IC will stop operation when the junction temperature is higher than 160°C. It will auto recover normal when fault removes.

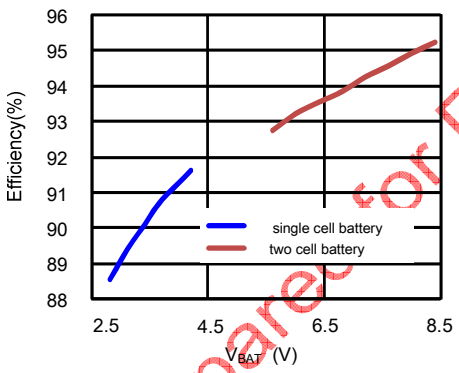
Typical Performance Characteristics

(T_A=25°C, V_{IN}=5V, V_{BAT}=3.6V for single-cell battery application. V_{IN}=9V, V_{BAT}=7.6V for two-cell battery application. R_s=7.1mΩ, C_{TIM}=330nf, unless otherwise specified.)

Efficiency vs. Charge Current (CV mode)

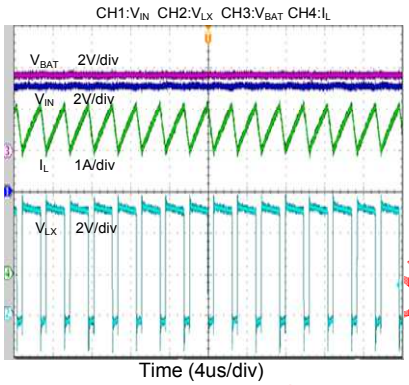


Efficiency vs. Charge Voltage (CC mode)



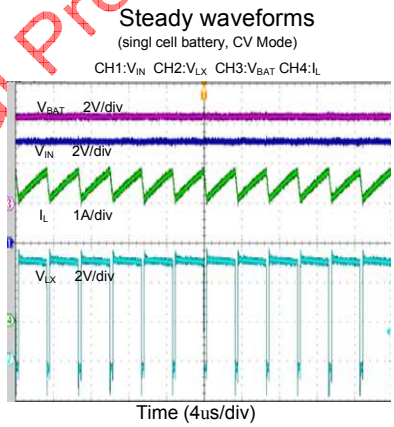
Steady waveforms

(singl cell battery, CC Mode)



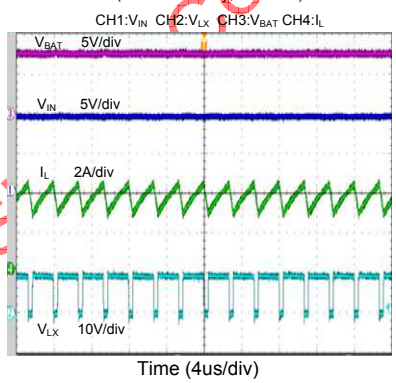
Steady waveforms

(singl cell battery, CV Mode)



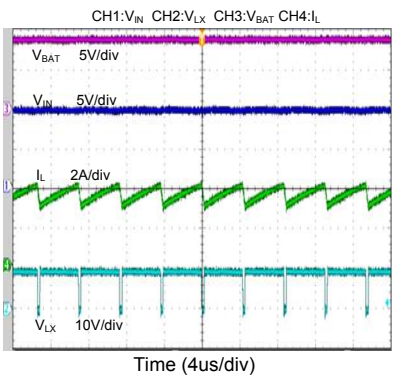
Steady waveforms

(Two cells battery, CC Mode)

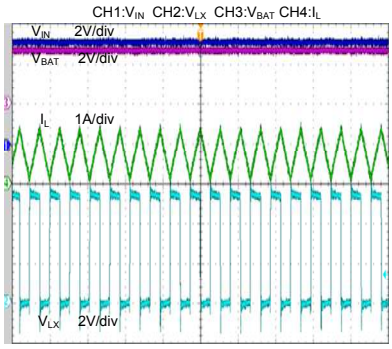


Steady waveforms

(Two cells battery, CV Mode)

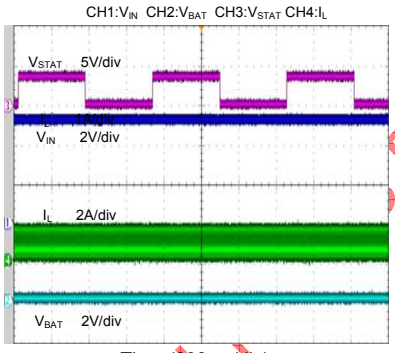


Steady waveforms
(TC Mode)



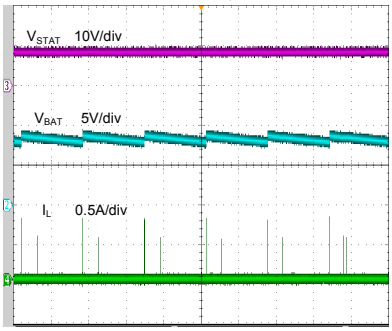
Time (4us/div)

Steady waveforms
(Short Mode)



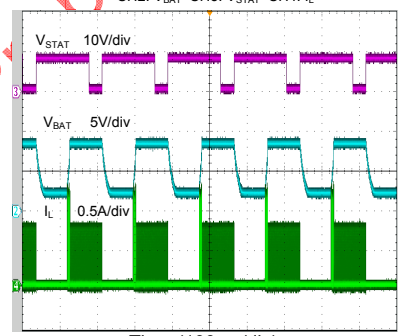
Time (200ms/div)

Steady waveform when no battery
(NTC=50% V_{IN}, No battery)



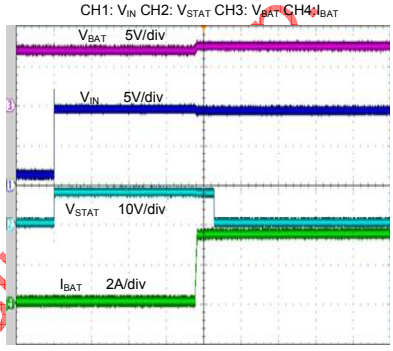
Time (100ms/div)

Steady waveform
(NTC=50% V_{IN},100mA load to BAT,V_{BAT}=3V)



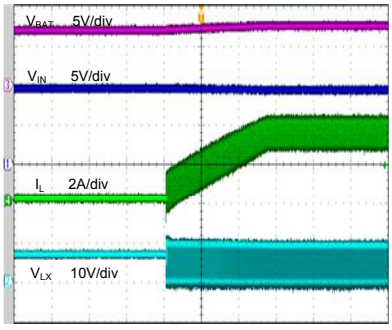
Time (100ms/div)

Power on
(Two Cell Battery)



Time (200ms/div)

Soft Start
(Two Cell Battery)

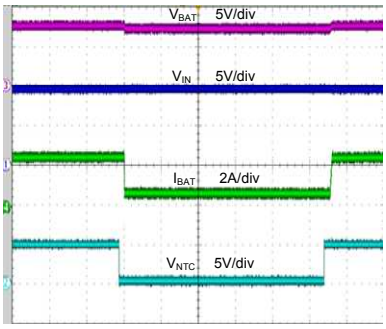


Time (4ms/div)

Low pulse on NTC pin

(V_{IN}=9V V_{BAT}=7.6V)

CH1: V_{IN} CH2: V_{NTC} CH3: V_{BAT} CH4:I_{BAT}

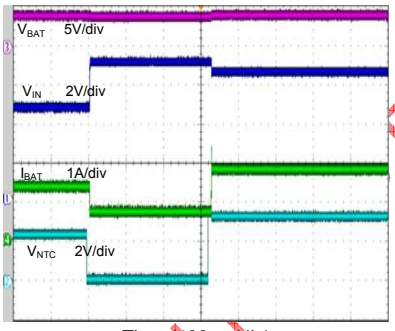


Time (200ms/div)

Adaptive Input Power Limit Reference Refresh

(Input Adapter changes to 7V/1A V_{BAT}=3.6V)

CH1: V_{IN} CH2:V_{NTC} CH3: V_{BAT} CH4:I_{BAT}



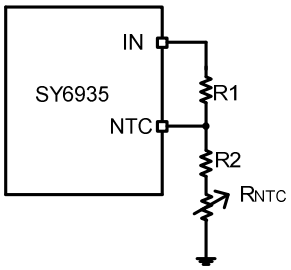
Time (400ms/div)

Applications Information

Because of the high integration of SY6935, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{BD}, output capacitor C_{OUT}, inductor L, NTC resistors R1, R2, charging current sense resistor Rs and timer capacitor C_{TIM} need to be selected for the targeted applications specifications.

NTC resistor:

SY6935 monitors battery temperature by measuring the input voltage and NTC voltage. The controller triggers the UTP or OTP when the ratio K (K= V_{NTC}/V_{IN}) reaches the threshold of UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is showed as below.
Choose R1 and R2 to program the proper UTP and OTP points.



The calculation steps are:

1. Define K_{UT}, K_{UT} =70~80%
2. Define K_{OT}, K_{OT} =43~47%
3. Assume the resistance of the battery NTC thermistor is R_{UT} at UTP threshold and R_{OT} at OTP threshold.
4. Calculate R2,

$$R2 = \frac{K_{OT}(1 - K_{UT})R_{UT} - K_{UT}(1 - K_{OT})R_{0T}}{K_{UT} - K_{OT}}$$

5. Calculate R1

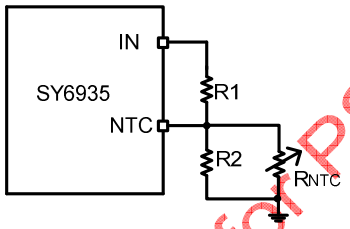
$$R1 = (1 / K_{OT} - 1)(R2 + R_{OT})$$

If choose the typical values K_{UT} =75% and K_{OT}=45%, then

$$R2 = 0.375R_{UT} - 1.375R_{OT}$$

$$R1 = 1.222(R2 + R_{OT})$$

SY6935 accepts flexible NTC divider circuits. For below method, R1 and R2 can be calculated by below equations.



$$R2 = \frac{R_{OT}R_{UT}(K_{UT} - K_{OT})}{K_{OT}K_{UT}(R_{OT} - R_{UT}) + R_{UT}K_{OT} - R_{OT}K_{UT}}$$

$$R1 = \frac{R_2R_{UT}(1 - K_{UT})}{K_{UT}(R_2 + R_{UT})}$$

If choose the typical values K_{UT} =75% and K_{OT}=45%, then

$$R2 = \frac{0.3R_{UT}R_{OT}}{0.1125R_{UT} - 0.4125R_{OT}}$$

$$R1 = \frac{R_2R_{UT}}{3(R_{UT} + R_2)}$$

Charging current sense resistor Rs

The charging current sense resistor Rs is calculated as below:

$$R_S = \frac{25}{I_{CC}}, \quad \text{Unit: m}\Omega$$

Where the I_{CC} is the battery constant charging current, unit is ampere.

Timer capacitor C_{TIM}

The charger also provides a programmable charging timer. The charging time is programmed by the capacitor connected between the TIM pin and GND. The capacitance is given by the formula:

$$C_{TIM} = 2*10^{-11}T_{CC} \quad \text{Unit: F}$$

T_{CC} is the permitted fast charging time, unit is second.

Input capacitor CBD:

The ripple current through input capacitor is greater than

$$I_{CBD\_MIN} = I_{CC}\sqrt{D(1-D)}$$

To minimize the potential noise problem, place a typical X7R or better grade ceramic capacitor really close to the BD and GND pins. Care should be taken to minimize the loop area formed by CBD, and BD/GND pins.

Output capacitor COUT:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7R or better grade ceramic capacitor with 10uF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average charge current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1-V_{OUT}/V_{IN,\,MAX})}{F_{SW}\times I_{OUT,\,MAX}\times 40\%}$$

Where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

SY6935 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{OUT,\,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,\ MAX})}{2\times F_{SW}\times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<20mohm to achieve a good overall efficiency.

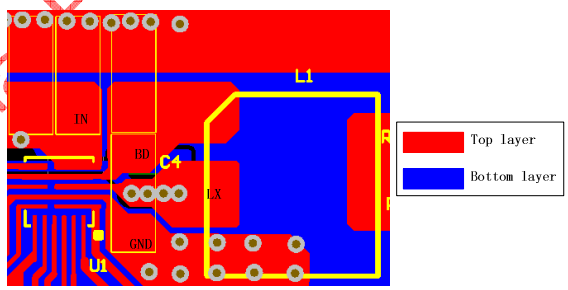
SY6935 is a high integrated charger and the internal compensation circuits also limit the inductor choice. Out of the range from 0.68uH to 3.3uH is not suggested. The 2.2uH inductor can almost cover the normal applications.

Layout Design:

The layout design of SY6935 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{BD}, L.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

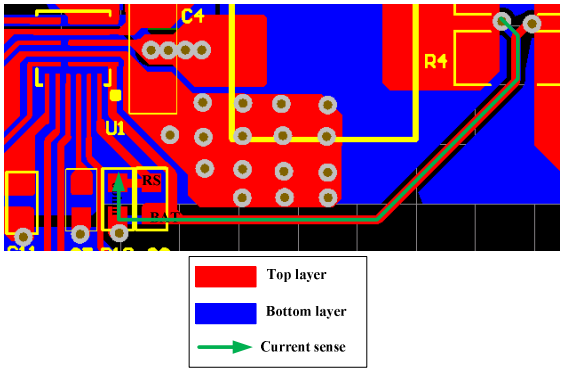
2) C_{BD} must be close to Pins BD and GND. The loop area formed by C_{BD} and GND must be minimized. Following picture is the recommended layout design of C_{BD}.



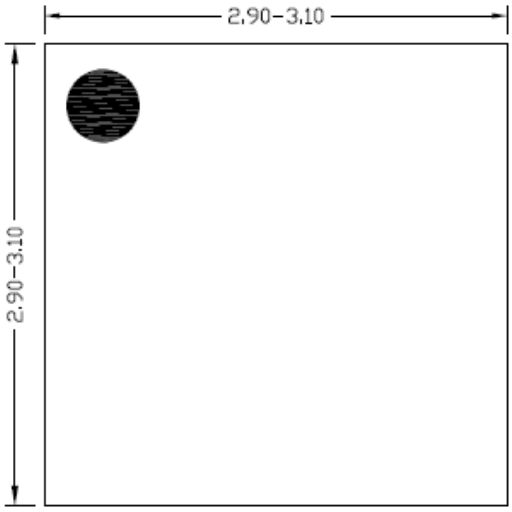
4) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

5) The capacitor CTIM and the trace connecting to the TIM pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

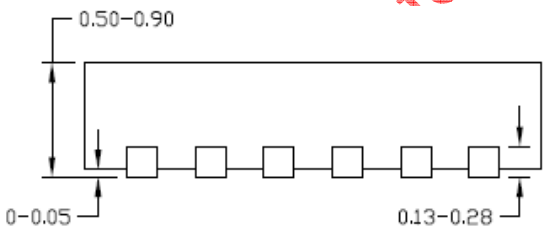
6) The current sense resistor should be adjacent to the junction of the inductor and output capacitor. The routes from the sense leads on the sense resistor to the IC pins should be close to each other to minimize loop area. Please don't route the sense leads through a high current path. Following picture is the recommended layout design.



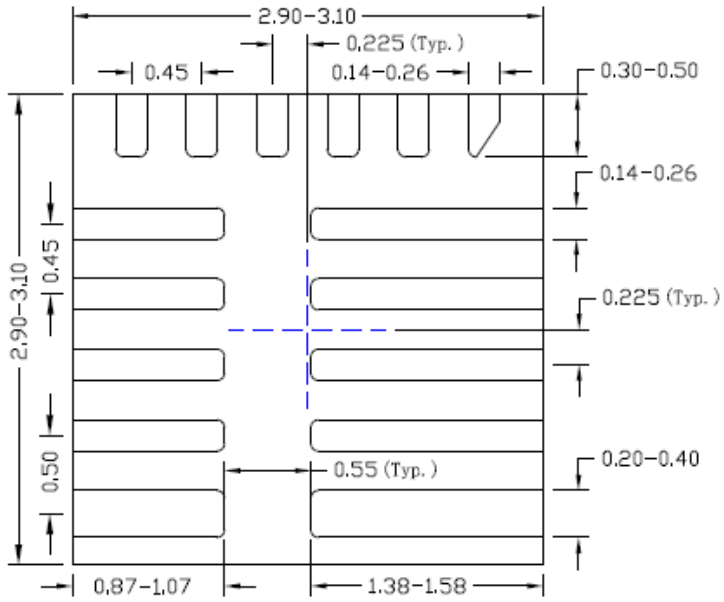
QFN3x3-16 Package Outline Drawing



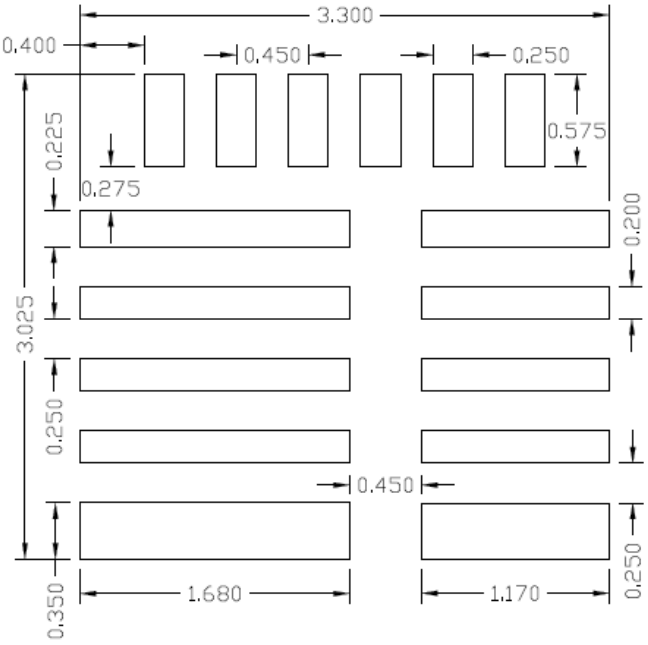
Top View



Side View



Bottom View



Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**