1.5MHZ,1000mA,High Efficiency Synchronous PSM/PWM Step-Down DC/DC Convert with Soft-start

General Description

The LP3220S is a constant frequency, current mode, PWM step-down converter. The device integrates a main switch and a synchronous rectifier for high efficiency. The 2.5V to 6.0V input voltage range makes the LP3220S is ideally suited for portable electronic devices that are powered from 1-cell Li-ion battery or from other power sources within the range such as cellular phones, PDAs and handy-terminals. Internal synchronous rectifier with low RDS(ON) dramatically reduces conduction loss at PWM mode. The internal synchronous switch increases efficiency while eliminate the need for an external Schottky diode. The switching ripple is easily smoothed-out by small package filtering elements due to a fixed operation frequency of 1.5MHz. This along with small SOT-23-5 package provide small PCB area application. Other features include soft start, lower internal reference voltage with 2% accuracy, over temperature protection, and over current protection.

Ordering Information

LP3220S -□ □ □ □ □

- F: Pb-Free
- Package Type
  - B5: SOT23-5
  - J5: TSOT23-5
- Output Voltage Type
  - A: Adjustable type
  - 18: 1.8V

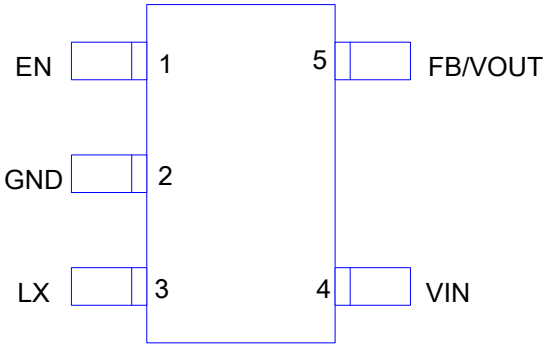
Features

- High Efficiency: 96%
- 1.5MHz Fixed-Frequency PWM Operation
- Adjustable Output From 0.6V to VIN
- 1000mA Output Current, 1.2A Peak Current
- No Schottky Diode Required
- 100% Duty Cycle Low Dropout Operation
- Available in SOT23-5/TSOT23-5 Package
- Short Circuit and Thermal Protection
- Over Voltage Protection
- Low than 1μA Shutdown Current

Applications

- Portable Media Players/MP3 players
- Cellular and Smart mobile phone
- PDA
- DSC
- Wireless Card

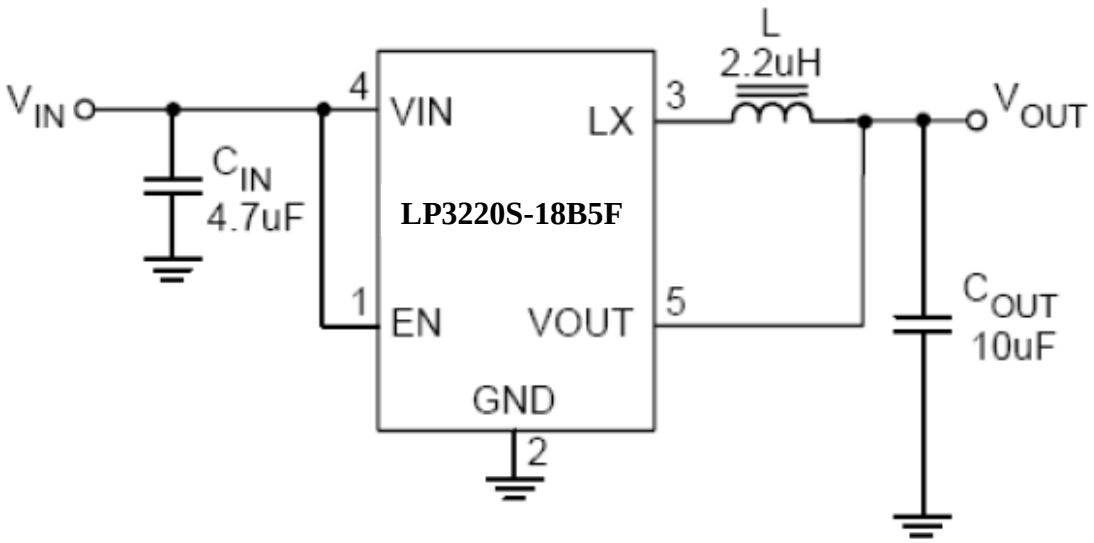
Pin Configurations

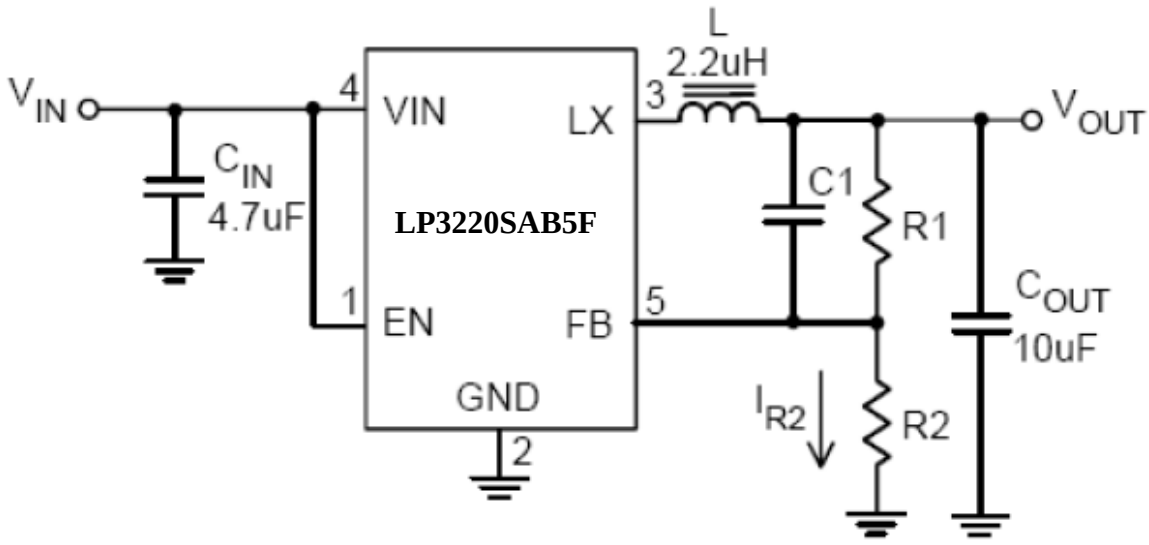


Marking Information

Device	Marking	Package	Shipping
LP3220S		SOT23-5 TSOT23-5	3K/REEL

Typical Application Circuit

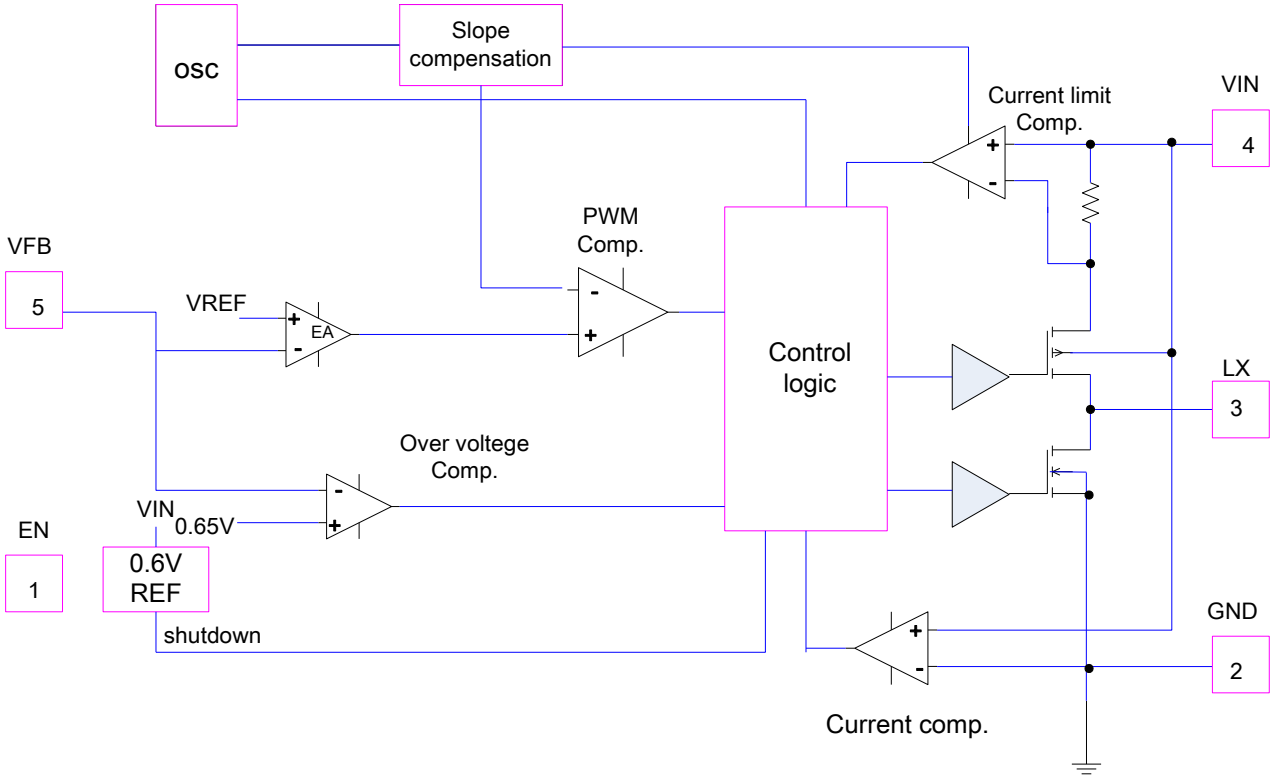




Functional Pin Description

Pin Number	Pin Name	Pin Function
1	EN	Chip Enable (Active High).
2	GND	Ground.
3	LX	Pin For Switching.
4	VIN	Power Input.
5	FB/Vout	Feedback Input Pin, Reference voltage is 0.6 V.

Function Block Diagram



Absolute Maximum Ratings

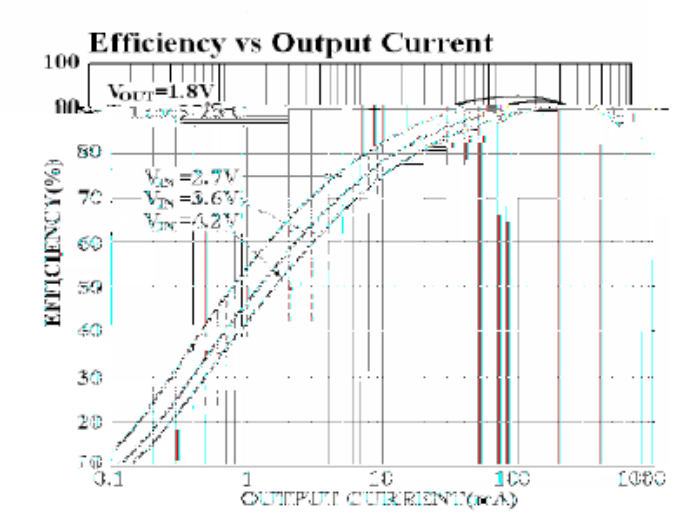
- Input Supply Voltage---------- -0.3V to 6.5V
- EN,VFB Voltage---------- -0.3V to Vin
- P-Channel Switch Source Current(DC) ----------1500mA
- N-Channel Switch Current(DC) ----------1500mA
- Peak SW Sink and Source Current ----------1.5A
- Operation Temperature Range ---------- -40℃ to 85℃
- Junction Temperature ----------125℃
- Storage Temperature----------65℃ to 150℃
- Lead Temp(Soldering,10sec)---------- 260℃
- ESD Rating(HBM)---------- 2KV

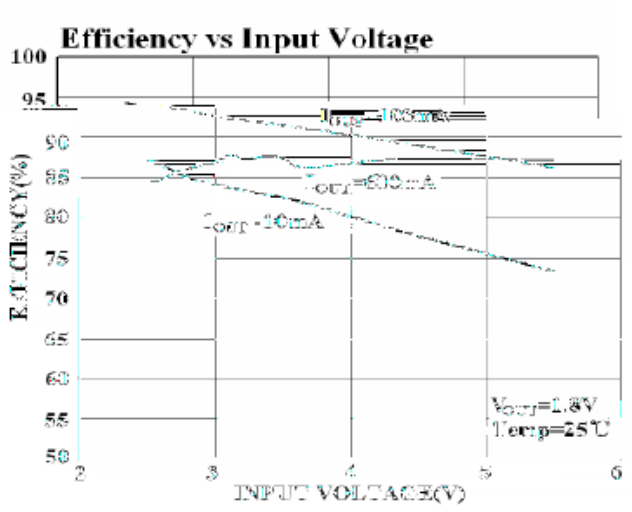
Electrical Characteristics

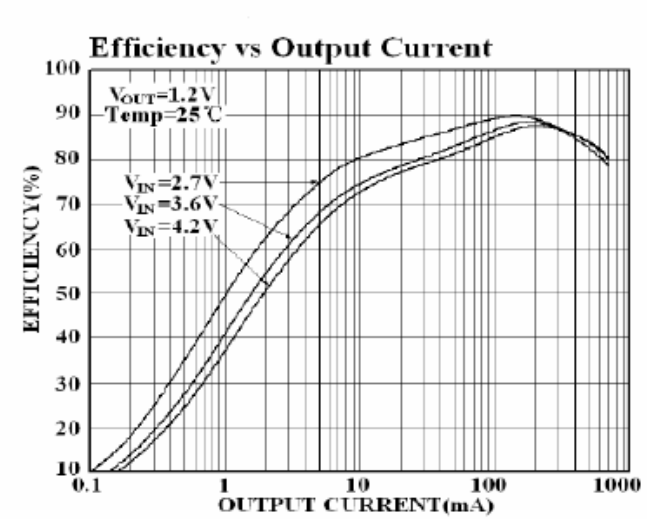
(VIN = 3.6V, VOUT = 2.5V, VREF = 0.6V, L = 2.2µH, CIN= 4.7µF, COUT= 10µF, TA= 25°C, IMAX =1000mA unless otherwise specified)

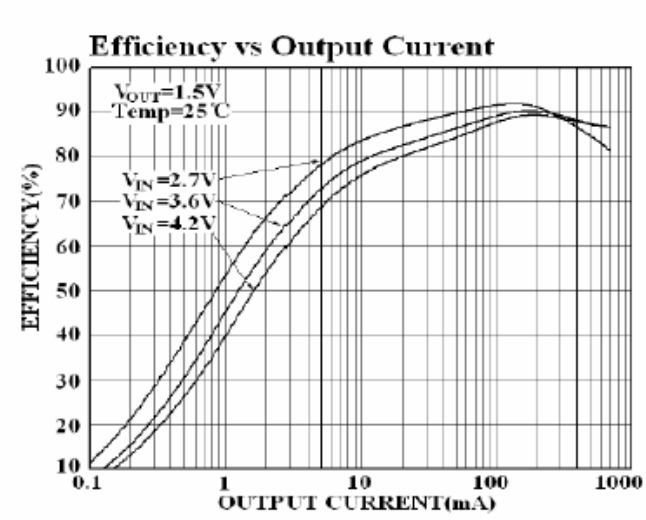
Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage Range		VIN		2.5		6.0	V
Quiescent Current		IQ	IOUT = 0mA, VFB =0.5V IOUT = 0mA, VFB =0.7V		50 25		uA
Shutdown Current		ISHDN	EN = GND		0.1	1	uA
Reference Voltage		VREF	For adjustable output voltage	0.588	0.6	0.612	V
Adjustable Output Range		VOUT		VREF		VIN − 0.2	V
Output Voltage Accuracy	Fixed	Δ VOUT	VIN = 2.2 to 5.5V, VOUT = 1.2V 0A < IOUT < 600mA	−3		+3	%
		Δ VOUT	VIN = 2.2 to 5.5V, VOUT = 1.5V 0A < IOUT < 600mA	−3		+3	%
		Δ VOUT	VIN = 2.2 to 5.5V, VOUT = 1.8V 0A < IOUT < 600mA	−3		+3	%
		Δ VOUT	VIN = 2.8 to 5.5V, VOUT = 2.5V 0A < IOUT < 600mA	−3		+3	%
		Δ VOUT	VIN = 3.5 to 5.5V, VOUT = 3.3V 0A < IOUT < 600mA	−3		+3	%
	Adjustable	Δ VOUT	VIN = VOUT + 0.2V to 5.5V, VIN ≧ 3.5V 0A < IOUT < 600mA	−3		+3	%
		Δ VOUT	VIN = VOUT + 0.4V to 5.5V, VIN ≧ 2.2V 0A < IOUT < 600mA	−3		+3	%
FB Input Current	IFB	VFB = VIN		-30		30	nA
PMOSFET RON	PRDS(ON)	IOUT = 200mA	VIN = 3.6V		0.20	0.38	Ω
NMOSFET RON	NRDS(ON)	IOUT = 200mA	VIN = 3.6V		0.25		Ω
P-Channel Current Limit	IP(LM)	VIN =2.2 to 5.5V			1.5		A
EN Threshold	VEN			0.3	1.0	1.5	V
EN Leakage Current	VENL			--	2		uA

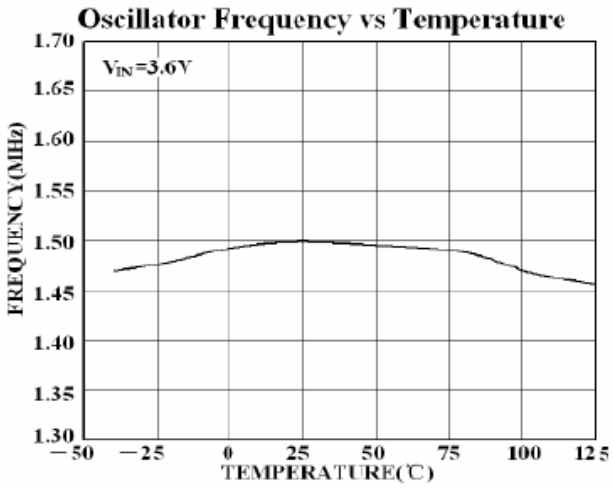
Typical Operating Characteristics

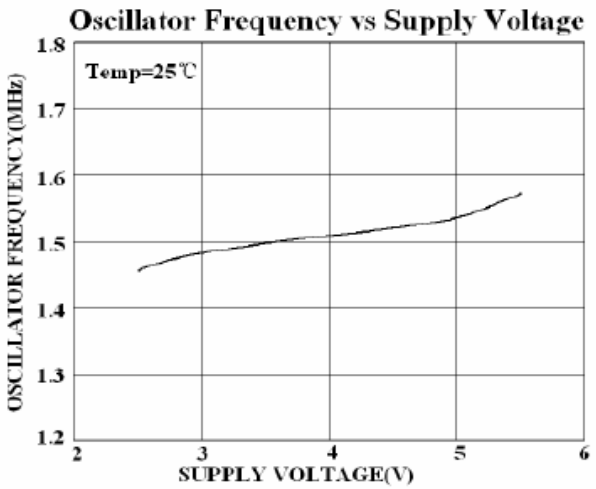


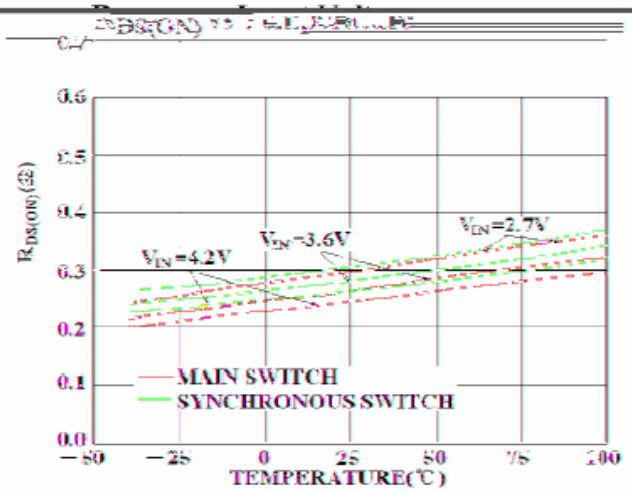


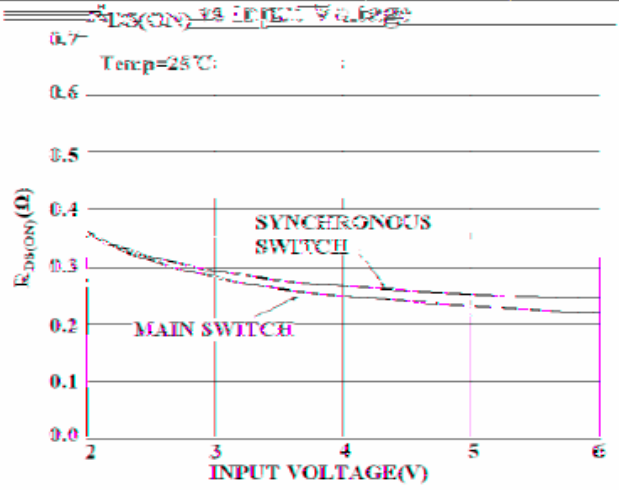


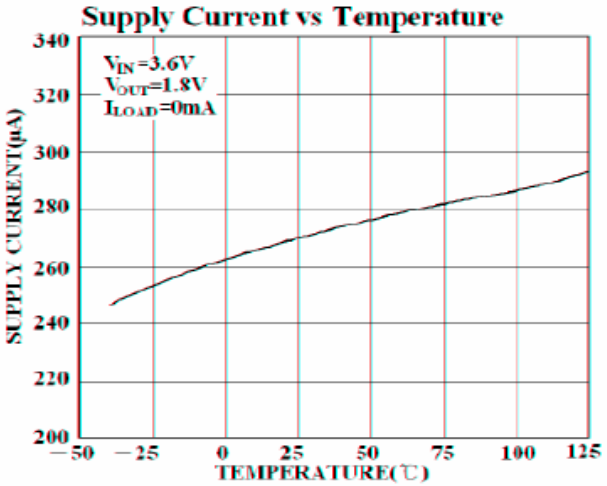


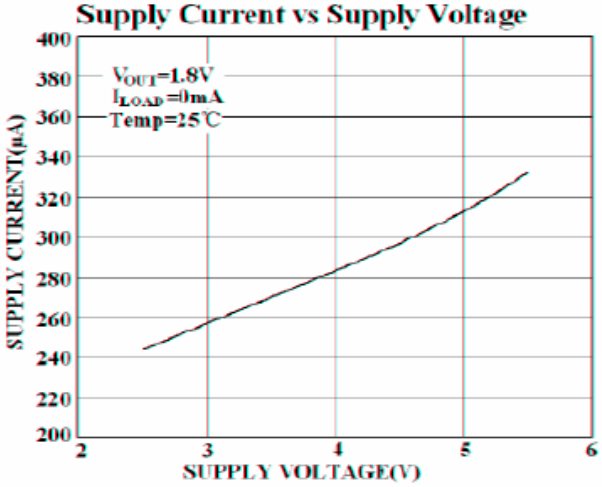

Oscillator Frequency vs Temperature
VIN=3.6V
FREQUENCY(MHz)
1.70
1.65
1.60
1.55
1.50
1.45
1.40
1.35
1.30
−50 −25 0 25 50 75 100 125
TEMPERATURE(℃)


Oscillator Frequency vs Supply Voltage
Temp=25℃
OSCILLATOR FREQUENCY(MHz)
1.8
1.7
1.6
1.5
1.4
1.3
1.2
2 3 4 5 6
SUPPLY VOLTAGE(V)


RDS(ON)(Ω)
VIN=4.2V
VIN=3.6V
VIN=2.7V
MAIN SWITCH
SYNCHRONOUS SWITCH
TEMPERATURE(℃)


Temp=25℃
RDS(ON)(Ω)
SYNCHRONOUS SWITCH
MAIN SWITCH
2 3 4 5 6
INPUT VOLTAGE(V)


Supply Current vs Temperature
VIN=3.6V
VOUT=1.8V
ILOAD=0mA
SUPPLY CURRENT(μA)
340
320
300
280
260
240
220
200
−50 −25 0 25 50 75 100 125
TEMPERATURE(℃)


Supply Current vs Supply Voltage
VOUT=1.8V
ILOAD=0mA
Temp=25℃
SUPPLY CURRENT(μA)
400
380
360
340
320
300
280
260
240
220
200
2 3 4 5 6
SUPPLY VOLTAGE(V)

characteristics and the Internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches .Each time the gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switches from high to low to high again, a packet of charge △Q moves from VIN to ground.
The resulting △Q/△t is the current out of VIN that is typically larger than the DC bias current. In continuous mode.

LGATCHG=f(QT+QB)

Where QT and QB are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to VIN and thus their effects will be more pronounced at higher supply voltages.

2. I2Rlosses tae calculated from the resistances of the internal switches, RSW and external inductor RL. in continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the LX pin is a function of both top and bottom MOSFER RDS(ON) and the duty cycle (DC) as follows:

RSW=RDS(ON)TOP×DC+RDS(ON)BOT×(1-DC)

The RDS(ON) for both the top and bottom MOSFETS can be obtained from the typical performance characteristics curves. Thus, to obtain I2R losses, simply add RSW to RL and multiply the square of the average output current.
Other losses including CIN and COUT ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

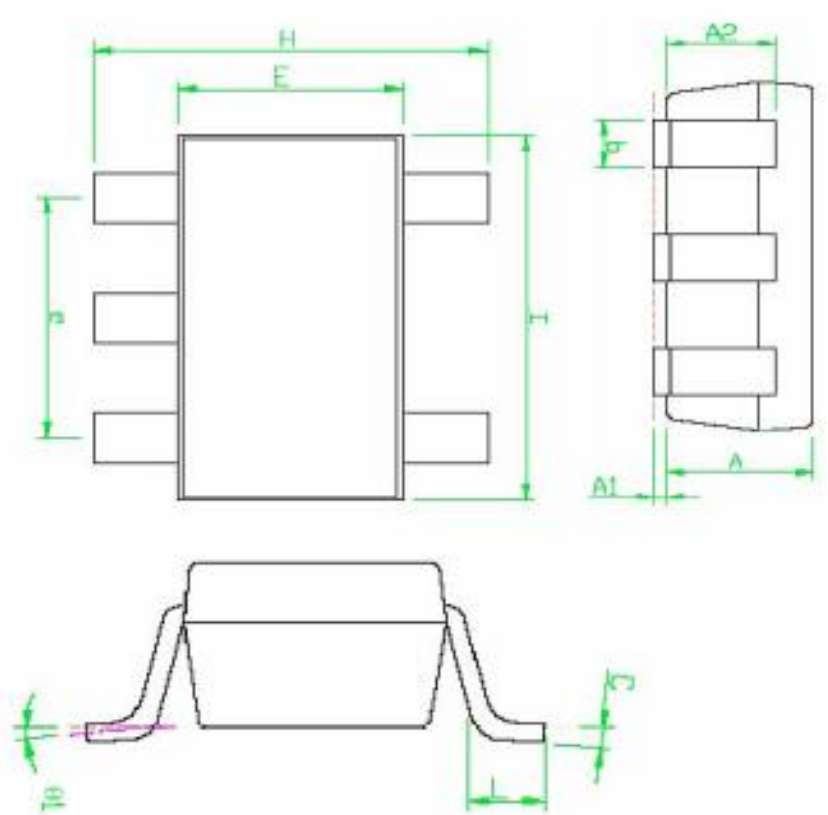
Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, VOUT immediately shifts by an amount equal to ΔILOAD (ESR), where ESR is the effective series resistance of COUT. ΔILOAD also begins to charge or discharge COUT generating a feedback error signal used by the regulator to return VOUT to its steady-state value. During this recovery time, VOUT can be monitored for overshoot or ringing that would indicate a stability problem.

Layout Considerations

- ✧ Follow the PCB layout guidelines for optimal performance of LP3220S.
- ✧ For the main current paths as indicated in bold lines, keep their traces short and wide.
- ✧ Put the input capacitor as close as possible to the device pins (VIN and GND).
- ✧ LX node is with high frequency voltage swing and should be kept small area. Keep analog components away from LX node to prevent stray capacitive noise pick-up.
- ✧ Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the LP3220S.
- ✧ Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

Packaging Information



Note:

1. Package body sizes exclude mold flash protrusions or gate burrs.
2. Tolerance ± 0.1000mm (4 mil) unless otherwise specified.
3. Coplanarity: 0.1000mm
4. Dimension L is measured in gage plane.

Symbols	Dimension in Millimeters		
	Min.	Nom	Max.
A	1.00	1.10	1.30
A1	0.00	-----	0.10
A2	0.70	0.80	0.90
b	0.35	0.40	0.50
C	0.12	0.15	0.20
D	2.70	2.90	3.10
E	1.50	1.60	1.70
e	-----	1.90(Typ.)	-----
H	2.6	2.8	3.00
L	0.37	-----	-----
θ•	14	5	9