



# 15V/4A P-Channel Enhancement Mode Field Effect Transistor

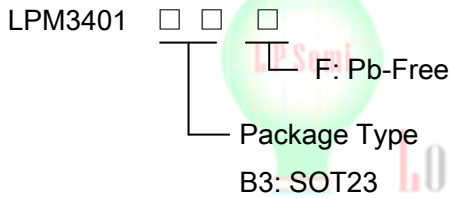
## General Description

The LPM3401 is the P-channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

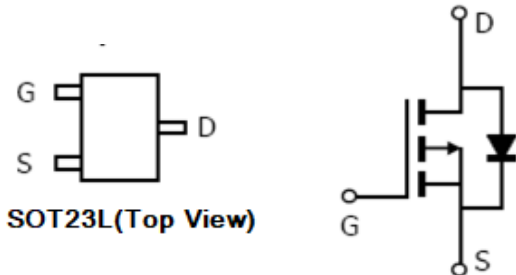
This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

## Order Information



## Pin Configurations



## Features

- ◆ -15V/-4.0A, RDS(ON) < 58mΩ (typ.) @ VGS = -10V
- ◆ -15V/-3.0A, RDS(ON) < 68mΩ (typ.) @ VGS = -4.5V
- ◆ Super high density cell design for extremely low RDS(ON)
- ◆ SOT23 Package

## Applications

- ✧ Portable Media Players/MP3 players
- ✧ Cellular and Smart mobile phone
- ✧ LCD
- ✧ DSC Sensor
- ✧ Wireless Card

## Marking Information

Device	Marking	Package	Shipping
LPM3401		SOT23	3K/REEL
Y: Year code. W: Batch numbers			

## Pin Description

Pin Number	Pin Description
1	Gate Pin
2	Source Pin
3	Drain Pin



## Absolute Maximum Ratings

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-15	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current	$I_D$	-4	A
Pulsed Drain Current B		-15	
Power Dissipation A	$P_D$	1.4	W
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 to 150 °C

## Thermal resistance ratings

Parameter	Symbol	Typ.	Max.	Units
Maximum Junction-to-Ambient	$R_{\theta JA}$	100	125	°C/W





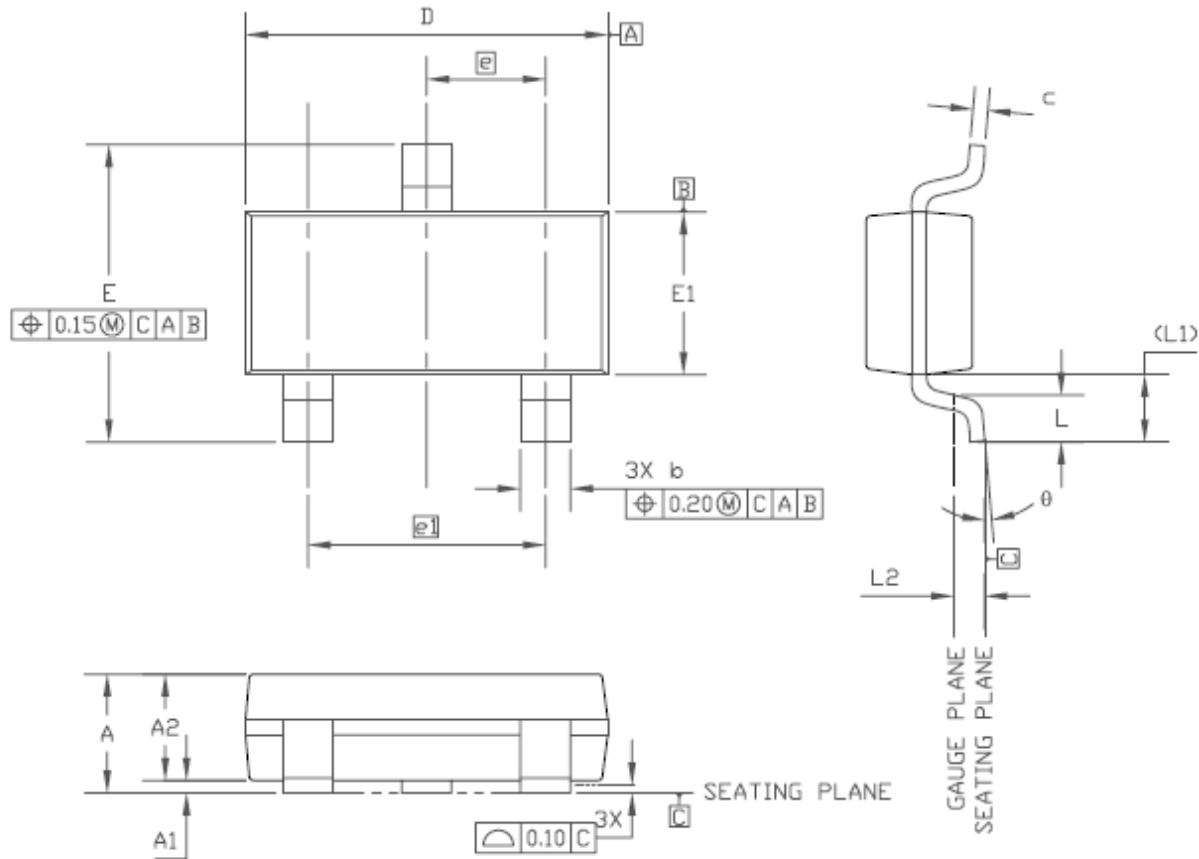
## Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ.	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-15			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-12V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -10	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±12V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =-250μA	-0.6		-1.2	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-4A		55	58	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-3A		64	68	
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-2A		85	95	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-4A		10		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.7	-1	V
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, f=1MHz		680		pF
C <sub>oss</sub>	Output Capacitance			320		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			65		pF
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-4A		7		nC
Q <sub>gs</sub>	Gate Source Charge			13		nC
Q <sub>gd</sub>	Gate Drain Charge			1.8		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, R <sub>L</sub> =3.6Ω, R <sub>GEN</sub> =6Ω		12	18	nS
t <sub>r</sub>	Turn-On Rise Time			3	7	
t <sub>D(off)</sub>	Turn-Off DelayTime			34	42	
t <sub>f</sub>	Turn-Off Fall Time			3	7	

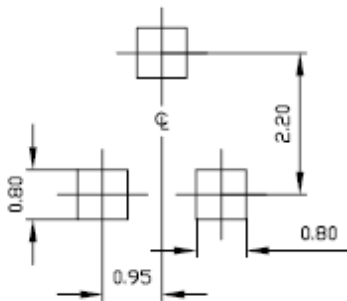


## Packaging Information

### SOT-23 STANDARD PACKAGE OUTLINE



#### RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	1.17	0.030	—	0.046
A1	0.05	—	0.15	0.002	—	0.006
A2	0.70	0.85	1.02	0.028	0.033	0.040
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10	—	2.64	0.083	—	0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.54 REF			0.021 REF		
L2	0.25			0.010		
$\theta$	0°	—	8°	0°	—	8°