# SiT1552

## Smallest (1.2 mm²), Ultra-Low Power, 32.768 kHz MEMS TCXO

**SiTime®**

## Features

- 32.768 kHz ±5, ±10, ±20 ppm frequency stability options over temp
- World's smallest TCXO in a 1.5 x 0.8 mm CSP
- Operating temperature ranges:
  - 0°C to +70°C
  - -40°C to +85°C
- Ultra-low power: <1 µA
- Vdd supply range: 1.5V to 3.63V
- Improved stability reduces system power with fewer network timekeeping updates
- Internal filtering eliminates external Vdd bypass cap and saves space
- Pb-free, RoHS and REACH compliant

## Applications

- Smart Meters (AMR)
- Health and Wellness Monitors
- Pulse-per-Second (pps) Timekeeping
- RTC Reference Clock

**TempFlat MEMS™**

INSTANT SAMPLES   SEARCH INVENTORY   GREEN SOLUTIONS   LIFETIME WARRANTY

## Electrical Specifications

### Table 1. Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Frequency and Stability** | | | | | | |
| Output Frequency | Fout | | 32.768 | | kHz | |
| Frequency Stability Over Temperature[1] (without Initial Offset[2]) | F_stab | -5.0 | | 5.0 | ppm | Stability part number code = E |
| | | -10 | | 10 | | Stability part number code = F |
| | | -20 | | 20 | | Stability part number code = 1 |
| Frequency Stability Over Temperature (with Initial Offset[2]) | F_stab | -10 | | 10 | ppm | Stability part number code = E |
| | | -13 | | 13 | | Stability part number code = F |
| | | -22 | | 22 | | Stability part number code = 1 |
| Frequency Stability vs Voltage | F_vdd | -0.75 | | 0.75 | ppm | 1.8V ±10% |
| | | -1.5 | | 1.5 | ppm | 1.5V – 3.63V |
| First Year Frequency Aging | F_aging | -1.0 | | 1.0 | ppm | $T_A$ = 25°C, Vdd = 3.3V |
| **Jitter Performance ($T_A$ = over temp)** | | | | | | |
| Long Term Jitter | | | | 2.5 | µs$_{pp}$ | 81920 cycles (2.5 sec), 100 samples |
| Period Jitter | | | 35 | | ns$_{RMS}$ | Cycles = 10,000, $T_A$ = 25°C, Vdd = 1.5V – 3.63V |
| **Supply Voltage and Current Consumption** | | | | | | |
| Operating Supply Voltage | Vdd | 1.5 | | 3.63 | V | $T_A$ = -40°C to +85°C |
| Core Supply Current[3] | Idd | | 0.99 | | µA | $T_A$ = 25°C, Vdd = 1.8V, LVCMOS Output configuration, No Load |
| | | | | 1.52 | | $T_A$ = -40°C to +85°C, Vdd = 1.5V – 3.63V, No Load |
| Power-Supply Ramp | t_Vdd_Ramp | | | 100 | ms | Vdd Ramp-Up 0 to 90% Vdd, $T_A$ = -40°C to +85°C |
| Start-up Time at Power-up | t_start | | 180 | 300 | ms | $T_A$ = -40°C +60°C, valid output |
| | | | | 350 | | $T_A$ = +60°C to +70°C, valid output |
| | | | | 380 | | $T_A$ = +70°C to +85°C, valid output |

**Notes:**

1. No board level underfill. Measured as peak-to-peak/2. Inclusive of 3x-reflow and ±20% load variation. Tested with Agilent 53132A frequency counter. Due to the low operating frequency, the gate time must be ≥100 ms to ensure an accurate frequency measurement.
2. Initial offset is defined as the frequency deviation from the ideal 32.768 kHz at room temperature, post reflow.
3. Core operating current does not include output driver operating current or load current. To derive total operating current (no load), add core operating current + output driver operating current, which is a function of the output voltage swing. See the description titled Calculating Load Current.

## Table 1. Electrical Characteristics (continued)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Operating Temperature Range** | | | | | | |
| Commercial Temperature | Op_Temp | 0 | | 70 | °C | |
| Industrial Temperature | | -40 | | 85 | °C | |
| **LVCMOS Output** | | | | | | |
| Output Rise/Fall Time | tr, tf | | 100 | 200 | ns | 10-90% (Vdd), 15 pF Load |
| | | | | 50 | | 10-90% (Vdd), 5 pF Load, Vdd ≥ 1.62V |
| Output Clock Duty Cycle | DC | 48 | | 52 | % | |
| Output Voltage High | VOH | 90% | | | V | Vdd: 1.5V – 3.63V. $I_{OH}$ = -1 µA, 15 pF Load |
| Output Voltage Low | VOL | | | 10% | V | Vdd: 1.5V – 3.63V. $I_{OL}$ = 1 µA, 15 pF Load |
| **NanoDrive™ Programmable, Reduced Swing Output** | | | | | | |
| Output Rise/Fall Time | tf, tf | | | 200 | ns | 30-70% ($V_{OL}/V_{OH}$), 10 pF Load |
| Output Clock Duty Cycle | DC | 48 | | 52 | % | |
| AC-coupled Programmable Output Swing | V_sw | | 0.20 to 0.80 | | V | SiT1552 does not internally AC-couple. This output description is intended for a receiver that is AC-coupled. See Table 4 for acceptable NanoDrive swing options. Vdd: 1.5V – 3.63V, 10 pF Load, $I_{OH}$ / $I_{OL}$ = ±0.2 µA. |
| DC-Biased Programmable Output Voltage High Range | VOH | | 0.60 to 1.225 | | V | Vdd: 1.5V – 3.63V. $I_{OH}$ = -0.2 µA, 10 pF Load. See Table 4 for acceptable $V_{OH}/V_{OL}$ setting levels. |
| DC-Biased Programmable Output Voltage Low Range | VOL | | 0.35 to 0.80 | | V | Vdd: 1.5V – 3.63V. $I_{OL}$ = 0.2 µA, 10 pF Load. See Table 4 for acceptable $V_{OH}/V_{OL}$ setting levels. |
| Programmable Output Voltage Swing Tolerance | | -0.055 | | 0.055 | V | $T_A$ = -40°C to +85°C, Vdd = 1.5V to 3.63V. |

## Table 2. Pin Configuration

| CSP Pin | Symbol | I/O | Functionality |
|---|---|---|---|
| 1, 4 | GND | Power Supply Ground | Connect to ground. All GND pins must be connected to power supply ground. The GND pins can be connected together, as long as both GND pins are connected ground. |
| 2 | CLK Out | OUT | Oscillator clock output. When interfacing to an MCU's XTAL, the CLK Out is typically connected to the receiving IC's X IN pin. The SIT1552 oscillator output includes an internal driver. As a result, the output swing and operation is not dependent on capacitive loading. This makes the output much more flexible, layout independent, and robust under changing environmental and manufacturing conditions. |
| 3 | Vdd | Power Supply | Connect to power supply 1.5V ≤ Vdd ≤ 3.63V. Under normal operating conditions, Vdd does not require external bypass/decoupling capacitor(s). For more information about the internal power-supply filtering, see Power-Supply Noise Immunity section in the detailed description. Contact SiTime for applications that require a wider operating supply voltage range. |

### CSP Package (Top View)

```
      GND  ( 1 )  ( 4 )  GND


  CLK Out  ( 2 )  ( 3 )  Vdd
```
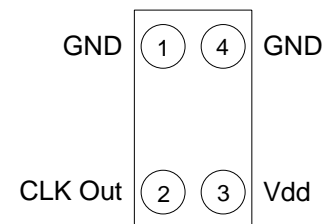
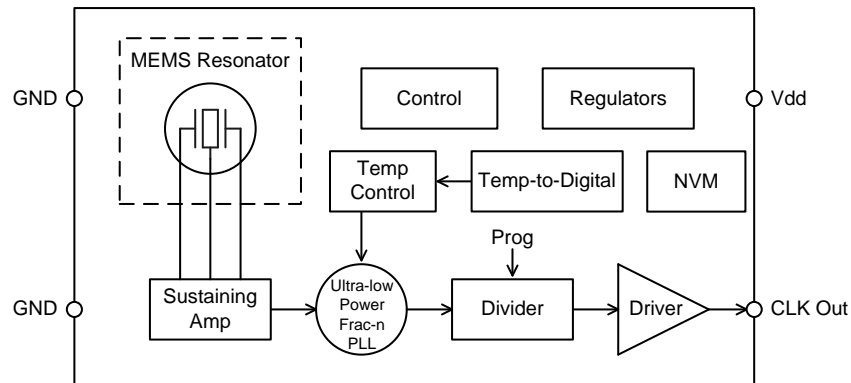**Figure 1. Pin Assignments**

## System Block Diagram



**Figure 2. SiT1552 Block Diagram**

### Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Test Condition | Value | Unit |
|---|---|---|---|
| **Continuous Power Supply Voltage Range (Vdd)** | | -0.5 to 3.63 | V |
| **Short Duration Maximum Power Supply Voltage (Vdd)** | ≤30 minutes | 4.0 | V |
| **Continuous Maximum Operating Temperature Range** | Vdd = 1.5V - 3.63V | 105 | °C |
| **Short Duration Maximum Operating Temperature Range** | Vdd = 1.5V - 3.63V, ≤30 mins | 125 | °C |
| **Human Body Model (HBM) ESD Protection** | JESD22-A114 | 3000 | V |
| **Charge-Device Model (CDM) ESD Protection** | JESD22- C101 | 750 | V |
| **Machine Model (MM) ESD Protection** | JESD22- A115 | 300 | V |
| **Latch-up Tolerance** | JESD78 Compliant | | |
| **Mechanical Shock Resistance** | Mil 883, Method 2002 | 10,000 | *g* |
| **Mechanical Vibration Resistance** | Mil 883, Method 2007 | 70 | *g* |
| **1508 CSP Junction Temperature** | | 150 | °C |
| **Storage Temperature** | | -65°C to 150°C | |

## Description

The SiT1552 is an ultra-small and ultra-low power 32.768 kHz TCXO optimized for battery-powered applications. SiTime's silicon MEMS technology enables the first 32 kHz TCXO in the world's smallest footprint and chip-scale packaging (CSP). Typical core supply current is only 1 µA.

SiTime's MEMS oscillators consist of MEMS resonators and a programmable analog circuit. Our MEMS resonators are built with SiTime's unique MEMS First™ process. A key manufacturing step is EpiSeal™ during which the MEMS resonator is annealed with temperatures over 1000°C. EpiSeal creates an extremely strong, clean, vacuum chamber that encapsulates the MEMS resonator and ensures the best performance and reliability. During EpiSeal, a poly silicon cap is grown on top of the resonator cavity, which eliminates the need for additional cap wafers or other exotic packaging. As a result, SiTime's MEMS resonator die can be used like any other semiconductor die. One unique result of SiTime's MEMS First and EpiSeal manufacturing processes is the capability to integrate SiTime's MEMS die with a SOC, ASIC, microprocessor or analog die within a package to eliminate external timing components and provide a highly integrated, smaller, cheaper solution to the customer.

## TCXO Frequency Stability

The SiT1552 is factory calibrated (trimmed) over multiple temperature points to guarantee extremely tight stability over temperature. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point with a 0.04 ppm/C2 temperature coefficient, the SiT1552 temperature coefficient is calibrated and corrected over temperature with an active temperature correction circuit. The result is 32 kHz TCXO with extremely tight frequency variation over the -40°C to +85°C temperature range. Contact SiTime for applications that require a wider supply voltage range >3.63V, or lower operating frequency below 32 kHz.

When measuring the SiT1552 output frequency with a frequency counter, it is important to make sure the counter's gate time is >100 ms. The slow frequency of a 32kHz clock will give false readings with faster gate times.

## Power Supply Noise Immunity

In addition to eliminating external output load capacitors common with standard XTALs, this device includes special power supply filtering and thus, eliminates the need for an external Vdd bypass-decoupling capacitor to keep the footprint as small as possible. Internal power supply filtering is designed to reject more than ±150 mV noise and frequency components from low frequency to more than 10 MHz.

## Start-up and Steady-State Supply Current

The SiT1552 TCXO starts-up to a valid output frequency within 300 ms (180 mstyp). To ensure the device starts-up within the specified limit, make sure the power-supply ramps-up in approximately 10 – 20 ms (to within 90% of Vdd).

During initial power-up, the SiT1552 power-cycles internal blocks, as shown in the power-supply start-up and steady state plot in the Typical Operating Curves section. Power-up and initialization is typically 200 ms, and during that time, the peak supply current reaches 28 µA as the internal capacitors are charged, then sequentially drops to its 990 nA steady-state current. During steady-state operation, the internal temperature compensation circuit turns on every 350 ms for a duration of approximately 10 ms.

## Output Voltage

The SiT1552 has two output voltage options. One option is a standard LVCMOS output swing. The second option is the NanoDrive reduced swing output. Output swing is customer specific and programmed between 200 mV and 800 mV. For DC-coupled applications, output $V_{OH}$ and $V_{OL}$ are individually factory programmed to the customers' requirement. $V_{OH}$ programming range is between 600 mV and 1.225V in 100 mV increments. Similarly, $V_{OL}$ programming range is between 350 mV and 800 mV. For example; a PMIC or MCU is internally 1.8V logic compatible, and requires a 1.2V $V_{IH}$ and a 0.6V $V_{IL}$. Simply select SiT1552 NanoDrive factory programming code to be "D14" and the correct output thresholds will match the downstream PMIC or MCU input requirements. Interface logic will vary by manufacturer and we recommend that you review the input voltage requirements for the input interface.

For DC-biased NanoDrive output configuration, the minimum $V_{OL}$ is limited to 350mV and the maximum allowable swing ($V_{OH}$ - $V_{OL}$) is 750 mV. For example, 1.1V $V_{OH}$ and 400 mV $V_{OL}$ is acceptable, but 1.2V $V_{OH}$ and 400 mV $V_{OL}$ is not acceptable.

When the output is interfacing to an XTAL input that is internally AC-coupled, the SiT1552 output can be factory programmed to match the input swing requirements. For example, if a PMIC or MCU input is internally AC-coupled and requires an 800 mV swing, then simply choose the SiT1552 NanoDrive programming code "AA8" in the part number. It is important to note that the SiT1552 does not include internal AC-coupling capacitors. Please see the Part Number Ordering section at the end of the datasheet for more information about the part number ordering scheme.

## SiT1552 NanoDrive™

Figure 3 shows a typical output waveform of the SiT1552 (into a 10 pF load) when factory programmed for a 0.70V swing and DC bias ($V_{OH}/V_{OL}$) for 1.8V logic:

**Example:**

- NanoDrive™ part number coding: **D14**.
  Example part number: SiT1552AI-JE-**D14**-32.768
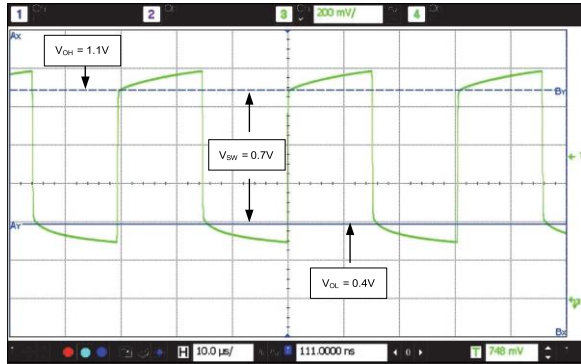
- $V_{OH}$ = 1.1V, $V_{OL}$ = 0.4V ($V_{\_sw}$ = 0.70V)



**Figure 3. SiT1552AI-JE-<u>D14</u>-32.768
Output Waveform** (10 pF load)

Table 4 shows the supported NanoDrive™ $V_{OH}$, $V_{OL}$ factory programming options.

### Table 4. Acceptable $V_{OH}/V_{OL}$ NanoDrive™ Levels

| NanoDrive | $V_{OH}$ (V) | $V_{OL}$ (V) | Swing (mV) | Comments |
|---|---|---|---|---|
| D26 | 1.2 | 0.6 | 600 ±55 | 1.8V logic compatible |
| D14 | 1.1 | 0.4 | 700 ±55 | 1.8V logic compatible |
| D74 | 0.7 | 0.4 | 300 ±55 | XTAL compatible |
| AA3 | n/a | n/a | 300 ±55 | XTAL compatible |

The values listed in Table 4 are nominal values at 25°C and will exhibit a tolerance of ±55 mV across Vdd and -40°C to 85°C operating temperature range.

## SiT1552 Full Swing LVCMOS Output

The SiT1552 can be factory programmed to generate full-swing LVCMOS levels. Figure 4 shows the typical waveform (Vdd = 1.8V) at room temperature into a 15 pF load.

**Example:**

- LVCMOS output part number coding is always **DCC**

- Example part number: SiT1552AI-JE-**DCC**-32.768
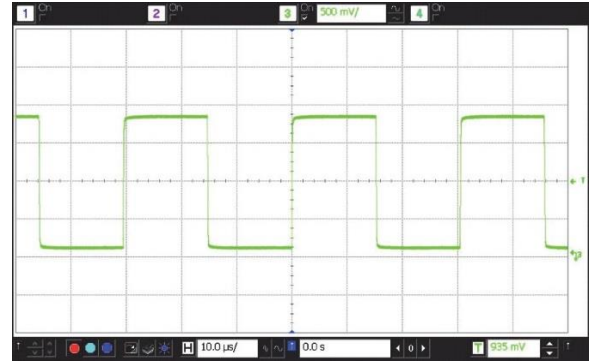


**Figure 4. LVCMOS Waveform**
(Vdd = 1.8V) into 15 pF Load

## Calculating Load Current

### No Load Supply Current

When calculating no-load power for the SiT1552, the core and output driver components need to be added. Since the output voltage swing can be programmed to minimize load current, the output driver current is variable. Therefore, no-load operating supply current is broken into two sections; core and output driver. The equation is as follows:

Total Supply Current (no load) = Idd Core + Idd Output Driver

#### Example 1: Full-swing LVCMOS

- Vdd = 1.8V
- Idd Core = 990nA (typ)
- Voutpp = 1.8V
- Idd Output Driver: (Cdriver)(Vout)(Fout) = (3.5pF)(1.8V)(32768Hz) = 206nA

Supply Current = 990nA + 206nA = 1.2µA

#### Example 2: NanoDrive™ Reduced Swing

- Vdd = 1.8V
- Idd Core = 990nA (typ)
- $Vout_{pp}$ (D14) = $V_{OH} - V_{OL}$ = 1.1V - 0.4V = 700mV
- Idd Output Driver: (Cdriver)(Vout)(Fout) = (3.5pF)(0.7V)(32768Hz) = 80nA

Supply Current = 990nA + 80nA = 1.07µA

### Total Supply Current with Load

To calculate the total supply current, including the load, follow the equation listed below.

Total Current = Idd Core + Idd Output Driver + Load Current

#### Example 1: Full-swing LVCMOS

- Vdd = 1.8V
- Idd Core = 990n
- Load Capacitance = 10pF
- Idd Output Driver: (Cdriver)(Vout)(Fout) = (3.5pF)(1.8V)(32768Hz) = 206nA

Load Current: (10pF)(1.8V)(32768Hz) = 590nA

Total Current = 990nA + 206nA + 590nA = 1.79µA

#### Example 2: NanoDrive™ Reduced Swing

- Vdd = 1.8V
- Idd Core = 990nA
- Load Capacitance = 10pF
- $Vout_{pp}$ (D14): $V_{OH} - V_{OL}$ = 1.1V - 0.4V = 700mV
- Idd Output Driver: (Cdriver)(Vout)(Fout) = (3.5pF)(0.7V)(32768Hz) = 80nA

Load Current: (10pF)(0.7V)(32.768kHz) = 229nA

Total Current = 990nA + 80nA + 229nA = 1.299µA

## Typical Operating Curves

**(T_A = 25°C, Vdd = 1.8V, unless otherwise stated)**



**Figure 5. Frequency Stability Over Temperature (Pre-Reflow)**



**Figure 6. Frequency Stability Over Temperature (Post-Reflow)**
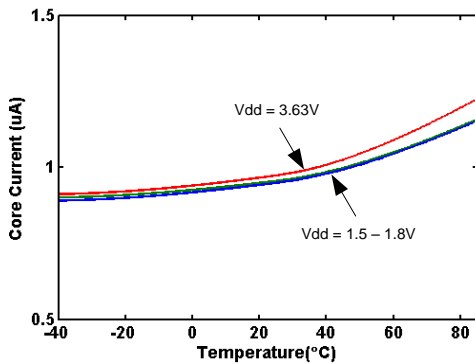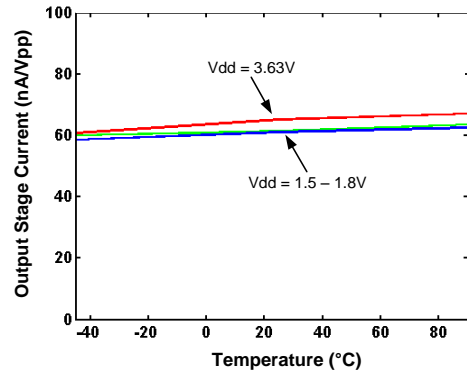


**Figure 7. Core Current Over Temperature**
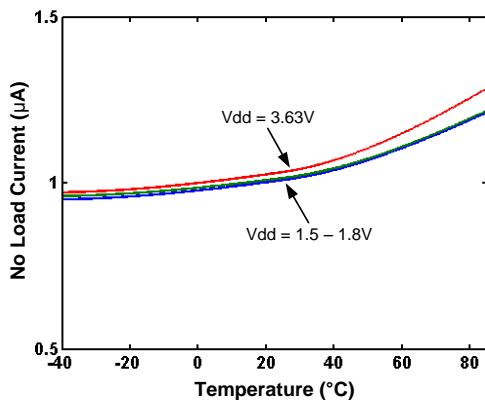


**Figure 8. Output Stage Current Over Temperature**



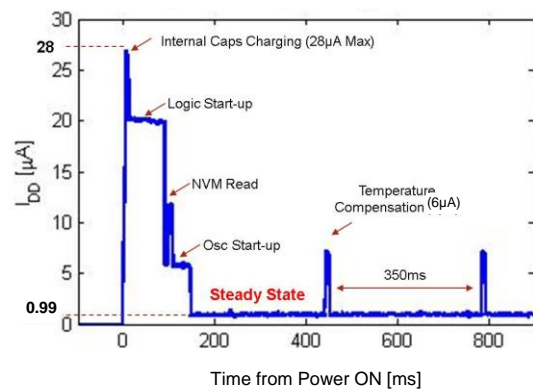**Figure 9. Total Supply Current Over Temperature, LVCMOS (Core + LVCMOS Output Driver, No Load)**



**Figure 10. Start-up and Steady-State Current Profile**

**Figure 11. Power Supply Noise Rejection (±150mV Noise)**
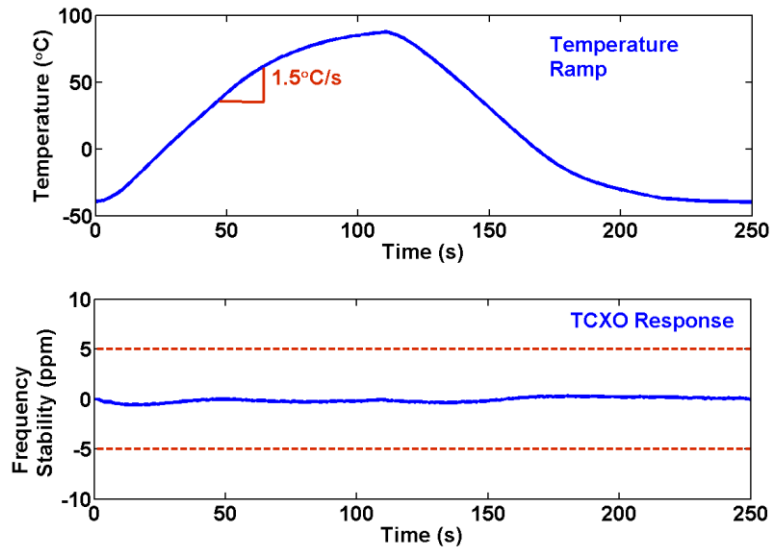


**Figure 12. Temperature Ramp Response**
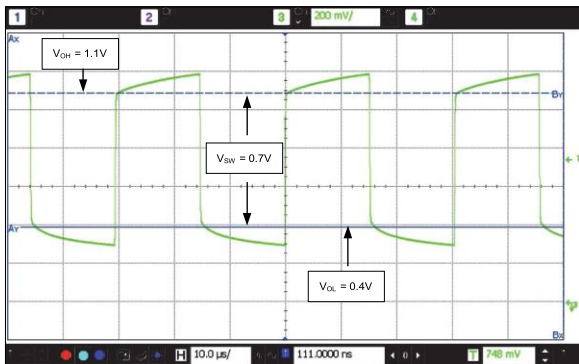


**Figure 13. NanoDrive™ Output Waveform**
(V$_{OH}$ = 1.1V, V$_{OL}$ = 0.4V; SiT1552AI-JE-D14-32.768)
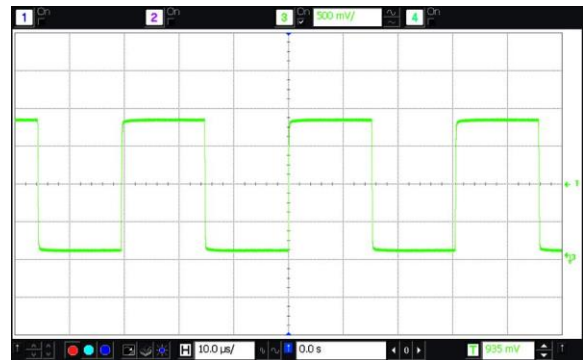


**Figure 14. LVCMOS Output Waveform**
(Vswing = 1.8V, SIT1552AI-JE-DCC-32.768, 10 pF Load)

## Dimensions and Patterns

**Package Size – Dimensions (Unit: mm)**



| Dimension Table (mm) | | | | |
|---|---|---|---|---|
| Item | SYMBOL | MINIMUM | NOMINAL | MAXIMUM |
| Total Thickness | A | 0.48 | 0.54 | 0.60 |
| Stand Off | A1 | 0.22 | | 0.28 |
| MEMS Clearance | A2 | 0.027 | | 0.113 |
| Film Thickness | A3 | 0.036 | 0.040 | 0.044 |
| Wafer Thickness | A4 | 0.225 | 0.250 | 0.275 |
| Ball Diameter | b | 0.30 | 0.315 | 0.33 |
| Ball Pitch X | e | 0.41 BSC | | |
| Ball Pitch Y | e1 | 1.00 BSC | | |
| MEMS X | D1 | 0.46 REF | | |
| MEMS Y | E1 | 0.46 REF | | |
| Body Size X | D | 0.84 BSC | | |
| Body Size Y | E | 1.54 BSC | | |
| Ball To Center X | SD | 0.205 BSC | | |
| Ball To Center Y | SE | 0.500 BSC | | |
| Package Edge Tolerance | aaa | 0.040 | | |
| Coplanarity | ccc | 0.075 | | |

4 LD – 1.5 x 0.8 x 0.55 mm

Package Outline

POD-35 Rev A

**Recommended Land Pattern (Unit: mm)**



Ø0.25 (4x) NSMD pads

Ø0.35 (4x) Soldermask openings

0.41

1.00

(soldermask openings shown with dashed line around NSMD pad)

**Recommended 4-mil (0.1mm) stencil thickness**

## Manufacturing Guidelines

1) No Ultrasonic Cleaning: Do not subject the SiT1552 to an ultrasonic cleaning environment. Permanent damage or long term reliability issues to the MEMS structure may occur.

2) Do not apply underfill to the SiT1552. The device will not meet the frequency stability specification if underfill is applied.

3) Reflow profile, per JESD22-A113D.

4) For additional manufacturing guidelines and marking/tape-reel instructions, refer to: SiTime Manufacturing Notes.

## Ordering Information

Part number characters in blue represent the customer specific options. The other characters in the part number are fixed.

SiT1552AI-JE-DCC-32.768S

**Part Family**
"SiT1552"

**Revision Letter**
"A": is the revision

**Temperature Range**
"C": Commercial, 0 to 70ºC
"I":  Industrial, -40 to 85ºC

**Package Size**
"J": 1.5 mm x 0.8 mm CSP

**Over Temperature Stability Options**
"E": ±5 ppm
"F": ±10 ppm
"1": ±20 ppm

**Packaging**
"S": 8 mm Tape & Reel, 10ku reel
"D": 8 mm Tape & Reel, 3ku reel
"E": 8 mm Tape & Reel, 1ku reel
Blank for Bulk
Samples in cut Tape & Reel strips

**Output Clock Frequency (kHz)**
32.768 kHz

**Output Voltage Setting**
DCC: LVCMOS Output

NanoDrive™ Reduced Swing Output
Refer to Table 5 for output setting options

"A": AC-coupled signal path
"D": DC-coupled signal path

The following examples illustrate how to select the appropriate temp range and output voltage requirements:

**Example 1: SiT1552AI-JE-DCC-32.768**

- Industrial temperature range
- CSP package
- 5 ppm frequency stability over temp
- Output swing requirements:
    a) Output frequency = 32.769 kHz
    b) "D" = DC-coupled receiver
    c) "C" = LVCMOS output swing
    d) "C" = LVCMOS output swing

**Example 2: SiT1552AC-JF-D14-32.768**

- Commercial temperature range
- CSP package
- 10 ppm frequency stability over temp
- Output swing requirements:
    a) Output frequency = 32.769 kHz
    b) "D" = DC-coupled receiver
    c) "1" = VOH = 1.1V
    d) "4" = VOL = 400mV

## Table 5. Acceptable $V_{OH}$/$V_{OL}$ NanoDrive™ Levels[4]

| NanoDrive | $V_{OH}$ (V) | $V_{OL}$ (V) | Swing (mV) | Comments |
|-----------|--------------|--------------|------------|----------|
| D26 | 1.2 | 0.6 | 600 ±55 | 1.8V logic compatible |
| D14 | 1.1 | 0.4 | 700 ±55 | 1.8V logic compatible |
| D74 | 0.7 | 0.4 | 300 ±55 | XTAL compatible |
| AA3 | n/a | n/a | 300 ±55 | XTAL compatible |

**Note:**

4. If these available options do not accommodate your application, contact SiTime for other NanoDrive options.

## Table 6. Revision History

| Version | Release Date | Change Summary |
|---------|--------------|----------------|
| 1.0 | 09/17/2014 | Rev 0.9 Preliminary to Rev 1.0 Production Release<br>Updated start-up time specification<br>Added typical operating plots<br>Removed SOT23 and 2012 SMD package options<br>Added "no underfill" in frequency stability specification condition<br>Added Manufacturing Guidelines section |
| 1.1 | 10/14/2014 | Improved Start-up Time at Power-up spec<br>Added 5 pF LVCMOS rise/fall time spec |
| 1.2 | 11/10/2014 | Updated 5 pF LVCMOS rise/fall time spec |
| 1.3 | 11/12/2015 | Removed NanoDrive from EC Table and Ordering Info |
| 1.31 | 01/18/2018 | Updated SPL, page layout changes |
| 1.32 | 03/15/2018 | Updated POD (Package Outline Drawing)<br>Updated logo and company address, other page layout changes |
| 1.4 | 04/12/2018 | Added the NanoDrive sections |