



APPROVAL SHEET

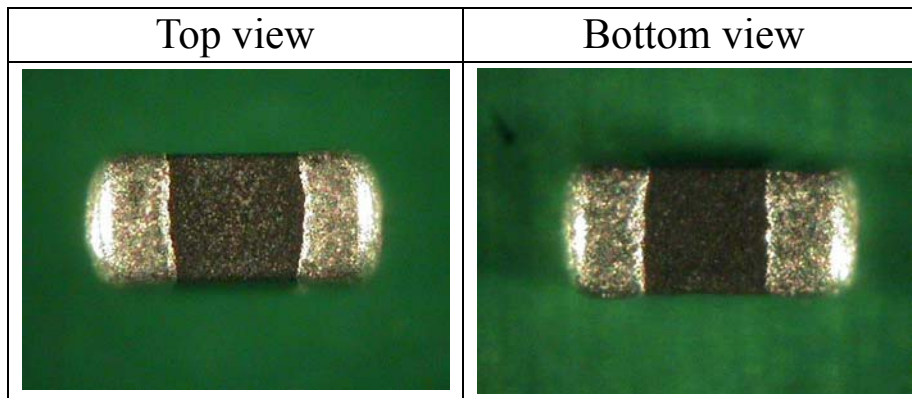
PAGE

MULTILAYER CHIP VARISTOR

1/16

APPROVAL SHEET

Product Name : MULTILAYER CHIP VARISTOR
Part No. : AVLC 3N 01 100
Customer : Apple



Rev. date : 2007. 02. 26.



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APPROVAL SHEET

PAGE

MULTILAYER CHIP VARISTOR

2/16

Contents

1. Revision History	-----	3
2. Parts Descriptions	-----	4
3. Applications	-----	4
4. Model name and Lot Description	-----	6
5. Specification	-----	7
5.1 Electrical specification.	-----	7
5.2 Mechanical specification.	-----	7
5.3 Measurement method	-----	8
6. Reliabilities and Test Conditions	-----	10
7. Soldering Condition	-----	12
7.1 Soldering Profile	-----	12
7.2 Land Pattern Design(Recommended)	-----	12
8. Structure and Materials	-----	13
8.1 Structure and Materials spec.	-----	13
8.2 Equivalent circuit	-----	13
9. Precautions	-----	13
10. Packaging Specifications	-----	14



APPROVAL SHEET

PAGE

MULTILAYER CHIP VARISTOR

3/16

1. Reversion History

Date	Content	Rev. no	Page
2007.02.26.	Initial Version	0	

2. Parts description

2.1 Introduction

Varistor is a component which acts as a nonconductor on the circuit in normal circumstances. When overvoltage is loaded, it becomes a conductor which diverts overcurrent from circuits to ground at critical voltage level.

2.2 Features

- Multilayer laminated structure
- Faster response time to outer overvoltage than diode
- High reliability over multi surge
- Forward & reverse(+, -) direction property
- Low leakage current and inductance
- Easy to control electric capacity
- Excellent reliability against ESD(ElectroStatic Discharge)
- Smaller size than ordinary ones

3. Applications

3.1 Basic theory

Varistor shows a non-linear V-I behavior similar to Si semiconductor. It has high resistance in normal situation but becomes drastically conducting at critical overvoltage level. Varistor normally acts as a nonconductor, but in case overvoltage is loaded, it becomes conductor that diverts current away from circuits to ground protecting equipments. Fig 2 shows how varistor works and protection effect against ESD in short period of time.

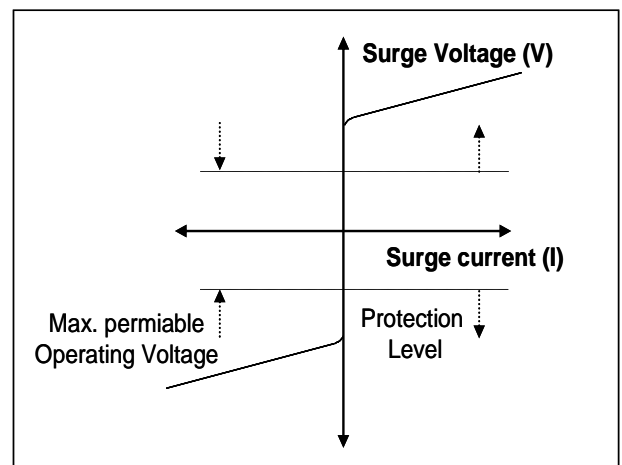


Fig. 1 V-I Characteristic Curve

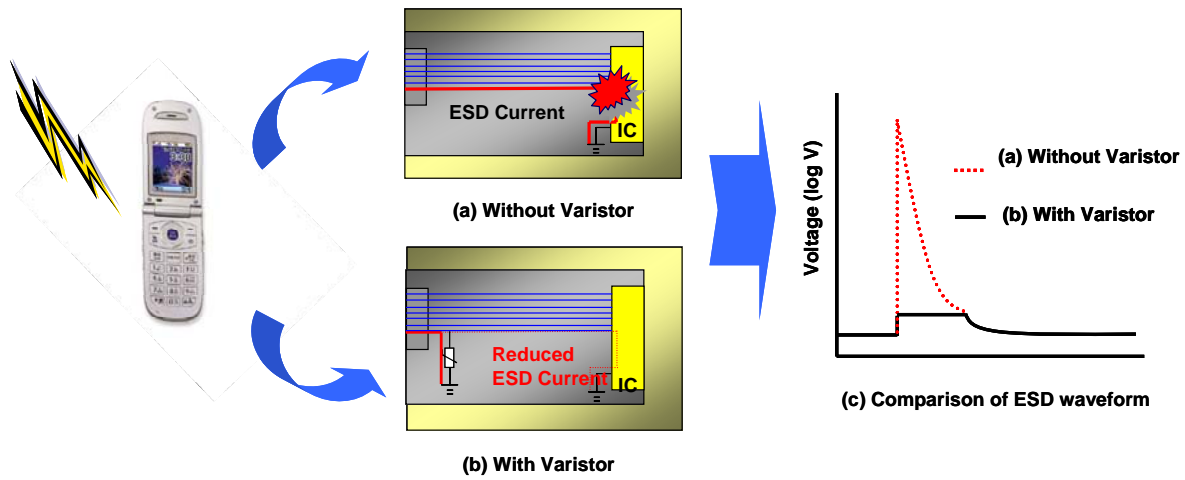


Fig 2) ESD Protection depending on the equipped varistor

3.2 Main application field

All of the circuits which can be damaged by ESD, surge

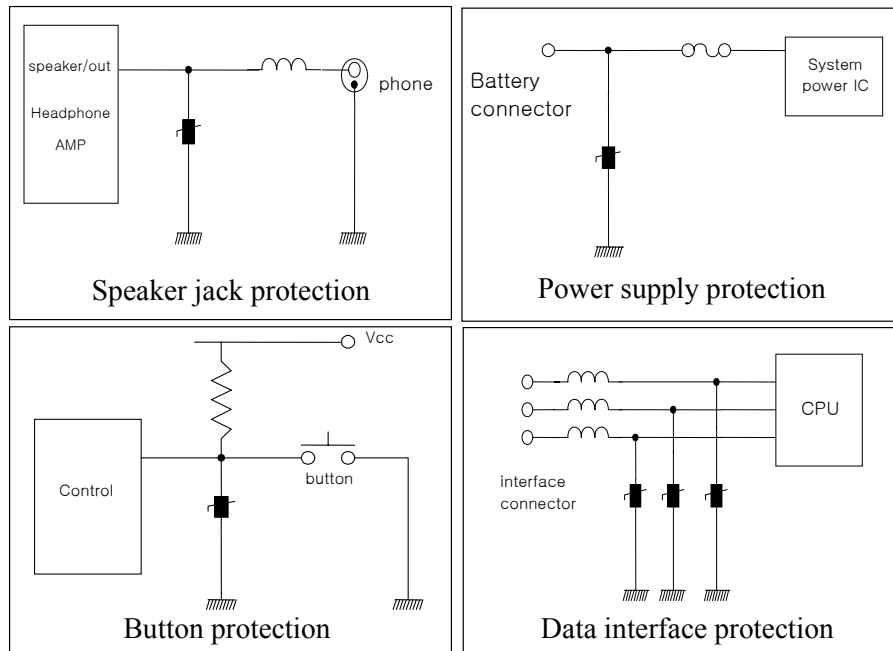


Fig 3) Applied example in Mobile Phone.



APPROVAL SHEET

PAGE

MULTILAYER CHIP VARISTOR

6/16

4. Model and Lot description system

Model : AVLC 3 N 01 100
 (1) (2) (3) (4) (5)

- (1) : Series name : Low Capacitance Type Varistor
- (2) : Maximum continuous working voltage – Vdc = 3.5 V
- (3) : Varistor voltage tolerance – N is ±30 % of varistor voltage
- (4) : Chip size, 01 means 0201 (0.6 x 0.3 mm)
- (5) : Capacitance, 100 means 100pF(typ.)

Lot : X 000 X X 00 X 00 XXX
 (1) (2) (3) (4) (5) (6) (7) (8)

- (1) : Display casting facility
- (2) : Ceramic Tape product #
- (3) : Display printing and stacking facility
- (4) : Display Product Type – P : Mass Production
- (5) : Produced year
- (6) : Produced Month ex) A : Jan. , B:Feb. ...
- (7) : Produced date
- (8) : Amotech Internal code

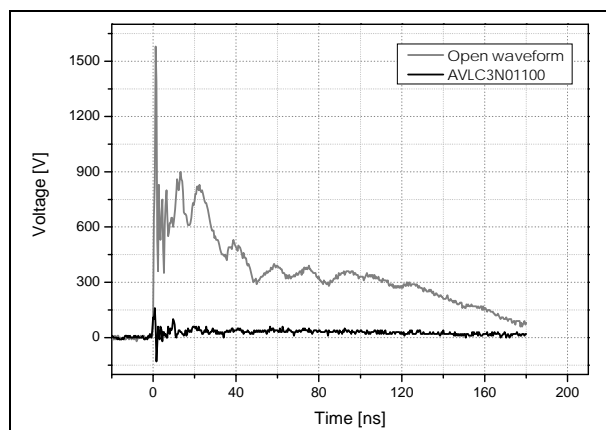
5. Specification

5.1 Electrical characteristics

Part No.	Vdc ⁽¹⁾	Varistor voltage (Vn) @1mA DC	Leakage Current @Vdc	Cp (@ 1KHz, V _{rms} =0.5V)
	(V)	(V)	(μA)	(pF)
AVLC 3N 01 100	3.5	6.8 (4.76 ~8.84)	Max. 20	100 (70 ~ 130)

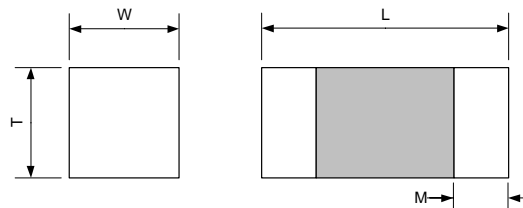
(1) Maximum continuous DC working voltage

◆ ESD waveform



5.2 Mechanical characteristics

- Appearance and dimension



Size(mm)	L	W	T	M
0603	0.60±0.03	0.30±0.03	0.30±0.03	Min. 0.1



APPROVAL SHEET

PAGE

MULTILAYER CHIP VARISTOR

8/16

5.3 Measurement method

5.3.1. Cp measure procedure (LCR Meter–Model Name : Agilent 4284A)

Cp is capacitance measured at 1kHz frequency and Vrms 0.5V biased voltage.

► Test Procedure

1. Turn on power of instrument
2. Press the Meas setup switch
3. Input the value moving arrow
 - FUNC : Cp-D
 - FREQ : 1 kHz
 - LEVEL : 500mV
4. Measure the both terminal of Varistor with probes

5.3.2 IL measure procedure

IL is a current through varistor when Vdc is loaded.

► Test Procedure

1. Turn on the power of instrument.
2. Press I button of 'V' MEAS section from Source area.
3. Press TRIG button after press CONFIG button.
4. Select 'ARM-LAYER' and press 'ENTER' button, and then select 'ARM-IN', press 'ENTER' button again, select 'MANUAL' and press 'ENTER' button.
5. Press twice consecutively 'EXIT' button to go to Main Menu.
6. Press 'CONFIG' button again, and press 'ON-OFF' button.
7. Select 'AUTO-OFF', PRESS 'ENTER', and select 'ENABLE', press 'ENTER' button, and select 'ALWAYS', and then press 'ENTER'.
8. Press once 'EXIT' button to go to the Main Menu.
9. Press blue color of 'EDIT' button from the far left to set the values for Vsrc = Vdc, and Cmpl = 105 μ A.
10. Turn "ON" the ON/OFF switch of OUTPUT.
11. Measure +,- terminals of source meter by connecting both sides of chip termination.



APPROVAL SHEET

PAGE

MULTILAYER CHIP VARISTOR

9/16

5.3.3 Vn measure procedure (Standard Source Meter- Model Name : Keithley 2400)

Vn is working voltage of varistor when 1mA is loaded

► Test Procedure

1. Turn 'OFF' the power, and then turn 'ON'.
2. Press 'V' of 'I' MEAS section of SOURCE area.
3. TRIG function is the same procedure with the above step # 3~#8 of 5.3.2.
4. Press blue color of 'EDIT' button from the far left to set the values for $I_{src} = 1mA$, and $Cmpl = 50V$.
5. Measure IN/OUT terminals of Source Meter by connecting both end of varistor.



APPROVAL SHEET

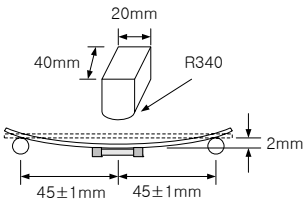
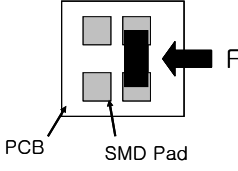
PAGE

MULTILAYER CHIP VARISTOR

10/16

6. Reliabilities and Test conditions

Parameter	Test	Test methods and remarks	Test requirement
Environmental reliability	ESD C=150 pF, R=330Ω	IEC 61000-4-2 1. ESD Level : ±4KV(Contact), ±8KV(Air) 2. Number of Discharge : 10 times 3. RC Network : 330Ω, 150pF	1. $d V_n / V_n \leq 30\%$ 2. No visible Damage.
	Thermal Shock	Condition for 1 cycle 1 step : Min. -40°C, 30±3 min. 2 step : Max. +125°C, 30±3 min. Number of cycles : 50 times Place for 48±2hrs at room temp. condition, then measure	1. $d V_n / V_n \leq 10\%$ 2. No visible Damage.
	Low temp. resistance	1. Temp. : -40 ± 5°C 2. time : 1000 ± 24 hrs 3. Place for 24±2hrs at room temp. condition, then measure	1. $d V_n / V_n \leq 10\%$ 2. No visible Damage.
	High temp. resistance	1. Temp : +125 ± 5°C 2. Time : 1000 ± 24 hrs 3. Place for 24±2hrs at room temp. condition, then measure	1. $d V_n / V_n \leq 10\%$ 2. No visible Damage.
	Heat resistance	1. Temp. : +85 ± 5°C 2. Time : 1000 ± 48 hrs 3. Applied voltage : Vdc 4. Place for 24±2hrs at room temp. condition, then measure	1. $d V_n / V_n \leq 10\%$ 2. No visible Damage.
	High Temp. & Humidity resistance	1. Temp. : +85 ± 5°C 2. Humidity : 85 ± 5 % RH. 3. Time : 500 ± 24 hrs 4. Applied voltage : Vdc 5. Place for 24±2hrs at room temp. condition, then measure	1. $d V_n / V_n \leq 10\%$ 2. No visible Damage.
	PCT (Pressure cooker test)	1. Temp : +121 ± 2°C 2. Humidity : 100% RH. 3. Atmosphere : 2 atm 4. Time : 60 hrs 5. Place for 24±2hrs at room temp. condition, then measure	1. $d V_n / V_n \leq 10\%$ 2. No visible Damage.
	Humidity Test	1. Temp. : +60 ± 5°C 2. Humidity : 90 ± 5 % RH. 3. Time : 1000 ± 48 hrs 4. Place for 24±2hrs at room temp. condition, then measure	1. $d V_n / V_n \leq 10\%$ 2. No visible Damage.

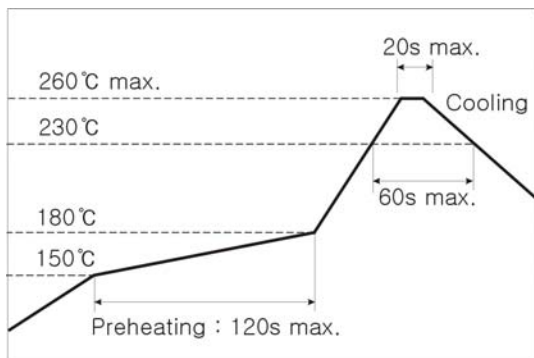
Parameter	Test	Test methods and remarks	Test requirement
Mechanical Reliability	Solderability	1. Test Machine : Solder Bath 2. Temp. : 230±5℃ 3. Time : 2s	At least 95% of terminal electrode is covered by new solder
	Resistance to soldering heat	1. Test Machine : Solder Bath 2. Temp. : 260 ± 5℃ 3. Time : 10±0.5s	1. $d V_n / V_n \leq 10\%$ 2. No visible Damage.
	Bending strength	1. Wrap: 2 mm 2. Speed: 0.5 mm/sec 3. Duration: 10sec  4. The measurement shall be made with board in the bent position	1. $d V_n / V_n \leq 10\%$ 2. No visible Damage.
	Adhesive strength	1. Applied force on SMD chip by fracture from PCB 	1. Strength > 0.8 Kgf (8N) 2. No visible Damage.

7. Soldering Condition

7.1 Soldering condition

A. Lead Free Solder paste

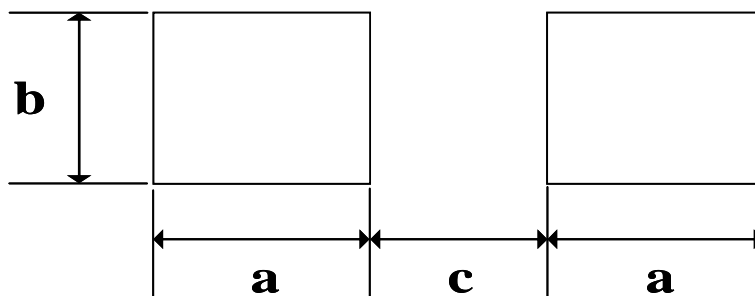
Solder paste : Sn / Ag / Cu : 96.5 / 3.0 / 0.5



Follow the recommended soldering conditions to avoid degradation of varistor performance .

- This product is designed for reflow soldering only. Do not use flow soldering.
- Use non-activated flux. (Max. Cl content less than 0.2%)
- Reflow cycle times should be done less than 3 times.

7.2 PCB pattern design condition (recommended)

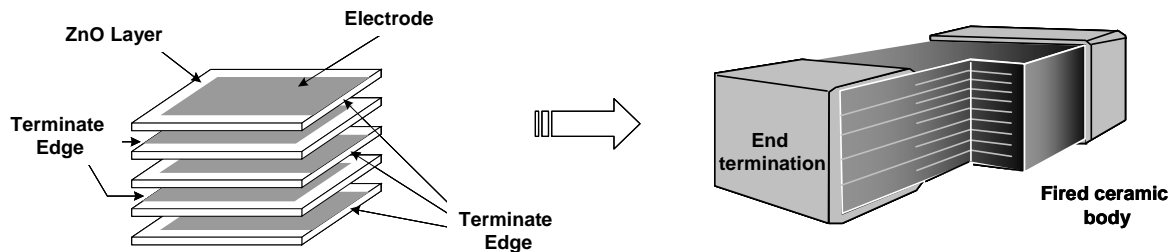


(Unit : mm)

size	a	b	c
0603	0.2~0.3	0.25~0.35	0.25~0.35

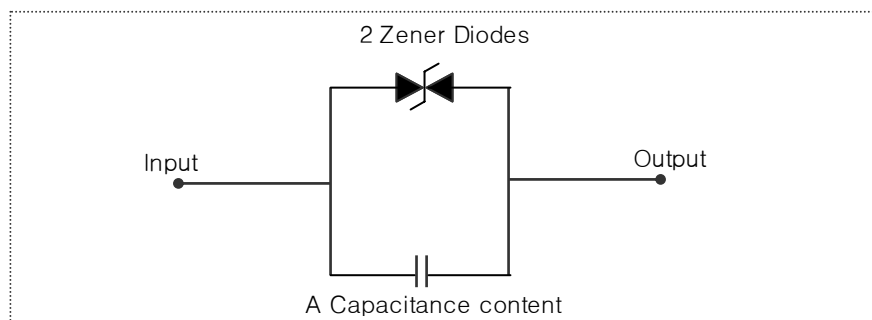
8. Structure and Materials

8.1 Structure and materials specification



Ceramic Body	ZnO System ceramics
Internal Electrode	Ag – Pd / Pd
External Electrode	Ag – Ni– Sn
Plating Layer(Thickness)	Ni \geq 1 μ m , Sn \geq 2 μ m

8.2 Equivalent circuit



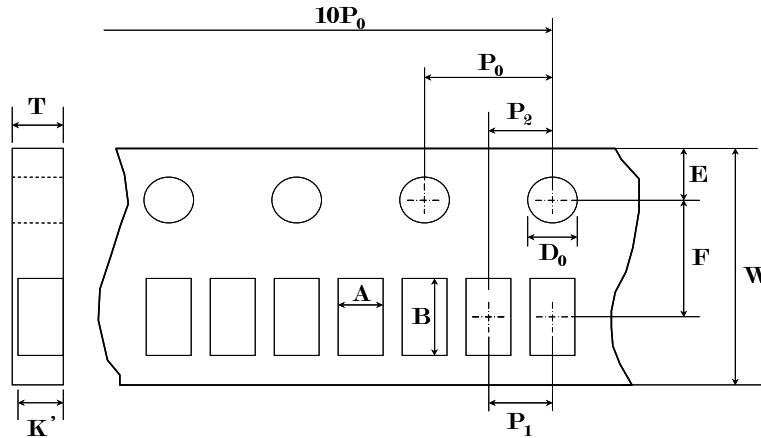
9. Caution

1. Storage environment : -5~40°C temperature, 20~70% humidity (MSL Level 1)
2. Do not use in high temperature/high humidity and a corrosive atmosphere like sulfide, chloride gas which could damage the solderability.
3. Do not expose varistor to mechanical shock to avoid crack.
4. Use chips within 6 months. If over 6 months, check solderability before use.

10. Packaging specification

10.1 Carrier tape Specification

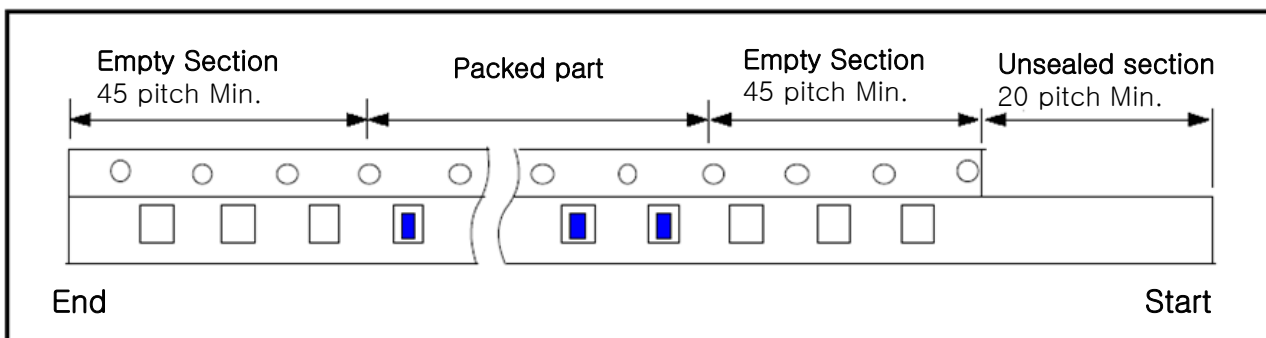
10.1.1 Size



unit : mm

	A	B	W	F	E	P1	P2	P0	D0	K'	T
Spec.	0.38	0.68	8.00	3.50	1.75	2.00	2.00	4.00	1.55	0.35	0.42
Tolerance	±0.03	±0.03	±0.10	±0.05	±0.05	±0.05	±0.05	±0.10	±0.05	±0.02	±0.02

10.1.2 Chip Locations

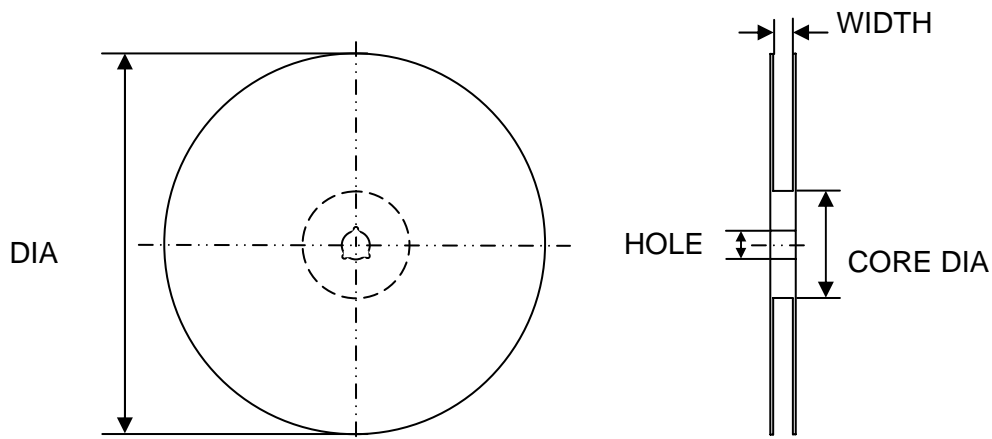


10.1.3 Materials

- 1) Paper carrier tape : Laminated virgin pulp
- 2) Top tape : Polyester film

10.2 Reel Specification

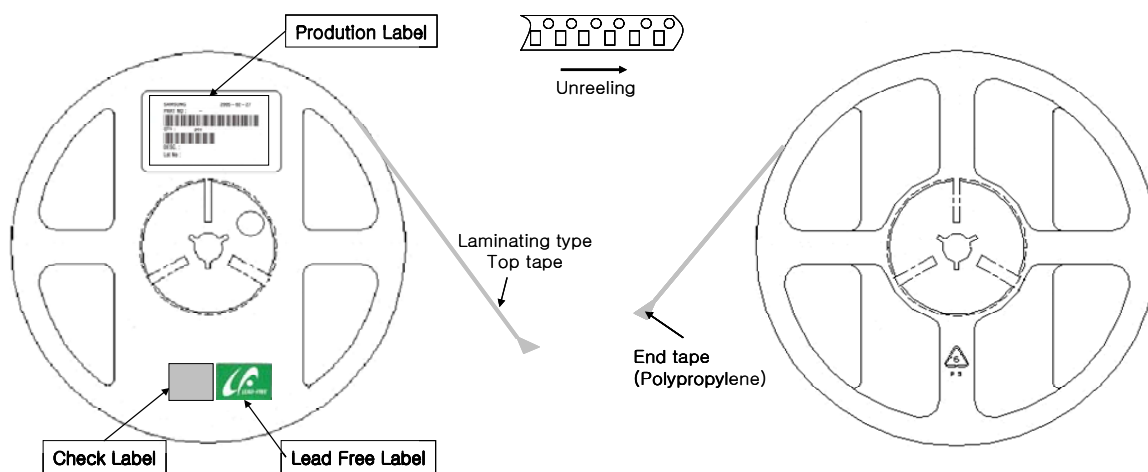
10.2.1 Size



unit : mm

SIZE	DIA	WIDTH	CORE DIA	HOLE
	178.0±0.5	9.0±0.5	60.0±1.0	13.2±0.3

10.2.2 Label adherence and winding direction



10.2.3 Material

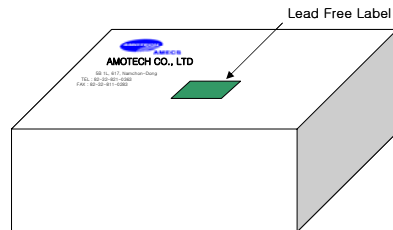
- 1) Plastic reel : GPPS (General Purpose Poly Styrene) resin

10.3 Box packaging Specification

10.3.1 Small Box

Size : 185 (W) x 185 (D) x 65 (T) (mm)

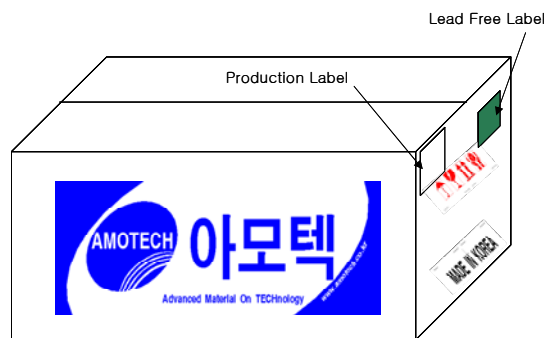
Quantity : 5 reel (10,000 ea/reel × 5 reel = 50,000 ea)



10.3.2 Medium Box

Size : 200 (W) x 375 (D) x 205 (T) (mm)

Quantity : 5 small boxes(50,000 ea/ small boxes × 5 small boxes = 250,000 ea)



10.3.3 Large Box

Size : 375 (W) x 390 (D) x 205 (T) (mm)

Quantity : 10 small boxes (50,000 ea/ small boxes × 10 small boxes = 500,000 ea)

