Parameters Subject to Change Without Notice

DESCRIPTION

The JW®5060T is a monolithic buck switching regulator based on I2 architecture for fast transient response. Operating with an input range of 4V~24V, JW5060T delivers 3A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. At light loads, the regulator operates in low frequency to maintain high efficiency and low output ripples.

JW5060T guarantees robustness with output short protection, thermal protection, current run-away protection, input under voltage lockout.

JW5060T is available in TSOT23-6 and TSOT23-8 packages, which provide a compact solution with minimal external components.

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FEATURES

- 4V to 24V operating input range
  3A output current
- Up to 95% efficiency
- High efficiency (>85%) at light load
- 800kHz switching frequency
- Internal soft-start
- Input under voltage lockout
- Current run-away protection
- Output short protection
- Thermal protection
- Available in TSOT23-6 and TSOT23-8 packages

APPLICATIONS

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/ Appliances
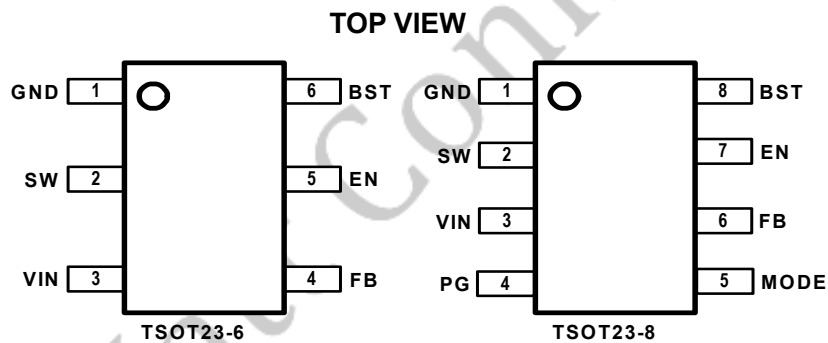- Notebook Computers

TYPICAL APPLICATION
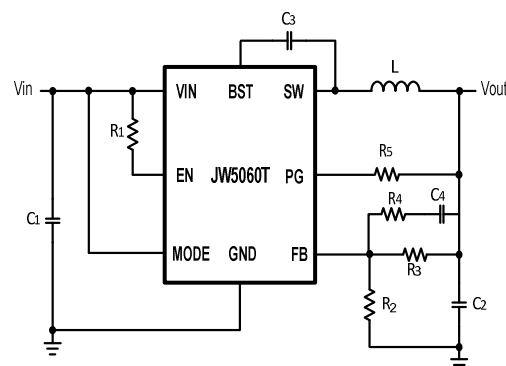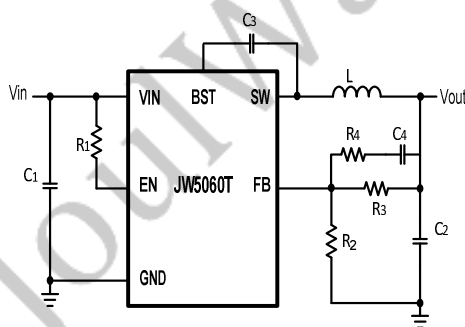
ORDER INFORMATION

DEVICE[1]	PACKAGE	TOP MARKING[2]
JW5060TTSOTB#TRPBF	TSOT23-6	JW6BX YWLLL
JW5060TTSOTC#TRPBF	TSOT23-8	JW6AX YWLLL

Notes：

1) JW☐☐ ☐☐# TRPBF
   PB Free
   Tape and Reel(If" TR" is not shown, it means tube)
   Package Code
   Part No.

2) Line1: JWPNA
   Initial control code
   Product code of JWXXXX
   Joulwatt LOGO
   Line2: YWLLL
   Lot number
   Week code
   Year code

PIN CONFIGURATION

TOP VIEW

GND	1		6	BST
SW	2		5	EN
VIN	3		4	FB

TSOT23-6

GND	1		8	BST
SW	2		7	EN
VIN	3		6	FB
PG	4		5	MODE

TSOT23-8

ABSOLUTE MAXIMUM RATING[1]

VIN, EN, PG, MODE, SW Pin .... -0.3V to 25V

BST Pin ....-0.3V(-3.1V for 10ns) to 25V (26V for 10ns)

All other Pins .... -0.3V to 6V

Junction Temp. [2] [3] 150ºC

Lead Temperature 260ºC

ESD Susceptibility (Human Body Model) 2kV

RECOMMENDED OPERATING CONDITIONS

Input Voltage VIN .... 4V to 24V

Output Voltage Vout ....0.8V to VIN-3V

THERMAL PERFORMANCE[4)] θ_{JA} θ_{Jc}

TSOT23-6...110....55ºC/W

TSOT23-8...110....55ºC/W

Note：

1) Exceeding these ratings may damage the device.

2) The JW5060T guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.

3) The JW5060T includes thermal protection that is intended to protect the device in overload conditions. Thermal protection is active when junction temperature exceeds the maximum operating junction temperature. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VIN=12V, T_A=25℃，Unless otherwise stated.

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IN} Under Voltage Lock-out Threshold	V_{IN_H}	V_{IN} rising			3.8	V
V_{IN} Under Voltage Lock-out Threshold	V_{IN_L}	Vin falling	3			V
V_{IN} Under voltage Lockout Hysteresis[5]	$V_{IN\_MIN\_HYST}$			200		mV
Shutdown Supply Current	I_{SD}	V_{EN}=0V, Vin=24V			1	µA
Supply Current	I_Q	V_{EN}=5V, V_{FB}=1.2V		250		µA
Feedback Voltage	V_{FB}	4V<V_{VIN}<24V	750	765	780	mV
Top Switch Resistance[5]	$R_{DS(ON)T}$			70		mΩ
Bottom Switch Resistance[5]	$R_{DS(ON)B}$			38		mΩ
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=24V, V_{EN}=0V, V_{SW}=0V			1	µA
Bottom Switch Leakage Current	I_{LEAK_BOT}	V_{IN}=24V, V_{EN}=0V, V_{SW}=24V			1	µA
Top Switch Current Limit[5]	I_{LIM_TOP}		5	6	7	A
Minimum On Time[5]	T_{ON_MIN}			120		ns
Minimum Off Time[5]	T_{OFF_MIN}	V_{FB}=0.4V		100		ns
EN Input High Voltage	V_{EN_H}		2.2			V
EN Input Low Voltage	V_{EN_L}				1.7	V
Soft-Start Time[5]	t_{SS}			1.6		ms
Power good lower threshold	PGD_{LTH}	FB falling		88%		
Power good upper threshold	PGD_{UTH}	FB rising		112%		
Power good delay[5]	PGD_{DLY}	PG from low to high		422		µs
Thermal Shutdown[5]	T_{TSD}			140		°C
Thermal Shutdown hysteresis[5]	T_{TSD_HYST}			15		°C

Note：

5) Guaranteed by design.

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PIN DESCRIPTION

Pin		Name	Description
TSOT23-6	TSOT23-8		
1	1	GND	Ground pin.
2	2	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
3	3	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4V to 24V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
4	6	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.765V. Connect a resistive divider at FB.
5	7	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
6	8	BST	Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.
	4	PG	Power good monitor output. This is an open-drain output so a 30kΩ to 100kΩ resistor should be connected at this pin to the VCC pin when output voltage is 5V. The resistor can be lower to 20kΩ if the output voltage is 3.3V.
	5	MODE	Pull MODE pin low to VIN to achieve PFM operation. Pull MODE up to GND or floating to achieve FCC operation.

BLOCK DIAGRAM

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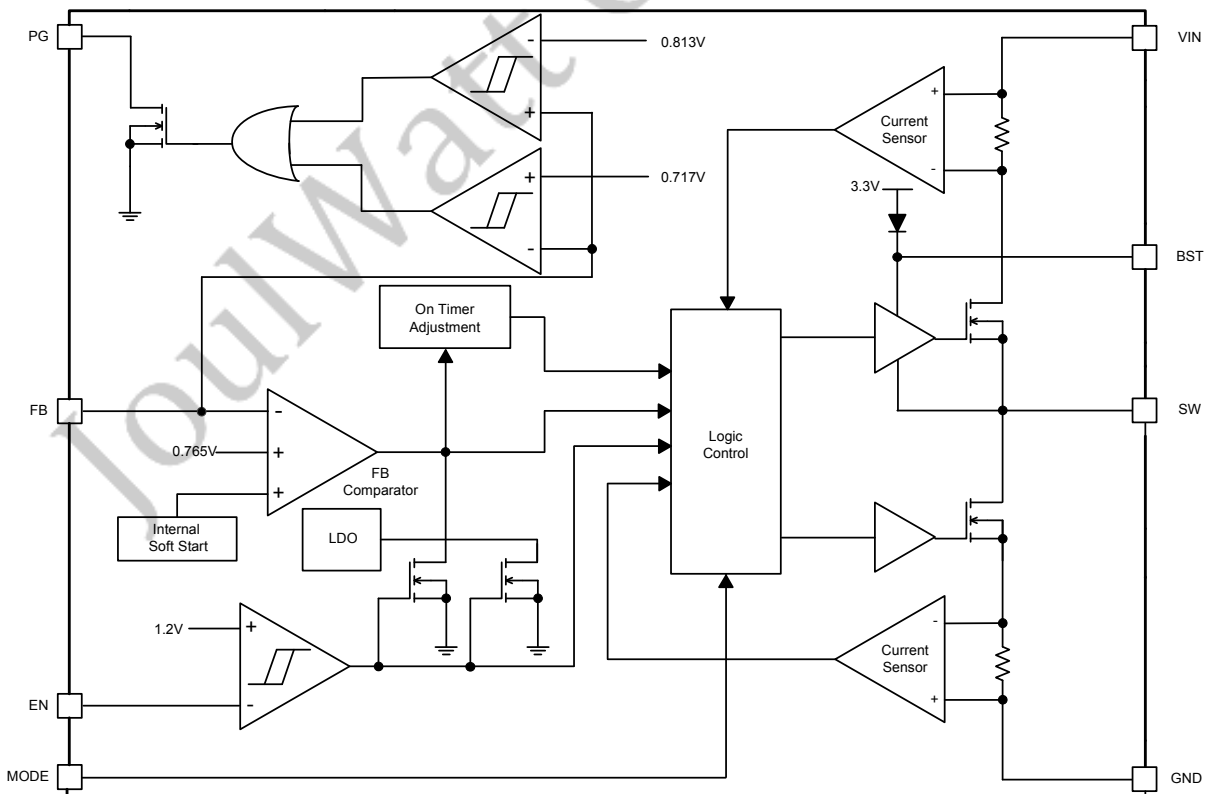
TYPICAL PERFORMANCE CHARACTERISTICS

Vin =12V, Vout = 3.3V, L = 2.2μH, Cout = 44μF, TA = +25°C, unless otherwise noted

Steady State Test
VIN=12V, Vout=3.3V
Iout=3A
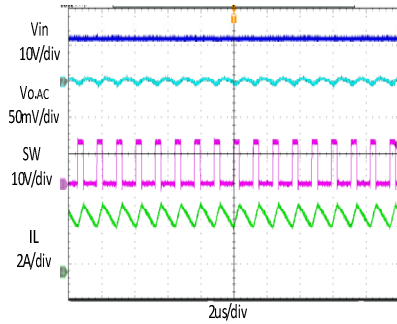
Startup through Enable
VIN=12V, Vout=3.3V
Iout=3A(Resistive load)
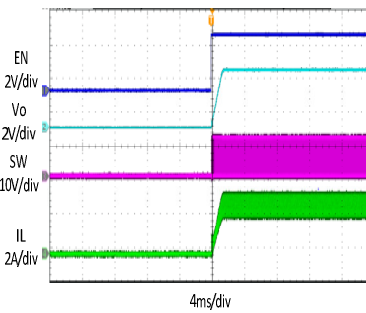
Shutdown through Enable
VIN=12V, Vout=3.3V
Iout=3A (Resistive load)
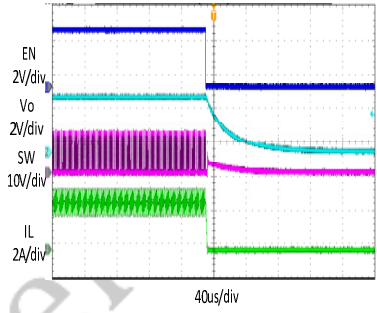
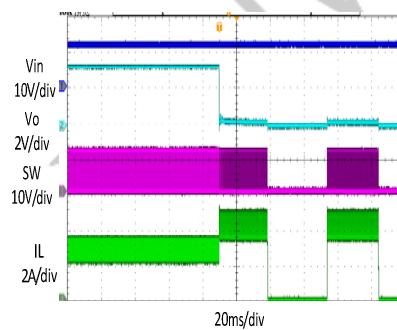**Heavy Load Operation**
3A LOAD
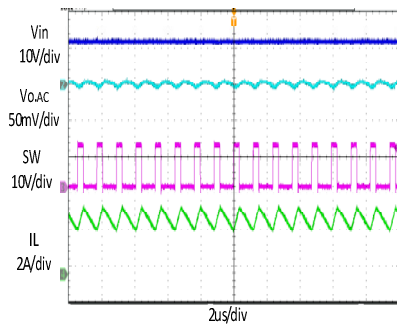
Medium Load Operation
0.3A LOAD
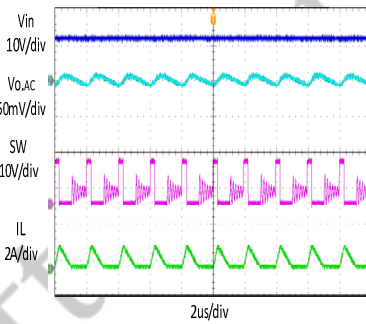
Light Load Operation
0 A LOAD
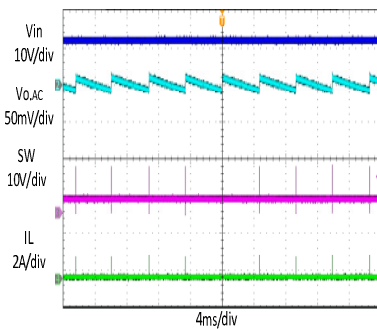
Short Circuit Protection
VIN=12V, Vout=3.3V
Iout=3A- Short

Short Circuit Recovery
VIN=12V, Vout=3.3V
Iout= Short-3A
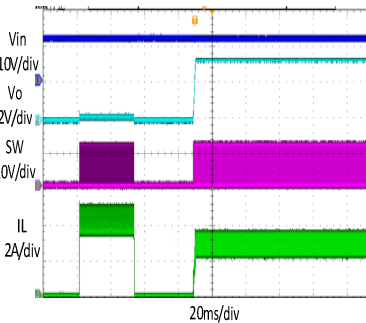
Load Transient
C4=100pF,R4=1k
0.3A LOAD → 3A LOAD → 0.3A LOAD
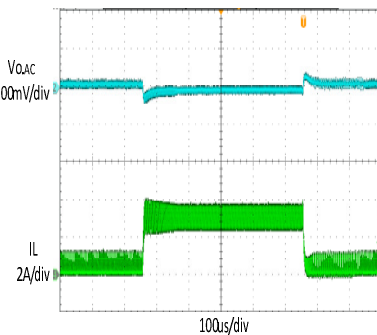
TYPICAL PERFORMANCE CHARACTERISTICS (PFM Mode)
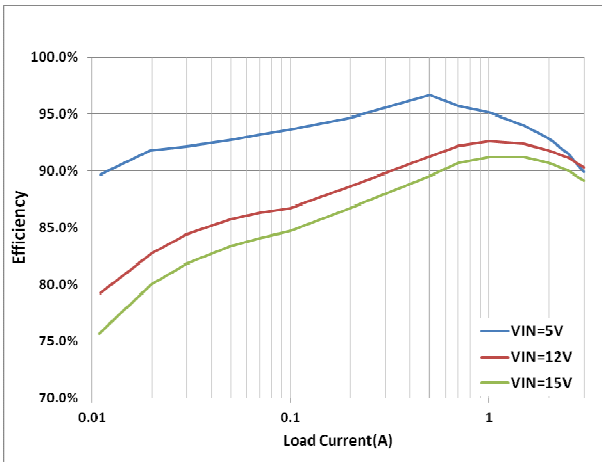
Figure 1. Efficiency vs Load Current
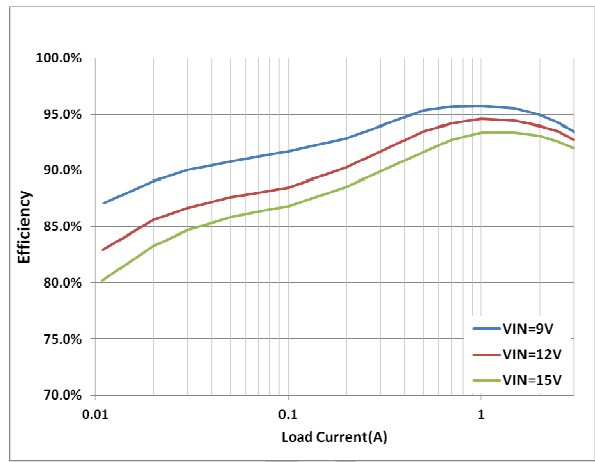
(Vout=3.3V, L=2.2uH)

Figure 2. Efficiency vs Load Current

(Vout=5V, L=3.3uH)
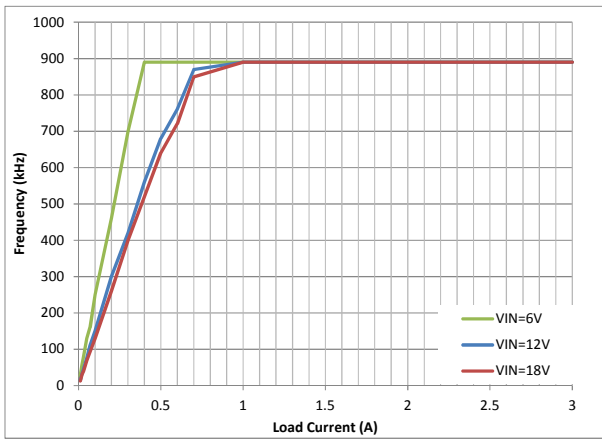
Figure 3. Frequency vs Load Current
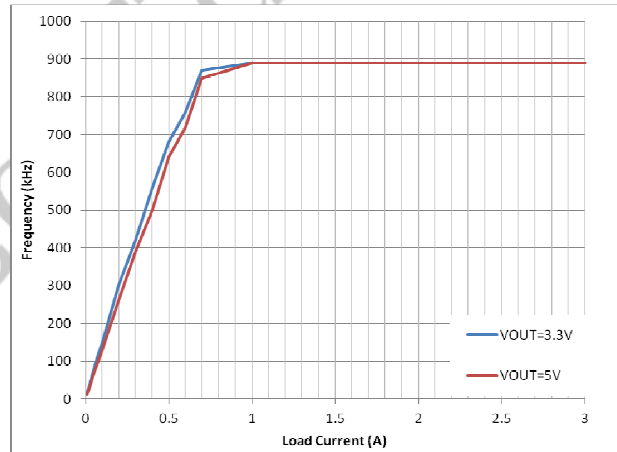
(Vout=3.3V, L=2.2uH)

Figure 4. Frequency vs Load Current

(Vin=12V)

FUNCTIONAL DESCRIPTION

JW5060T is a synchronous step-down regulator based on I2 control architecture. It regulates input voltages from 4V to 24V down to an output voltage as low as 0.765V, and is capable of supplying up to 3A of load current.

Shut-Down Mode

JW5060T shuts down when voltage at EN pin is driven below 0.3V. The entire regulator is off and the supply current consumed by JW5060T drops below 1uA.

Power Switch

N-Channel MOSFET switches are integrated on the JW5060T to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage great than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 3.7V rail when SW is low.

Vin Under-Voltage Protection

A resistive divider can be connected between Vin and ground, with the central tap connected to EN, so that when Vin drops to the pre-set value, EN drops below 2V to trigger input under voltage lockout protection.

Thermal Protection

When the temperature of the JW5060T rises above 140°C, it is forced into thermal shut-down. Only when core temperature drops below 125°C can the regulator becomes active again.

Output Current Run-Away Protection

At start-up, due to the high voltage at input and low voltage at output, current inertia of the output inductor can be easily built up, resulting in a large start-up output current.
A valley current limit is designed in JW5060T so that only when output current drops below the valley current limit can the top power switch be turned on. By such control mechanism, the output current at start-up is well controlled.

Output Short Protection

When the output is shorted to ground, the regulator is allowed to switch for 1024 cycles. If the short condition is cleared within this period, then the regulator resumes normal operation. If the short condition is still present after 1024 switching cycles, then no switching is allowed and the regulator enters hiccup mode for 2048 cycles. After the 2048 hiccup cycles, the regulator will try to start-up again. If the short condition still exists after 1024 cycles of switching, the regulator enters hiccup mode. This process of start-up and hiccup iterate itself until the short condition is removed.

Power Good

The JW5060T has power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect to a voltage source (such as Vout) through a resistor. When the output voltage becomes within +-12% of the target value, internal comparators detect power good state and the power good signal becomes high. If the feedback voltage goes under or higher 12% of the target value, the power good signal becomes low.

APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

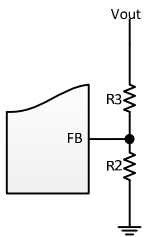$$V_{FB} = V_{out} \cdot \frac{R_2}{R_2 + R_3}$$

where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Choose R_2 around 15kΩ, and then R_3 can be calculated by:

$$R_3 = R_2 \cdot \left(\frac{V_{out}}{0.765} - 1 \right)$$

Too large resistance and the following table lists the recommended values.

V_{OUT}(V)	R2(kΩ)	R3(kΩ)
1	13.3	4.02
1.2	28	16
1.5	16	15.4
2.5	20.5	46.4
3.3	16	53.1
5	16	88.7

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

where I_{LOAD} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{f_s \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where C_1 is the input capacitance value, fs is the switching frequency, $\triangle V_{IN}$ is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 22uF ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot f_s \cdot C_2} \right)$$

where C_2 is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage. The output capacitors also affect the system stability and transient response, and a 22uF~66uF ceramic capacitor is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the

ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_S is the switching frequency, and $\triangle I_L$ is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

A bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1uF low ESR ceramic capacitor is recommended to connected to the BST pin and SW pin.

Feedforward Capacitor

In order to minimize the ripple of output voltage at light load, a feedforward capacitor in series with a resistor should be in parallel to the upper divider resistor. Choose R_4 around 1kΩ and C_4 around 100pF.
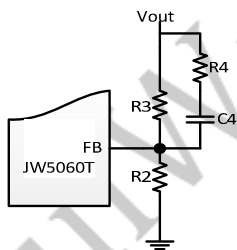
Start up through EN

If JW5060T start up through EN, a 10nF or larger capacitor should be connected between EN pin and GND to eliminate noise.
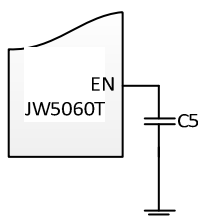
PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5060T (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as far away from the inductor and noisy power traces as possible.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.
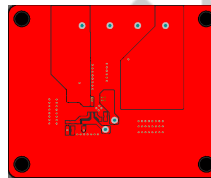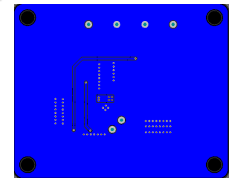
TSOT23-6:

Figure 1. Top Layer
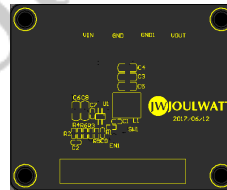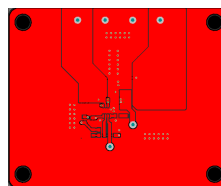

Figure 2. Bottom Layer

Figure 3. Top Silk Layer
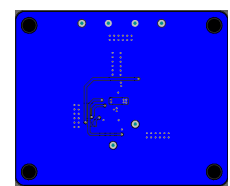
TSOT23-8:

Figure 1. Top Layer

Figure 2. Bottom Layer
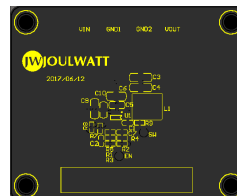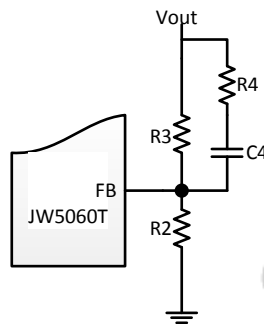

Figure 3. Top Silk Layer

External Components Suggestion:

VOUT(V)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	C4 (pF)	L(uH)	Cout(uF)
1	13.3	4.02	1	100	2.2	54~66
1.2	28	16	1	100	2.2	54~66
1.5	16	15.4	1	100	2.2	54~66
2.5	20.5	46.4	1	100	2.2	22~66
3.3	16	53.1	1	100	2.2	22~66
5	16	88.7	1	100	3.3	22~66

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REFERENCE DESIGN

Reference 1:

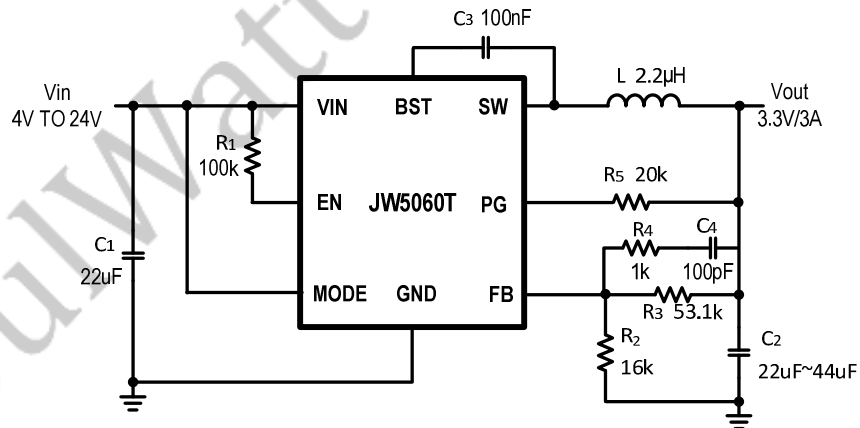Vin :   4V~24V

Vout: 3.3V
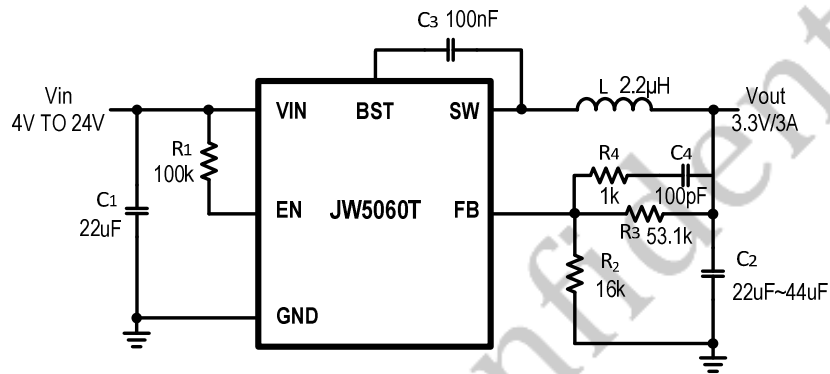
Iout :   0~3A

TSOT23-6:

TSOT23-8:

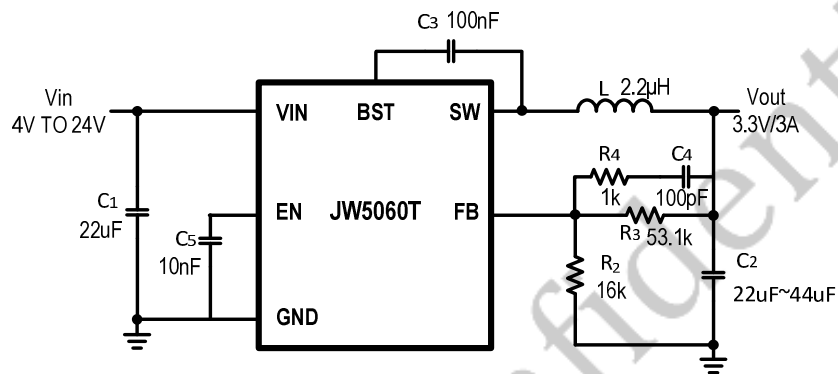## Start up Through EN

Vin :   4V~24V

Vout: 3.3V

Iout :   0~3A

TSOT23-6:

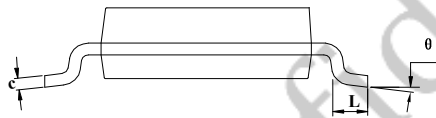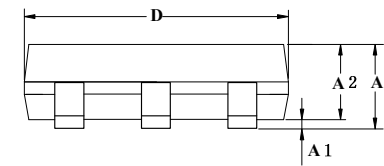

TSOT23-8:

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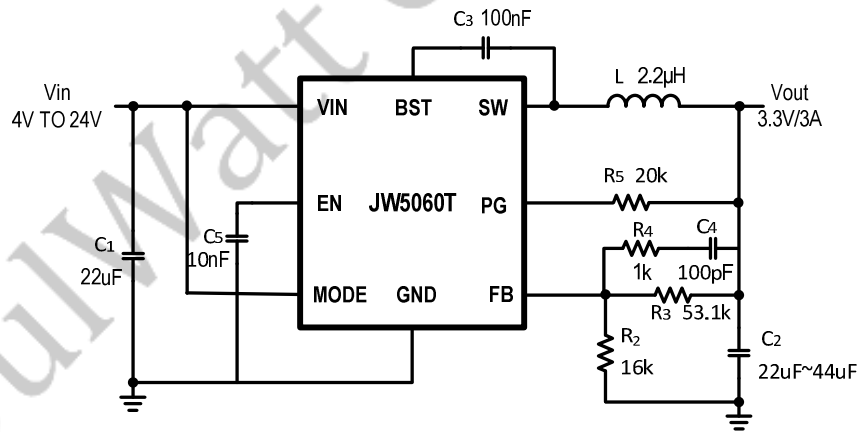
PACKAGE OUTLINE

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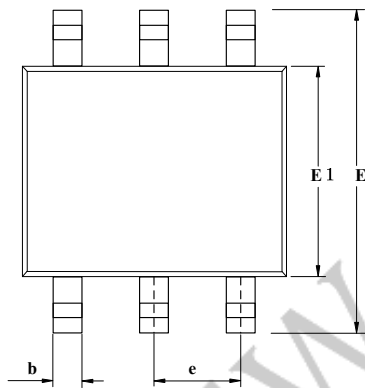
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0	—	0.15
A2	0.55		1.00
b	0.30	0.40	0.50
c	0.08	0.15	0.30
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95（BSC）		
L	0.30	0.45	0.60
θ	0°	—	10°

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TSOT23-8   UNIT: mm
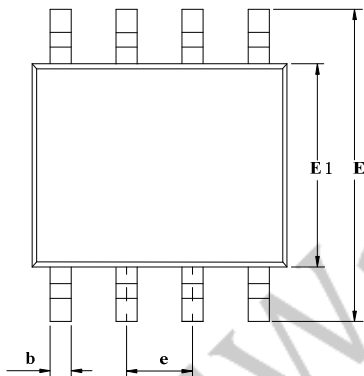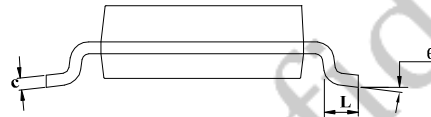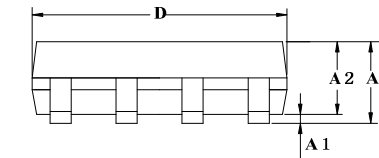
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.10
A1	0	—	0.15
A2	0.55	0.65	1.00
b	0.20	0.40	0.50
c	0.08	0.15	0.30
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95（BSC)		
L	0.30	0.45	0.60
θ	0º	—	10º

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