10-pin, 24-Bit, 192 kHz Stereo D/A Converter for PCM Audio

GENERAL DESCRIPTION

The ES7144LV is a low cost 10-pin stereo digital to analog converter. The ES7144LV can accept I²S serial audio data format up to 24-bit word length. The device uses advanced multi-bit Δ-∑ modulation technique to convert data into two channel analog outputs. The multi-bit Δ -∑ modulator makes the device with very low sensitivity to clock jitter and very low out of band noise.

FEATURES

- 100 dB SNR
- -85 dB THD+N
- Up to 200 kHz sampling frequency
- I^2S audio data format, 16-24 bits
- Single power supply 3V to 5.5V

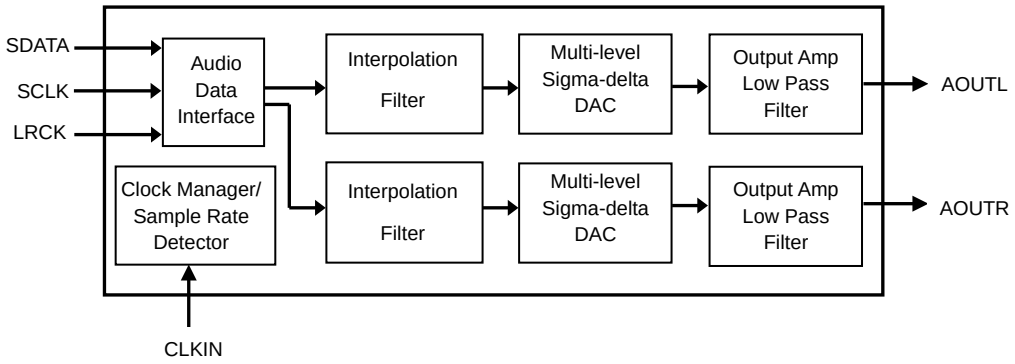
APPLICATIONS

- Digital Photo Frame
- Set top box
- Digital TV
- DVD player
- Audio player

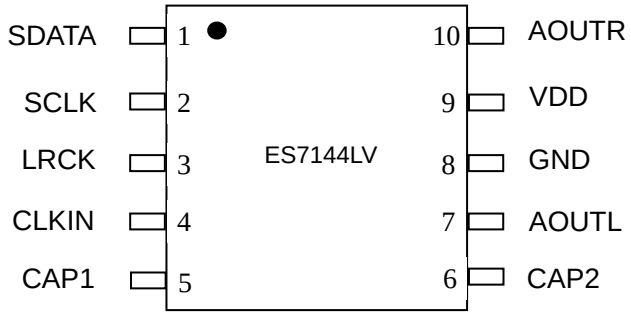
ORDERING INFORMATION

ES7144LV -40°C ~ +85°C TSSOP-10 (Same as MSOP-10)

BLOCK DIAGRAM



1. PIN DESCRIPTIONS



PIN	PIN	I/O	DESCRIPTION
1	SDATA	I	Serial audio data input
2	SCLK	I	Bit clock input
3	LRCK	I	Left and right channel clock input indicating input data sampling rate (Fs) and channel selection
4	CLKIN	I	System clock input
5	CAP1	O	Filtering capacitor
6	CAP2	O	Filtering capacitor
7	AOUTL	O	Analog output of left channel
8	GND	I	Ground
9	VDD	I	Device power supply
10	AOUTR	O	Analog output of right channel

2. RECOMMENDED APPLICATION CIRCUIT

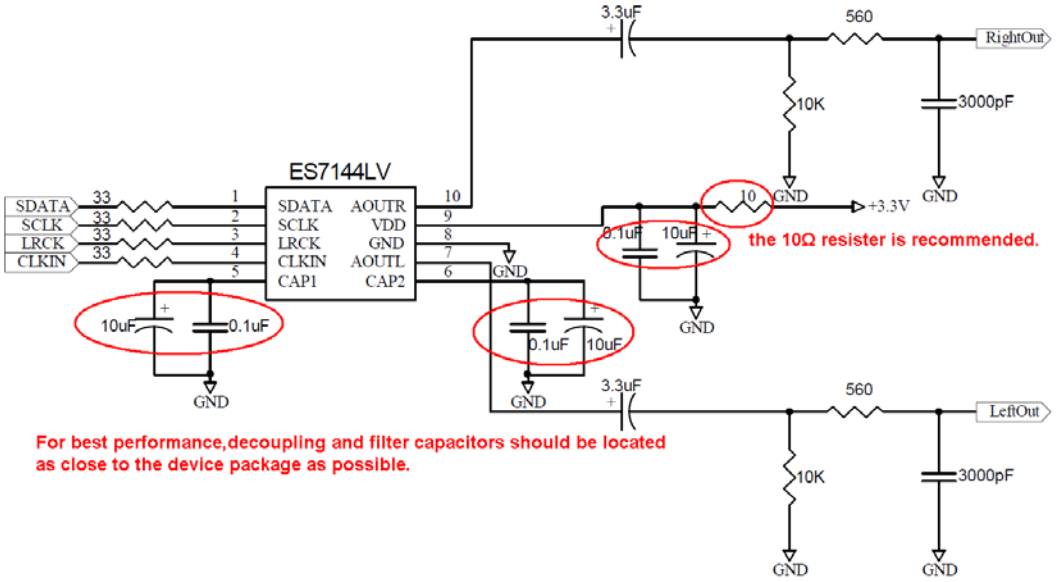


Figure 1 Recommended Application Circuit

3. APPLICATION DESCRIPTIONS

Sampling Rate and Input Clocks

The serial audio input data is transmitted to the device at SDATA pin. According to the sampling rate, the device can work in three speed modes, single speed, double speed and quad speed. The device can detect the speed mode of the input data stream automatically when the sampling rate falls into the auto detection ranges listed in Table1. If the sampling rate is outside the auto detection ranges, the device will not work properly.

Table 1 Auto Detection Ranges and CLKIN/LRCK Ratio

MODE	Fs Auto Detection Range	CLKIN/LRCK Ratio
Single Speed	8kHz – 50kHz	256, 384, 512, 768, 1024
Double Speed	84kHz – 100kHz	128, 192, 256, 384, 512
Quad Speed	167kHz – 200kHz	128, 192, 256

The device works with the input system clock CLKIN, sample data clock LRCK and bit clock SCLK. The data clock and bit clock must be synchronously derived from the system clock with some specific rates. The device only supports the CLKIN/LRCK ratios listed in Table1. The LRCK/SCLK ratio is normally 64. The device detects clock ratios automatically, and it will not work properly if any ratio is incorrect.

Audio Data Input

The ES7144LV can accept I²S serial audio input data from 16-bit to 24-bit. The device can detect the data word length automatically. The relationship of SDATA, SCLK and LRCK for the format is illustrated through Figures 2.

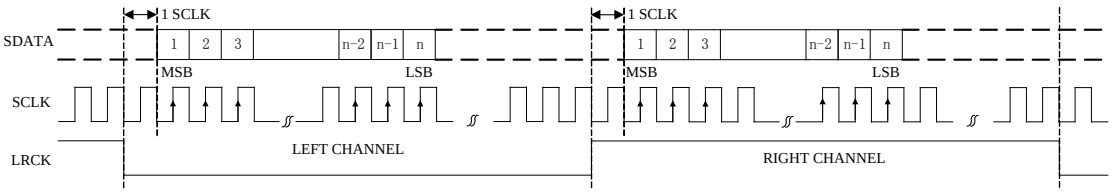


Figure 2 I²S serial audio data format up to 24-bit

Power Up and Power Down

The device resets itself when VDD ramp from ground voltage to supply voltage. The ground voltage needs to be less than 0.2V for proper reset. When VDD voltage is removed, it is important to let it drop below 0.2V before next power up. An optional discharge resistor (3.3K, for example) can be placed between VDD and GND.

Upon applying VDD, the device will reset itself and enter power down state. During this state, the device clamps outputs to ground and power down the device operation except for clock management unit. Once proper CLKIN and LRCK clocks are applied, the device will leave power down state, and the device outputs ramp from ground to common mode voltage softly. Then the device enters the normal operation.

4. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

At or beyond this condition, operating continuously may cause permanent damage to the device. The performance and functions of the device are not guaranteed at these extremes.

PARAMETER	MIN	MAX
Supply Voltage Level	-0.3V	+7.0V
Input Voltage Range	GND-0.3V	VDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNIT
Supply Voltage Level	3	3.3	5.5	V

Analog Characteristics

Test conditions: VDD=3.3V, GND=0V, ambient temperature=25°C, Fs=48KHz, CLKIN/LRCK=256, input 0dB 1KHz sinewave

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Signal to Noise Ratio (Note 1)	90	100		dB
THD+N		-85	-80	dB
Channel Separation (1KHz)		100		dB
Dynamic Range		100		dB
Interchannel Gain Mismatch		0		dB
Frequency Response (20Hz-20KHz)	-0.02		+0.08	dB
Filter Frequency Response characteristics				
Single Speed				
Passband	0		0.454	Fs
Stopband	0.547			Fs
Passband Ripple		±0.05		dB

Stopband Attenuation	-53			dB
Double Speed				
Passband	0		0.417	Fs
Stopband	0.583			Fs
Passband Ripple		±0.005		dB
Stopband Attenuation	-56			dB
Quad Speed				
Passband	0		0.2083	Fs
Stopband	0.792			Fs
Passband Ripple		±0.006		dB
Stopband Attenuation	-50			dB
Analog Output Characteristics				
Full Scale Output Level		0.7*VDD		Vpp
Output Impedance		120		Ω
Minimum Load Resistance		2		KΩ
Maximum Capacitance		100		pF

Note 1. A-weighted filter is used in measurement.

Serial Audio Port Switching Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNIT
CLKIN Frequency			51.2	MHz
CLKIN Duty Cycle		40	60	%
LRCK Frequency			200	KHz
LRCK Duty Cycle		40	60	%
SCLK Frequency			26	MHz
SCLK Pulse Width Low	T_{SCKL}	15		ns
SCLK Pulse Width High	T_{SCKH}	15		ns
SCLK Rising to LRCK Edge Delay	T_{LRH}	10		ns
SCLK Rising to LRCK Edge Setup Time	T_{RSU}	10		ns
SDATA Valid to SCLK Rising Setup Time	T_{SDS}	10		ns
SCLK Rising to SDATA Hold Time	T_{SDH}	10		ns

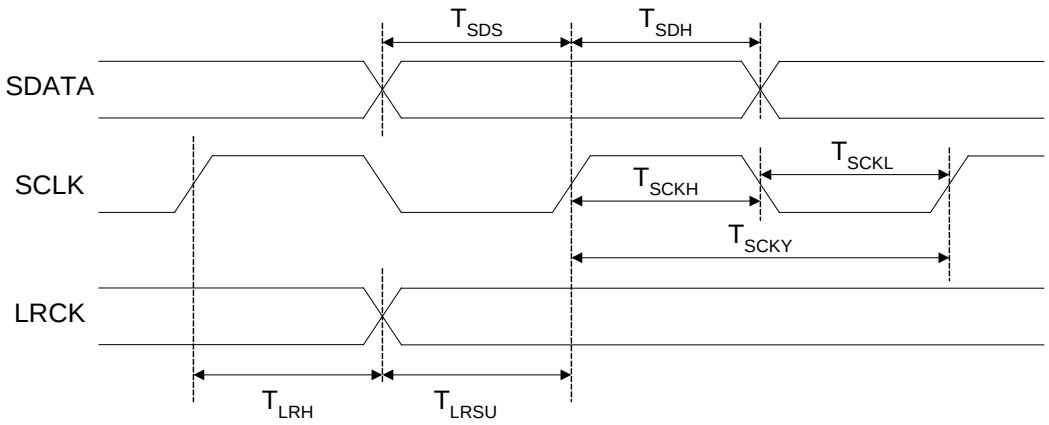


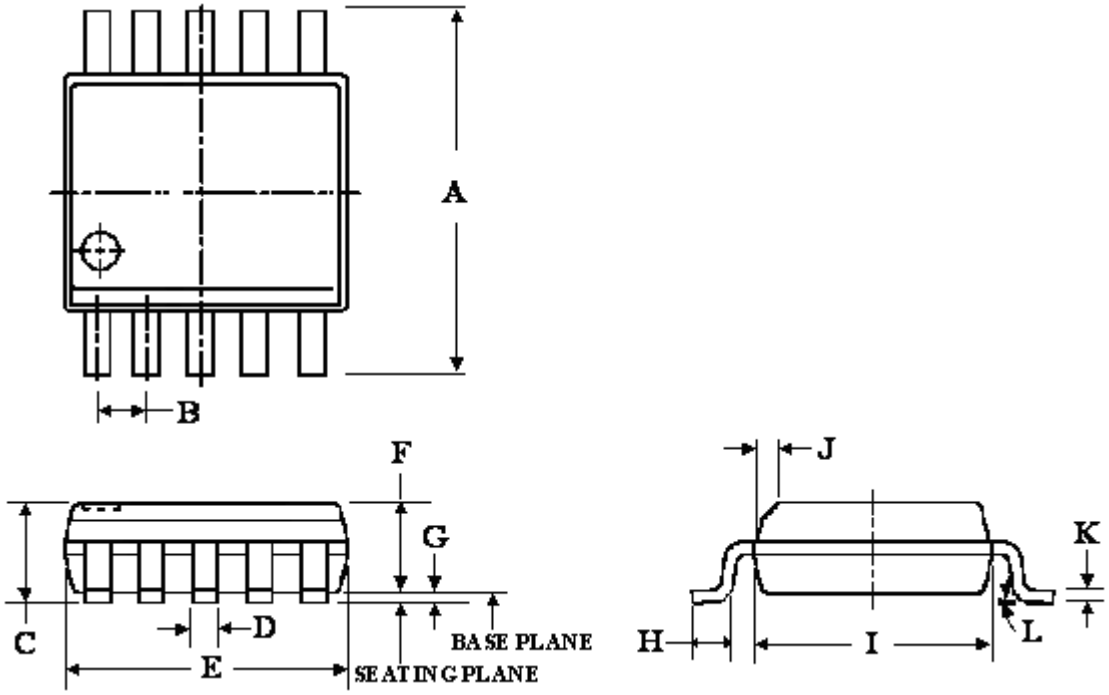
Figure 3 Serial Audio Port Timing

DC Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
VDD Current VDD=3.3V		15	20	mA
Power Dissipation VDD=3.3V		50	70	mW
Digital Voltage Level				
Input High-level Voltage	2.0			V
Input Low-level Voltage			0.8	V
Output High-level Voltage		VDD		V
Output Low-level Voltage		0		V

5. PACKAGE INFORMATION

TSSOP-10 (3mm BODY) Outline Dimensions



Symbols	Dimensions (inch)			Dimensions (mm)		
	Min	TYP	Max	Min	TYP	Max
A	---	0.1929	---	---	4.9	---
B	---	0.0197	---	---	0.5	---
C	---	---	0.0433	---	---	1.10
D	0.0059	---	0.0118	0.15	---	0.30
E	---	0.1181	---	---	3.0	---
F	0.0295	---	0.0374	0.75	---	0.95
G	0	---	0.0059	0	---	0.15
H	0.0157	0.0236	0.0315	0.40	0.60	0.80
I	---	0.1181	---	---	3.0	---
J	0.0100x45°	---	0.0160 x45°	0.254 x45°	---	0.406 x45°
K	0.0031	---	0.0091	0.08	---	0.23
L	0°	---	8°	0°	---	8°

Note:
1. Reference JEDEC MO-187

6. Contact Information:

Everest Semiconductor Co., Ltd.
苏州工业园区金鸡湖大道 1355 号国际科技园，邮编 215021
Email: info@everest-semi.com