General Description

The WST4040 is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The WST4040 meet the RoHS and Green Product requirement,100% EAS guaranteed with full function reliability approved.

Product Summery

BVDSS	RDSON	ID
40V	35mΩ	5.8A

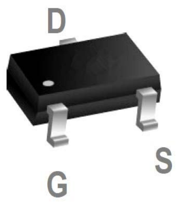
Applications

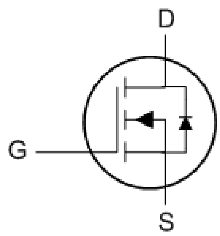
- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

SOT-23-3L Pin Configuration





Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 4.5V[1]	5.8	A
I_D@T_C=70℃	Continuous Drain Current, V_{GS} @ 4.5V[1]	2.5	A
I_{DM}	Pulsed Drain Current[2]	16	A
P_D@T_A=25℃	Total Power Dissipation[3]	1.0	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient [1]	---	125	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	75	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	40	---		V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.0	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=3A	---	35	50	mΩ
		V_{GS}=4.5V , I_D=2A	---	50	60	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, I_D =250uA	0.6	1.0	1.6	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.5	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=32V , V_{GS}=0V , T_J=25℃	---	-	1	uA
		V_{DS}=32V , V_{GS}=0V , T_J=55℃	---	-	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	-	±100	nA
gfs	orward Transconductance	V_{DS}=5V , I_D=3A	---	18	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	1.7	---	Ω
Q_g	Total Gate Charge (4.5V)	V_{DS}=20V , V_{GS}=4.5V , I_D=2A	---	6.5	12.5	nC
Q_{gs}	Gate-Source Charge		---	0.8	3.5	
Q_{gd}	Gate-Drain Charge		---	1.65	4.2	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=20V , V_{GS}=10V , R_G=3.3Ω I_D=1A	---	1.5	4.8	ns
T_r	Rise Time		---	42	14	
$T_{d(off)}$	Turn-Off Delay Time		---	18	44	
T_f	Fall Time		---	5.9	8	
C_{iss}	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	396	---	pF
C_{oss}	Output Capacitance		---	47	---	
C_{rss}	Reverse Transfer Capacitance		---	35	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy[5]	V_{DD}=25V , L=0.1mH , I_{AS}=2A	9	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,6]	$V_G=V_D$=0V , Force Current	---	---	1	A
I_{SM}	Pulsed Source Current[2,6]		---	---	16	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	---	1.2	V
t_{rr}	Reverse Recovery Time	I_F=2A , dI/dt=100A/μs , T_J=25℃	---	18	---	nS
Q_{rr}	Reverse Recovery Charge	I_F=2A , dI/dt=100A/μs , T_J=25℃	---	70	---	nC

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper,t<10sec.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=2A
4.The power dissipation is limited by 150℃ junction temperature
5.The Min. value is 100% EAS tested guarantee.
6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

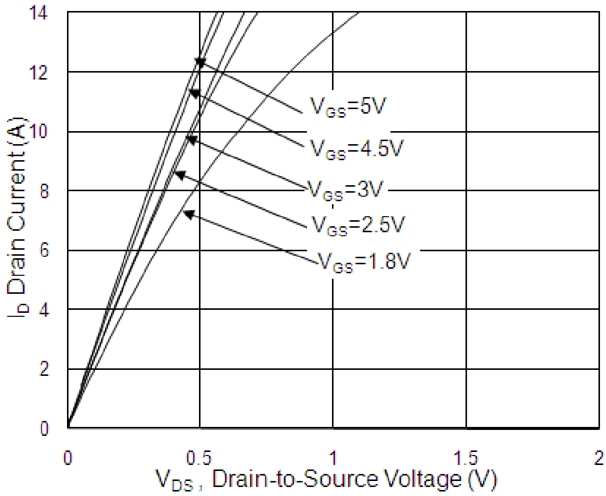


Fig.1 Typical Output Characteristics

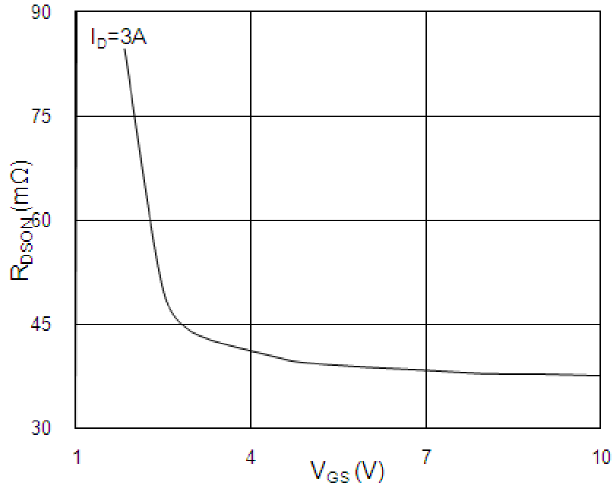


Fig.2 On-Resistance vs. Gate-Source

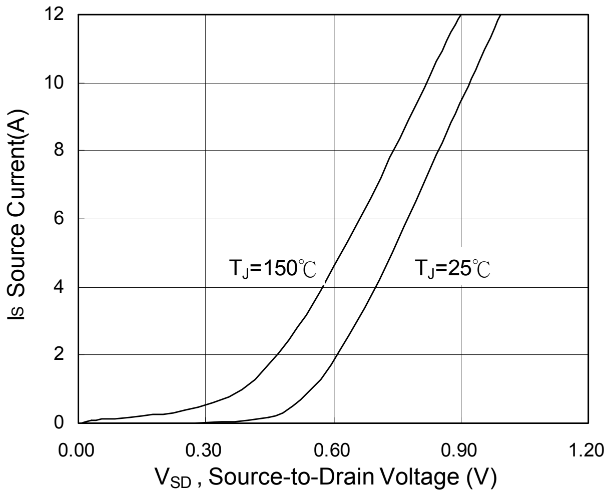


Fig.3 Forward Characteristics Of Reverse

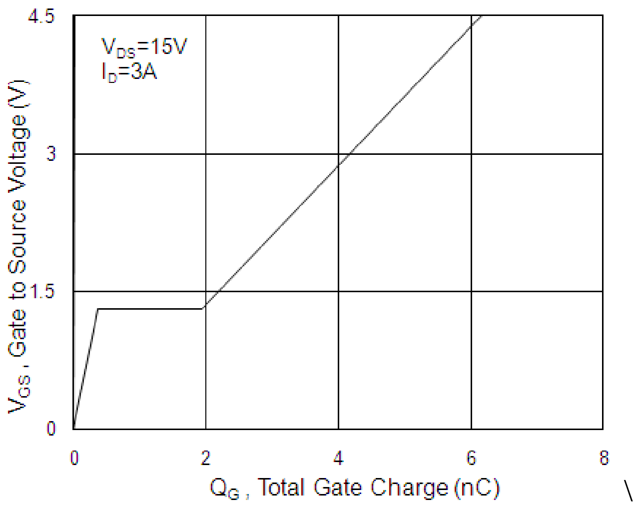


Fig.4 Gate-Charge Characteristics

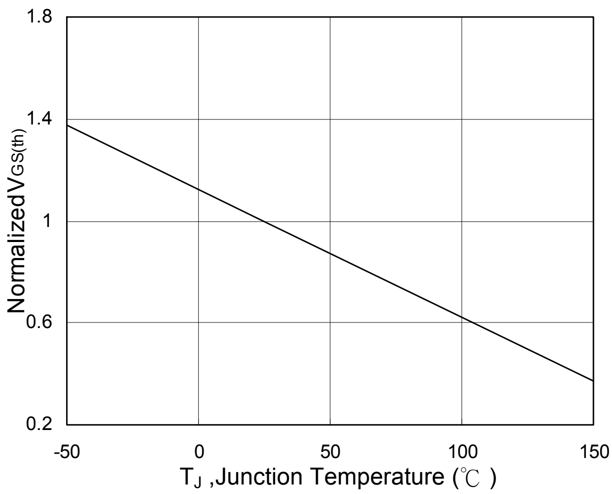


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

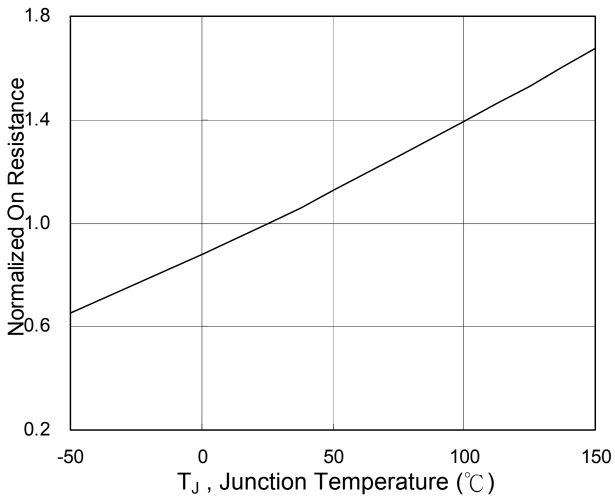


Fig.6 Normalized R_{DSON} vs. T_J

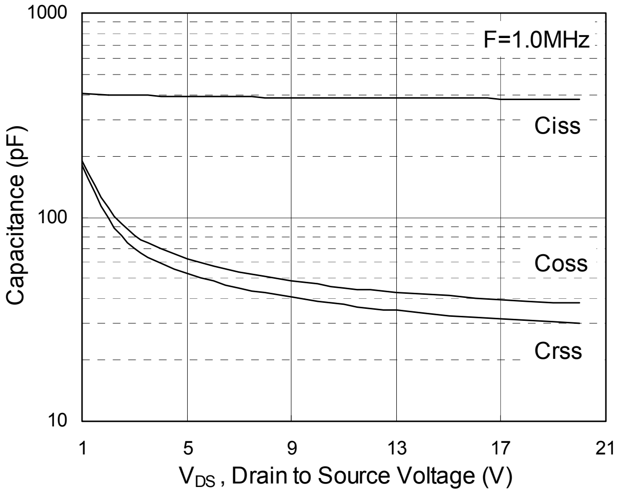


Fig.7 Capacitance

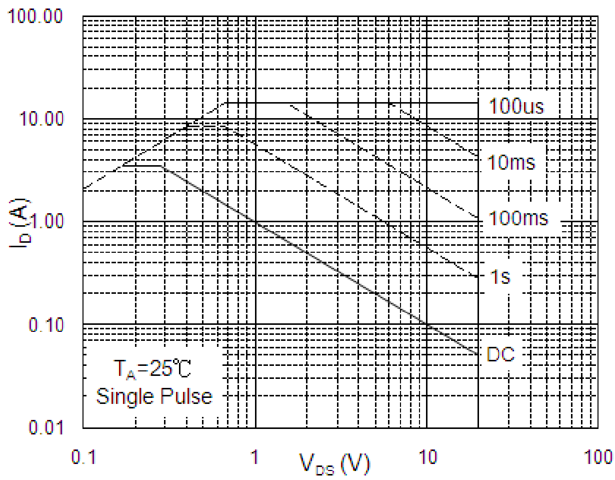


Fig.8 Safe Operating Area

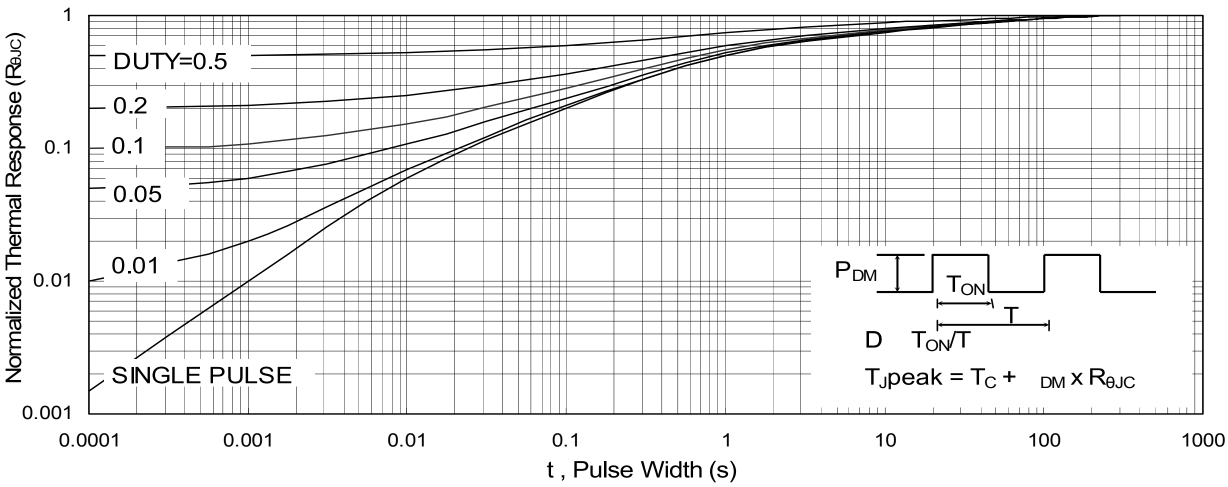


Fig.9 Normalized Maximum Transient Thermal Impedance

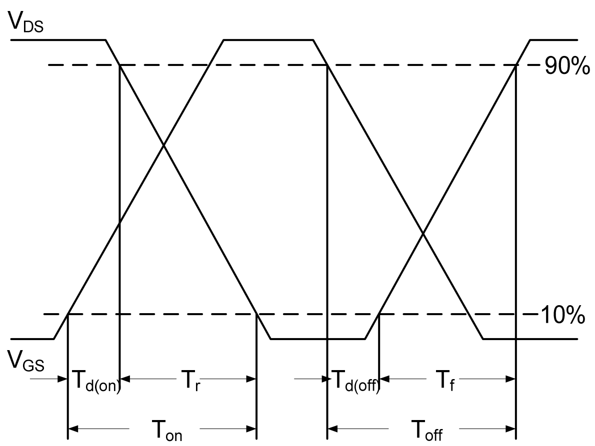


Fig.10 Switching Time Waveform

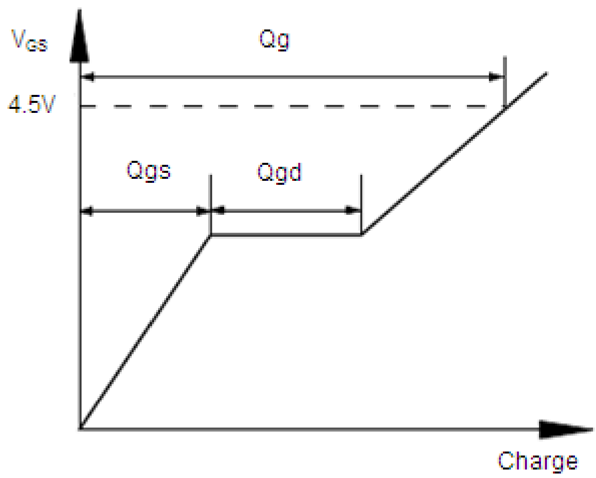


Fig.11 Gate Charge Waveform

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