SiI9135/SiI9135A HDMI Receiver with
Enhanced Audio and Deep lor Outputs

Data Sheet

Document # SiI-DS-0206-F02

, Inc.

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Revision History

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Revision	Date	
A	01/07	Initial Production Data Sheet
B	02/07	Updates to template and timing measurements
C	06/07	Updated to DSD Audio specifications
D	12/07	ntent rrections, remat, pyedit clarity
E	02/08	Updates to frequencies supported by MCLK and to Power-Down current spec
F	06/08	Updated ePad dimensions
F01	4/2010	Updated page 1 and layout to prepare Data Brief; minor editing throughout.
F02	8/2010	Removed Patent inmation from DB, rolled the revision.

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Introduction

The SiI9135/SiI9135A HDMI Receiver with Enhanced Audio and Deep lor Outputs is a send-generation dual-input High Definition Multimedia Interface (HDMI) receiver. It is software-mpatible with the SiI9133 receiver, but adds audio support DTS-HD and Dolby TrueHD. Digital televisions that can display 10- or 12-bit lor depth can now provide the highest quality protected digital audio and video over a single cable. The SiI9135 and SiI9135A devices, which are functionally identical, can receive Deep lor video up to 12-bit, 1080p @ 60 Hz. Backward mpatibility with the DVI 1.0 specification allows HDMI systems to nnect to existing DVI 1.0 hosts, such as HD set-top boxes and PCs. HDMI receivers the latest generation Transition

Minimized Differential Signaling (TMDS) re that runs at 25–225 MHz.

The chip mes pre-programmed with High-bandwidth

Digital ntent Protection (HDCP) keys receiving protected audio and video ntent. This set of keys simplifies the manufacturing process and lowers sts

while providing the highest level of HDCP key[2] security.

The SiI9135/SiI9135A receiver can send and receive up to eight channels of unmpressed digital audio at 192 kHz and 2-channel digital audio up to 192 kHz.

mpressed streams are also supported through either the S/PDIF port or over I^{2}S DTS-HD and Dolby TrueHD. An industry-stard I S port allows direct

S/PDIF port supports up to 192 kHz audio. The device supports Super Audio mpact Disc (SACD) and

provides Direct Stream Digital (DSD) ports that support

44.1 and 88.2-kHz one-bit audio.
A low-power standby feature of the SiI9135/SiI9135A receiver enables flexible power management.

Digital Video Interface

- ☐ Flexible support many different stard- and high-definition video mats (36-bit RGB/YCbCr 4:4:4, 16/20/24-bit YCbCr 4:2:2, 8/10/12-bit YCbCr 4:2:2 (ITU BT.656))
- ☐ 12/15/18-bit Digital Multimedia Output (DMO) RGB/YCbCr 4:4:4 (clocked with rising and falling edges)
- ☐ lor Space nversion both RGB-to-YCbCr and YCbCr-to-RGB (both 601 and 709)
- ☐ True 12-bit accurate data using 14-bit processing
- ☐ Auto video mode nfiguration simplifies system firmware design

Digital Audio Interface

- ☐ DTS-HD and Dolby TrueHD high bit rate audio
- ☐ Four I$_2$S inputs accept Dolby Digital, DVD-Audio input (2-channel 192 kHz and 8-channel 192 kHz)
- ☐ S/PDIF input supports PCM, Dolby Digital, DTS

digital audio transmission (32–192 kHz Fs sample

- ☐ IEC60958 or IEC61937 mpatible
- ☐ Flexible, programmable I^{2}S channel mapping

HDCP Decryption

lower st

level of key security, simplify manufacturing, and

- ☐ Full support HDCP repeaters (up to 16 attached downstream devices)

Package
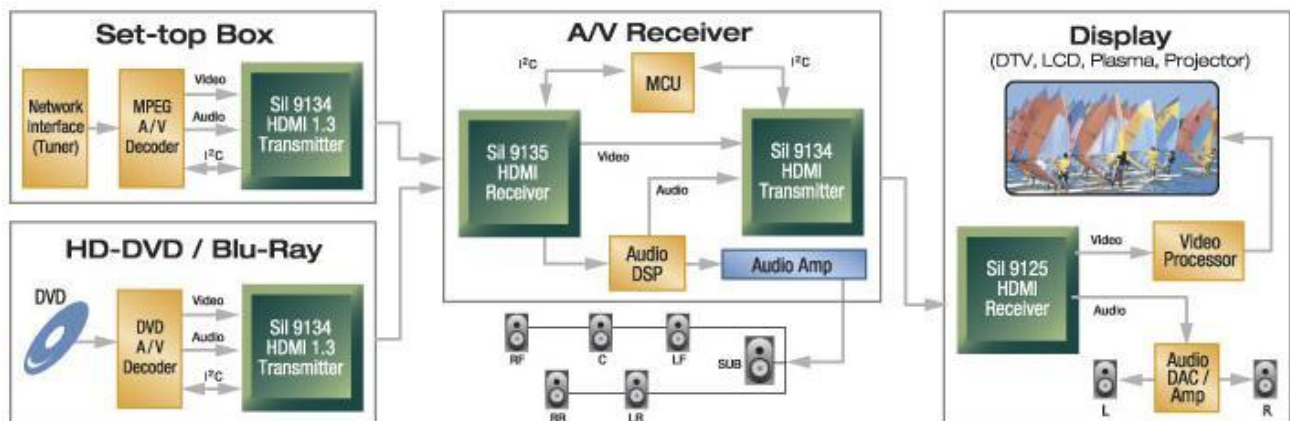
Figure 1. Typical Application of SiI9135/SiI9135A Receiver

System Applications

The SiI9135/SiI9135A receiver is designed AV receivers that require support HDMI Deep lor and the latest audio technologies: DTS-HD and Dolby TrueHD. The receiver allows receiving 10/12-bit lor depth up to 1080p resolutions. A single device provides two HDMI input ports. The video output goes to a video processor or HDMI transmitter. Besides DTS-HD and Dolby TrueHD, the device supports full surround sound audio including DVD-Audio and SACD. The audio output can go directly to an audio DAC or an audio digital signal processor further processing.

mparing the SiI9135/SiI9135A Receiver with the SiI9033 and SiI9133 Receivers

Table 1 summarizes the functional differences among the SiI9033, the SiI9133, and the SiI9135/SiI9135A receivers.

Table 1. Summary of New Features

Feature	SiI9033	SiI9133	SiI9135/SiI9135A
HDMI Input nnections			
TMDS Input Ports	2	2	2
lor Depth	8-bit	8/10/12-bit	8/10/12-bit
DDC Input Ports	2	2	2
Maximum TMDS Input Clock	165 MHz	225 MHz	225 MHz
Digital Video Output Ports	1	1	1
Maximum Output Pixel Clock	165 MHz.	165 MHz.	165 MHz.
Maximum Output Bus Width	24	36	36
Analog Video Output Ports	0	0	0
DSD Output	8 channel	8 channel	6 channel
Video Processing			
lor Space nverter	RGB to/from YcbCr	RGB to/from YcbCr	RGB to/from YcbCr
Pixel Clock Divider ^{2} **Digital Video Bus Mapping**	0.25, 0.5 swap Cb, Cr pins	0.25, 0.5 swap Cb, Cr pins	0.25, 0.5 swap Cb, Cr pins
Maximum Audio Sample Rate (Fs)			
2-channel (I S or S/PDIF)	192 kHz	192 kHz	192 kHz
8-channel (I^{2}S)	192 kHz	192 kHz	192 kHz
8-channel (DSD)	88.2 kHz	88.2 kHz	88.2 kHz (6 channel)
High Bit Rate Audio Support mpressed DTS-HD and Dolby True-HD	No	N o	Yes
Other Features			
MCLK Generation	No external nnection required.	No external nnection required	No external nnection required.
HDCP Repeater Support	Yes	Yes	Yes
Interlaced mat Detection Pin	Yes	Yes	Yes
TMDS R$_{\text{EXT\_SWING}}$	Not d	Not d	Not d
Package	144-pin TQFP ePad	404-pin BGA w/Heat Slug	144-pin TQFP ePad

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Pin Diagrams

Figure 2 shows the pin nnections the SiI9135 receiver in the 144-pin TQFP package. Individual pin functions are described in the Pin Descriptions section beginning on page 28. Packaging and pin assignments are identical the SiI9135A device.

Figure 2. Pin Diagram

Functional Description

The SiI9135/SiI9135A receiver provides a mplete solution receiving HDMI-mpliant digital audio and video. Specialized audio and video processing is available within the receiver to add HDMI capability to nsumer such as AV receivers. Figure 3 shows the receiver inrporated into a digital television. Figure 4 on the next page shows the functional blocks of the chip. The device supports two HDMI input ports.

Unless otherwise specified, all mentions of the SiI9135 receiver in this datasheet also refer to the SiI9135A receiver.
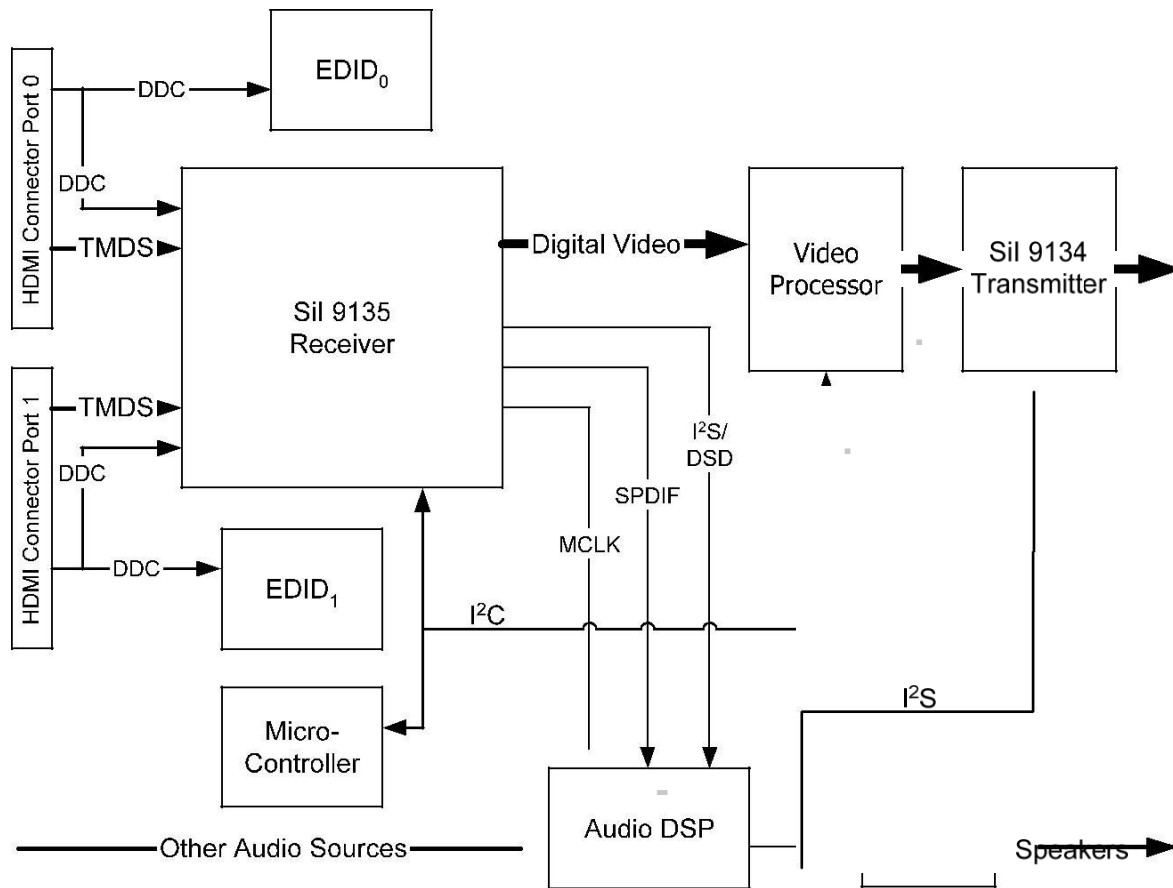
Figure 3. Digital Television Receiver Block Diagram

TMDS Digital res

The two TMDS digital res are the latest-generation res that have the ability to carry 10/12-bit lor depth. The res can receive TMDS data at up to 225 MHz. Each re perms 10-to-8 bit TMDS deding on the audio and video data received over the three TMDS differential data lines. The TMDS res can sense a stopped clock or stopped video, which allows the firmware to put the receiver into power-down mode.

Active Port Detection and Selection

one port can be active at a time. Active TMDS signals can arrive at both ports, but the ntrol of the HDMI receiver, one has circuitry enabled. Display firmware sets registers to ntrol this process.

Other ntrol signals are associated with the TMDS signals on each HDMI port. The HDMI receiver can monitor the +5 V supply from each attached host, poll the registers to check on which ports are nnected, and ntrol the nnection to one of the two E-DDC bs. An attached host determines the active status of an attached HDMI device by polling the E-DDC bus.

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Refer to the *SiI9125/9135 Programmers Reference*, listed in Table 31 on page 65, a mplete description of port detection and selection.
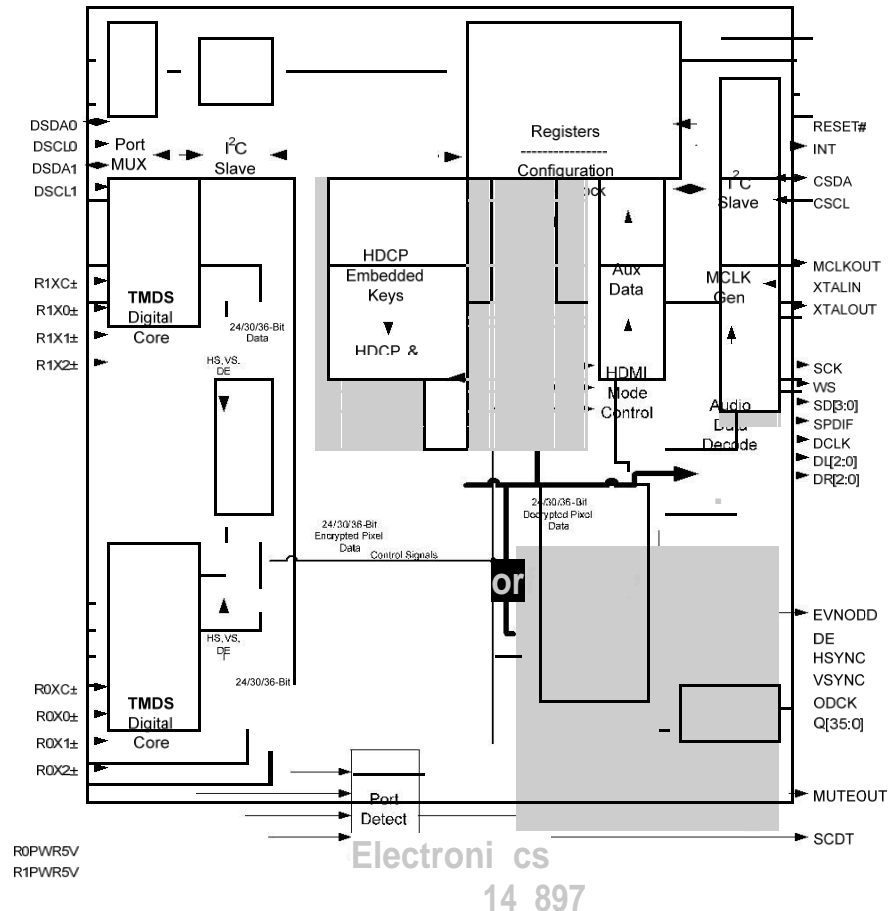
Figure 4. Functional Block Diagram

and writes over theDDC channel.The decryption process s pre-programmed HDCP keys and a Key Selection Vector

HDCP Decryption Engine and XOR Mask

The HDCP decryption engine ntains all the necessary logic to decrypt the inming audio and video data. The host-side microntroller or microprocessor ntrols the decryption process by perming a set sequence of register reads

(KSV) stored in the on-chip non-volatile memory. A value calculated from the keys is applied to an XOR mask

during each clock cycle to decryptthe audio and videodata.

The SiI9135/SiI9135A receiver also ntains all the necessary logic to support full HDCP repeaters. The KSV values of downstream devices (up to a total of 16) are written into the receiver through the local I^2C bus (CSDA/CSCL). As defined in the HDCP Specification, Vi′ is calculated and made available to the host on the DDC bus (DSDA/DSCL).

HDCP Embedded Keys

The SiI9135/SiI9135A HDMI receiver mes pre-programmed with a set of production HDCP keys. System manufacturers do not need to purchase key sets from the Digital-ntent LLC. All purchasing, programming, and security the HDCP keys is handled by . The pre-programmed HDCP keys provide the highest level of security, beca the keys cannot be read out of the device after they are programmed. Bee receiving samples of the SiI9135/SiI9135A receiver, customers must sign the HDCP license agreement (www.digital-cp.m) or a special with .

Data Input and nversion

Mode ntrol Logic

The mode ntrol logic determines if the decrypted data is video, audio, or auxiliary inmation and directs it to the appropriate logic block.

Video Data nversion and Video Output

The HDMI receiver can provide video in many different mats (see Table 2) and can process the video data bee it is output, as shown in Figure 5. Setting appropriate register bits allows each of the processing blocks to be bypassed.

Table 2. Digital Video Output mats

lor Space	Video mat	Bus Width	HSYNC/ VSYNC	Output Clock (MHz) 480i/576i[2, 3]	480p	XGA	720p	1080i	SXGA	1080p	Notes
RGB	4:4:4	36	Separate	27	27	65	74.25	74.25	108	148.5	—
		30	Separate	27	27	65	74.25	74.25	108	148.5	—
		24	Separate	27	27	65	74.25	74.25	108	148.5	—
		12/15/18	Separate	27	27	65	74.25	74.25	—	—	4
YCbCr	4:4:4	36	Separate	27	27	65	74.25	74.25	108	148.5	—
		30	Separate	27	27	65	74.25	74.25	108	148.5	—
		24	Separate	27	27	65	74.25	74.25	108	148.5	—
		12/15/18	Separate	27	27	65	74.25	74.25	—	—	4
	4:2:2	16/20/24	Separate	27	27	—	74.25	74.25	—	148.5	—
		16/20/24	Embedded	27	27	—	74.25	74.25	—	148.5	1
		8/10/12	Separate	27	54	—	148.5	148.5	—	—	—
		8/10/12	Embedded	27	54	—	148.5	148.5	—	—	1

Notes:

1. Embedded syncs SAV/EAV ding.
2. 480i and 576i modes can provide a 13.25 MHz clock using the clock divider.
3. Output clock frequency depends on programming of registers.Differential TMDS clock is always faster than 25 MHz.
4. Output clock supports 12/15/18-bit mode by using both edges.

lor Range Scaling

The lor range depends on the video mat that is described by the CEA-861B specification. In some applications the 8-bit input range s the entire span of 0x00 (0) to 0xFF (255) values. In other applications the range is scaled narrower.

The receiver cannot detect the inmingvideo data range and there is no required range specified in the HDMI AVI packet. The HDMI receiver selects the lor rangescaling based on the detected video mat. Both 10- and 12-bit

scaling are handled the same way. Refer to the *SiI9125/SiI9135 Programmers Reference* more inmation.

When the HDMI receiver output mat includes embedded   syncs (SAV/EAV des), it also limits the YCbCr data output values from 1 to 254.

Up Sample / Down Sample

Additional logic can nvert from 4:2:2 to 4:4:4 (8/10/12-bit) or from 4:4:4 to 4:2:2 YCbCr mat. All processing is done with 14 bits of accuracy true 12-bit data.

Deep-lor Packetizing and Un-packetizing

The SiI9135/SiI9135A HDMI receiver perms the nversion from the10/12-bit Deep lor video input data to 8-bits by increasing the TMDS clock frequency and packing the extra bits into the next byte, as described in the HDMI specification. The receiver unpacks the Deep lor data and places it on the 10/12-bit video bus.
 24-bit (8 bit-per-pixel) inputs, the TMDS clock frequency on the HDMI link equals the output pixel clock frequency
30-bit (10 bit-per-pixel) inputs, the TMDS clock frequency on the HDMI link is 1.25 times the output pixel clock frequency.

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36-bit (12 bit-per-pixel) inputs, the TMDS frequency clock on the HDMI link is 1.5 times the output pixel clock frequency.

lor Space nversion

RGB to YCbCr The RGB→YCbCr lor space nverter (CSC) can nvert from video data RGB to stard definition (ITU.601) or to high definition (ITU.709) YCbCr mats. The HDMI AVI packet defines the lor space of the inming video.

Table 3. lor Space versus Video mat

Video mat	nversion	mulae
		CE Mode 16-235 RGB
640 x 480	ITU-R BT.601	
480i	ITU-R BT.601	
576i	ITU-R BT.601	$Y = 0.299R' + 0.587G' + 0.114B'$
480p	ITU-R BT.601	$Cb = -0.172R' - 0.339G' + 0.511B' + 128$
576p	ITU-R BT.601	$Cr = 0.511R' - 0.428G' - 0.083B' + 128$
240p	ITU-R BT.601	
288p	ITU-R BT.601	
720p	ITU-R BT.709	$Y = 0.213R' + 0.715G' + 0.072B'$
1080i	ITU-R BT.709	$Cb = -0.117R' - 0.394G' + 0.511B' + 128$
1080p	ITU-R BT.709	$Cr = 0.511R' - 0.464G' - 0.047B' + 128$

YCbCr to RGB The YCbCr→RGB lor space nverter can interface to MPEG deders with RGB- inputs. The CSC can nvert from YCbCr in stard- definition (ITU.601) or high-definition (ITU.709) to RGB. Refer to the detailed mulas in Table 4. Note the difference between RGB range CE modes and PC modes.

Table 4. YCbCr-to-RGB lor Space nversion mulas

RGB Output Bits	nversion	YCbCr Input lor Range
YCbCr 16-235 Input to RGB 16-235 Output	601	$R' = Y + 1.371(Cr - 128)$ $G' = Y - 0.698(Cr - 128) - 0.336(Cb - 128)$ $B' = Y + 1.732(Cb - 128)$
	709	$R' = Y + 1.540(Cr - 128)$ $G' = Y - 0.459(Cr - 128) - 0.183(Cb - 128)$ $B' = Y + 1.816(Cb - 128)$
YCbCr 16-235 Input to RGB 0-255 Output	601	$R' = 1.164((Y - 16) + 1.371(Cr - 128))$ $G' = 1.164((Y - 16) - 0.698(Cr - 128) - 0.336(Cb - 128))$ $B' = 1.164((Y - 16) + 1.732(Cb - 128))$
	709	$R' = 1.164((Y - 16) + 1.540(Cr - 128))$ $G' = 1.164((Y - 16) - 0.459(Cr - 128) - 0.183(Cb - 128))$ $B' = 1.164((Y - 16) + 1.816(Cb - 128))$

Default Video nfiguration

A hardware RESET nfigures the receiver chip to its default mode, summarized in Table 5. more details and a mplete register listing, refer to the *SiI9125/SiI9135 Programmers Reference*.

Table 5. Default Video Processing

Video ntrol	Default after Hardware Reset	Note
HDCP Decryption	HDCP decryption is OFF	*
lor Space nversion	No lor space nversion	*
lor Space Selection	BT.601 selected	—
lor Range Scaling	No range scaling	*
Upsampling/Downsampling	No upsampling or downsampling	—
HSYNC & VSYNC Timing	No inversions of HSYNC or VSYNC	—
Data Bit Width	s 8-bit data	*
Pixel Clock Replication	No pixel clock replication	*
Power Down	Everything is powered down	—

*Note: The HDMI receiver assumes DVI mode (RGB 24-bit 4:4:4 video with 0:255 range) after reset.
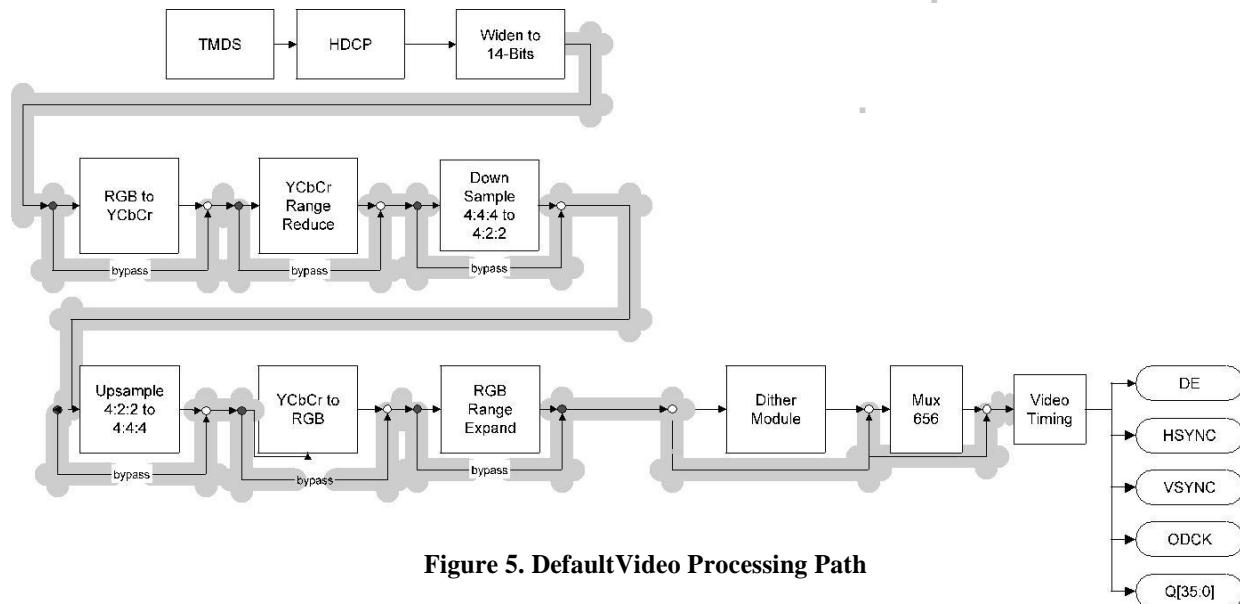
Figure 5. DefaultVideo Processing Path

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Automatic Video nfiguration

The SiI9135/SiI9135A receiver provides automatic video nfiguration to simplify updating the video path whenever the inming video changes mat. Bits in the HDMI Auxiliary Video Inmation (AVI) InfoFrame reprogram the registers in the video path.

Table 6. AVI InfoFrame Video Path Details

AVI Byte 1 Bits [6:5]		AVI Byte 2 Bits [7:6]		AVI Byte 5 Bits [3:0]	
Y[1:0]	lor Space	C[1:0]	lorimetric	PR[3:0]	Pixel Repetition
00	RGB 4:4:4	00	No Data	0000	No repetition
01	YCbCr 4:4:4	01	ITU 601	0001	Pixel sent 2 times
10	YCbCr 4:2:2	10	ITU 709	0010	Pixel sent 3 times
11	Future	11	Future	0011	Pixel sent 4 times
				0100	Pixel sent 5 times
				0101	Pixel sent 6 times
				0110	Pixel sent 7 times
				0111	Pixel sent 8 times
				1000	Pixel sent 9 times
				1001	Pixel sent 10 times

Notes:

1. The Auto Video nfiguration assumes that the AVI inmation is accurate. If inmation is not available, then the receiver must choose the video path based on measurement of the inming resolution.
2. Refer to EIA/CEA-861B Specification details.
3. The receiver can support pixel replication modes 0b0000, 0b0001, and 0b0011. Other modes are unsupported and can result in unpredictable behavior.

Output modes are specified using the OutMode register. Other modes are reserved.   future expansion.

Table 7. OutMode Programming

OutMode[7:0]	Digital Output				
	lor	Width		MUX	Sync
0b00000000	RGB	4:4:4	36	N	Sep.
0b00000010	RGB	4:4:4	36	N	Sep.
0b00000100	RGB	4:4:4	36	N	Sep.
0b00000110	RGB	4:4:4	36	N	Sep.
0b00000001	RGB	4:4:4			36NSep.
0b00000011	RGB	4:4:4	36	N	Sep.
0b00000101	RGB	4:4:4	36	N	Sep.
0b00000111	RGB	4:4:4	36	N	Sep.
0b10000000	YCbCr	4:4:4	36	N	Sep.
0b10000010	YCbCr	4:4:4	36	N	Sep.
0b10000100	YCbCr	4:4:4	36	N	Sep.
0b10000110	YCbCr	4:4:436		N	Sep.
0b10000001	YCbCr	4:4:4	36	N	Sep.
0b10000011	YCbCr	4:4:4	36	N	Sep.
0b10000101	YCbCr	4:4:4	36	N	Sep.
0b10000111	YCbCr	4:4:4	36	N	Sep.
0b11000000	YCbCr	4:2:2	8	N	Sep.
0b11001000	YCbCr	4:2:2	10	N	Sep.
0b11100000	YCbCr	4:2:2	8	Y	Sep.
0b11101000	YCbCr	4:2:2	10	Y	Sep.
0b11110000	YCbCr	4:2:2	8	Y	Emb.
0b11111000	YCbCr	4:2:2	10	Y	Emb.

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Audio Data Output Logic

The SiI9135/SiI9135A receiver provides digital audio output over S/PDIF, four I^2S ports, or eight one-bit audio ports.

S/PDIF

The S/PDIF stream can carry 2-channel unmpressed PCM data (IEC 60958) or a mpressed bit stream multi-channel (IEC 61937) mats. The audio data capture logic ms the audio data into packets acrding to the HDMI specification. The S/PDIF output supports audio sampling rates from 32 to 192 kHz. A separate master clock output (MCLK), herent with the S/PDIF output, is provided time-stamping purposes. *herent* means that the MCLK and S/PDIF are created from the same clock source. This is usually done by using the original MCLK to strobe out the S/PDIF from the sourcing chip. There is no setup or hold timing requirement on an output with respect to MCLK.

I^2S

Four I^2S outputs allow transmission of DVD-Audio or deded Dolby Digital to AV receivers and high-end displays. The interface supports up to 8-channels at 192 kHz. Signals on the I^2S output pins must also be *herent* with MCLK. The appropriate registers must be nfigured to describe the mat of the audio input to the device. The CEA-861B Audio Info (AI) packet passes this inmation over the HDMI link.

MCLK frequencies support various audio sample rates as shown in Table 8.

Table 8. Supported MCLK Frequencies

Multiple of Fs	Audio Sample Rate, Fs						
	I^2S and S/PDIF Supported Rates						
	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.864 MHz	36.864 MHz		
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz		

Note: An Fs multiple of 512 is not supported in S/PDIF mode.

One-Bit Audio Input (DSD/SACD)

Direct Stream Digital (DSD) is an audio data mat defined Super Audio CD (SACD) applications. It nsists of

audio sources provide MCLK. One-bit Audio supports 64 • Fs, with Fsbeing either 44.1 kHz or 88.2 kHz.

ly, the one-bit audio inputs are sampled on the positive edge of the DSD clock, assembled into 56-bit packets, and then mapped to the appropriate FIFO. The SiI9135/SiI9135A receiver generates a *static one-bit audio detect*

interrupt if it receives 28nsecutivezeros or ones, and an *invalid one bit audio detect* interrupt if it receives more than 24 zeros or ones out of 28 bits. one-bit audio,the Audio InfoFrame, instead of the Channel Status bits, carries the sampling inmation.

High-Bitrate Audio on HDMI

The new high-bitrate mpressed stards, such as DTS-HD and Dolby TrueHD transmit data at bitrates as high as 18 to 24 Mbps. Beca these bitrates are so high, source devices and sink devices must carry the data using four I^2S lines rather than a single very-high-speed S/PDIF or I^2S bus (refer to Figure 6).
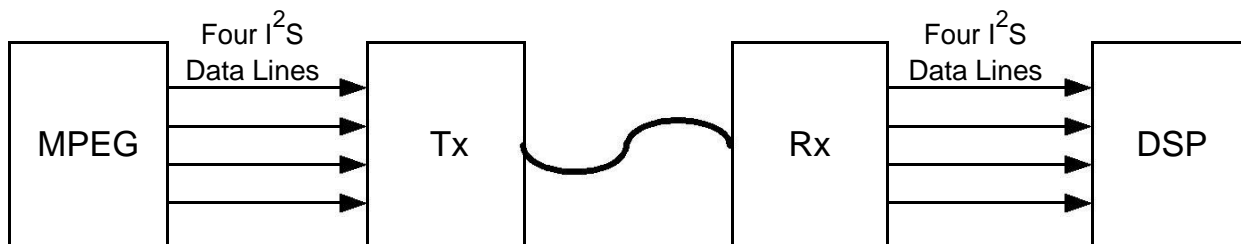
Figure 6: High Speed Data Transmission

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The high-bitrate audio stream is originally ended as a single stream. To send it over four I^{2}S lines, the DVD deder splits it into four streams. Beca the single stream of data is being sent over four lines, the programmable Audio Clock Regeneration (ACR) rate is now four times the 96 kHz or the 192 kHz sample rate, that is, 384 kHz or 768 kHz, respectively.

Figure 7 shows the high bitrate stream bee it is split into four I^{2}S lines and after it is reassembled. Figure 8 shows the same high bitrate audio stream after it is split into four I^{2}S lines.
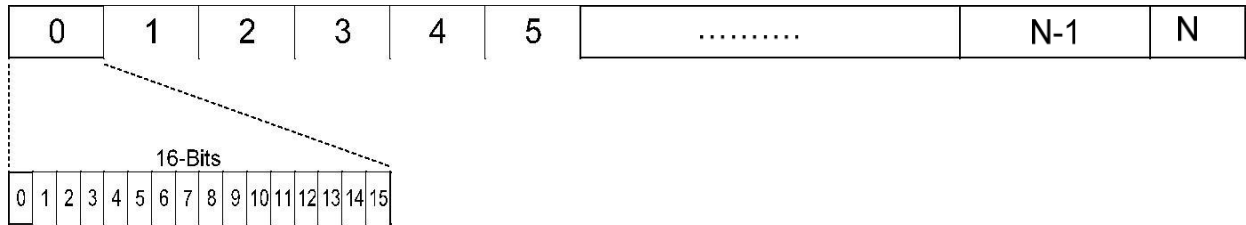
Figure 7: High Bitrate Stream Bee and After Reassembly and Splitting
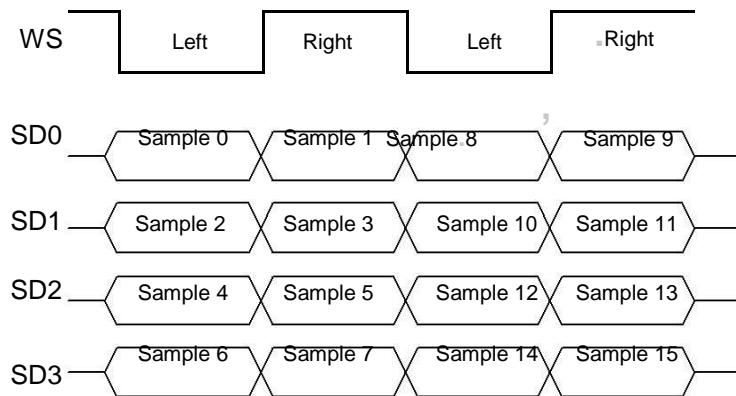
Figure 8. High Bitrate StreamAfter Splitting

Table 9. Maximum Audio Sampling Frequency All Video mat Timings

Description	mat Timing	Pixel Repetition	Vertical Freq. (Hz)	Max Fs 8 ch (kHz)			Max Fs 2 ch (kHz)
				4:2:2 and 4:4:4 24-bit	4:4:4 Deep lor (depth in bits)		
60 Hz mats				**Stard**	**10**	**12**	
VGA	640x480p	none	59.94/60	48	48	48	192
480i	1440x480i	2	59.94/60	48	48	48	192
480i	2880x480i	4	59.94/60	192	192	192	192
240p	1440x240p	2	59.94/60	48	48	48	192
240p	2880x240p	4	59.94/60	192	192	192	192
480p	720x480p	none	59.94/60	48	48	48	192
480p	1440x480p	2	59.94/60	96	96	96	192
480p	2880x480p	4	59.94/60	192	192	192	192
720p	1280x720p	none	59.94/60	192	192	192	192
1080i	1920x1080i	none	59.94/60	192	192	192	192
1080p	1920x1080p	none	59.94/60	192	192	192	192
50 Hz mats				**Stard**	**10**	**12**	
576i	1440x576i	2	50	48	48	48	192
576i	2880x576i	4	50	192	192	192	192
288p	1440x288p	2	50	48	48	48	192
288p	2880x288p	4	50	192	192	192	192
576p	720x576p	none	50	48	48	48	192
576p	1440x576p	2	50	96	96	96	192
576p	2880x576p	4	50	192	192	192	192
720p/50	1280x720p	none	50	192	192	192	192
1080i/50	1920x1080i	none	50	192	192	192	192
1080p/50	1920x1080p	none	50	192	192	192	192
1080p @ 24-30 Hz				**Stard**	**10**	**12**	
1080p	1920x1080p	none	24		192	192	192
1080p	1920x1080p	none	25	192	192	192	192
1080p	1920x1080p	none	29.97/30	192	192	192	192

Auto Audio nfiguration

ECC, ACR, PLL, InfoFrame, and HDMI. Audio output is enabled when all necessary nditions are met. If any

critical ndition is missing, the audio output is automatically   disabled.

Soft Mute

On mmand from a register bit or when triggered with the Automatic Audio ntrol (AAC), the receiver gradually reduces the audio data amplitude to mute the sound. This prevents an audible pop from being sent to the I^2S, S/PDIF, or DSD outputs when there is an error or an interruption to the HDMI audio stream.

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ntrol and nfiguration

Register/nfiguration Logic

The register/nfiguration logic block inrporates all the registers required nfiguring and managing the features of the SiI9135/SiI9135A receiver. These registers perm HDCP authentication, process audio, video, and auxiliary mats, mat CEA-861B InfoFrame Packets, and ntrol power-down modes.

These registers are accessible from one of two serial ports. The first port is the DDC port nnected through the HDMI cable to the HDMI host. It is d to ntrol the receiver from the host device HDCP operation. The send port is the local I^2C port, which is d to ntrol the chip from the display device. The Local Bus accesses the General Registers and the mmon Registers. The DDC Bus accesses the HDCP Operation registers and the mmon Registers. Figure 9 shows the relationship between the ports and registers accessible from them.
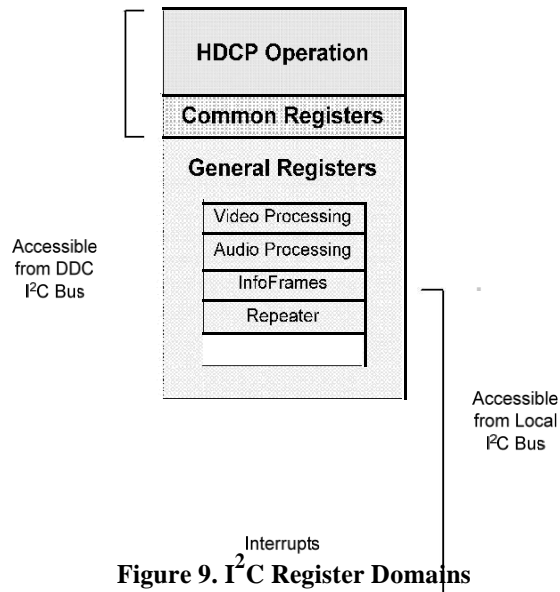
Figure 9. I^2C Register Domains

Serial Ports

The HDMI receiver provides three 5 V tolerant serial interfaces: two DDC ports to mmunicate with the HDMI or DVI

hosts, and one I^2C port initialization and ntrol by a local microntroller in the display. The receiver is accessible

on the local I ^{2} C bus at two device addresses. Refer to the *SiI9125/SiI9135 Programmers Reference* more inmation.

100 kHz. Each interfacennects to one E-DDC bus and is d HDCP authentication.

E-DDC Bus Interface to HDMI Host

The two DDC slave interfaces (DSDA0/DSCL0 and DSDA1/DSCL1) on the device are capable of running up to
The receiver is accessible on the E-DDCbus at device address 0x74, as required by the HDCP Specification.

I₂C Interface to Displayntroller

The ntroller I^2C slave interface (CSDA, CSCL) on the chip can run at up to 400 kHz. This bus is d to nfigure the receiver by reading from and writing to the appropriate registers.

Electrical Specifications

Absolute Maximum nditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O Pin supply voltage	−0.3	—	4.0	V	1, 2, 3
AVCC18	TMDS PLL #0 supply voltage	−0.3	—	2.5	V	1, 2
AVCC33	TMDS analog supply voltage	−0.3	—	4.0	V	1, 2
DVCC18	Audio PLL supply voltage	−0.3	—	2.5	V	1, 2, 3
CVCC18	Digital re supply voltage	−0.3	—	2.5	V	1, 2, 3
XTALVCC	ACR PLL crystal oscillator supply voltage	−0.3	—	4.0	V	1, 2
REGVCC	ACR PLL regulator supply voltage	−0.3	—	4.0	V	1, 2
V_I	Input voltage	−0.3	—	IOVCC33 + 0.3	V	1, 2
$V_{5V\text{-Tolerant}}$	Input voltage on 5 V tolerant pins	−0.3	—	5.5	V	5
T_J	Junction temperature	—	—	125	°C	—
T_{STG}	Storage temperature	−65	—	150	°C	—

Notes:

1. Permanent device damage can occur if absolute maximum nditions are exceeded.

2. Functional operation should be restricted to the nditions described Normal Operating nditions.
3. Voltage shoot or overshoot cannot exceed absolute maximum nditions.
4. Refer to the SiI9135/SiI9135A Qualification Report inmation onESD permance.

5. _____

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Normal Operating nditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
IOVCC33	I/O pin supply voltage	3.15	3.3	3.45	V	1, 4
AVCC33	TMDS analog supply voltage	3.0	3.3	3.6	V	1, 7
AVCC18	TMDS analog supply voltage	1.62	1.8	1.98	V	3, 5
CVCC18	Digital re supply voltage	1.62	1.8	1.98	V	2
DVCC18	ACR supply voltage	1.62	1.8	1.98	V	—
XTALVCC	ACR PLL crystal oscillator supply voltage	3.0	3.3	3.6	V	4
REGVCC	ACR PLL regulator supply voltage	3.0	3.3	3.6	V	4, 5
R0PWR5V R1PWR5V	DDC I^{2}C I/O reference voltage	—	5.00	—	V	10
DIFF33	Difference between two 3.3 V power pins	—	—	1.0	V	4
DIFF18	Difference between two 1.8 V power pins	—	—	1.0	V	4
DIFF3318	Difference between any 3.3 V and 1.8 V Pins	−1.0	—	2.0	V	4, 6
V_{CCN}	Supply voltage noise	—	—	100	mV$_{P-P}$	8
T_A	Ambient temperature (with power applied)	0	25	70	°C	—
Θ_{ja}	Ambient thermal resistance (Theta JA)	—	—	27	°C/W	9

Notes:
1. IOVCC33 and AVCC33 pins should be ntrolled from one power source.
2. CVCC18 should be ntrolled from one power source.

3. AVCC18 pin should be regulated.
4. Power supply sequencing must guarantee that power pins stay within these limits of each other. See Figure 13.

5. REGVCC is ly regulated to 1.8 V and ntrols the audio PLL. DVCC18 supplies the audio PLL logic.
6. No 1.8 V pin can be more than DIFF3318[min] higher than any 3.3 V pin. No 3.3 V pin can be more than DIFF3318[max] higher than any 1.8 V pin.

7. The HDMI Specification requires termination voltage (AVCC33) to be ntrolled to 3.3 V ±5%. The SiI9135/SiI9135A receiver tolerates a wider range of ±300 mV.
10. 5 V tolerant
8. The supply voltage noise is measured at test point VCCTP in Figure 22 on page 31. The ferrite bead provides filtering of power supply noise. The figure is representative and applies other VCC pins as well.

9. Airflow at 0 m/s.

The schematics on page 57 show deupling and power supply regulation.

DC Specifications

Digital I/O Specifications

Symbol	Parameter	Pin Type[3]	nditions[2]	Min	Typ	Max	Units	Note
V$_{IH}$	HIGH-level input voltage	LVTTL	—	2.0	—	—	V	—
V$_{IL}$	LOW-level input voltage	LVTTL	—	—	—	0.8	V	—
V$_{TH+}$	LOW to HIGH threshold RESET # Pin	Schmitt	—	1.46	—	—	V	5
V$_{TH-}$	HIGH to LOW threshold RESET# Pin	Schmitt	—	—	—	0.96	V	5
DDC V$_{TH+}$	LOW to HIGH threshold DSDA0, DSDA1, DSCL0, and DSCL1 pins.	Schmitt	—	3.0	—	—	V	—
DDC V$_{TH-}$	HIGH to LOW threshold DSDA0, DSDA1, DSCL0, and DSCL1 pins.	Schmitt	—	—	—	1.5V	V	—
Local I2C V$_{TH+}$	LOW to HIGH threshold CSCL and CSDA pins	Schmitt	—	2.1	—	—	V	11, 13
	HIGH to LOW threshold CSCL and CSDA pins		VOUT = 0.4 V	4	—	—	mA	1, 6, 7
V$_{OH}$	HIGH-level output voltage	LVTTL	—	2.4	—	—	V	10
V$_{OL}$	LOW-level output voltage	LVTTL	—	—	—	0.4	V	10
I$_{OL}$	Output leakage Current	—	High impedance	–10	—	10	µA	—
V$_{ID}$	Differential input voltage	—	—	75	250	780	mV	4
I$_{OD4}$	4 mA digital output drive	Output	VOUT = 2.4 V	4	—	—	mA	1, 6, 7
			VOUT = 0.4 V	8	—	—	mA	1, 6, 8
I$_{OD12}$	12 mA digital outputdrive	Output	VOUT = 2.4 V	12	—	—	mA	1, 6, 9
			VOUT = 0.4 V	12	—	—	mA	1, 6, 9
R$_{PD}$	pull down resistor	Outputs	IOVCC33 = 3.3 V	25	50	110	KΩ	1, 12
I$_{OPD}$	Output pull down current	Outputs	IOVCC33 = 3.45 V	—	60	90	µA	1, 12
I$_{IPD}$	Input pull down current	Input	IOVCC33 = 3.45 V	—	60	90	µA	1

1.   These limits are guaranteed by design.
2.   normal operating nditions unless otherwise specified, including output pin loading C$_L$ = 10 pF.
3.   Refer to the Pin Descriptions section (beginning on page 28) pin type designations all package pins.
4.   Differential input voltage is a single-ended measurement, acrding to the DVI Specification.
5.   Schmitt trigger input pin thresholds V$_{TH+}$ and V$_{TH-}$ rrespond to V$_{IH}$ and V$_{IL}$, respectively.
6.   Minimum output drive specified at ambient = 70 °C and IOVCC33 = 3.0 V. Typical output drive specified at ambient = 25 °C and IOVCC33 = 3.3 V. Maximum output drive specified at ambient = 0 °C and IOVCC33 = 3.6 V.
7.   The I$_{OD4}$ output applies to pins SPDIF, SCK, WS, SD[3:0], DCLK, INT, and CSDA.
8.   The I$_{OD8}$ output applies to pins DE, HSYNC, VSYNC, Q[35:0], and MCLK.
9.   The I$_{OD12}$ output applies to pin ODCK.
10. Note that the S/PDIF output drives LVTTL levels, not the low-swing levels defined by IEC958.
11. The SCL and SDA pins are not true open-drain buffers. When no VCC is applied to the chip, these pins can ntinue to draw a small current and prevent the host ntroller from mmunicating with other devices on the I^{2}C bus. Theree, do not power-down the receiver (remove VCC) unless the attached I^{2}C bus is mpletely idle.
12. The chip includes an pull-down resistor on many of the output pins. When tri-stated, these pins draw a pull down current acrding to this specification when the signal is driven HIGH by another source device.

13. With a tolerance of -10% on the IOVCC33 supply, the HIGH-to-LOW threshold on DDC and I^2C bus is marginal.   remmends a -5% tolerance on the IOVCC33 power supply.

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DC Power Supply Pin Specifications

Total Power versus Power-Down Modes

Symbol	Parameter	Mode	Frequency	Typ[3]		Max[4]		Units	Notes
				3.3 V	1.8 V	3.3 V	1.8 V		
I$_{PDQ3}$	mplete power-down current	A	X	—	—	4	< 1	mA	1, 6
I$_{PDS}$	Sleep power-down current	B	27 MHz	—	—	5	4	mA	2, 7
			74.25 MHz	—	—	6	4	mA	
			150 MHz	—	—	4	4	mA	
			225 MHz	—	—	7	5	mA	
I$_{STBY}$	Standby current	C	27 MHz	—	—	13	6	mA	2, 8
			74.25 MHz	—	—	13	6	mA	
			150 MHz	—	—	11	6	mA	
			225 MHz	—	—	11	6	mA	
I$_{UNS}$	Unselected current	D	27 MHz	15	25	19	33	mA	2, 9
			74.25 MHz	17	27	21	34	mA	
			150 MHz	16	28	18	36	mA	
			225 MHz	18	30	23	39	mA	
I$_{CCTD}$	Full power digital out current	E	27 MHz	81	76	105	88	mA	2, 10
			74.25 MHz	100	160	165	181	mA	
			150 MHz	123	279	247	337	mA	
			225 MHz	139	394	316	472	mA	

Notes:

1. Power is not related to input TMDS clock frequency beca the selected TMDS port is powered down.
2. Power is related to input TMDS clock frequency at the selected TMDS port. one port can be selected.

3. Typical power specifications measured with supplies at typical normal operating nditions and a video pattern that mbines

   gray scale, checkerboard, and text.
8. Power-down ModeC: Powersdown re logic, ACR PLL, and output pins. HDCP does not ntinue. Interrupts disabled. INT
   temperature, and a video pattern of single-pixel vertical lines.

5. Registers are always accessible on local I^{2}C (CSDA/CSCL) without an active link clock.
6. Power-down Mode A: Everything is powered off. The host sees no termination of TMDS signals at either TMDS port. I^{2}C access
   is still available.
   pin show state of SCDT the selectedTMDS port.
7. Power-down Mode B: Powers down as in Mode C, but also powers down SCDT logic. The CKDT state can be polled in the
   registers, but interrupts and the INT output pin are inactive. The host device can sense TMDS termination.

9. Power-down Mode D: Monitor SCDT on selected TMDS port with outputs in the high-impedance state. HDCP ntinues in the
   selected port, but theoutput of the HDMI receiver can be nnected to a shared bus.
10. Digital Functional Mode E: Full operation on one port with digital outputs.

Power Down Mode Definitions

	Mode	PDTOT#	PD_12CH#	PD Clks[1]	PD Outs[2]	PD#	Description
				Bit States			
A	Power Down	0	X	X	X	X	Minimum power. Everything is powered off. The host sees no termination of TMDS signals at either TMDS port. I^{2}C access is still available.
B	Sleep Mode Power	1	0	0	X	0	Powers down as in Mode C, but also powers down SCDT logic. The CKDT state can be polled in the registers, but interrupts and the INT output pin are inactive. The host device can sense TMDS termination.
C	Standby Power	1	1	1	1	0	Powers down re logic, ACR PLL, and output pins. HDCP does not ntinue. Interrupts disabled. INT pin show state of SCDT the selected TMDS port.
D	Unselected Power	1	1	1	0	1	Monitor SCDT on selected TMDS port with outputs in the high-impedance state. HDCP ntinues in the selected port, but the output of the HDMI receiver can be nnected to a shared bus.
E	Digital	1	1	1	1	1	Full operation on one port with digital outputs.

Notes:
1. PD Clks includes the PD_MCLK#, PD_XTAL#, PD APLL#, and PD PCLK# pins, and all are set to zero.
2. PD Outs includes the PD_AO# and PD_VO#, and both are set to zero.

AC Specifications

TMDS Input Timings									
T$_{DPS}$	Intra-pair differential input skew	—	—	—	0.6		T$_{BIT}$	—	2, 4
T$_{CCS}$	Channel to channel differential input skew	—	—	—	0.2T$_{PIXEL}$	+ 1.78	ns	Figure 12	2, 3
F$_{RXC}$	Differential input clock frequency	—	25	—	225		MHz	—	—
T$_{RXC}$	Differential input clock period	—	4.44	—	40		ns	—	—
	Differential input clock jitter tolerance								

Notes:
1. normal operating nditions unless otherwisespecified, including output pin loading of C$_L$ = 10 pF.
2. Guaranteed by design.
3. IDCK Period (see applicable HDMI Transmitter Data Sheet).
4. 1/10 of IDCK Period (see applicable HDMI Transmitter Data Sheet).
5. Jitter is defined acrding to the HDMI Specification
6. Jitter is measured with Clock Revery Unit per HDMI Specification. Actual jitter tolerance can be higher depending on the frequency of the jitter.

Refer to the *SiI9125/SiI9135 Programmers Reference* more details on ntrolling timing modes.

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Video Output Timings

12/15/18-Bit Data Output Timings

Symbol	Parameter	nditions	Min	Typ	Max	Units	Figure	Notes
D_{LHT}	LOW-to-HIGH rise time transition	$C_L = 10$ pF	—	—	3	ns	Figure 15	2
D_{HLT}	HIGH-to-LOW fall time transition	$C_L = 10$ pF	—	—	3	ns	Figure 15	2
R_{CIP}	ODCK cycle time	$C_L = 10$ pF	13	—	40	ns	Figure 16	8
F_{CIP}	ODCK frequency	$C_L = 10$ pF	25	—	82.5	MHz		5
T_{DUTY}	ODCK duty cycle	$C_L = 10$ pF	40%	—	60%	R_{CIP}	Figure 16	3
T_{CK2OUT}	Clock-to-output delay (OCLKINV = 0)	$C_L = 10$ pF	0.8	—	3.8	ns	Figure 16	—
	Clock-to-Output Delay (OCLKINV = 1)		1.0	—	3.8	ns		

16/20/24/30/36-Bit Data Output Timings

Symbol	Parameter	nditions	Min	Typ	Max	Units	Figure	Notes
D_{LHT}	LOW-to-HIGH rise time transition	$C_L = 10$ pF	—	—	3	ns	Figure 15	2
D_{HLT}	HIGH-to-LOW fall time transition	$C_L = 10$ pF	—	—	3	ns	Figure 15	2
T_{DUTY}	ODCK duty cycle	$C_L = 10$ pF	40%	—	60%	R_{CIP}	Figure 16	3
T_{CK2OUT}	ODCK-to-output delay	$C_L = 10$ pF	0.92	—	2.9	ns	Figure 16	—
R_{CIP}	Output clock cycle time	$C_L = 10$ pF	6.06	—	40	ns	Figure 16	5, 8
F_{CIP}	Output clock frequency	$C_L = 10$ pF	25	—	165	MHz	Figure 16	5

Notes:

1. normal operating nditions unless otherwise specified, including output pin loading of $C_L = 10$ pF.

2. Rise time and fall time specifications apply to the HSYNC, VSYNC, DE, ODCK, EVNODD, and Q[35:0] pins.
3. Output clock duty cycle is independent of the differential input clock duty cycle. Duty cycle is a mponent of output setup and hold times.
4. See Table 16 on page 26 calculation of worst-case output setup and hold times.

5. All output timings are defined at the maximum operating ODCK frequency, F_{CIP}, unless otherwise specified.

6. F_{CIP} can be the same as F_{RXC} or one-half of F_{RXC}, depending on OCLKDIV setting. F_{CIP} can also be $F_{RXC} \div 1.25$ or $F_{RXC} \div 1.5$ if

   Deep lor mode is being transmitted.

7. R_{CIP} is the inverse of F_{CIP} and is not a ntrolling specification.
8. Output skew specified when ODCK is programmed to divide -by-two mode.

| Symbol | Parameter | nditions | Min | Typ | Max | Units | Figure | Notes |

Audio Output Timings

Table 10. I^{2}S Output Port Timings								
T_{HC}	SCK clock HIGH time	$C_L = 10$ pF	0.35	—	—	T_{tr}		1
T_{SU}	Setup time, SCK to SD/WS	$C_L = 10$ pF	$0.4T_{TR} - 5$	—	—	ns	Figure 17	1
T_{HD}	Hold time, SCK to SD/WS	$C_L = 10$ pF	$0.4T_{TR} - 5$	—	—	ns		1
$T_{SCKDUTY}$	SCK duty cycle	$C_L = 10$ pF	40%	—	60%	T_{tr}		1
T_{SCK2SD}	SCK to SD or WS delay	$C_L = 10$ pF	−5	—	+5	ns		2
T_{AUDDLY}	Audio pipeline delay	—	—	40	80	μs	—	—

Notes:

1. Refer to Figure 17. Meets timing required by the Philips I^{2}S Specification.
2. Applies also to SDC-to-WS delay.

Table 11. S/PDIF Output Port Timings

Symbol	Parameter	nditions	Min	Typ	Max	Units	Figure	Notes
T_{SPCYC}	S/PDIF cycle time	$C_L = 10$ pF	—	1.0		UI	Figure 18	1, 2
F_{SPDIF}	S/PDIF frequency	—	4	—	24	MHz		3
T_{SPDUTY}	SPDIF duty cycle	$C_L = 10$ pF	90%	—	110%	UI		2, 5
$T_{MCLKCYC}$	MCLK cycle time	$C_L = 10$ pF	20	—	250	ns	Figure 19	1, 2, 4
F_{MCLK}	MCLK frequency	$C_L = 10$ pF	4	—	50	MHz		1, 2, 4
$T_{MCLKDUTY}$	MCLK duty cycle	$C_L = 10$ pF	40%	—	60%	$T_{MCLKCYC}$		2, 4
T_{AUDDLY}	Audio pipeline delay	—	—	40	80	µs	—	—

Notes:
1. Guaranteed by design.
2. Proportional to unit time (UI), acrding to sample rate.
3. SPDIF is not a true clock, but is generated from the 128Fs clock, sample frequencies from 32 to 192 kHz.
4. MCLK refers to MCLKOUT.
5. Intrinsic jitter on S/PDIF output can limit its as an S/PDIF transmitter. The S/PDIF intrinsic jitter is approximately 0.1 UI.

Table 12. Audio Crystal Timings

Symbol	Parameter	nditions	Min	Typ	Max	Units	Figure	Notes
F_{XTAL}	External crystal freq.	—	26	27	28.5	MHz	Figure 10	1, 2
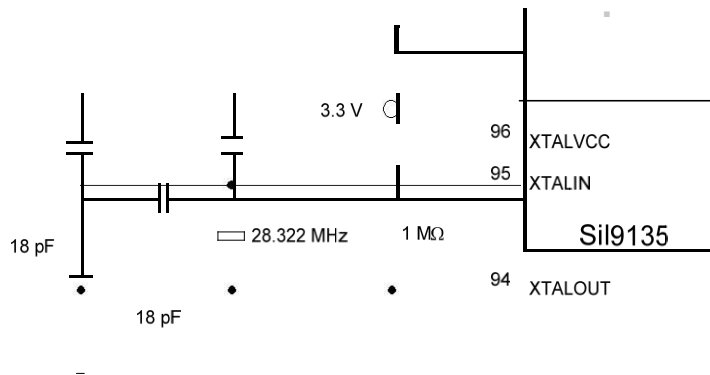
Figure 10. Audio Crystal Schematic the SiI9135/SiI9135A

Notes:
1. The HDMI receiver has been fully characterized optimum audio quality using 28.322 MHz. the crystal, Citizen part number CSA309-28.322MABJ or equivalent. A less expensive, but not fully characterized, circuit can a TTL-level clock source. Refer to the XTALIN Clock Requirement section on page 56 more inmation.
2. The XTALIN/XTALOUT pin pair must be driven with a clock in all applications.

Miscellaneous Timings

Table 13. Miscellaneous Timings

Symbol	Parameter	nditions	Min	Typ	Max	Units	Figure	Notes
T_{I2CDVD}	SDA data valid delay from SCL falling edge	$C_L = 400$ pF	—	—	700	ns	—	—
F_{DDC}	Speed on TMDS DDC ports	$C_L = 400$ pF	—	—	100	kHz	—	2
F_{I^2C}	Speed on local I^2C port	$C_L = 400$ pF	—	—	400	kHz	—	3
T_{RESET}	RESET# signal LOW time valid reset	—	50	—	—	µs	Figure 14	—
$T_{BKSVINIT}$	HDCP BKSV load time	—	—	—	2.2	ms	—	4

Notes:
1. normal operating nditions unless otherwise specified, including output pin loading of $C_L = 10$ pF.
2. DDC ports are limited to 100 kHz by the HDMI Specification, and meet I^2C stard-mode timings.
3. The local I^2C port (CSCL/CSDA) meets stard-mode I^2C timing requirements to 400 kHz.
4. The time required to load the KSV values to the HDMI receiver after a RESET#.

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Interrupt Timings

Table 14 Interrupt Output Pin Timings

Symbol	Parameter	nditions	Min	Typ	Max	Units	Figure	Notes
T_{FSC}	Link disabled (DE inactive) to SCDT LOW	—	—	0.15	40	ms	Figure 11	1, 2, 3, 8
T_{HSC}	Link enabled (DE active) to SCDT HIGH	—	—	—	4	DE	Figure 11	1, 2, 4, 8
T_{CICD}	RXC inactive to CKDT LOW	—	—	—	100	µs	Figure 11	1, 2, 8
T_{CACD}	RXC active to CKDT HIGH	—	—	—	10	µs	Figure 11	1, 2, 8
T_{INT}	Response time INT from input change	—	—	—	100	µs	—	1, 5, 8
T_{CIOD}	RXC inactive to ODCK inactive	—	—	—	100	ns	—	1, 8
T_{CAOD}	RXC active to ODCK active and stable	—	—	—	10	ms	—	1, 6, 8
T_{SRRF}	Delay from SCDT rising edge to Software Reset falling edge	—	—	—	100	ms	Figure 14	7

Notes:

1. Guaranteed by design.
2. SCDT and CKDT are register bits in this device.
3. SCDT changes to LOW after DE is HIGH approximately 4096 pixel clock cycles, or after DE is LOW approximately 1,000,000 clock cycles. With a 27 MHz pixel clock, the delay DE HIGH is approximately 150 µs, and the delay DE LOW is approximately 40 ms.
4. SCDT changes to HIGH when clock is active (T_{CACD}) and at least 4 DE edges have been regnized. At 720p, the DE period is 22 µs, so SCDT responds approximately 50 µs after TCACD.
    pin whenever SCDT changes from LOW toHIGH or from HIGH to LOW.
5. The INT pin changes state after a change in input ndition when the rresponding interrupt is enabled.
6. Output clock (ODCK) bemes active bee it bemes stable. the SCDTsignal as the indicator of stable video output

    timing, as this depends on deding of DE signals with active RXC (see T_{FSC}).
7. Software Reset must be asserted and then deasserted within the specified maximum time after rising edge of Sync Detect
    (SCDT). Access to both SWRST and SCDT can be limited by the speed of the I^2C nnection.
8. SCDT is HIGH when CKDT is also HIGH. When the HDMI receiver is in a powered-down mode, the INT output pin

    indicates the current state of SCDT. Theree, a powered-down HDMI receiver signals a microprocessor nnected to the INT
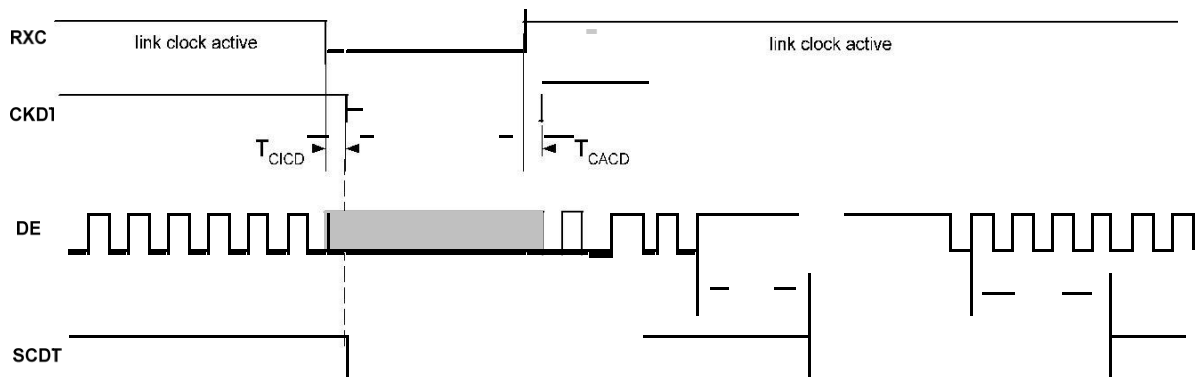
Figure 11. SCDT and CKDT Timing from DE or RXC Inactive/Active

Notes:

1. The SCDT shown in Figure 11 is a register bit. SCDT remains HIGH if DE is held LOW while RXC remains active, but SCDT changes to LOW if DE is held HIGH while RXC remains active.
2. The CKDT shown in Figure 11 is a register bit. CKDT changes to LOW whenever RXC stops, and changes to HIGH when RXC starts. SCDT changes to LOW when CKDT changes to LOW.
3. SCDT changes to LOW when CKDT changes to LOW. SCDT changes to HIGH at T_{HSC} after CKDT changes to HIGH.
4. The INT output pin changes state after the SCDT or CKDT register bit is set or cleared if those interrupts are enabled.

Refer to the *SiI9125/SiI9135 Programmers Reference* more details on ntrolling timing modes.

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Timing Diagrams

TMDS Input Timing Diagrams
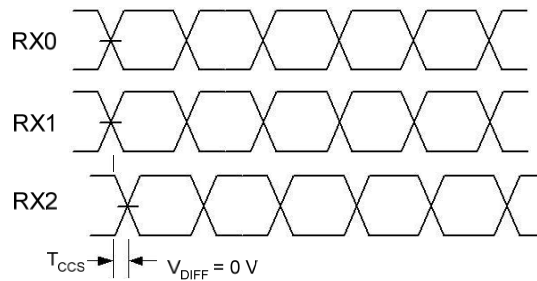
Figure 12. TMDS Channel-to-Channel Skew Timing

Power Supply ntrol Timing

Power Supply Sequencing
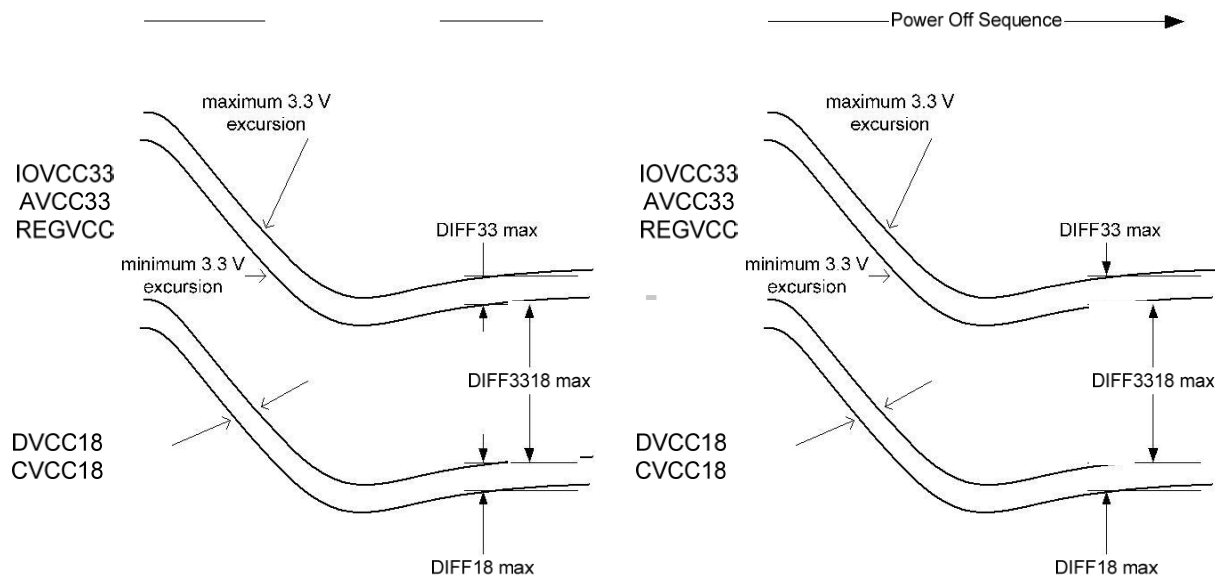
Figure 13. Power Supply Sequencing

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Reset Timings

RESET# must be pulled LOW T_{RESET} bee accessing registers.

This is be done by holding RESET# LOW until T_{RESET} after stable power (shown at left), OR by pulling RESET# LOW

from a HIGH state (shown above) at least T_{RESET}.
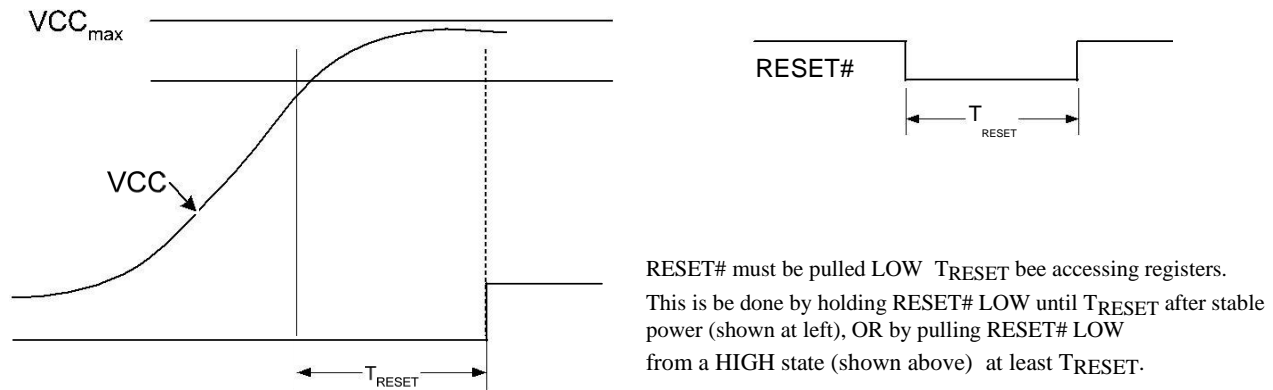
Note that VCC must be stable between its limits Normal

Operating nditions T_{RESET} bee RESET# goes HIGH.

Figure 14. RESET# Minimum Timings

Digital Video Output Timing Diagrams
Output Transition Times

Figure 15. Video **Digital Output** Transition D_{HLT} **Times**
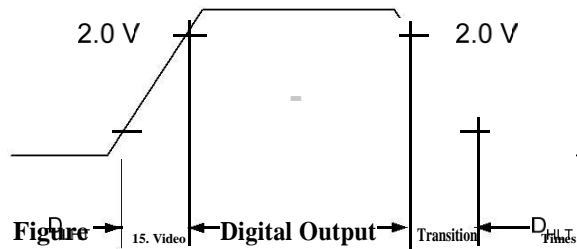
Output Clock to Output Data Delay
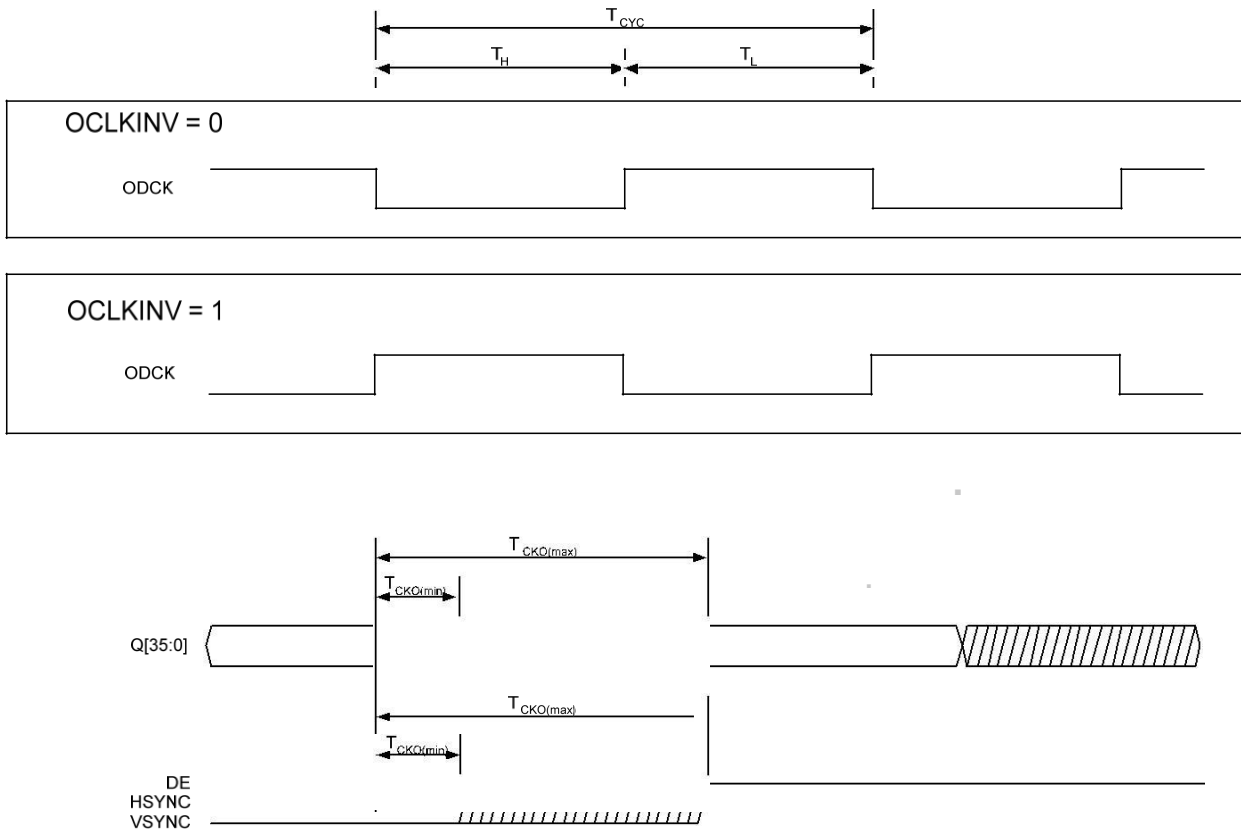
Figure 16. Receiver Clock-to-Output Delay and Duty Cycle Limits

Digital Audio Output Timings
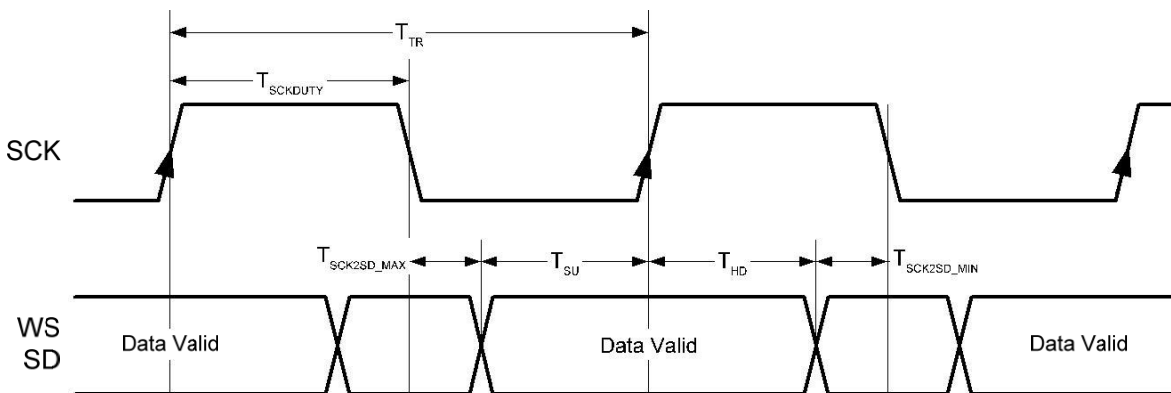
Figure 17. I^{2}S Output Timings

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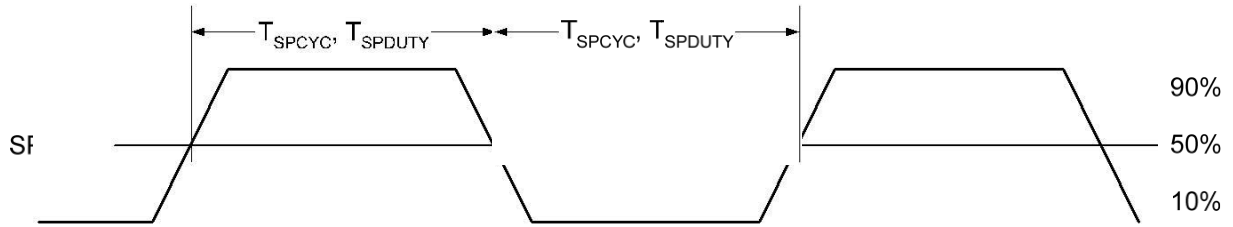
Figure 18. S/PDIF Output Timings

Figure 19. MCLK Timings
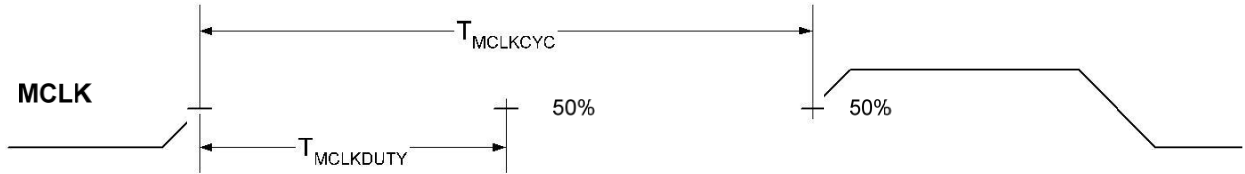
Calculating Setup and Hold Times: Video Bus

24/30/36-Bit Mode

Output data is clocked out on one edge (either rising or falling) of ODCK, and is then captured downstream using the same ODCK edge one clock period later. The setup time of data to ODCK and hold time of ODCK to data are theree

a function of the worst case ODCK to output delay. This is shown in Figure 20. The rising active ODCK edge is shown

with an arrowhead. The logic is reversed OCK INV = 1.
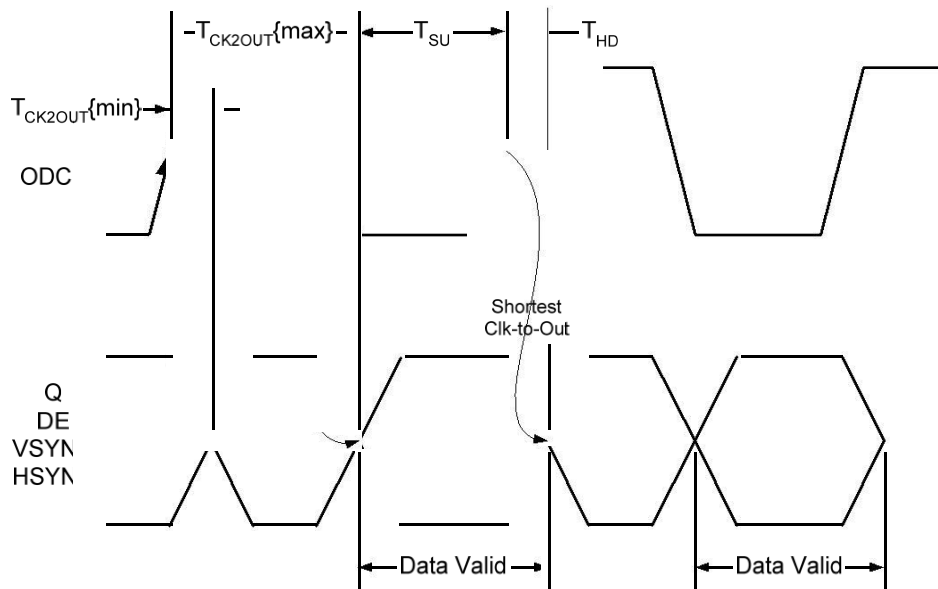
Figure 20. 24/30/36-Bit Mode Receiver Output Setup and Hold Times

Table 15 shows minimum calculated setup and hold times mm d ODCK frequencies. The setup and hold times apply to DE, VSYNC, HSYNC, and Data output pins, with an output load of 10 pF. These are approximations. Hold time is not related to ODCK frequency.

Table 15. Calculation of 24/30/36-Bit Output Setup and Hold Times

Output	Symbol	Parameter	T_{ODCK}		Min
			Frequency	Period	
24/30/36-Bit Mode	T_{SU}	Setup Time to ODCK $= T_{ODCK} - T_{CK2OUT}\{max\}$	27 MHz	37.0 ns	33.2 ns
			74.25 MHz	13.5 ns	9.7 ns
	T_{HD}	Hold Time from ODCK = $T_{CK2OUT}\{min\}$	—	—	0.8 ns

12/15/18-Bit Dual-Edge Mode

Output data is clocked out on each edge of ODCK (both rising and falling), and is then captured downstream using the opposite ODCK edge. The setup time of data to ODCK is a function of the shortest duty cycle and the longest ODCK-to-output delay. The hold time does not depend on duty cycle (beca every edge is d), and is a function of the longest ODCK-to-output delay.
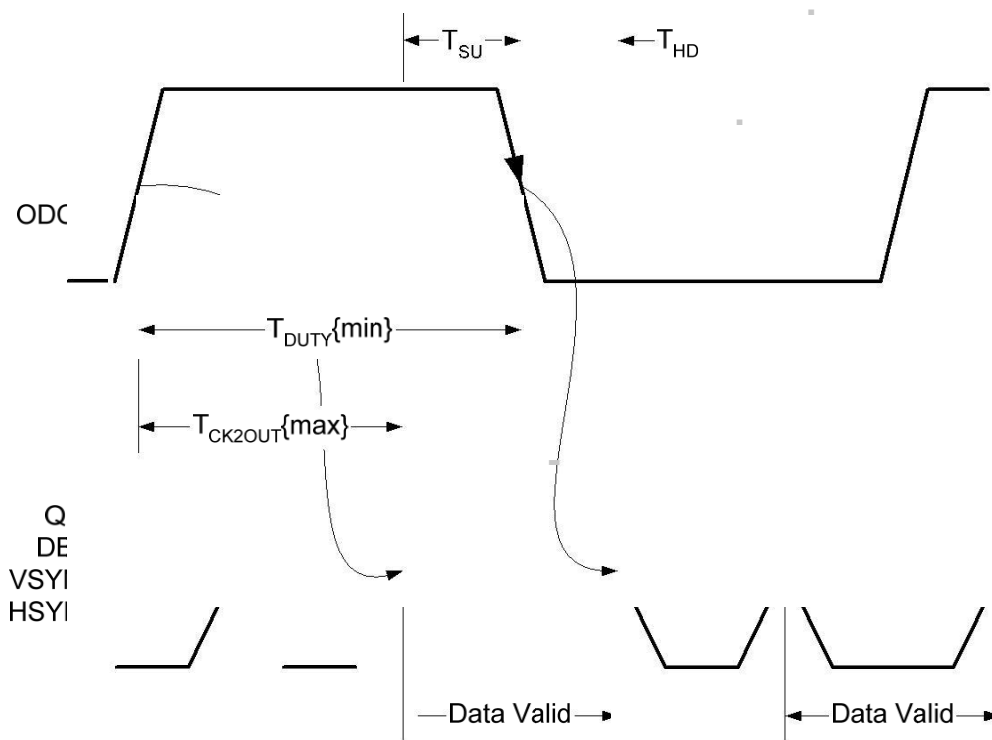
Figure 21. 12/15/18-Bit Mode Receiver Output Setup and Hold Times

Table 16 shows minimum calculated setup and hold times mm d ODCK frequencies, up to the maximum allowed 12/15/18-bit mode. The setup and hold times apply to DE, VSYNC, HSYNC, and Data output pins, with an output load of 10 pF. These are approximations. Hold time is not related to ODCK frequency.

Table 16. Calculation of 12/15/18-Bit Output Setup and Hold Times

Output	Symbol	Parameter	T_{ODCK}		Min
			Frequency	Period	
12/15/18-Bit Mode	T_{SU}	Setup Time to ODCK $= T_{ODCK} \cdot T_{DUTY}\{min\} = T_{CK2OUT}\{max\}$	27 MHz	37.0 ns	34.1 ns
			74.25 MHz	13.5 ns	9.7 ns
	T_{HD}	Hold Time from ODCK = $T_{CK2OUT}\{min\}$	—	—	0.8 ns

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Calculating Setup and Hold Times I^{2}S Audio Bus

Valid serial data is available at T_{SCK2SD} after the falling edge of the first SCK cycle, and is then captured downstream using the active rising edge of SCK one clock period later. The setup time of data to SCK (T_{SU}) and hold time of SCK to data (T_{HD}) are theree a function of the worst case SCK-to-output data delay (T_{SCK2SD}). Figure 17 illustrates this timing relationship. Note that the active SCK edge (rising edge) is shown with an arrowhead. The logic is reversed a falling edge sampling clock.

Table 17 shows the setup and hold time calculation examples various audio sample frequencies. The mula d in these examples also applies when calculating the setup and hold times other audio sampling frequencies.

Table 17. I^{2}S Setup and Hold Time Calculations

Symbol	Parameter		FWS (kHz)	FSCLK (MHz)	Ttr	Min
T_{SU}	Setup Time, SCK to SD/WS $= T_{TR} - (T_{SCKDUTY\_WORST} + T_{SCK2SD\_MAX})$ $= T_{TR} - (0.6 T_{TR} + 5ns)$ $= 0.4 T_{TR} - 5ns$		32 kHz	2.048	488 ns	190 ns
			44.1 kHz	2.822	354 ns	136 ns
			48 kHz	3.072	326 ns	125 ns
			96 kHz	6.144	163 ns	60 ns
			192 kHz	12.288	81 ns	27 ns
T_{HD}	Hold Time, SCK to SD/WS $= (T_{SCKDUTY\_WORST} - T_{SCK2SD\_MIN})$		32 kHz	2.048	488 ns	190 ns
			44.1 kHz	2.822	354 ns	136 ns
			48 kHz	3.072	326 ns	125 ns

Note: The sample calculations shown in Table 17 are based on WS = 64 SCLK rising edges.

Pin Descriptions

Digital Video Data Output Pins

Pin Name	Pin #	Strength	Type	Dir	Description
Q0	16	8 mA	LVTTL	Output	36-Bit Output Pixel Data Bus.
Q1	15		LVTTL	Output	Q35:0 is highly nfigurable using the
Q2	14		LVTTL	Output	VDD_NFIG register. It supports a wide array of
Q3	13		LVTTL	Output	output mats, including multiple RBG and YCbCr
Q4	10		LVTTL	Output	bus mats. Using the appropriate bits in the PD
Q5	9		LVTTL	Output	register, the output drivers can be put into a high
Q6	8		LVTTL	Output	impedance (tri-state) mode. A weak, pull-
Q7	7		LVTTL	Output	down resistor brings each output to ground.
Q8	3		LVTTL	Output	
Q9	2		LVTTL	Output	
Q10	1		LVTTL	Output	
Q11	144				
Q12	141		LVTTL	Output	
Q13	140		LVTTL	Output	
Q14	139		LVTTL	Output	
Q15	138		LVTTL	Output	
Q16	135		LVTTL	Output	
Q17	134		LVTTL	Output	
Q18	133		LVTTL	Output	
Q19	132		LVTTL	Output	
Q20	129		LVTTL	Output	
Q21	128				
Q22	127				
Q23	126				
Q24	123				
Q25	122		LVTTL	Output	
Q26	121		LVTTL	Output	
Q27					
Q28	117		LVTTL	Output	
Q29	116		LVTTL	Output	
Q30	115		LVTTL	Output	
			LVTTL	Output	
			LVTTL	Output	
			LVTTL	Output	
Q31	114		LVTTL	Output	
Q32	111		LVTTL	Output	
Q33	110		LVTTL	Output	
Q34	109		LVTTL	Output	
Q35	108		LVTTL	Output	

Notes:

1. When transporting video data that s fewer than 36 bits, the und bits on the Q[35:0] bus can still carry switching pixel data signals. Und Q[35:0] bus pins should be left unnnected, masked, or ignored by downstream devices. example, carrying YCbCr 4:2:2 data with 24-bit width (refer to page 39), bits Q[0] through Q[11] are not d and should be ignored or left unnnected.
2. The output data bus, Q0 to Q35, can be wire-ORed to another device such that one device is always tri-stated. However, the Q0–Q35 pins do not have pull-up or pull-down resistors, so they cannot pull the bus either up or down when all nnected devices are in the high-impedance state.

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Digital Video ntrol Output Pins

Pin Name	Pin #	Strength	Type	Dir	Description
DE	19	8 mA	LVTTL	Output	Data Enable.
HSYNC	20	8 mA	LVTTL	Output	Horizontal Sync Output.
VSYNC	21	8 mA	LVTTL	Output	Vertical Sync Output.
EVNODD	22	8 mA	LVTTL	Output	Indicates Even or Odd Field Interlaced mats.
ODCK	5	12 mA	LVTTL	Output	Output Data Clock.

Note: HSYNC and VSYNC outputs carry sync signals both embedded and explicit sync nfigurations.

Digital Audio Output Pins

Pin Name	Pin #	Strength	Type	Dir	Description
XTALIN	95	—	5 V tolerant LVTTL	In	Crystal Clock Input. Also allows LVTTL input. Requires 26–28.5 MHz.
XTALOUT	94	4 mA	LVTTL	Out	Crystal Clock Output.
MCLK	89	8 mA	LVTTL	Out	Audio Master Clock Output .
SCK/DCLK	86	4 mA	LVTTL	Out	I^2S Serial Clock Output. DSD Clock Out.
WS/DR0	85	4 mA	LVTTL	Out	I^2S Word Select Output. DSD Serial Right Ch0Data Output.
SD0/DL0	81	4 mA	LVTTL	Out	I S Serial Data Output / DSD Audio Output. nfigurable to be shared with DSD.
SD1/DR1	82	4 mA	LVTTL	Out	
SD2/DL1	83	4 mA	LVTTL	Out	SD0 = DSD Serial Left Ch0 Data Output
SD3/DR2	84	4 mA	LVTTL	Out	SD1 = DSD Serial Right Ch1 Data Output SD2 = DSD Serial Left Ch1 Data Output SD3 = DSD Serial Right Ch2 Data Output
SPDIF/DL2	78	4 mA	LVTTL	Out	S/PDIF Audio Output.

Differential SignalSIIItaPins

MUTEOUT	75	4 mA	LVTTL	Out	Mute Audio Output.

DSD Serial Left Ch2 Data Output

Signal to the external downstream audio device to mute the audio output.

Note: The XTALIN pin can either be driven at LVTTL levels by a clock (leaving XTALOUT unnnected), or nnected through a crystal to XTALOUT. Refer to the schematic on page 60 and the XTALIN Clock Requirement section on page 56.

Pin Name	Pin #	Type	Description	
R0XC+	40	Analog	TMDS Input Clock Pair.	HDMI Port 0
R0XC-	39	Analog		
R0X0+	44	Analog	TMDS Input Data Pair.	
R0X0-	43	Analog		
R0X1+	48	Analog	TMDS Input Data Pair.	
R0X1-	47	Analog		
R0X2+	52	Analog	TMDS Input Data Pair.	
R0X2-	51	Analog		

R1X2-	69	Analog	

R1XC+	58	Analog	TMDS Input Clock Pair.	HDMI Port 1

R1XC-	57	Analog	
R1X0+	62	Analog	TMDS Input Data Pair.
R1X0-	61	Analog	
R1X1+	66	Analog	TMDS Input Data Pair.
R1X1-	65	Analog	
R1X2+	70	Analog	TMDS Input Data Pair.

nfiguration/Programming Pins

Pin Name	Pin #	Strength	Type	Dir	Description
INT	102	4 mA	LVTTL Or Open drain	Out	Interrupt Output. nfigurable polarity and push-pull output. Multiple sources of interrupt can be enabled through the INT_EN register. See Note 1.
RESET#	100	—	Schmitt	In	Reset Pin. Active LOW. 5 V tolerant
DSCL0	34	—	Schmitt Open drain	In	DDC I²C Clock Port 0. 5 V tolerant. HDCP KSV, An, and Ri values are exchanged over an I²C port during authentication. True open drain, so does not pull to GND if R0PWR5V is not applied.
DSDA0	33	3 mA	Schmitt Open drain	Bi-Di	DDC I²C Data Port 0. 5 V tolerant. HDCP KSV, An, and Ri values are exchanged over an I²C port during authentication. True open drain, so does not pull to GND if R0PWR5V is not applied.
DSCL1	29	—	Schmitt Open drain	In	DDC I2C Clock Port 1. 5 V tolerant. HDCP KSV, An, and Ri values are exchanged over an I²C port during authentication. Trueopen drain, so does not pull to GND if R1PWR5V is not applied.
DSDA1	28	3 mA	Schmitt Open drain	Bi-Di	DDC I2C Data Port 1. 5 V tolerant. HDCP KSV, An, and Ri values are exchanged over an I²C port during authentication. True open drain, so does not pull to GND if R1PWR5V is not applied.
CSCL	27	—	Schmitt Open drain	In	nfiguration/Status I²C Clock. 5 V tolerant. Chip nfiguration/status, CEA-861 registers areaccessed via this I C port. True open drain, so does not pull to GND if power is not applied.
CSDA	26	3 mA	Schmitt	Bi-Di	nfiguration/Status I C Data. support and downstream HDCP repeater-specific registers are accessed via this I²C port. True open drain, so does not pull to GND if power is not applied.
CI2CA	105		LLVTTL	In	Local I²C Address Select. 5 V tolerant. LOW = Addresses 0x60/0x68 HIGH = Addresses 0x62/0x6A
SCDT	101	12 mA	LVTTL	Out	Indicates Active Video at HDMI Input Port. Sync detection indicator.
R0PWR5V	35	—	LVTTL	In	Port 0 Transmitter Detect. 5 V tolerant. d MUTEIN function. See Notes 2 and 3.
R1PWR5V	30	—	LVTTL	In	Port 1 Transmitter Detect. 5 V tolerant. d MUTEIN function. See Notes 2 and 3.
RSVDNC	98, 77, 76, 55	—	—		Reserved, must be left unnnected.
RSVDL	99	—	—	In	Reserved, must be tied to ground.

Notes:

1. The INT pin can be programmed to be either a push-pull LVTTL output or an open-drain output.

2. There is no power sequence requirement on the R0PWR5V and R1PWR5V pins.

3. The operating requirement of the R0PWR5V and R1PWR5V pins is 5 V ±5%.

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Power and Ground Pins

Pin Name	Pin #	Type	Description	Supply
CVCC18	12, 24, 25, 80, 91, 107, 119, 131, 143	Power	Digital Logic VCC	1.8 V
CGND	11, 23, 79, 90, 106, 118, 130, 142	Ground	Digital Logic GND	
IOVCC33	6, 18, 32, 74, 88, 104, 113, 125, 137	Power	Input/Output VCC	3.3 V
IOGND	4, 17, 31, 73, 87, 103, 112, 124, 136	Ground	Input/Output GND	
AVCC33	38, 42, 46, 50, 56, 60, 64, 68	Power	TMDS Analog VCC 3.3 V	3.3 V
AGND	36, 41, 45, 49, 53, 59, 63, 67, 71	Ground	TMDS Analog GND	
AVCC18	37, 54, 72	Power	TMDS Analog VCC 1.8 V	1.8 V
DVCC18	92	Power	Audio Clock Regeneration PLL Analog VCC. Must be nnected to 1.8 V	1.8 V
DGND	93	Ground	Audio Clock Regeneration PLL Analog Ground.	
XTALVCC	96	Power	Audio Clock Regeneration PLL Crystal Oscillator Power. Must be nnected to 3.3V	3.3 V
REGVCC	97	Power	Audio Clock Regeneration PLL Crystal Regulator Power. Must be nnected to 3.3 V	3.3 V
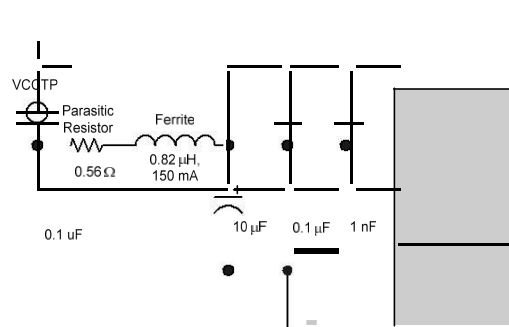
3. The LC filter can help lowerthe st of the power supply filter circuits. The separate voltage regulator may not be

Figure 22. Test Point VCCTP VCC Noise Tolerance Spec

Notes:

1. The ferrite (0.82 μH, 150 mA) attenuates the PLL power supply noise at 10 kHz and above.
2. The optional parasitic resistor minimizes the peaking. The typical value d here is 0.56 Ω. One Ω is the maximum.

Video Path

The SiI9135/SiI9135A receiver accepts all valid HDMI input mats and can transm that video in a variety of ways to produce a desired video output mat. The following pages describe how to ntrol the video path matting and how to assign output pins each video output mat. The processing blocks in Figure 23 rrespond to those shown in Figure 24 through Figure 26.

Figure 23. Receiver Video and Audio Data Processing Paths
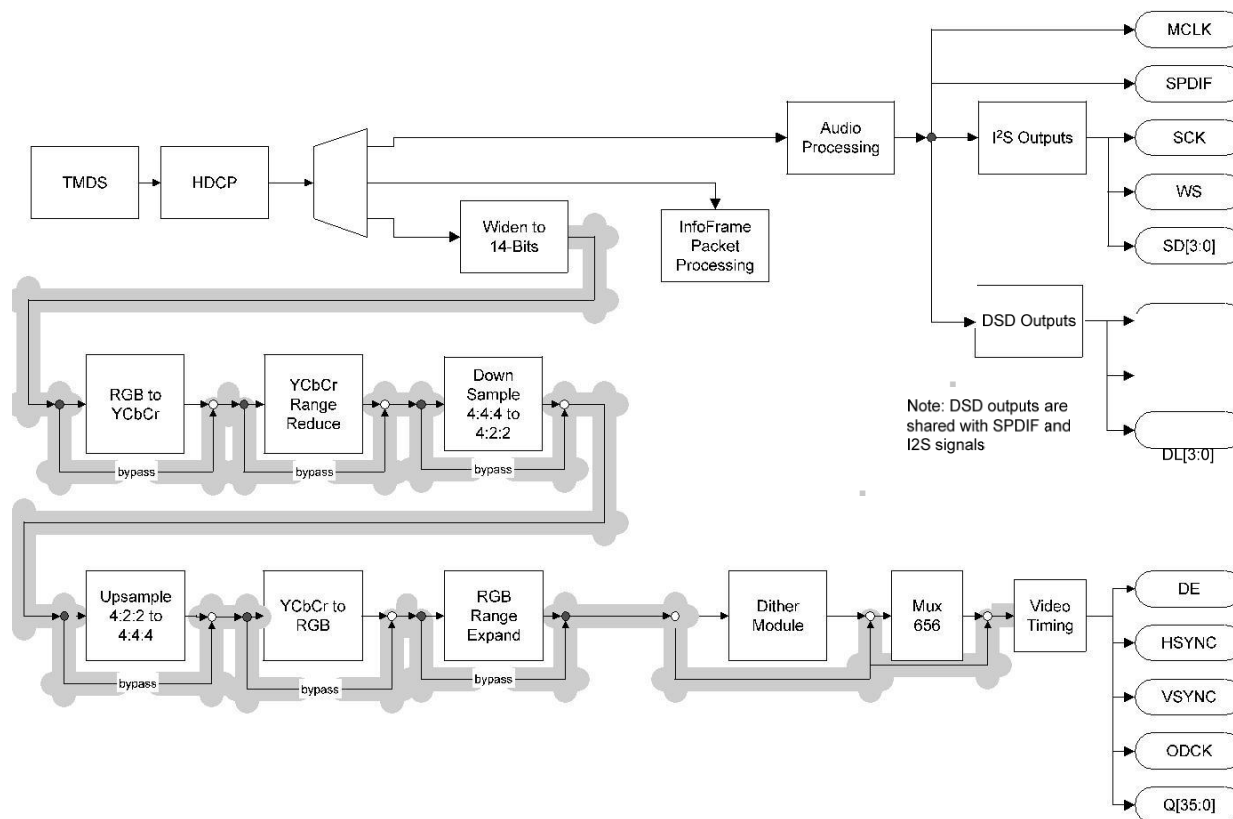
The HDMI link supports the transport of video in any of three modes: RGB 4:4:4, YCbCr 4:4:4, or YCbCr 4:2:2. The flexible video path in the receiver allows rematting of video data to a set of output modes. Table 18 lists the supported transmations and points to the appropriate figure each. In every case, the HDMI link itself carries separate syncs.

Table 18. Translating HDMI mats to Output mats

HDMI	Output mat (Digital)					
Input mat	RGB 4:4:4 Separate sync	YCbCr 4:4:4 Separate sync	YCbCr 4:2:2 Separate sync	YCbCr 4:2:2 Embedded sync	YC Mux Separate sync	YC Mux Embedded sync
RGB 4:4:4	Figure 24A	Figure 24B	Figure 24C	Figure 24D	Figure 24E	Figure 24F
YCbCr 4:4:4	Figure 25A	Figure 25B	Figure 25C	Figure 25D	Figure 25E	Figure 25F
YCbCr 4:2:2	Figure 26A	Figure 26B	Figure 26C	Figure 26D	Figure 26E	Figure 26F

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HDMI RGB 4:4:4 Input Processing
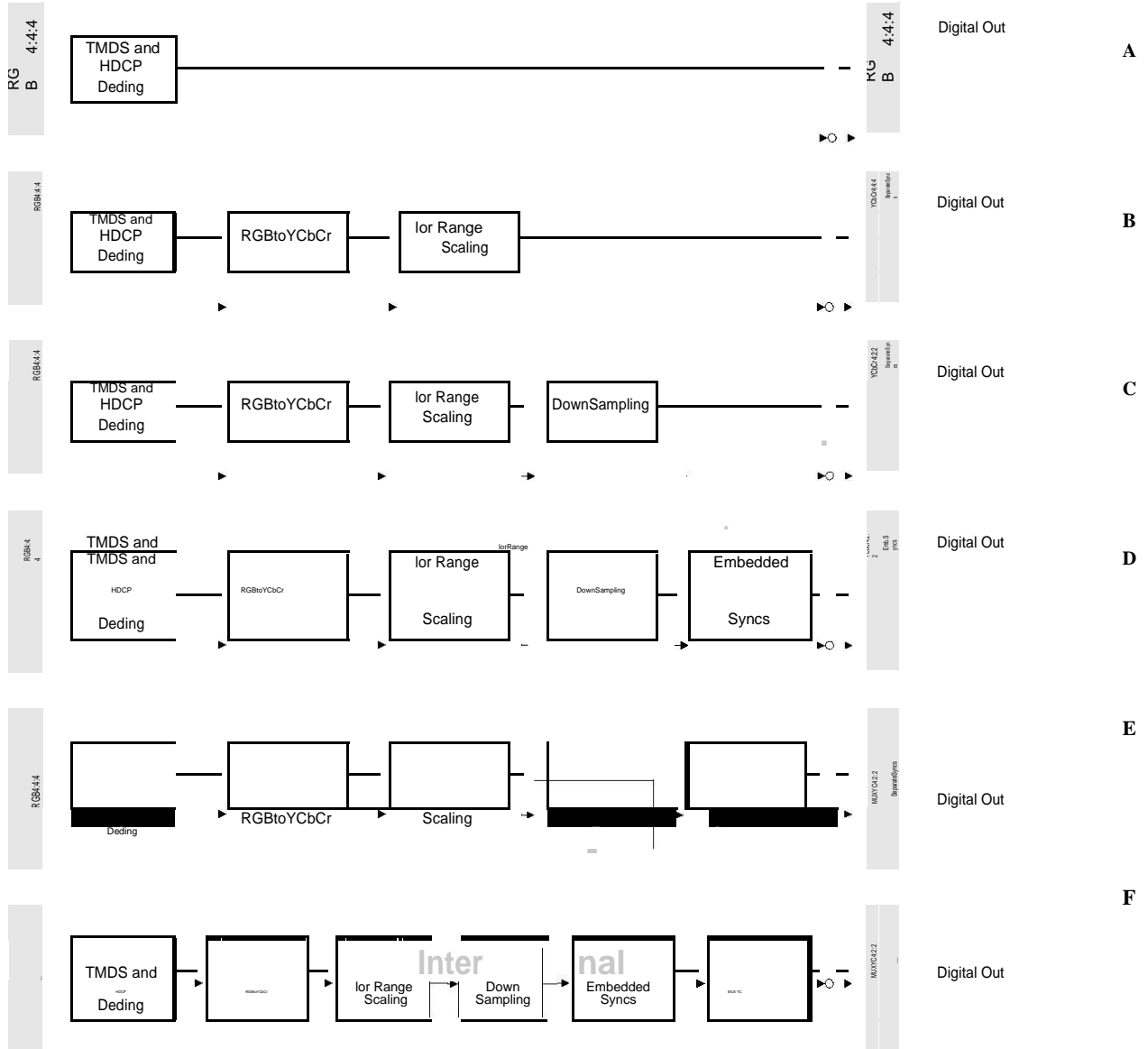
Figure 24. HDMI RGB 4:4:4 Input to Video Output Transmations

HDMI YCbCr 4:4:4 Input Processing
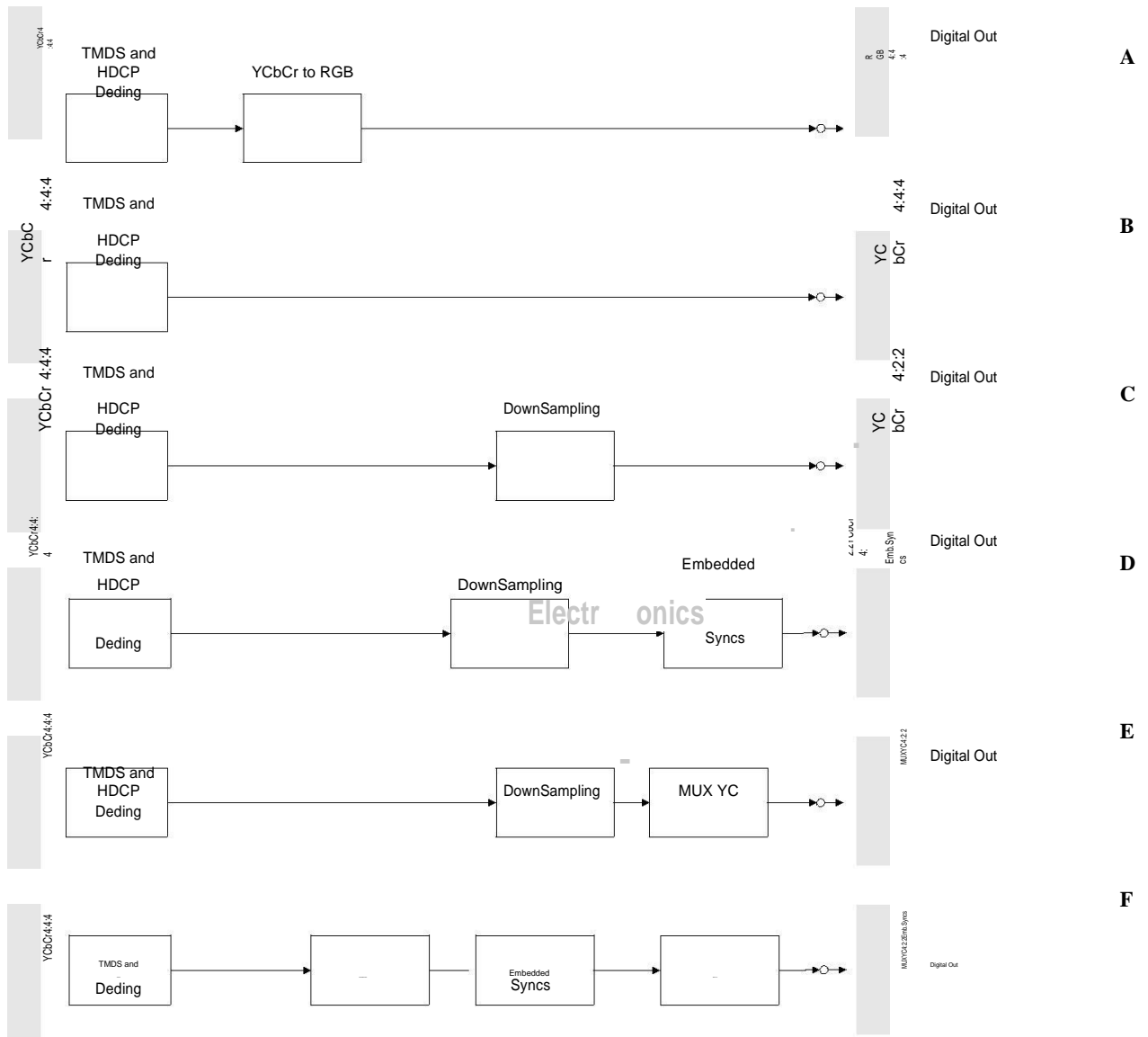
Figure 25. HDMI YCbCr 4:4:4 Input to Video Output Transmations

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HDMI YCbCr 4:2:2 Input Processing
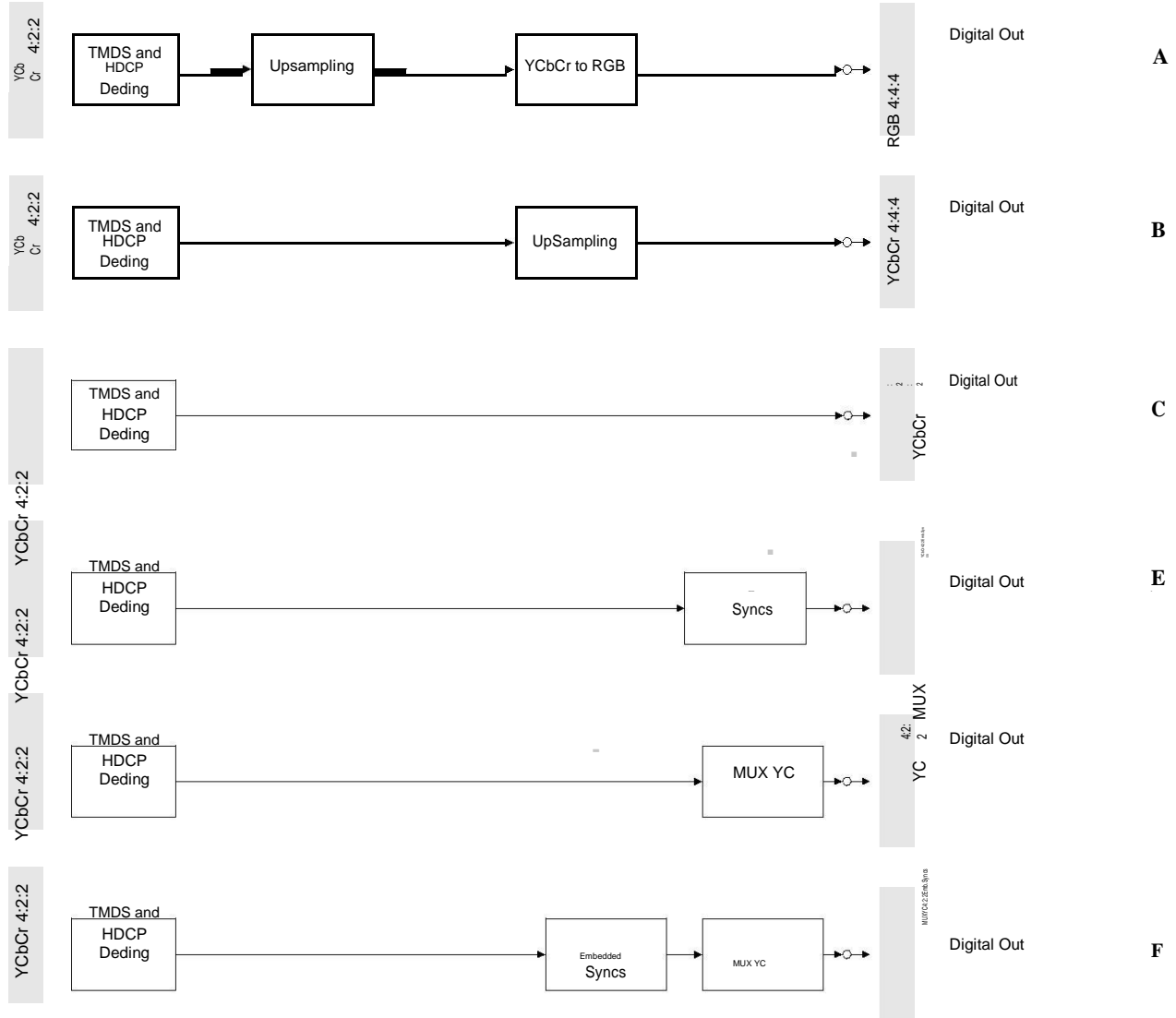
Figure 26. HDMI YCbCr 4:2:2 Input to Video Output Transmations

SiI9135/SiI9135A Output Mode nfiguration

The SiI9135/SiI9135A receiver supports multiple output data mappings. Some mappings have explicit ntrol signals while others have embedded ntrol signals. The selection of data mapping mode should be nsistent at the pins and in the rresponding register settings. Refer to the *SiI9125/SiI9135 Programmers Reference*, listed in Table 31 on page 65, more details.

Table 19. Output Video mats

Output Mode	Data Widths	Pixel Replication	Syncs	Page	Notes
RGB 4:4:4	24, 30, 36	1x	Explicit	37	3, 7
YCbCr 4:4:4	24, 30, 36	1x	Explicit	37	1, 3, 7
YC 4:2:2 Sep. Syncs	16, 20, 24	1x	Explicit	39	2, 3
YC 4:2:2 Sep. Syncs	16, 20, 24	2x	Explicit	39	2, 3, 8
YC 4:2:2 Emb. Syncs	16, 20, 24	1x	Embedded	42	2, 5
YC MUX 4:2:2	8, 10, 12	2x	Explicit	45	2, 4, 8
YC MUX 4:2:2 Emb. Syncs	8, 10, 12	2x	Embedded	47	2, 5, 6, 8, 9

Notes:

1. YC 4:4:4 data ntains one Cr, one Cb, and one Y value every pixel.

7. A 2x clock can also be sent with 4:4:4 data.

3. These mats can be carried across the HDMI link. Refer to the HDMI Specification, Section 6.2.3. The link clock must be within the specified range of the receiver.

4. In YC MUX mode data is output on one or two 8/10/12-bit channels.

5. YC MUX with embedded SAV/EAV signal.

6. Syncs are embedded using SAV/EAV des.

8. When sending a 2x clock the HDMI source must also send AVI InfoFrames with an accurate pixel replication immediately after the TMDS and (optional)HDCP deding. The HDMI link always carries explicit HSYNC, VSYNC,

9. 2x clocking does not support YC 4:2:2 embedded sync timings 720p or 1080i, as the output clock frequency would exceed the

The receiver can provide video in various mats on its parallel digital output bus. Some transmation of the data

The diagrams do not include separation of the audio and InfoFrame packets from the HDMI stream, which occurs

and DE. Theree the SAV/EAV sync ender must be d whenever the output mode includes embedded sync. The timing diagrams in Figure 27 through Figure 31 show a representation of the DE, HSYNC, and VSYNC timing. This timing is specific to the video resolution, as defined by EIA/CEA-861B and other specs. The number of pixels shown each DE HIGH time is representative, to show the data matting.

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RGB and YCbCr 4:4:4 mats with Separate Syncs

The pixel clock runs at the pixel rate and a mplete definition of each pixel is output on each clock. Figure 27 shows RGB data. The same timing mat is d YCbCr 4:4:4 as listed in Table 20. Figure 27 shows timings with

Figure 27. 4:4:4 Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are ntrolled by setting the appropriate registers, beca no pixel data is carried on HDMI during blanking.

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YC 4:2:2 mats with Separate Syncs

The YC 4:2:2 mats output one pixel every pixel clock period. A luminance (Y) value is output every pixel, but the chrominance values (Cb and Cr) are sent over two clock cycles. Pixel data can be 24-bit, 20-bit or 16-bit. HSYNC and VSYNC are output explicitly on their own pins. The DE HIGH time must ntain an even number of pixel clocks. Figure 28 shows timings with OCLKDIV = 0 and OCKINV = 1.

Table 21. YC 4:2:2 Non-Ended-Sync Pin Mappings

Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	NC	NC
Q5	NC	NC	NC	NC	NC	NC
Q6	NC	NC	NC	NC	NC	NC
Q7	NC	NC	NC	NC	NC	NC
Q8	NC	NC	NC	NC	NC	NC
Q9	NC	NC	NC	NC	NC	NC
Q11	NC	NC	NC	NC	NC	NC
Q12	NC	NC			Y0	Y0
Q13	NC	NC	NC	NC	Y1	Y1
Q14	NC	NC	Y0	Y0	Y2	Y2
Q15	NC	NC	Y1	Y1	Y3	Y3
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q21	Y5	Y5	Y7			Y9
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q25	NC	NCNC		NC	Cb1	Cr1
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q26	NC	NC	Cb0	Cr0	Cb2	Cr2
Q27	NC	NC	Cb1	Cr1	Cb3	Cr3
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

, Inc.

Table 22. YC 4:2:2 (Pass Through) Non-Ended-Sync Pin Mapping

Pin	16-bit YC		20-bit YC		24-bit YC	
Name	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	Y0	Y0
Q5	NC	NC	NC	NC	Y1	Y1
Q6	NC	NC	Y0	Y0	Y2	Y2
Q7	NC	NC	Y1	Y1	Y3	Y3
Q8	NC	NC	NC	NC	Cb0	Cr0
Q9	NC	NC	NC	NC	Cb1	Cr1
Q10	NC	NC	Cb0	Cr0	Cb2	Cr2
Q11	NC	NC	Cb1	Cr1	Cb3	Cr3
Q12	NC	NC	NC	NC	NC	NC
Q13	NC	NC	NC	NC	NC	NC
Q14	NC	NC	NC	NC	NC	NC
Q15	NC	NC	NC	NC	NC	NC
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	NC	NC
Q25	NC	NC	NC	NC	NC	NC
Q26	NC	NC	NC	NC	NC	NC
Q27	NC	NC	NC	NC	NC	NC
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Note: This pin mapping is valid when the input video mat is YC 4:2:2 and the output video mat is also YC 4:2:2. No video processing block is enabled when this pin mapping is d.
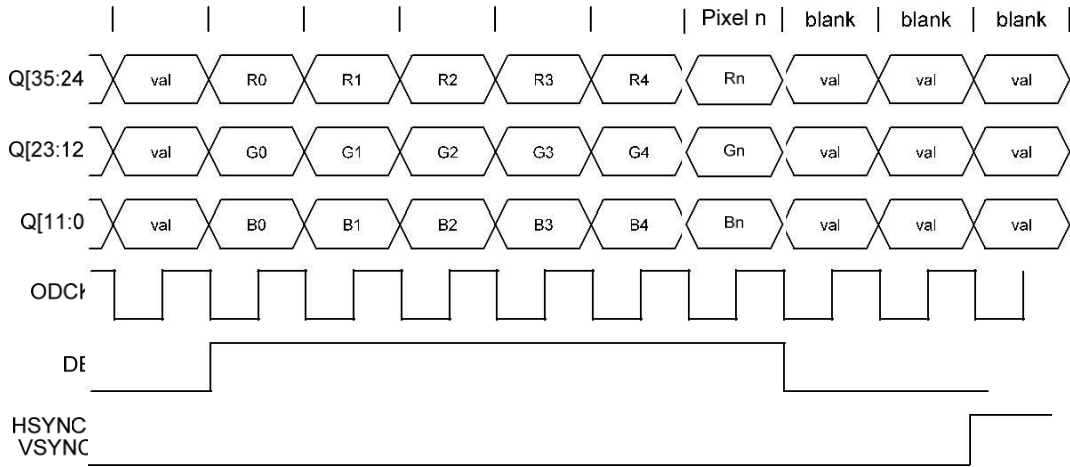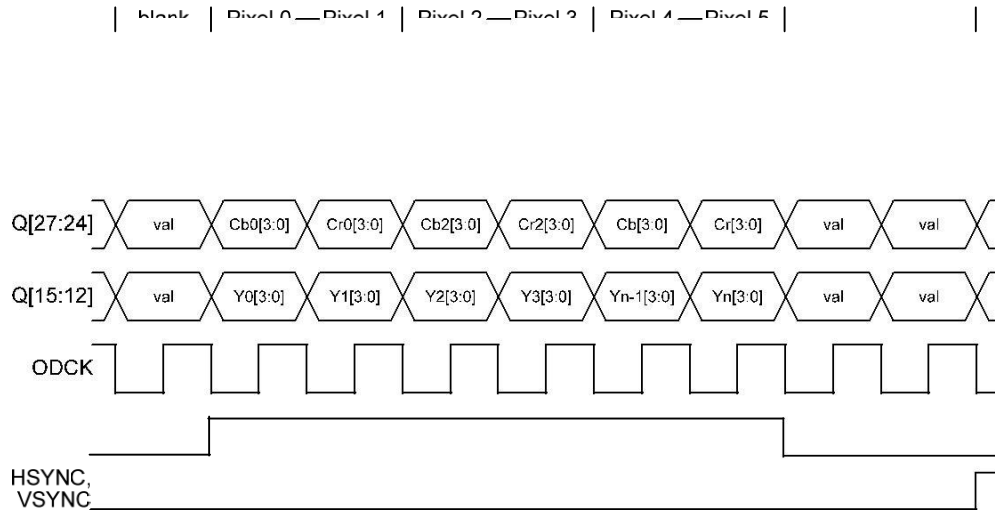
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Figure 28. YC Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are ntrolled by setting the appropriate registers, beca no pixel data is carried on HDMI during blanking.

YC 4:2:2 mats with Embedded Syncs

The YC 4:2:2 embedded sync mat is identical to the previous mat (YC 4:2:2), except that the syncs are embedded. Pixel data can be 24-bit, 20-bit or 16-bit. DE output is always provided. Figure 29 shows the Start of Active Video (SAV) preamble, the End of Active Video (EAV) suffix, and shows timing with OCLKDIV = 0 and OCKINV = 1.

Table 23. YC 4:2:2 Embedded Sync Pin Mappings

Pin	16-bit YC		20-bit YC		24-bit YC	
Name	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	NC	NC
Q5	NC	NC	NC	NC	NC	NC
Q6	NC	NC	NC	NC	NC	NC
Q7	NC	NC	NC	NC	NC	NC
Q8	NC	NC	NC	NC	NC	NC
Q9	NC	NC	NC	NC	NC	NC
Q10	NC	NC	NC	NC	NC	NC
Q11	NC	NC	NC	NC	NC	NC
Q14	NC	NC	Y0	Y0	Y2	Y2
Q15	NC	NC	Y1	Y1	Y3	Y3
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q26	NC	NC	Cb0	Cr0	Cb2	Cr2
Q27	NC	NC	Cb1	Cr1	Cb3	Cr3
Q24	NC	NC	NC	NC	Cb0	Cr0
Q25	NC	NC	NC	NC	Cb1	Cr1
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded

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Table 24. YC 4:2:2 (Pass Through) Embedded Sync Pin Mapping

Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	Y0	Y0
Q5	NC	NC	NC	NC	Y1	Y1
Q6	NC	NC	Y0	Y0	Y2	Y2
Q7	NC	NC	Y1	Y1	Y3	Y3
Q8	NC	NC	NC	NC	Cb0	Cr0
Q9	NC	NC	NC	NC	Cb1	Cr1
Q10	NC	NC	Cb0	Cr0	Cb2	Cr2
Q11	NC	NC	Cb1	Cr1	Cb3	Cr3
Q12	NC	NC	NC	NC	NC	NC
Q13	NC	NC	NC	NC	NC	NC
Q14	NC	NC	NC	NC	NC	NC
Q15	NC	NC	NC	NC	NC	NC
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	NC	NC
Q25	NC	NC	NC			NC
Q26	NC	NC	NC	NC	NC	NC
Q27	NC	NC	NC	NC	NC	NC
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2Cr2		Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded

Note: This pin mapping is valid when the input video mat is YC 4:2:2 and the output video mat is YC 4:2:2 also. No video processing block is enabled when this pin mapping is d.
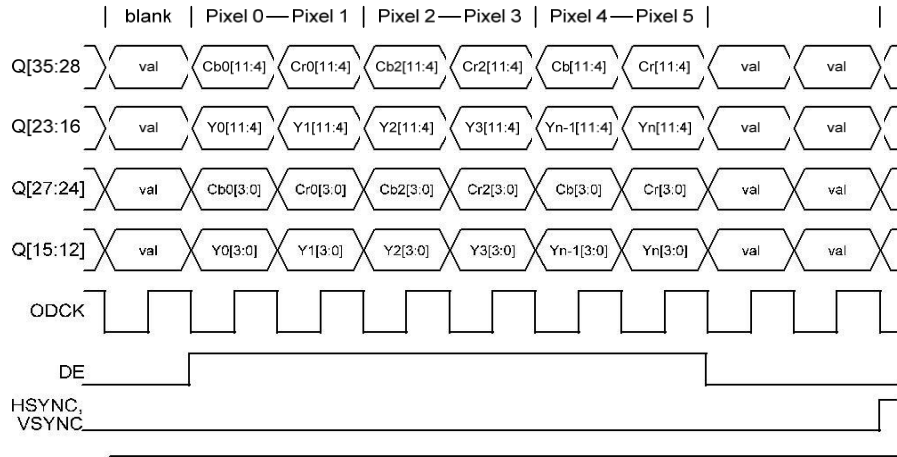
Figure 29. YC Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are ntrolled by setting the appropriate

registers, beca no pixel data is carried on HDMI during blanking. SAV/EAV des appear as an 8-bit field on both Q[35:28] (per
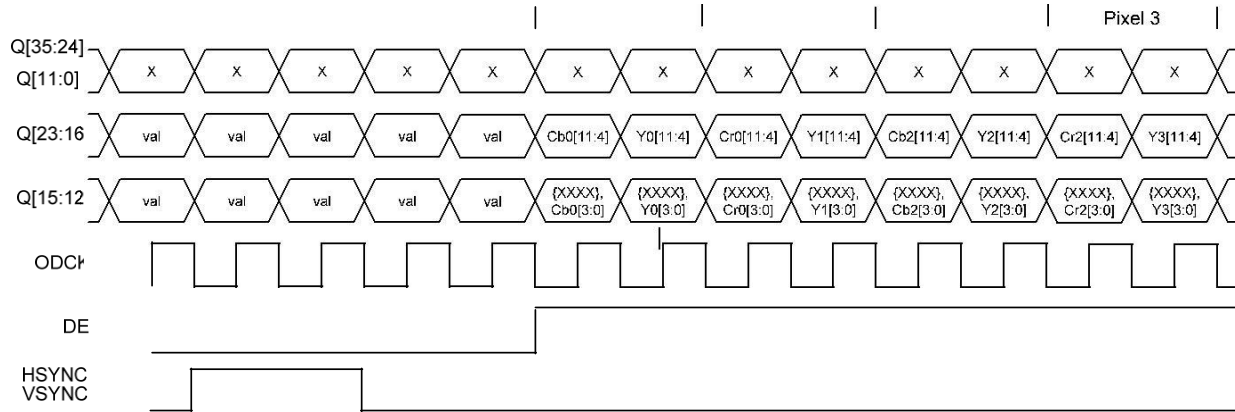
SMPTE) and Q[23:16].

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YC Mux 4:2:2 mats with Separate Syncs

The video data is multiplexed onto fewer pins than the mapping in Table 25, but mplete luminance (Y) and chrominance (Cb and Cr) data is still provided each pixel beca the output pixel clock runs at twice the pixel rate. Figure 30 shows the 24- bit mode. The 16- and 20-bit mappings fewer output pins the pixel data. Note the explicit syncs. The figure shows OCLKDIV = 0 and OCKINV = 1.

Table 25. YC Mux 4:2:2 Mappings

Pin Name	8-bit YCbCr	10-bit YCbCr	12-bit YCbCr
Q0	NC	NC	NC
Q1	NC	NC	NC
Q2	NC	NC	NC
Q3	NC	NC	NC
Q4	NC	NC	NC
Q5	NC	NC	NC
Q6	NC	NC	NC
Q7	NC	NC	NC
Q8	NC	NC	NC
Q9	NC		
Q10	NC	NC	NC
Q11	NC	NC	NC
Q12	NC		
Q13	NC	NC	
Q14	NC		
Q15	NC	NC	D1
Q16	D0	D0	D2
Q17	D1	D1	D3
Q18	D2	D2	D4
Q19	D3	D3	D5
Q20	D4		
Q21	D5 NC		
Q22	D6	D6	D8
Q23	D7	D4	D6
Q24	NC		
Q25		D7	D9
Q26	NC	D8	D10
Q27	NC	D9	D11
Q28	NC	NC	NC
Q29	NC	NC	NC
Q30	NC		
Q31	NC		
Q32	NC	NC	NC
Q33	NC	NC	NC
Q34	NC	NC	NC
Q35	NC	NC	NC
		NC	NC
		NC	NC
		NC	NC
		NC	NC
		NC	NC
		NC	NC
HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE

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Figure 30. YC Mux 4:2:2 Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are ntrolled by setting the appropriate registers, beca no pixel data is carried on HDMI during blanking.

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YC Mux 4:2:2 mats with Embedded Syncs

This mode is similar to the one on page 45, but with embedded syncs. It is similar to YC 4:2:2 with embedded syncs, but also multiplexes the luminance (Y) and chrominance (Cb and Cr) onto the same pins on alternating pixel clock cycles. Normally this mode is d 480i, 480p, 576i and 576p modes. The output clock rate is half the pixel clock rate on the link. SAV de is shown bee the rise of DE. EAV follows the fall of DE. See the ITU- R BT.656 Specification. 480p 54 MHz output can be achieved if the input differential clock is 54 MHz. Figure 31 shows OCLKDIV = 0 and OCKINV = 1.

Table 26. YC Mux 4:2:2 Embedded Sync Pin Mapping

Pin Name	8-bit YCbCr	10-bit YCbCr	12-bit YCbCr
Q0	NC	NC	NC
Q1	NC	NC	NC
Q2	NC	NC	NC
Q3	NC	NC	NC
Q4	NC	NC	NC
Q5	NC	NC	NC
Q6	NC	NC	NC
Q7			
Q8	NC	NC	NC
Q9	NC	NC	NC
Q10	NC	NC	NC
Q11	NC	NC	NC
Q12	NC	NC	NC
Q13	NC	NC	D0
Q14	NC	NC	D1
Q15	NC	D0	D2
Q16	NC	D1	D3
Q17			
Q18			
Q19	D2	D4	D6
Q20			
Q21			
Q22	D5 / D3	D7 / D5	D9 / D7
Q23	D4	D6	D8
Q24	D6	D8	D10
Q25	D7	D9	D11
Q26	NC	NC	NC
Q27			
Q28	NC	NC	NC
Q29			
Q30	NC	NC	NC
Q31	NC	NC	NC
Q32	NC	NC	NC
Q33	NC	NC	NC
Q34	NC	NC	NC
Q35	NC	NC	NC
	NC	NC	NC
HSYNC	NC	NC	NC
VSYNC	NC	NC	NC
DE			
	Embedded	Embedded	Embedded
	Embedded	Embedded	Embedded
	Embedded	Embedded	Embedded

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12/15/18-Bit RGB and YCbCr 4:4:4 mats with Separate Syncs

The output clock runs at the pixel rate and a mplete definition of each pixel is output on each clock. One clock edge drives out half the pixel data on 12/15/18 pins. The opposite clock edge drives out the remaining half of the pixel data on the same 12/15/18 pins. Figure 32 shows RGB data. The same timing mat is d YCbCr 4:4:4 as listed in the lumns of Table 27. ntrol signals (DE, HSYNC, and VSYNC) change state with respect to the first edge of ODCK.

Table 27. 12/15/18-Bit Output 4:4:4 Mappings

Pin Name	24-bit RGB		24-bit YCbCr		30-bit RGB		30-bit YCbCr		36-bit RGB		36-bit YCbCr	
	First Edge	Send Edge	First Edge	Send Edge	First Edge	Send Edge	First Edge	Send Edge	First Edge	Send Edge	First Edge	Send Edge
Q0	NC	NC	NC	NC	NC	NC	NC	NC	B0	G6	Cb0	Y6
Q1	NC	NC	NC	NC	NC	NC	NC	NC	B1	G7	Cb1	Y7
Q2	NC	NC	NC	NC	NC	NC	NC	NC	B2	G8	Cb2	Y8
Q3	NC	NC	NC	NC	B0	G5	Cb0	Y5	B3	G9	Cb3	Y9
Q4	NC	NC	NC	NC	B1	G6	Cb1	Y6	B4	G10	Cb4	Y10
Q5	NC	NC	NC	NC	B2	G7	Cb2	Y7	B5	G11	Cb5	Y11
Q6	B0	G4	Cb0	Y4	B3	G8	Cb3	Y8	B6	R0	Cb6	Cr0
Q7	B1	G5	Cb1	Y5	B4	G9	Cb4	Y9	B7	R1	Cb7	Cr1
Q9	B3	G7	Cb3	Y7	B6	R1	Cb6	Cr1	B9	R3	Cb9	Cr3
Q10	B4	R0	Cb4	Cr0	B7	R2	Cb7	Cr2	B10	R4	Cb10	Cr4
Q11	B5	R1	Cb5	Cr1	B8	R3	Cb8	Cr3	B11	R5	Cb11	Cr5
Q12	B6	R2	Cb6	Cr2	B9	R4	Cb9	Cr4	G0	R6	Y0	Cr6
Q13	B7	R3	Cb7	Cr3	G0	R5	Y0	Cr5	G1	R7	Y1	Cr7
Q14	G0	R4	Y0	Cr4	G1	R6	Y1	Cr6	G2	R8	Y2	Cr8
Q15	G1	R5	Y1	Cr5	G2	R7	Y2	Cr7	G3	R9	Y3	Cr9
Q16	G2	R6	Y2	Cr6	G3	R8	Y3	Cr8	G4	R10	Y4	Cr10
HSYNC VSYNC	HSYNC VSYNC	HSYNC VSYNC	HSYNC VSYNC	HSYNC VSYNC	HSYNC VSYNC	HSYNC VSYNC	HSYNC VSYNC	HSYNC VSYNC	HSYNC VSYNC	HSYNC VSYNC	HSYNC VSYNC	HSYNC VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE

Figure 32. 18-Bit Output 4:4:4 Timing Diagram
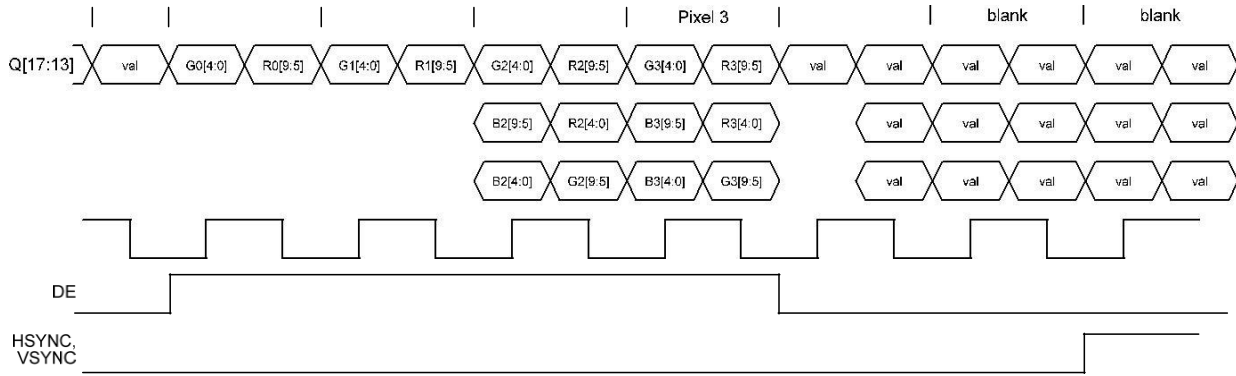
Figure 33. 15-Bit Output 4:4:4 Timing Diagram
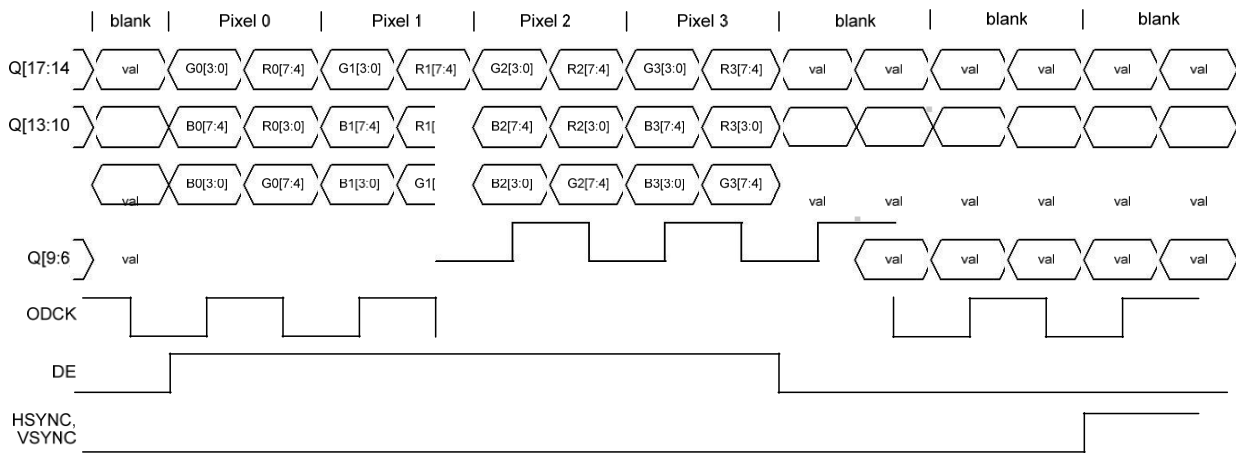
Figure 34. 12-Bit Output 4:4:4 Timing Diagram

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I²C Interfaces

HDCP E-DDC / I²C Interface

The HDCP protol requires values to be exchanged between the video transmitter and receiver. These values are exchanged over the DDC channel of the DVI interface. The E-DDC channel follows the I²C serial protol. In a design using the SiI9135/SiI9135A receiver, it has a nnection to the E- DDC bus with a slave address of 0x74. The I²C read operation is shown in Figure 35, and the write operation in Figure 36.
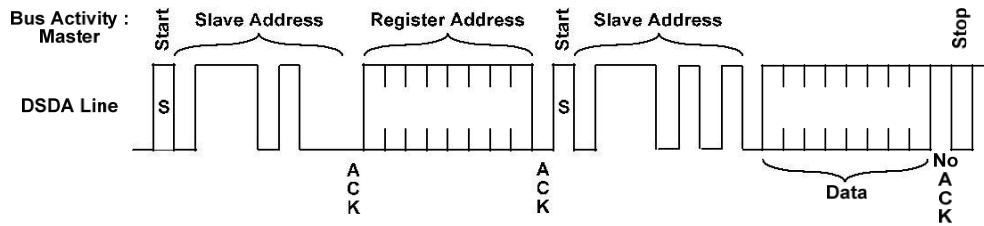
Figure 35. I²C Byte Read
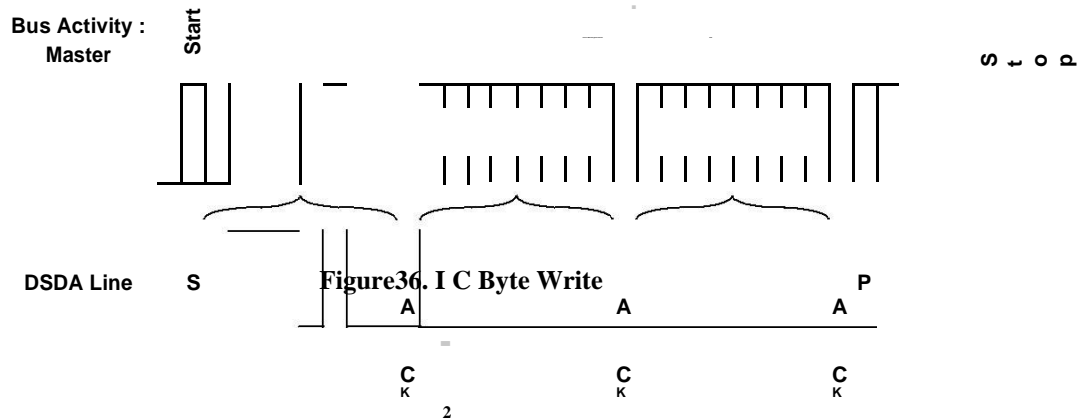
Figure36. I C Byte Write

Multiple bytes can be transferredin each transaction, regardless of whether they are reads or writes. The operations are similar to those in Figure 35 and Figure 36 except that there is more than one data phase. An ACK follow each byte

except the last byte in a read operation, which is followed by a NACK. Byte addresses increment, with the least significant byte transferred first, and the most significant byte last. See the I²C specification more inmation.

There is also a Short Read mat that improves the efficiency of reading the Ri register, which must be done every two sends while encryption is enabled. This transaction is shown in Figure 37. Note that the slave address phase is d, beca the register address is reset to 0x08 (Ri) after a hardware or software reset, and after the STOP ndition

on any preceding I2C transaction.
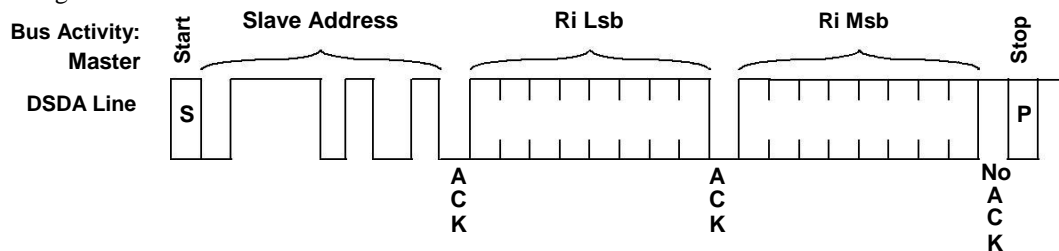
Figure 37. Short Read Sequence

Local I^{2}C Interface

The SiI9135/SiI9135A receiver has a send I^{2}C port accessible to the ntroller in the display device. It is separate from the E-DDC bus. The receiver is a slave device that responds to two seven-bit binary I^{2}C device addresses: 0x60 and 0x68. Two device addresses are d to acmmodate the long list of registers in the device, beca I^{2}C can access 256 registers at any one device address. This I^{2}C interface supports the read and write operations described above. It does not support the short read operation.

Note that the I^{2}C data pin the local I^{2}C bus is the CSDA pin, instead of the DSDA pin shown in the preceding figures.

Video Requirement I^{2}C Access

The receiver does not require an active video clock to access its registers from either the E-DDC port or the local I^{2}C port. Read-write registers can be written and then read back. Read- registers that provide values an active video or audio stream return indeterminate values, if there is no video clock and no active syncs.

the SCDT and CKDT register bits to determine when active video is being received by the chip.

I^{2}C Registers

The register values that are exchanged over the HDMI DDC I^{2}C serial interface with the receiver HDCP are described in the HDCP Specification in *Section 2.6 – HDCP Port*. Refer to the *SiI9125/SiI9135 Programmers Reference*

details on these and all the other registers.

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Design Remmetions

The remmetions provided in this section are based on the experience of   engineers and customers.   suggests that you ntact our technical representative an evaluation if a design a particular application deviates from these remmetions.

Power ntrol

The low- power standby feature of the SiI9135/SiI9135A receiver provides a design option of always providing power to the chip. Leaving the chip powered and using the PD# register bit to put it in a low power state can result in faster system response time, depending on the system Vcc supply ramp-up delay.

Power Pin Current Demands

The limits shown in Table 28 indicate the current demanded by each group of power pins on the device. These limits were characterized at maximum VCC, 0 ℃ ambient temperature, and fast-fast rner . Actual application current demands can be lower than these figures, and also depend on video resolution and audio clock frequency.

Table 28. Maximum Current Requirement Various Video Modes[2, 3, 4]

Mode	ODCK (MHz)	3.3 V Power Domain Currents (mA)			
		IOVCC33	AVCC33	XTALVCC	REGVCC
480p	27.0	39	51	,7	6
1080i	74.25	100	51	7	6
1080p	148.5	182	51	7	6
1080p @ 12-bit[1]	225	252	51	7	6

Mode	ODCK (MHz)	1.8 V Power Domain Currents (mA)		
		AVCC18	CVCC18	DVCC18
1080p	148.5	84	253	1
1080i	74.25	54	127	1
1080p @ 12-bit[1]	225	129	343	1

Notes:

4.   one re can be selected at a time. The RX0_ENor RX1 EN register bit turns off the unselected re, except the
1.   Measured with 12-bits/pixel video data.

2.   Measured with 192 kHz, 8-channel audio, except 480p mode which d 48 kHz, 8-channel audio.
3.   Measured with RGB input, vertical black-white/1-pixel stripe (Moire2) pattern, nverting to YCbCr output (digital IOVCC33).

termination to AVCC33.

HDMI Receiver DDC Bus Protection

The VESA DDC Specification (available at http://www.vesa.org) requires a 5 V signal path the DDC that carries the I^2C bus. The I^2C pins on the receiver chip are 5 V tolerant, and they are true open-drain I/O. The pull-up resistors on the DDC bus should be tied to the 5 V supply from the HDMI nnector. Refer to Figure 46 on page 61.

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Deupling Capacitors

Designers should include deupling and bypass capacitors at each power pin in the layout. These are shown schematically in Figure 41 on page 58. Place these mponents as close as possible to the receiver pins and avoid routing them through vias. Figure 38 shows the various types of power pins on the receiver.

VCC

C1   C2   L1

VCC

GND

Ferrite

C3

Via to GND
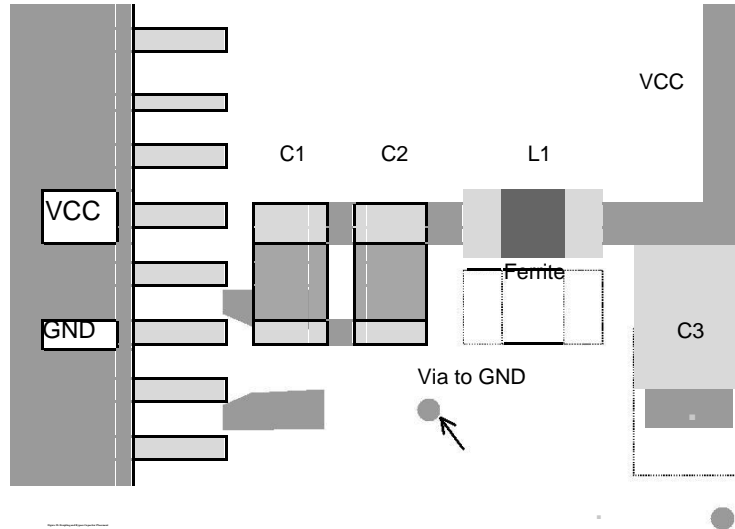
ESD Protection

The SiI9135/SiI9135A receiver can withstand an electrostatic discharge of up to 2 kV. In applications where higher protection levels are required, ESD limiting mponents can be placed on the differential lines ming into the chip.
These mponents typically have a capacitive effect, reducing the signal quality at higher clock frequencies on the link. the lowest capacitance devices possible. In no case should the capacitance value exceed 5 pF.

Series resistors can be included on the TMDS lines (refer to Figure 46 on page 61) to unteract the impedance effects of ESD protection diodes. The diodes typically lower the impedance beca of their capacitance. The resistors raise the impedance of the differential TMDS signal pairs to around 100 Ω, to stay within the HDMI specification.

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HDMI Receiver Layout

The layout guidelines below help to ensure signal integrity, and enurages the board designer to follow them if possible.

☐ Place the input and output nnectors that carry the TMDS signals as close as possible to the chip.

☐ Route the differential lines as directly as possible from the nnector to the device when using industry-stard HDMI nnectors.

☐ Route the two traces of each differential pair together.

☐ Minimize the number of vias through which the signal lines are routed.

☐ Lay out the two traces of each differential pair with a ntrolled differential impedance of 100 Ω.

• Cut-out all ground and power pper planes that are less than 45 mils below the TMDS traces within the area having the dimensions shown in Figure 39.

☐ If ESD suppression devices or mmon mode chokes are d, place them near the HDMI nnector, away from the receiver. Do not place them over the ground and power plane cutout described above.

Beca HDMI buffers are tolerant of skews between differential pairs, spiral skew mpensation path length differences is not required.
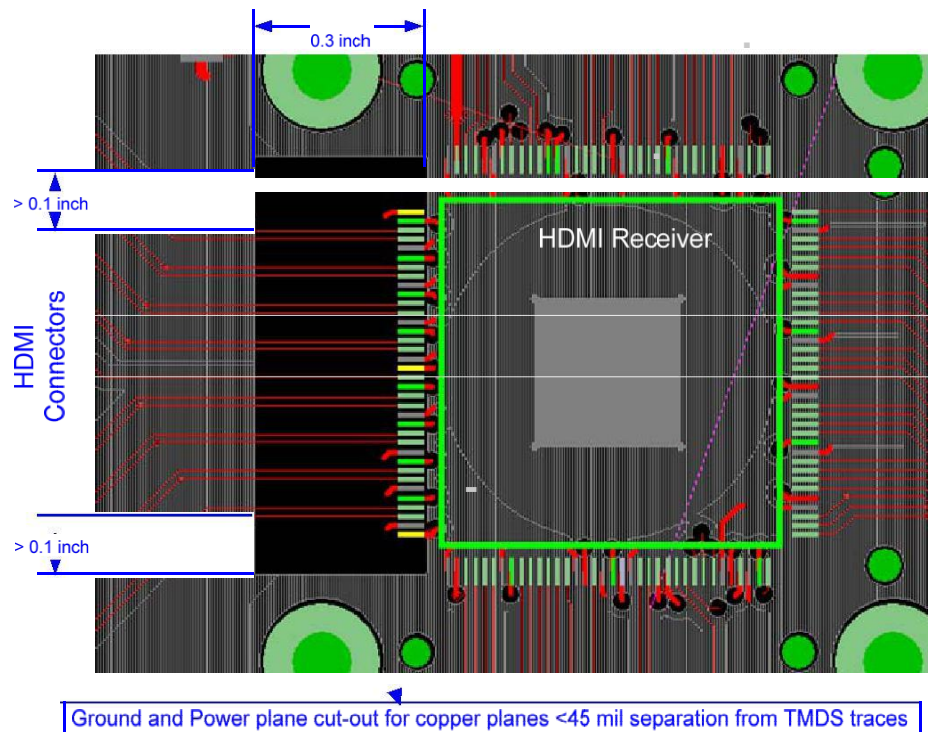
Figure 39. Cut-out Reference Plane Dimensions

The sixteen TMDS traces nnect directly from the HDMI nnectors to the pins on the receiver. The differential trace impedance should be 100 Ω and the single-ended trace impedance should be 50 ohms. Trace width and pitch depend on the PCB nstruction. Not all nnections are shown; the drawing demonstrates routing of TMDS lines without crossovers, vias, or ESD protection. Refer to Figure 40.
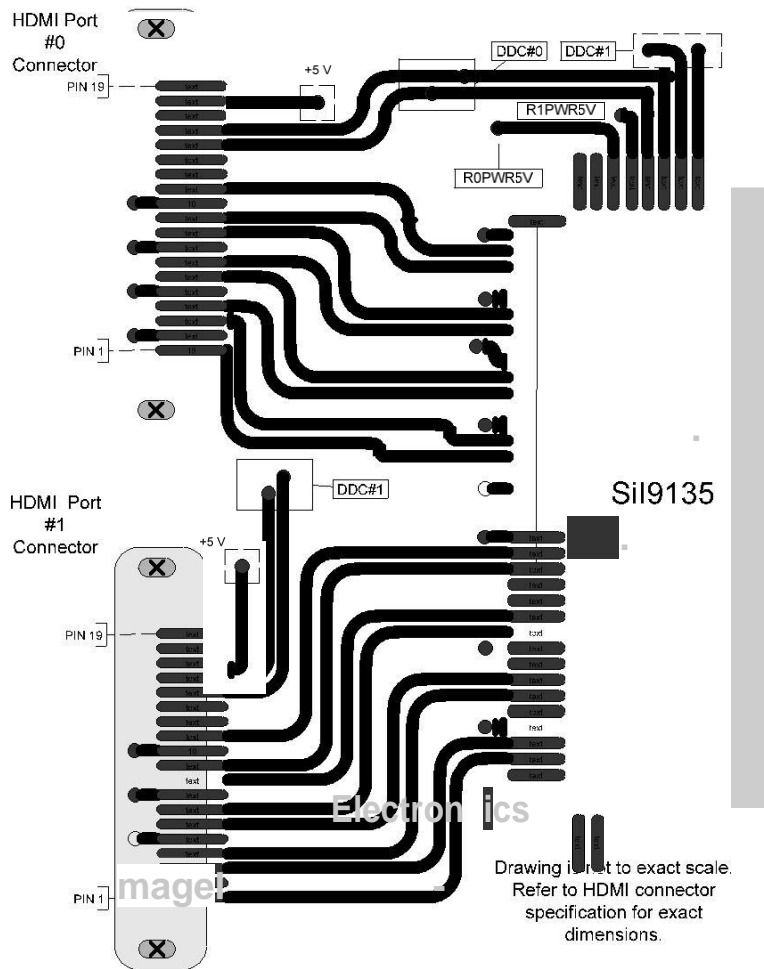
Figure 40. HDMI to Receiver Routing – Top View

EMI nsiderations

Electromagnetic interference is a function of board layout, shielding, receiver mponent operating voltage, frequency of operation, and so on. When attempting to ntrol emissions, it is important not to place any passive mponents on the differential signal lines, except ESD protection described earlier. The differential signaling d in HDMI is inherently low in EMI if the routing remmetions described in this section are followed.

The PCB ground plane should extend unbroken as much of the receiver chip and associated circuitry as possible, with all ground pins of the chip using a mmon ground.

XTALIN Clock Requirement

Description

The SiI9135/SiI9135A receiver s the clock at the XTALIN/XTALOUT pin pair to ntrol the audio pipeline. This clock also ntrols interrupt processing and the reading of HDCP keys.

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The XTALIN/XTALOUT pin pair must be driven with a clock in all applications, even when the design does not support audio processing. The clock frequency must be within the range of 26–28.5 MHz.

Remmetion

designs that do not support audio, the XTALIN pin can be nnected to an ordinary 27 MHz LVTTL clock source, which is mm available on HDMI sink designs. This clock source does not have to have low jitter. If an LVTTL clock signal is applied to XTALIN, leave the XTALOUT pin unnnected.

Typical Circuit

Representative circuits application of the SiI9135/SiI9135A HDMI receiver chip are shown in Figure 41 through Figure 45. a detailed review of your intended circuit implementation, ntact your   representative.

Power Supply Deupling
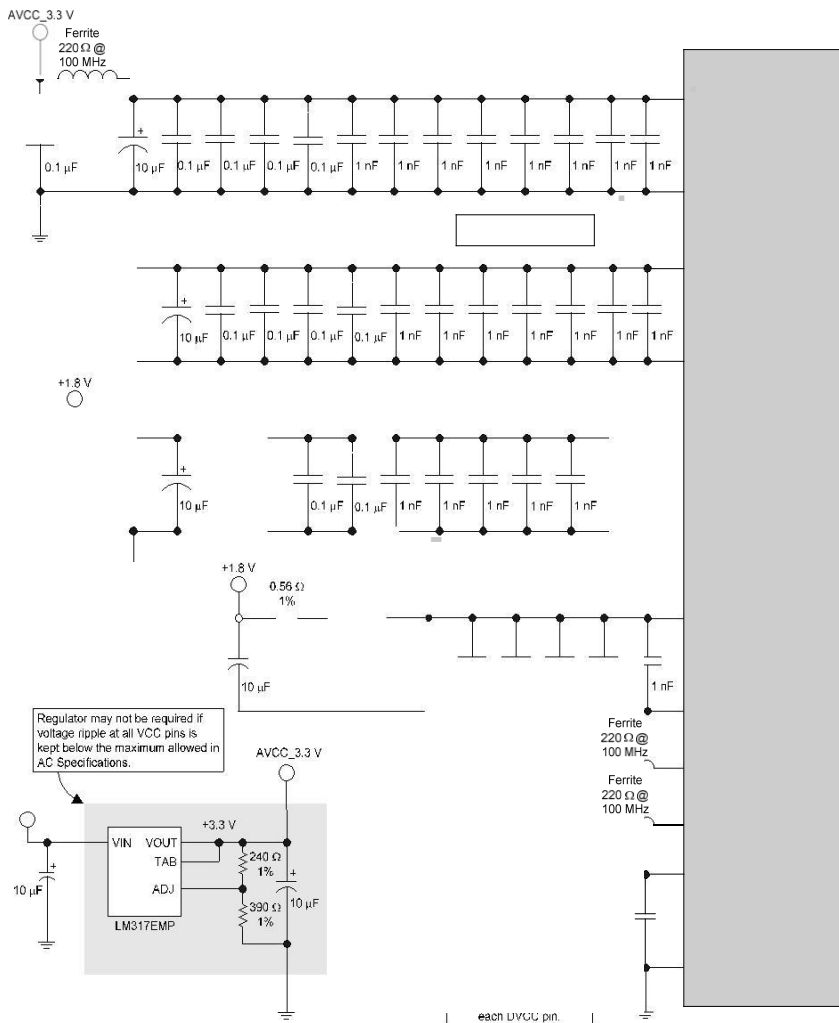
Figure 41. Power Supply Deupling and PLL Filtering Schematic

The ferrite on AVCC18 attenuates noise at 10 kHz and above. A parasitic resistor helps minimize the peaking. An example device (surface mount, 0805 package) is part number MLF2012DR82 from TDK. A data sheet is available at http://www.tdk..jp/tefe02/e511_MLF2012.pdf

HDMI Port TMDS nnections
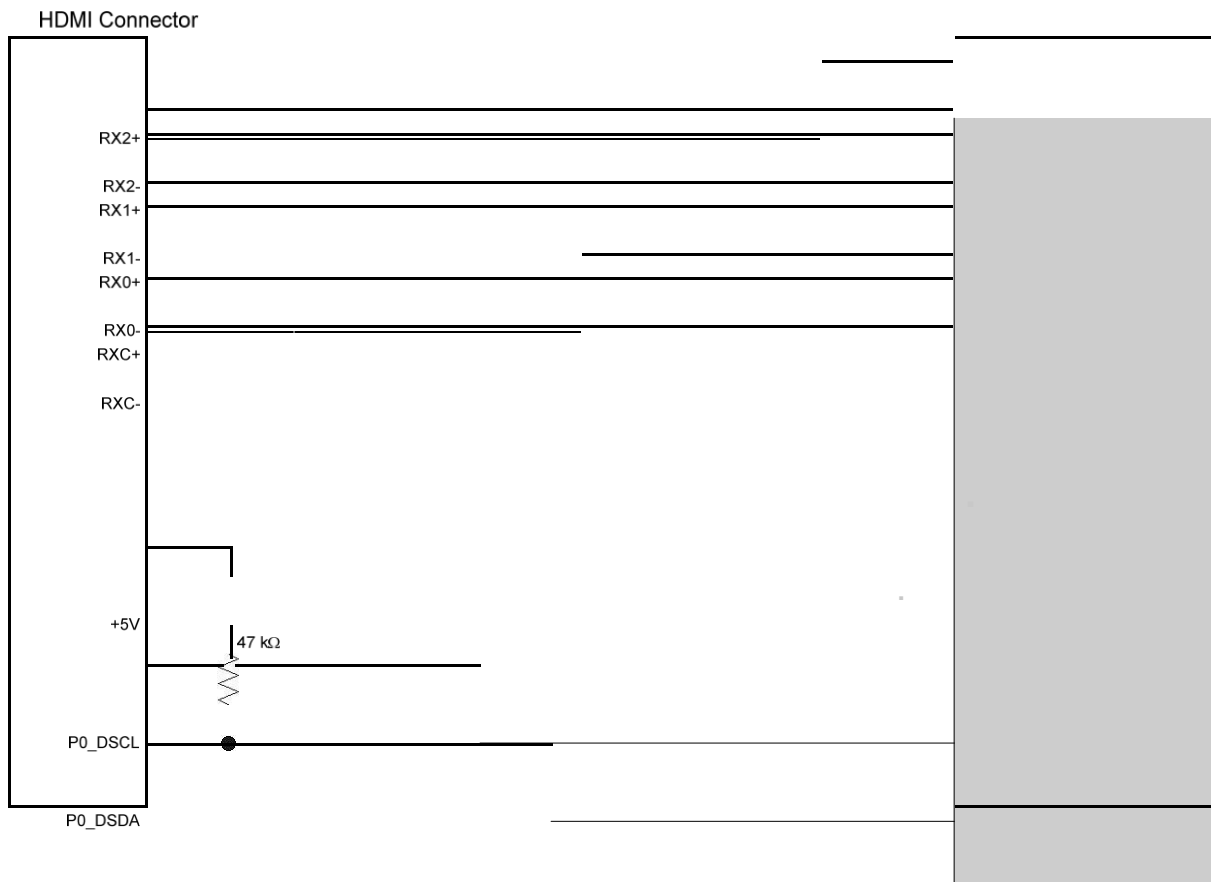
Figure 42. HDMI Port nnections Schematic

Notes: Repeat the schematic the other HDMI input port.

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Digital Video Output nnections

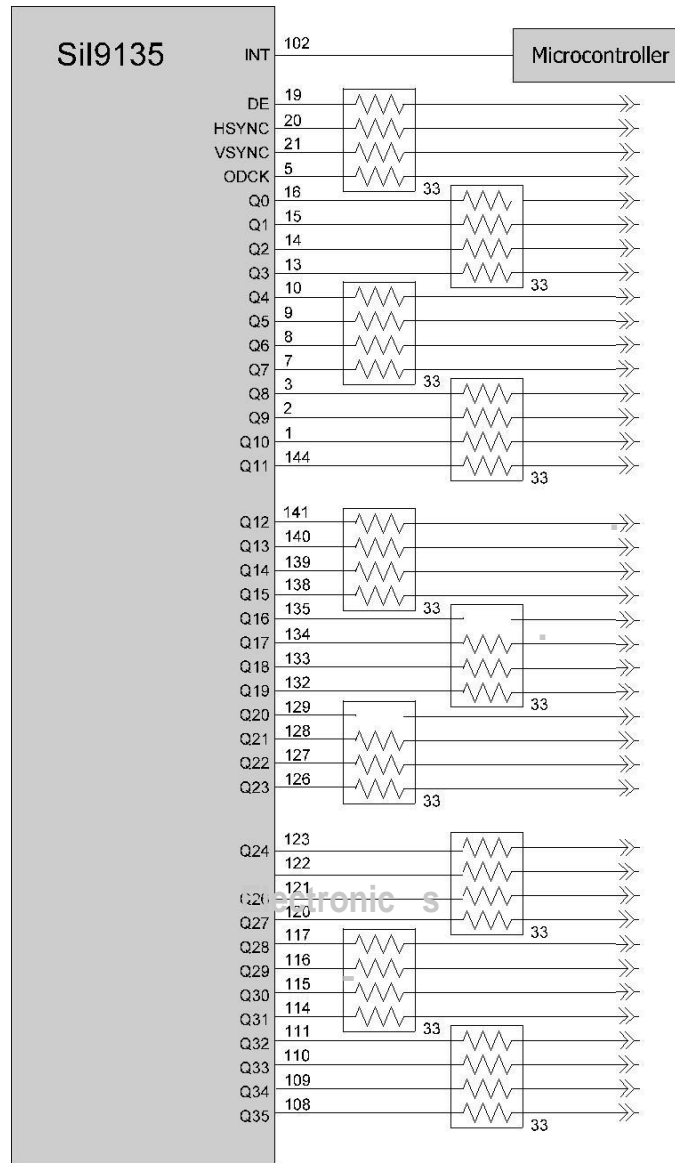**Figure43. Digital Display Schematic**

The INT output can be nnected as an interrupt to the microntroller, or the microntroller can poll register 0x70 (INTR_STATE) to determine if any of the enabled interrupts has occurred. Refer to the *SiI9125/SiI9135 Programmers Reference* details. The VSYNC output can be nnected to the microntroller if it is necessary to monitor the vertical refresh rate of the inming video.

Digital Audio Output nnections
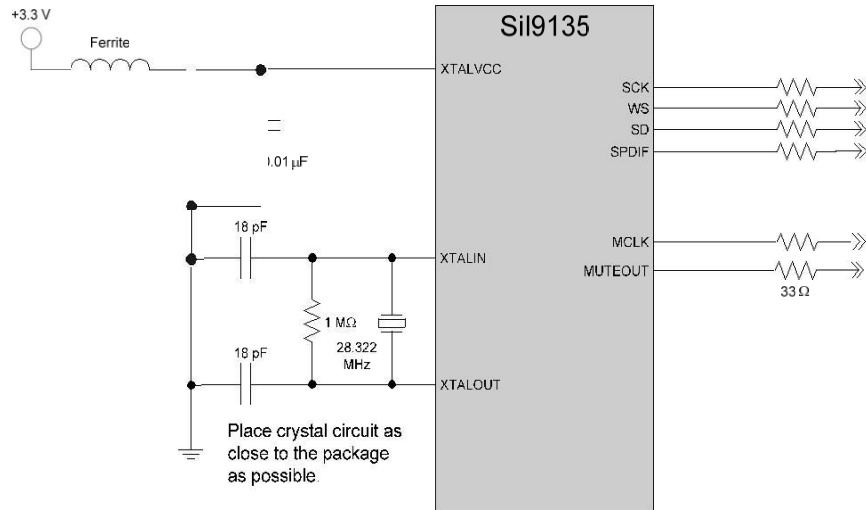
Figure 44. Audio Output Schematic

ntrol Signal nnections
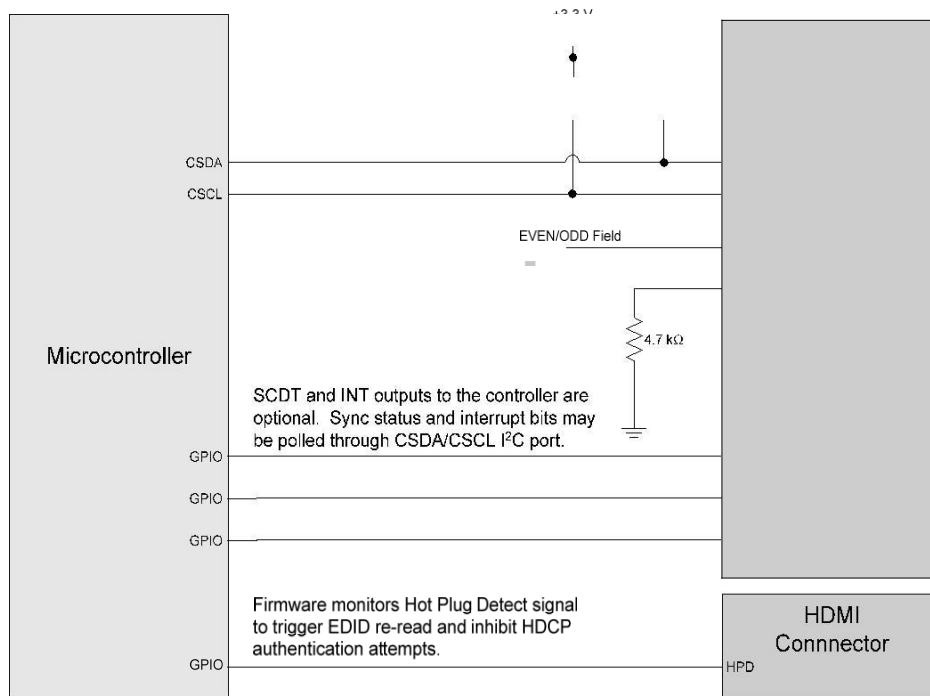
Figure 45. ntroller nnections Schematic

Layout

shows an example of routing TMDS lines between the receiver and the HDMI nnector.

TMDS Input Port nnections

DDC SCL
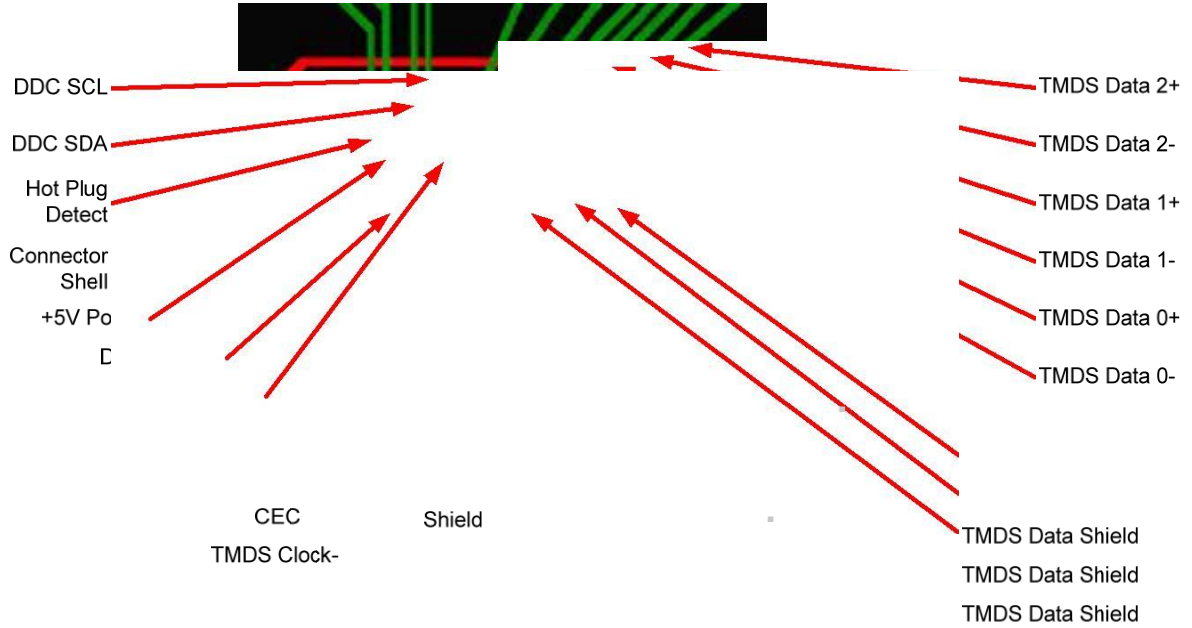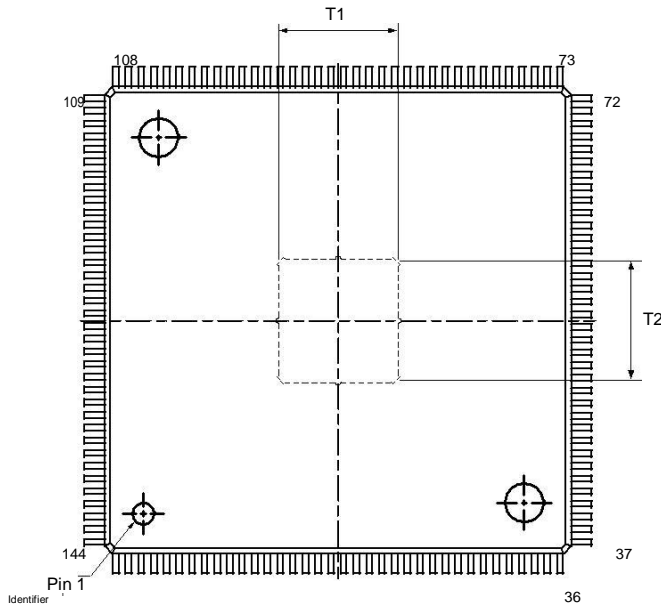DDC SDA
Hot Plug Detect
Connector Shell
+5V Po
C

CEC   Shield
TMDS Clock-

TMDS Data 2+
TMDS Data 2-
TMDS Data 1+
TMDS Data 1-
TMDS Data 0+
TMDS Data 0-

TMDS Data Shield
TMDS Data Shield
TMDS Data Shield

Figure 46. TMDS Input Signal Assignments

Packaging

ePad Enhancement

The SiI9135/SiI9135A receiver is packaged in a 144-pin TQFP package with an ePad™. The ePad dimensions are shown in Figure 47.

ePad Dimensions: Amkor and SPIL

Item	Description	Typ	Max
T1	ePad height	4.60	4.64
T2	ePad width	5.20	5.24

ePad Dimensions: ASE

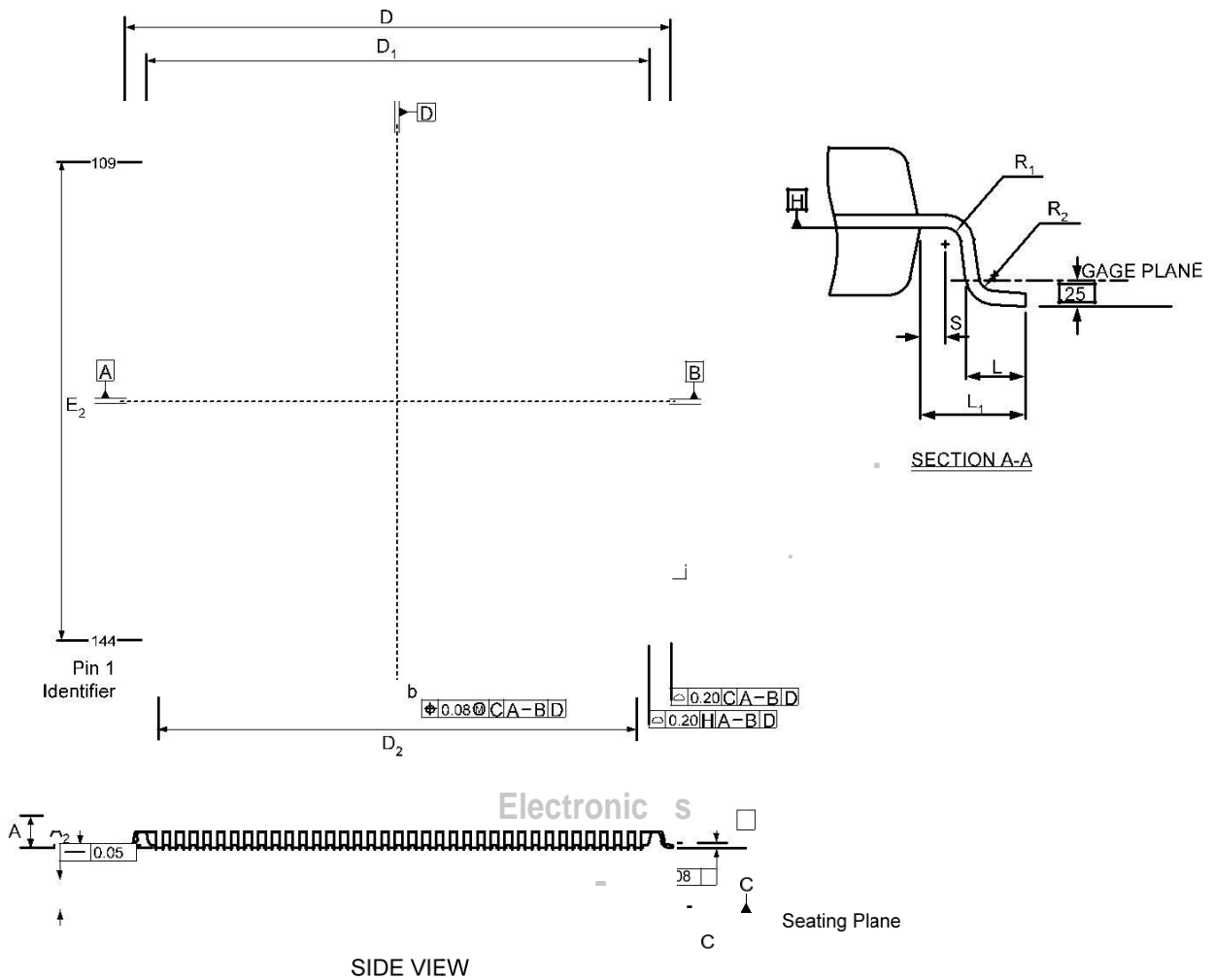| Item	Description	Typ	Max
T1	ePad height	5.25	5.29
T2	ePad width	5.25	5.29

All dimensions are in millimeters.

The ePad is centered on the package center lines. The measurement tolerance is ±0.04 mm all manufacturers. The ePad tab dimensions may vary.

A clearance of at least 0.25 mm should be provided on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical shorts.

remmends that the ePad be soldered to the PCB and electrically grounded on the PCB. The ePad must not be nnected toany other voltage level.

Figure 47. ePad Diagram

PCB Layout Guidelines

PCB layout designers should refer to application note *PCB Layout Guidelines: Designing with Exposed*

the Exposed Pad.

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Package Dimensions

SECTION A-A

SIDE VIEW

JEDEC Package de MS-026-AFB

Item	Description	Min	Typ	Max	Item	Description	Min	Typ	Max
A	Thickness	1.00	1.10	1.20	b	Lead width	0.17	0.22	0.27
A1	Stand-off	0.05		0.15	C	Lead thickness	0.09	—	0.20
A2	Body thickness	0.95	1.00	1.05	e	Lead pitch		0.50 BSC	
D	Footprint		22.00 BSC		L	Lead foot length	0.45	0.60	0.75
E	Footprint		22.00 BSC		L_1	Total lead length		1.00 REF	
D_1	Body size		20.00 BSC		R_1	Lead radius, inside	0.08	—	—
E_1	Body size		20.00 BSC		R_2	Lead radius, outside	0.08	—	0.20
D_2	Lead Row Width		17.5 BSC		S	Lead horizontal run	0.20	—	—
E_2	Lead Row Width		17.5 BSC						

Dimensions in millimeters.

Overall thickness A = A1 + A2.

Figure 48. Package Diagram

Marking Specification

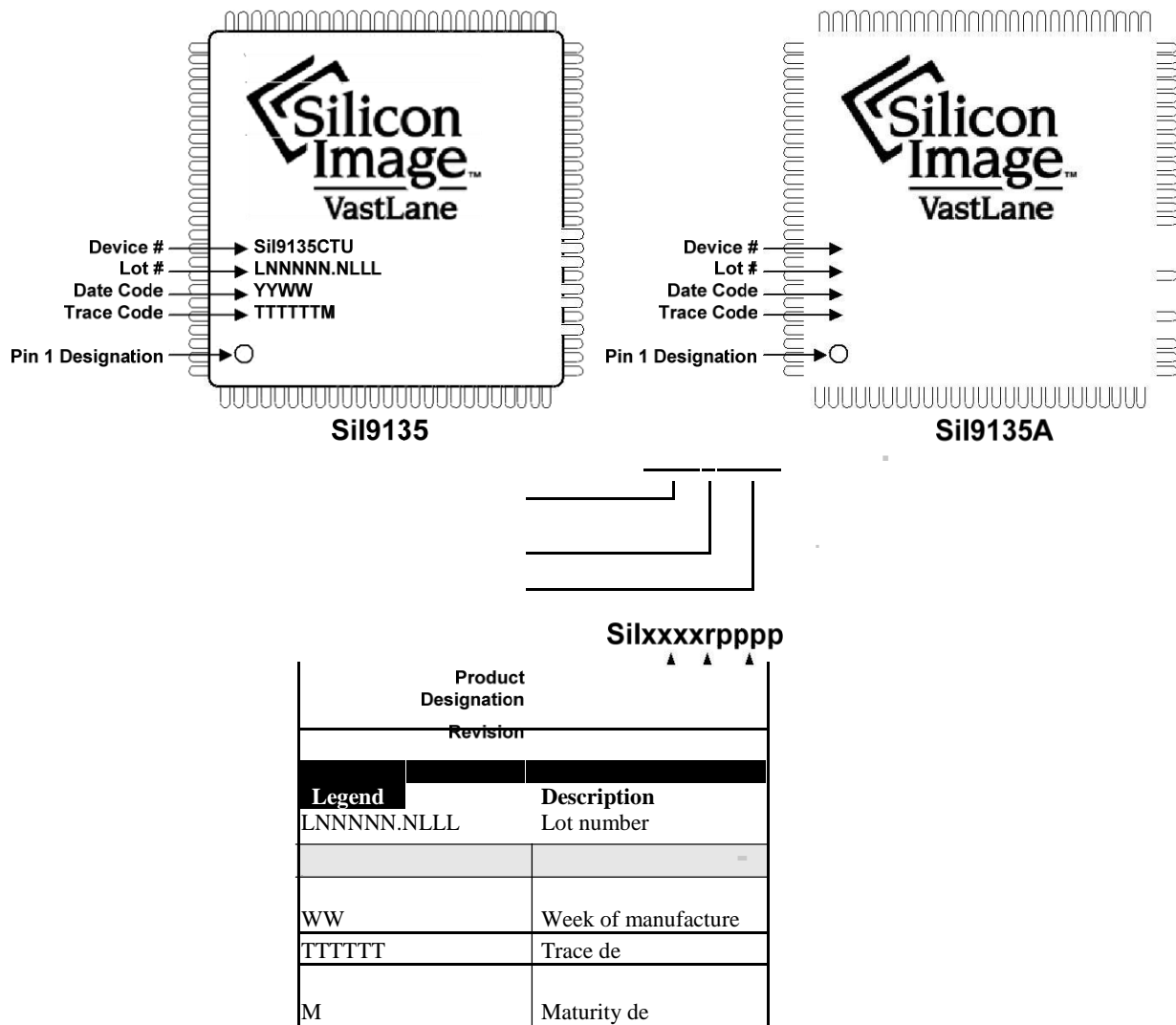Drawing is not to scale and pin unt shown is representative. Refer to specifics in Figure 48 on page 63.

Figure 49. Marking Diagram

Legend	Description
LNNNNN.NLLL	Lot number
WW	Week of manufacture
TTTTTT	Trace de
M	Maturity de

The universal package may be d in lead-free and ordinary process lines

Ordering Inmation

Production Part Numbers:

TMDS Input Clock Range	Part Number
25–225 MHz	SiI9135CTU
25–225 MHz	SiI9135ACTU

SiI-DS-0206-F02

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References

Stards Documents

Table 29 lists the abbreviations d in this document. ntact the responsible stards groups listed in Table 30 more inmation on these specifications.

Table 29. Referenced Documents

Abbreviation	Stards publication, organization, and date	
HDMI	*High Definition Multimedia Interface*, Revision 1.2, HDMI nsortium	
HCTS	*HDMI mpliance Test Specification,* Revision 1.1, HDMI nsortium, June 2004	
HDCP	*High-bandwidth Digital ntent Protection*, Revision 1.1, Digital-ntent Protection, LLC; February 2000	
DVI	*Digital Visual Interface*, Revision 1.0, Digital Display Working Group; April 1999	
E-EDID	*Enhanced Extended Display Identification Data Stard*, Release A Revision 1, VESA; Feb. 2000	
CEA861	*A DTV Profile Unmpressed High Speed Digital Interfaces*, EIA/CEA; January 2001	
CEA861B	*A DTV Profile Unmp. High Speed Digital Interfaces*, Draft 020328, EIA/CEA; March 2002	
EDDC	*Enhanced Display Data Channel Stard*, Version 1, VESA; September 1999	

Table 30. Stards Groups ntact Inmation

Stards Group	Web URL	e-mail	phone
ANSI/EIA/CEA	http://global.ihs.m	global@ihs.m	800-854-7179
VESA	http://www.vesa.org		408-957-9270
DVI	http://www.ddwg.org	ddwg.if@intel.m	
HDCP	http://www.digital-cp.m	info@digital-cp.m	
HDMI	http://www.hdmi.org	admin@hdmi.org	

Documents

The following are available from your   sales representative.

Table 31. Publications

Document	Title	
SiI-AN-0118	*SiI9021/9031 HDMI Receiver Software Application Note*	
SiI-PR-0042	*SiI9125/9135 HDMI Receiver Programmer's Reference*	

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