SiI9777 18 Gb/s HDCP 2.2 Transmitter and Port Processor for HDMI 2.0 and MHL 3

Preliminary **Data Sheet**

SiI-DS-1166-0.80

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Glossary

A glossary of terms used in this document.

Acronym	Definition
ARC	Audio Return Channel
AVR	Audiovisual Receiver
CBUS	Control Bus
CMS	Color Management System
DDC	Display Data Channel
eCBUS	Enhanced CBUS
EDDC	Enhanced Display Data Channel
EDID	Extended Display Identification Data
ESD	Electrostatic Discharge
FRC	Frame Rate Control
GPIO	General Purpose Input/Output
HBRA	High Bitrate Audio
HDCP	High-bandwidth Digital Content Protection
HDMI	High Definition Multimedia Interface
HPD	Hot Plug Detect
I^2C	Inter-Integrated Circuit
LQFP	Low Profile Quad Flat Package
MCU	Microcontroller Unit
MHL	Mobile High-Definition Link
MISO	Master In Slave Out
MOSI	Master Out Slave In
oCBUS	Operating CBUS
OTP	One Time Programmable
PCM	Pulse Code Modulation
S/PDIF	Sony/Philips Digital Interface Format
SPI	Serial Peripheral Interface
TMDS	Transition Minimized Differential Signaling
VTPG	Video Test Pattern Generator

1. General Description

The Silicon Image SiI9777 is a versatile High Definition Multimedia Interface 2.0 (HDMI®) transmitter/port processor, with support for Mobile High-Definition Link 3 (MHL®) and High-bandwidth Digital Content Protection 2.2 (HDCP). The device's 18 Gb/s transmitter and receiver features support delivery of full resolution 4K Ultra High Definition (UltraHD) 4:4:4 video to a 4K television set at 50 Hz or 60 Hz frame rate.

As port processor, all four inputs support HDMI 2.0 at up to 18 Gb/s, and two of the inputs can also support MHL 3 input at resolutions of up to 4K @30 Hz. The three outputs offer a flexible configuration, including the ability to split an 18 Gb/s signal into two 9 Gb/s outputs. Audio and video can be routed to separate transmitters and two separate 300 MHz output streams can be routed from two input sources.

As a transmitter, the SiI9777 supports one output with HDMI 2.0 at up to 18 Gb/s with HDCP 2.2. A second output offers legacy-compatible HDMI 1.4 with audio output only.

In transmitter configuration, the SiI9777 can merge two video input streams up to 9 Gb/s each into one 18 Gb/s output stream. This is useful to merge two 300 MHz input streams that contain one-half of a 4K × 2K @ 60 Hz 4:4:4 frame each, into one 18 Gb/s, 600 Mega-characters/second/channel (Mcsc) stream with HDCP 2.2.

As a transmitter, the SiI9777 can also convert certain types of reduced blanking formats such as a 337 MHz TMDS™ input of 10-bit 4K @ 60 Hz 4:2:0 into an HDMI 2.0 standard 4K @ 60 Hz 4:2:2 10-bit output with HDCP 2.2. This enables the design of a set-top box that can deliver full quality, 10-bit UltraHD with HDCP 2.2, using a decoder circuit built with HDMI 1.4 technology.

The SiI9777 implements the HDCP 2.2 Specification to protect the delivery of premium content. HDCP 2.2 can be applied in transmitter, receiver, and repeater configurations. HDCP 1.4 support is also included, allowing the transmitter to interoperate with the installed base of legacy source devices.

The SiI9777 transmitter/port processor supports AVR compatibility mode, which enables it to output audio/video content through one transmitter with HDCP 1.4 or 2.2 content protection, while the second transmitter outputs audio-only content through a transmitter with HDCP 1.4 protection.

An internal Microcontroller Unit (MCU) greatly simplifies software development and reduces the amount of I^2C data transactions required to control the transmitter. The MCU firmware is loaded into the transmitter from external SPI flash at reset. A slim programming interface allows host control with minimal software effort.

1.1. HDMI and MHL Inputs

- Four 18 Gb/s HDMI 2.0 compatible input ports
- HDCP 2.2 and HDCP 1.4 support on all four ports
- MHL 3 with HDCP 2.2, including MHL 1.x and 2.x compatibility, available on two ports

1.2. HDMI Outputs

- One 18 Gb/s HDMI 2.0 compatible output supports up to 18 Gb/s (6 Gb/s per channel). Supports HDMI 2.0 and 1.4 up to 600 Mcsc with HDCP 1.4 and 2.2
- One output supports HDMI 1.4
- One output supports HDMI 1.4 audio-only applications without HDCP
- High-speed port supports video resolutions up to UltraHD 4K × 2K @ 50/60 Hz with RGB or YCbCr 4:4:4 pixel encoding

1.3. Video Merging

- Merges two video input streams into one output stream with double the input clock frequency
- Even/Odd Pixel merge mode
- Left/Right Frame merge mode
- Combined stream output with HDMI 2.0 compatible signaling

1.4. Video Splitting

- Splits a single 18 Gb/s HDMI 2.0 input stream into two HDMI 1.4 output streams
- Even/Odd Pixel split mode
- Left/Right Frame split mode
- Supports up to 600 Mcsc or 18 Gb/s bandwidth

1.5. Color Management System

Independent control of RGBCMYW chromaticity coordinates for gamut adjustment

1.6. Video Format Conversion

- BT.601/BT.709/BT.2020 color space conversion
- xvYCC colorimetry support
- Supports 8/10-bit YCbCr 4:2:0 to 8/10/12-bit 4:2:2/4:4:4 chroma upsampling
- Supports 8/10/12-bit YCbCr 4:2:2 to 8/10/12-bit 4:4:4 chroma upsampling and downsampling

1.7. Audio Features

- Audio routing supports up to 8-channel 192 kHz PCM and compressed audio formats, including high-bitrate formats
- Able to route audio to one of the transmitters independently of the video output
- Audio insertion through S/PDIF or 2-channel I^2S input
- Audio extraction to S/PDIF or 8-channel I^2S
- S/PDIF output signal supports reception of single mode Audio Return Channel (ARC) signal from downstream device
- S/PDIF input supports single mode transmission of ARC signal to upstream device

1.8. Programming Interface

- Local I^2C bus
- Serial Peripheral Interface (SPI)

1.9. Packaging

208-pin, 28 mm × 28 mm, 0.5 mm pitch LQFP package with an exposed pad (ePad)

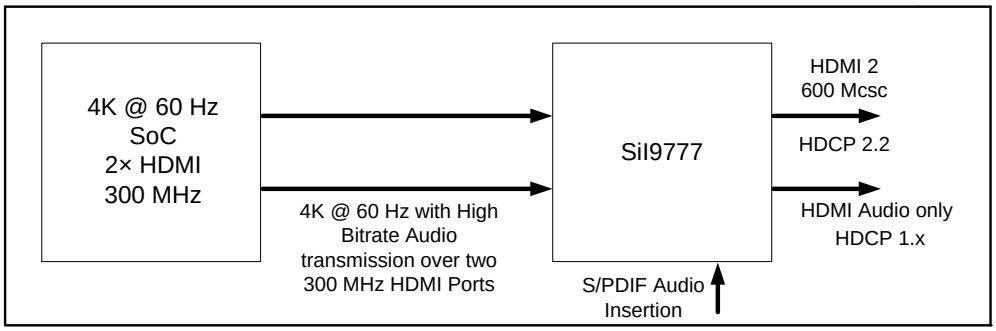


Figure 1.1. Typical 4K @ 60 Hz Transmitter Application

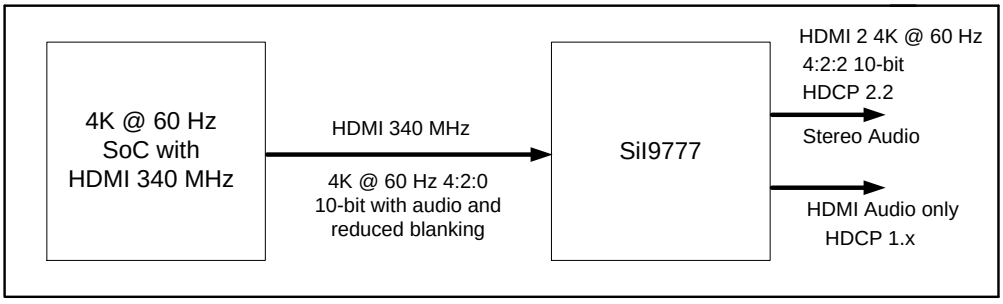


Figure 1.2. Typical 4K @ 60 Hz 4:2:0 Transmitter Application

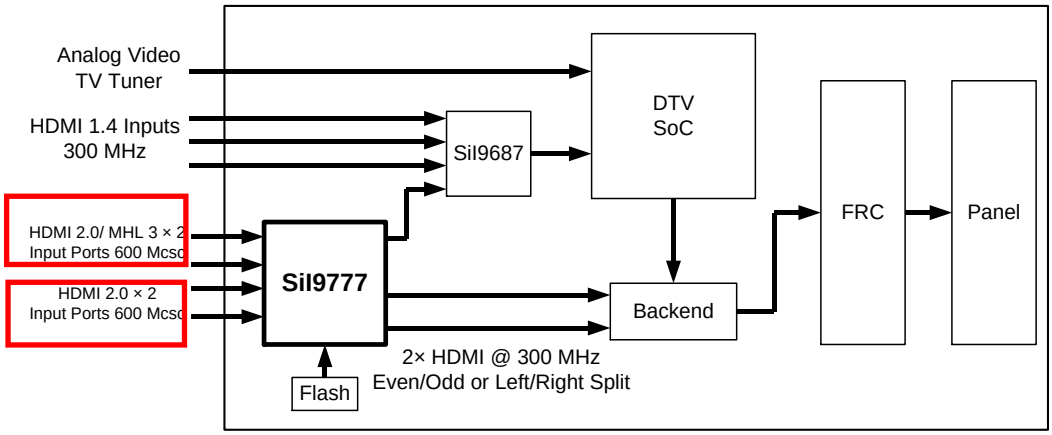


Figure 1.3. Typical 4K @ 60 Hz Port Processor Application

2. Functional Description

Figure 2.1 shows the block diagram of the SiI9777 transmitter/port processor.

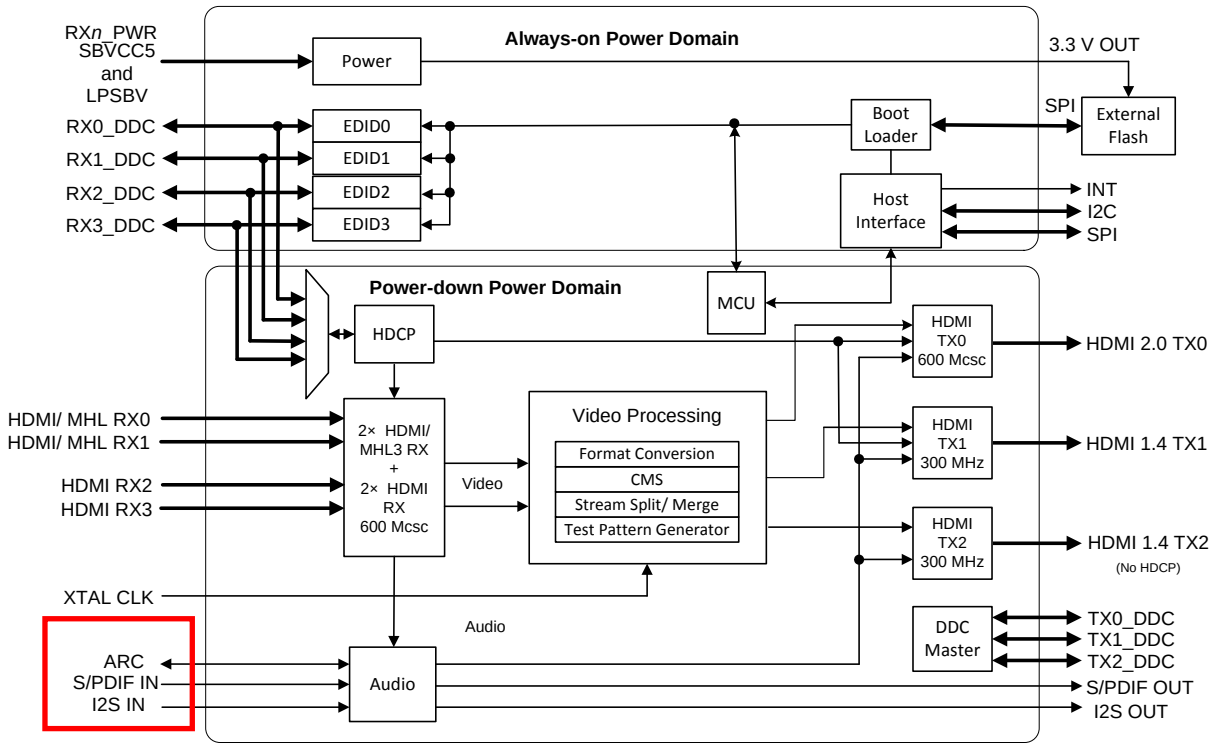


Figure 2.1. Functional Block Diagram

2.1. Power Domains

The SiI9777 transmitter/port processor has separate power domains in order to support low and ultra-low system power states. The low power domain is called the AON (Always On) power domain, and the main power partition is called the PDN (Power Down Domain). The AON domain is actually two power domains. The Ultra-Low power domain derives power from the LPSBV (5 V) power pin, which supplies power for logic supporting wakeup detection on the MHL CBUS RX input and the corresponding signals WAKEUP_INT, WAKEUP, and LPSB_RSTN.

The main AON standby power domain derives power through either SBVCC5V or one of the RX*n*_PWR5V inputs. From this power source, internal voltage regulators supply the internal 3.3 V and 1.0 V standby power for the logic and I/O. The functions that are powered by the AON power are as follows:

- Boot loader and SPI Master (Flash Interface)
- Certain registers in the AON domain logic
- EDID read through RX DDC
- RX cable detection logic
- Reset logic

The PDN (Power Down) Domain contains all of the primary chip functions and is powered by the main power supply inputs when the system is in the full power on state.

2.2. HDMI 2.0 Transmitter – Port 0

The SiI9777 transmitter/port processor Port 0 features a TMDS core with the capability to transmit data at up to 6 Gb/s per channel, for a total data bandwidth of 18 Gb/s. This allows transmitter Port 0 to output UltraHD 4:4:4 format at 50 or 60 Hz in HDMI 2.0 mode. Two 300 MHz HDMI video streams on the receiver ports can be merged to produce a 600 Mcsc video stream on Port 0. Port 0 supports HDCP 2.2 and HDCP 1.4 encryption.

2.3. HDMI 1.4 Transmitter – Port 1

The SiI9777 transmitter/port processor Port 1 is an HDMI 1.4 transmitter with a 300 MHz TMDS core. This port is normally used in a TX application to carry secondary video, audio or the primary link in a split mode UHD configuration. Transmitter Port 1 can transmit data at up to 9 Gb/s (3 Gb/s per channel) over the HDMI link, and comes with a built-in source termination to minimize reflection and ensure the highest quality of the transmitted signal. This port supports HDCP 1.4 encryption.

2.4. HDMI 1.4 Transmitter – Port 2

The SiI9777 transmitter/port processor Port 2 is an HDMI 1.4 transmitter with a 300 MHz TMDS core. It is typically used to carry the secondary link in a split mode UltraHD configuration. Transmitter Port 2 can transmit data at up to 9 Gb/s (3Gb/s per channel) over the HDMI link, and comes with a built-in source termination to minimize reflection and ensure the highest quality of the transmitted signal. This port does not support HDCP encryption.

2.5. Video Stream Merging and Processing

The SiI9777 transmitter/port processor provides a merging function that can be used to merge two video input streams into one video stream with double the input clock frequency. See the Merging Two Video Streams section on page 17.

Additional processing can be performed on the video output data to reformat it, so that it matches the requirements of the downstream devices.

Data processing functions provided are chroma upsampling, color space conversion and chroma downsampling. Additional functions include a dither/rounding module that can be used to minimize quantization errors when reducing color depth and a range clipping module for enforcing a programmable dynamic range for the video output. The blanking level and sync polarity of the video output are adjustable through this module.

2.6. Video Stream Splitting

On the sink device side, the inverse to Video Stream Merging is to split the video stream into two substreams. Streams can be split in two formats; left/right which splits the horizontal line into two halves, and odd/even pixel. Normally the split function is used in conjunction with splitting a 600 Mcsc stream into two 300 MHz HDMI 1.4 streams, but lower resolution streams can be split as well. See the Splitting the Video Stream section on page 21 for more information.

2.7. Video Test Pattern Generator

The SiI9777 transmitter/port processor provides a Video Test Pattern Generator (VTPG) to facilitate transmission of internal video test patterns to any Transmitter Port. For details see the Video Test Patterns section on page 24.

2.8. HDCP Cores

The HDCP Cores contain the necessary logic to encrypt HDCP audio/visual streams and support HDCP authentication and repeater check. Two separate HDCP engines are available for HDCP encryption: one supports HDCP 1.4 and the other supports HDCP 2.2.

Both Transmitter Port 0 and Port 1 support HDCP encryption. Only Transmitter Port 0 supports HDCP 2.2 in addition to HDCP 1.4. Transmitter Port 0 can automatically choose HDCP 1.4 mode or HDCP 2.2 mode by reading the HDCP 2 version register of the downstream device over the DDC channel. The SoC application can query the HDCP status through the host interface. All receiver ports support HDCP 1.4 and 2.2 decryption.

2.9. HDMI Receivers

The SiI9777 transmitter/port processor supports four HDMI receiver ports. The receivers feature the latest TMDS cores that are capable of receiving data at 300 MHz simultaneously on two of its 4 ports, or one at 600 Mcsc. In addition, the HDMI receivers accept TMDS data and decode the data to extract video, audio, and auxiliary data from the input stream. For example, when the SiI9777 device transmits UltraHD 4:4:4 @ 50/60 Hz video, data from two 300 MHz TMDS links are merged in the video processing block to produce a single UltraHD 4:4:4 @ 50/60 Hz video stream.

2.10. Audio Data Path

The audio streams extracted by any of the receivers are routed for transmission to the downstream device. An audio multiplexer selects which audio stream the transmitter will combine with the outgoing video signal, to form the HDMI output stream. Audio streams can be inserted to any of the three transmitters.

Supported audio types include PCM audio streams with sample rates ranging from 32 kHz to 192 kHz and high bitrate compressed audio formats, such as Dolby® TrueHD and DTS-HD Master Audio™, at sample rates of up to 768 kHz. Other supported audio formats include low bitrate compressed formats, such as Dolby® Digital, DTS, and 8-channel one bit audio (DSD) format at 44.1 and 88.2 kHz sample rates.

2.11. Audio Return Channel

This pin is used to either transmit or receive an IEC60958-1 audio stream over the utility pin of the HDMI cable, using single-mode ARC transmission.

In ARC receiver mode, this pin receives an S/PDIF signal from an ARC transmitter-capable Sink and outputs it on the AO_SPDIF pin. In transmit mode, the Audio Return Channel (ARC) transmitter takes the audio signal from the S/PDIF input pin and sends it upstream over the HDMI cable to the Source or Repeater device.

In either transmit or receive mode, the ARC channel supports 32, 44.1 and 48 kHz audio sample rates.

2.12. Boot Loader

The Boot Loader block fetches the EDID defaults, configuration settings, and MCU binary from the external flash memory. The boot sequence is triggered when the standby power is applied to the device or when the RESET_N pin of the device is toggled.

2.13. Microcontroller Unit

The internal Microcontroller Unit (MCU) integrates all SiI9777 internal functions and is powered up when main power is applied. The MCU also provides a high-level control interface to allow an external application controller to change operation modes or retrieve status information.

2.14. Host Interface

The active state and modes of the SiI9777 transmitter/port processor can be controlled through the local I^2C or SPI slave bus interface.

The local I^2C interface supports up to 400 kHz data transfer rate. The device address of the local I^2C interface can be set to either 0x40 or 0x42 through a strapping option available on the GPIO0 pin. An INT pin generates a notification to the host controller of a status change in the device that requires attention from the host controller. See the Local Host Interface section on page 28 for more information.

2.15. Color Space Conversion

The SiI9777 transmitter/port processor supports many different color space conversion options. These are performed in individual small steps. This modular concept allows the most flexibility to support different standards. See the Color Space Conversion section on page 27 for more information.

3. Feature Information

3.1. Video Input Format Support

The SiI9777 transmitter/port processor can support a large array of video formats. Table 3.1 shows a sample list of video input formats supported, other formats not listed may also be supported. The rules to implement support for particular video formats are as follows:

- TMDS link speed cannot exceed 600 Mcsc, or equivalent pixel clock cannot exceed 600 MHz.
- RX ports support video formats with a link speed up to 600 Mcsc, including video formats with deep color.
- 4:2:0 upsampling can only be done with 8-bit or 10-bit per component input data, not 12-bit.
- "Retiming" (that is the conversion from reduced blanking to standard blanking) can only be done with up to 30 bits per pixel.
- Split/merge can only be performed with up to 24-bit per pixel. 4:2:0 or 4:4:4/RGB data with 8-bit per component, and 4:2:2 with up to 12-bit per component are supported.
- Downsampling to 4:2:0 is not supported.
- TX0 supports video formats with up to 600 Mcsc. Deep color is supported within that link speed limit.
- TX1 and TX2 support video formats with up to 300 MHz pixel clock or TMDS clock. Deep color is supported within that frequency limit.

Table 3.1. Video Input Formats – HDMI Video Modes

Video Mode	3D Mode	Video Resolution	Color Space and Pixel Depth	Refresh (Hz)
2D	—	VGA (640 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp	59.94/60
		WVGA (800 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp	60
		SVGA (800 × 600p)	RGB 4:4:4 – 24, 30, 36 bpp	60
		XGA (1024 × 768p)	RGB 4:4:4 – 24, 30, 36 bpp	60
		SXGA (1280 × 1024p)	RGB 4:4:4 – 24, 30, 36 bpp	60
		UXGA (1600 × 1200p)	RGB 4:4:4 – 24, 30, 36 bpp	60
		WUXGA (1900 × 1200p)	RGB 4:4:4 – 24, 30, 36 bpp	60
		480i 2x (1440 × 480i)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	59.94/60
		480i 4x (2880 × 480i)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	59.94/60
		480p (720 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	59.94/60
		480p 2x (1440 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	59.94/60
		480p 4x (2880 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	59.94/60
		576i 2x (1440 × 480i)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50
		576i 4x (2880 × 480i)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50

Table 3.1. Video Input Formats – HDMI Video Modes *(continued)*

Video Mode	3D Mode	Video Resolution	Color Space and Pixel Depth	Refresh (Hz)
2D	—	576p (720 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50
		576p 2x (1440 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50
		576p 4x (2880 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50
		720p (1280 × 720p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	23.98/24/25/ 29.97/30/50/ 59.94/60
		1080i (1920 × 1080i)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50/59.94/60
		1080p (1920 × 1080p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	23.98/24/25/ 29.97/30/ 50/59.94/60/ 100/119.88/120
		4K × 2K (3840 × 2160p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	23.98/24/25/ 29.97/30/50/ 59.94/60
		4K × 2K (3840 × 2160p)	YCbCr 4:2:0 – 24, 30, 36 bpp	50/59.94/60
		4K × 2K (4096 × 2160p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	23.98/24/25/ 29.97/30/50/ 59.94/60
		4K × 2K (4096 × 2160p)	YCbCr 4:2:0 – 24, 30, 36 bpp	50/59.94/60
3D	Frame Packing	720p (1280 × 720p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50/59.94/60
		1080p (1920 × 1080p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	23.98/24/25/ 29.97/30/50/ 59.94/60
	Side-by-Side (Half)	1080i (1920 × 1080i)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50/59.94/60
	Top-and-Bottom	720p (1280 × 720p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50/59.94/60
		1080p (1920 × 1080p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	23.98/24/25/ 29.97/30/50/ 59.94/60

3.2. Video Output Format Support

The SiI9777 transmitter/port processor provides two HDMI outputs: TX0 supports TMDS character rate of up to 600 Mcsc, while TX1 and TX2 support TMDS clock speeds of up to 300 MHz. Table 3.2 lists the video output formats supported for each output.

The SiI9777 supports up to 36-bit pixel depth for RGB 4:4:4 and YCbCr 4:4:4 modes, and up to 24-bit pixel depth for YCbCr 4:2:2 mode.

Table 3.2. Video Output Formats – HDMI Mode

Video Mode	3D Mode	Video Resolution	Color Space and Pixel Depth	Refresh (Hz)
2D	—	VGA (640 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp	59.94/60
		WVGA (800 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp	60
		SVGA (800 × 600p)	RGB 4:4:4 – 24, 30, 36 bpp	60
		XGA (1024 × 768p)	RGB 4:4:4 – 24, 30, 36 bpp	60
		SXGA (1280 × 1024p)	RGB 4:4:4 – 24, 30, 36 bpp	60
		UXGA (1600 × 1200p)	RGB 4:4:4 – 24, 30, 36 bpp	60
		WUXGA (1900 × 1200p)	RGB 4:4:4 – 24, 30, 36 bpp	60
		480i 2x (1440 × 480i)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	59.94/60
		480i 4x (2880 × 480i)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	59.94/60
		480p (720 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	59.94/60
		480p 2x (1440 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	59.94/60
		480p 4x (2880 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	59.94/60
		576i 2x (1440 × 480i)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50
		576i 4x (2880 × 480i)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50
		576p (720 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50
		576p 2x (1440 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50
		576p 4x (2880 × 480p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50
		720p (1280 × 720p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	23.98/24/25/ 29.97/30/50/ 59.94/60

Table 3.2. Video Output Formats – HDMI Mode *(continued)*

Video Mode	3D Mode	Video Resolution	Color Space and Pixel Depth	Refresh (Hz)
2D	—	1080i (1920 × 1080i)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	23.98/24/25/ 29.97/30/50/ 59.94/60
		1080p (1920 × 1080p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	23.98/24/25/ 29.97/30/ 50/59.94/60/ 100/119.88/120
		1080p (1920 × 1080p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	23.98/24/25/ 29.97/30/ 50/59.94/60/ 100/119.88/120
		4K × 2K (3840 × 2160p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	23.98/24/25/ 29.97/30/50/59.94/60
		4K × 2K (4096 × 2160p)	RGB 4:4:4 – 24 bpp YCbCr 4:4:4 – 24 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	23.98/24/25/ 29.97/30/50/ 59.94/60
3D	Frame Packing	720p (1280 × 720p)	RGB 4:4:4 – 24bpp YCbCr 4:4:4 – 24, bpp YCbCr 4:2:2 – 16, bpp	50/59.94/60
		1080p (1920 × 1080p)	RGB 4:4:4 – 24, bpp YCbCr 4:4:4 – 24, bpp YCbCr 4:2:2 – 16, bpp	23.98/24/25/ 29.97/30/50/ 59.94/60
	Side-by-Side (Half)	1080i (1920 × 1080i)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50/59.94/60
	Top-and-Bottom	720p (1280 × 720p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	50/59.94/60
		1080p (1920 × 1080p)	RGB 4:4:4 – 24, 30, 36 bpp YCbCr 4:4:4 – 24, 30, 36 bpp YCbCr 4:2:2 – 16, 20, 24 bpp	23.98/24/25/ 29.97/30/50/ 59.94/60

3.3. Reduced Blanking Support

The SiI9777 transmitter/port processor supports reduced blanking to convert 4K × 2K 10-bit 4:2:0 @ 50/60 Hz (reduced blanking format) to standard 4K × 2K 10-bit 4:2:2 @ 50/60 Hz format. Table 3.3 on the next page describes the detailed timings of the two reduced blanking formats, other possible reduced blanking formats may also be supported.

Table 3.3. Reduced Blanking Support Timings

Description	4K × 2K @ 60 Hz	4K × 2K @ 50 Hz
Pixel Frequency (MHz)	540	540
Vfreq (Hz)	60	50
Hactive	3840	3840
Hblank	160	960
Hfront	16	16
Hsync	44	44
Hback	100	900
Vactive	2160	2160
Vblank	90	90
Vfront	8	8
Vsync	10	10
Vback	72	72

3.4. Merging Two Video Streams

The SiI9777 transmitter/port processor provides a merging function that can be used to merge two video input streams into one video stream with double the input pixel rate. This function is primarily used to merge two 300 MHz pixel frequency input streams that contain one half of a 4K × 2K (60/50 Hz) 4:4:4 frame each, into the original 600 Mcsc stream.

The function is capable of merging other 4K × 2K formats with lower frame rates as well. Table 3.4 shows typical video resolutions for which the merge operation is supported and Table 3.5 shows the video timing before and after the merge operation.

Table 3.4. Supported Resolutions for Merge Operation

Vsync Frequency (Hz)	Pixel Frequency (MHz)	Htotal	Hactive	Hfront	Hsync	Hback	Hblank	Vtotal	Vactive	Vfront	Vsync	Vback	Vblank	VIC
3840×2160P 4:4:4														
24/23.98	297	5500	3840	1276	88	296	1660	2250	2160	8	10	72	90	93, 103
25	297	5280	3840	1056	88	296	1440	2250	2160	8	10	72	90	94, 104
30/29.97	297	4400	3840	176	88	296	560	2250	2160	8	10	72	90	95,105
50	594	5280	3840	1056	88	296	1440	2250	2160	8	10	72	90	96, 106
60/59.94	594	4400	3840	176	88	296	560	2250	2160	8	10	72	90	97, 107
4096×2160P 4:4:4														
24/23.98	297	5500	4096	1020	88	296	1404	2250	2160	8	10	72	90	98
25	297	5280	4096	968	88	128	1404	2250	2160	8	10	72	90	99
30/29.97	297	4400	4096	88	88	128	304	2250	2160	8	10	72	90	100
50	594	5280	4096	968	88	128	1184	2250	2160	8	10	72	90	101
60/59.94	594	4400	4096	88	88	128	304	2250	2160	8	10	72	90	102

Table 3.5 on the next page shows the timing parameters of the video signals before and after merging.

Table 3.5. Video Output Timings before and after Merge Operation

Format	Clock	VSYNC Frequency (Hz)	Htotal	Hactive	Hfront	Hsync	Hback	Hblank	Vtotal	Vactive	Vfront	Vsync	Vback	Vblank
Before merge	297.000	60.00	2200	1920	88	44	148	280	2250	2160	8	10	72	90
	296.703	59.94	2200	1920	88	44	148	280	2250	2160	8	10	72	90
4K × 2K @ 600 MHz, pixel frequency (VIC = 97, 107), after merge	594.000	60.00	4400	3840	176	88	296	560	2250	2160	8	10	72	90
	593.406	59.94	4400	3840	176	88	296	560	2250	2160	8	10	72	90
Before merge	297.000	50.00	2640	1920	528	44	148	720	2250	2160	8	10	72	90
4K × 2K @ 600 MHz, pixel frequency (VIC = 96, 106), after merge	594.000	50.00	5280	3840	1056	88	296	1440	2250	2160	8	10	72	90
Before merge	297.000	60.00	2200	2048	44	44	64	152	2250	2160	8	10	72	90
	296.703	59.94	2200	2048	44	44	64	152	2250	2160	8	10	72	90
4K × 2K @ 600 MHz, pixel frequency (VIC = 102), after merge	594.000	60.00	4400	4096	88	88	128	304	2250	2160	8	10	72	90
	593.406	59.94	4400	4096	88	88	128	304	2250	2160	8	10	72	90
Before merge	297.000	50.00	2640	2048	484	44	64	592	2250	2160	8	10	72	90
4K × 2K @ 600 MHz, pixel frequency (VIC = 101), after merge	594.000	50.00	5280	4096	968	88	128	1184	2250	2160	8	10	72	90

3.5. Merge Modes

The SiI9777 transmitter/port processor supports two different methods of merging the input signals: Even/Odd Pixel and Left/Right Frame modes. Although the typical case is to merge two 300 MHz streams into a single 600 Mcsc stream, lower frequency streams can be merged as well.

3.5.1. Even/Odd Pixel Merge Mode

In Even/Odd Pixel merge mode, videos from Receiver Port 0 and Port 1 in even/odd format are merged into one video stream and output to Transmitter Port 0. Receiver Port 0-4 can receive video up to maximum 300 MHz pixel clock, and Transmitter Port 0 works at maximum of 600 Mcsc.

The skew between the video input signals must be 100 pixel clocks or less.

Figure 3.1 depicts the operation of the Even/Odd Pixel merge mode for the 4K × 2K 4:4:4 @ 60 Hz video format.

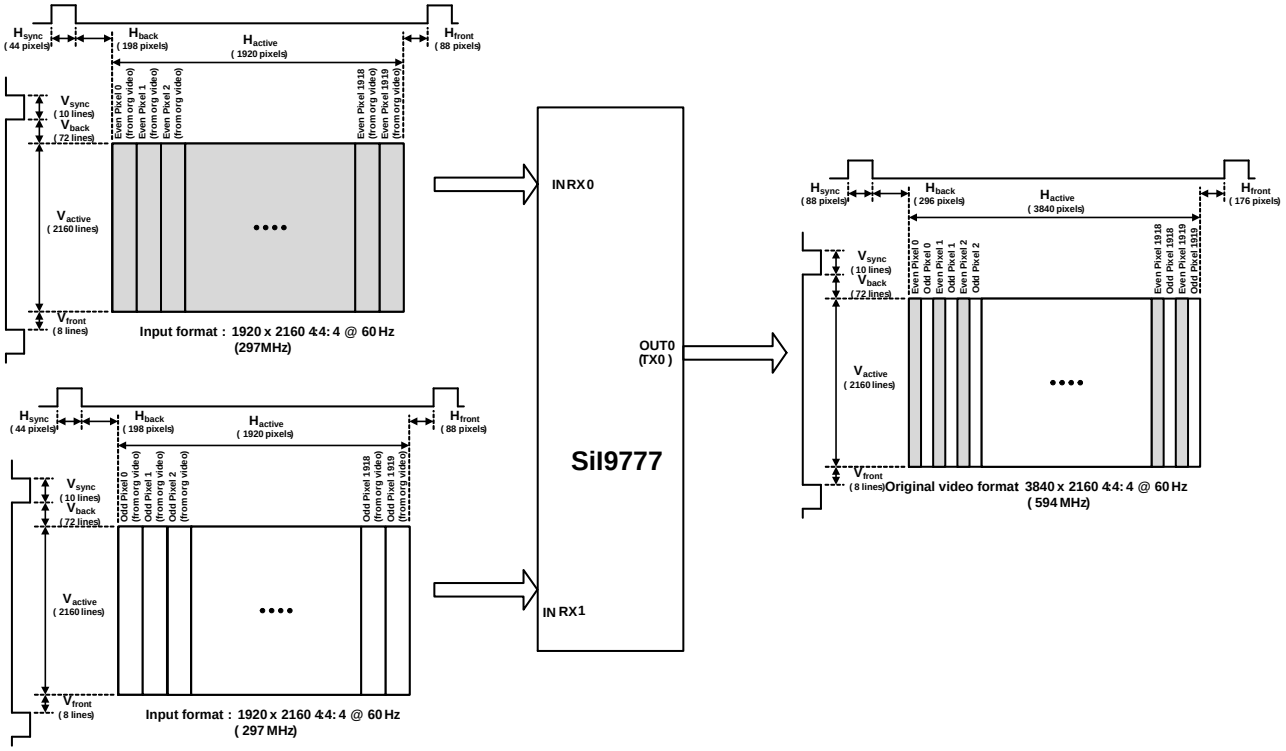


Figure 3.1. Even/Odd Pixel Merge Operation on a 4K × 2K 4:4:4 @ 60 Hz Video Signal

3.5.2. Left/Right Frame Merge Mode

In Left/Right Frame merge mode, the video streams from any two of four Receiver Ports in left/right frame format are merged into one video stream and output to Transmitter Port 0. Receiver Ports operate up to a maximum of 300 MHz and Transmitter Port 0 works at maximum of 600 Mcsc

The skew between the video input signals must be 100 pixel clocks or less.

Figure 3.2 on the next page depicts the operation of the Left/Right Frame merge mode for the 4K × 2K 4:4:4 @ 60 Hz video format.

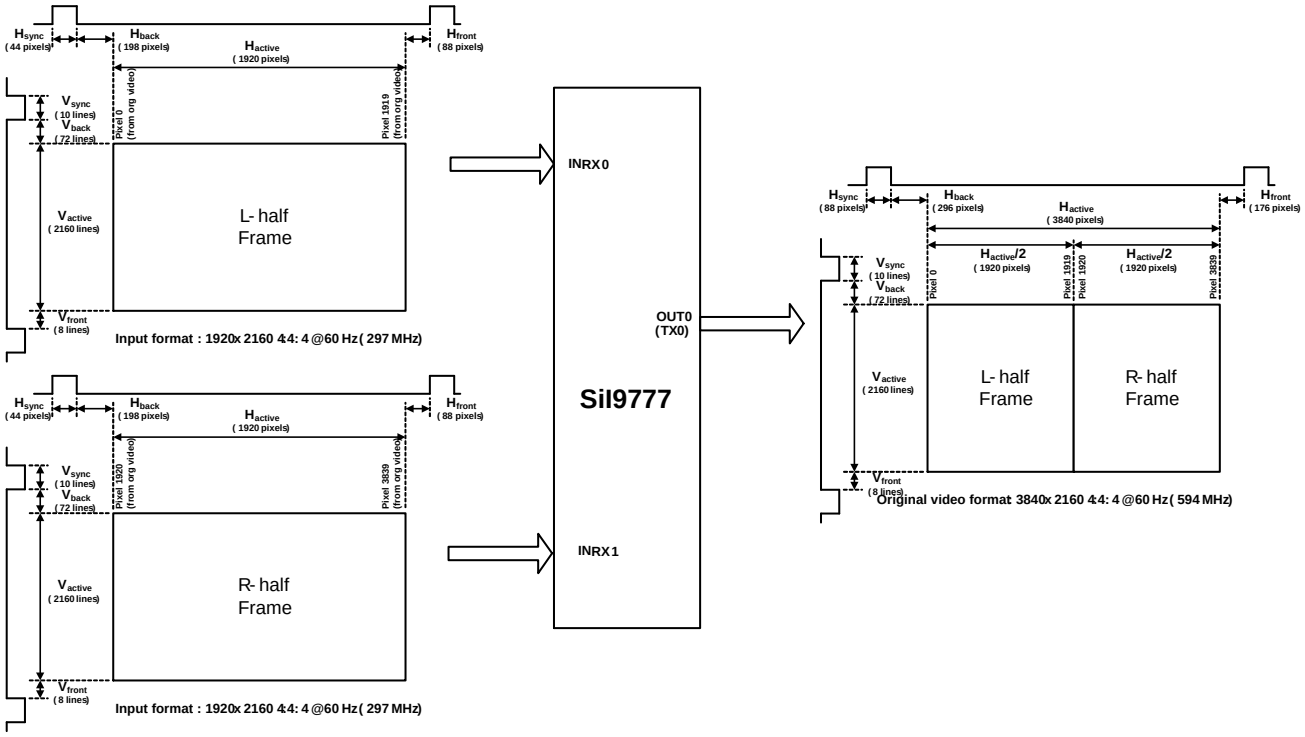


Figure 3.2. Left/Right Frame Merge Operation on a 4K × 2K 4:4:4 @ 60 Hz Video Signal

3.6. Splitting the Video Stream

The SiI9777 transmitter/port processor provides a splitter function that can be used to split a single video input stream into two separate streams with half the pixel rate. Primarily, this function is used to split an HDMI 2 600 Mcsc input stream into two 300 MHz output streams. In terms of video resolution, this means splitting a 4K × 2K 4:4:4 @ 50/60 Hz signal into two signals, each with half the number of horizontal pixels of the original input signal. In other words, each output signal has an active area of 2K × 2K. Although the typical case is to split a 600 Mcsc stream into two 300 MHz streams, lower frequency streams can be split as well.

The function is capable of splitting other 4K × 2K formats with lower frame rates as well. Table 3.6 shows all the video resolutions for which the split operation is supported and Table 3.7 shows the output timing after the split.

Table 3.6. Supported Resolutions for Split Operation

Vsync Frequency (Hz)	Pixel Frequency (MHz)	Htotal	Hactive	Hfront	Hsync	Hback	Hblank	Vtotal	Vactive	Vfront	Vsync	Vback	Vblank	VIC
3840×2160P 4:4:4														
24/23.98	297	5500	3840	1276	88	296	1660	2250	2160	8	10	72	90	93, 103
25	297	5280	3840	1056	88	296	1440	2250	2160	8	10	72	90	94, 104
30/29.97	297	4400	3840	176	88	296	560	2250	2160	8	10	72	90	95,105
50	594	5280	3840	1056	88	296	1440	2250	2160	8	10	72	90	96, 106
60/59.94	594	4400	3840	176	88	296	560	2250	2160	8	10	72	90	97, 107
4096×2160P 4:4:4														
24/23.98	297	5500	4096	1020	88	296	1404	2250	2160	8	10	72	90	98
25	297	5280	4096	968	88	128	1404	2250	2160	8	10	72	90	99
30/29.97	297	4400	4096	88	88	128	304	2250	2160	8	10	72	90	100
50	594	5280	4096	968	88	128	1184	2250	2160	8	10	72	90	101
60/59.94	594	4400	4096	88	88	128	304	2250	2160	8	10	72	90	102

Table 3.7 on the next page shows the video timing parameters of the output signals after splitting the original 4K × 2K input signal. In the split operation, only the horizontal parameters of the input signal are divided by 2.

Table 3.7. Video Output Timings after Split Operation

Format	Pixel Frequency (MHz)	Vsync Frequency (Hz)	Htotal	Hactive	Hfront	Hsync	Hback	Hblank	Vtotal	Vactive	Vfront	Vsync	Vback	Vblank
4K × 2K @ 600 MHz pixel frequency (VIC = 97, 107)	594.000	60.00	4400	3840	176	88	296	560	2250	2160	8	10	72	90
	593.406	59.94	4400	3840	176	88	296	560	2250	2160	8	10	72	90
After Split	297.000	60.00	2200	1920	88	44	148	280	2250	2160	8	10	72	90
	296.703	59.94	2200	1920	88	44	148	280	2250	2160	8	10	72	90
4K × 2K @ 600 MHz pixel frequency (VIC = 96, 106)	594.000	50.00	5280	3840	1056	88	296	1440	2250	2160	8	10	72	90
After Split	297.000	50.00	2640	1920	528	44	148	720	2250	2160	8	10	72	90
4K × 2K @ 600 MHz pixel frequency (VIC = 102)	594.000	60.00	4400	4096	88	88	128	304	2250	2160	8	10	72	90
	593.406	59.94	4400	4096	88	88	128	304	2250	2160	8	10	72	90
After Split	297.000	60.00	2200	2048	44	44	64	152	2250	2160	8	10	72	90
	296.703	59.94	2200	2048	44	44	64	152	2250	2160	8	10	72	90
4K × 2K @ 600 MHz pixel frequency (VIC = 101)	594.000	50.00	5280	4096	968	88	128	1184	2250	2160	8	10	72	90
After Split	297.000	50.00	2640	2048	484	44	64	592	2250	2160	8	10	72	90

3.7. Split Modes

The SiI9777 transmitter/port processor supports two different methods of splitting the input signal: Even/Odd Pixel and Left/Right Frame modes.

3.7.1. Even/Odd Pixel Split Mode

In Even/Odd Pixel split mode, the even pixels of the active video line are sent to the Transmitter Port 1 output port and the odd pixels are sent to the Transmitter Port 2 output port. The pixels are driven out by a clock that is one half the frequency of the pixel clock rate of the input signal. The Vsync and Hsync signals are duplicated on both outputs with the horizontal parameters such as the front porch, sync pulse width, and the back porch having half the timing of the input signal.

The output streams are synchronized with a maximum skew of three pixel clocks.

Figure 3.3 shows the operation of the Even/Odd Pixel split mode for a 600 MHz pixel frequency 4K × 2K input signal.

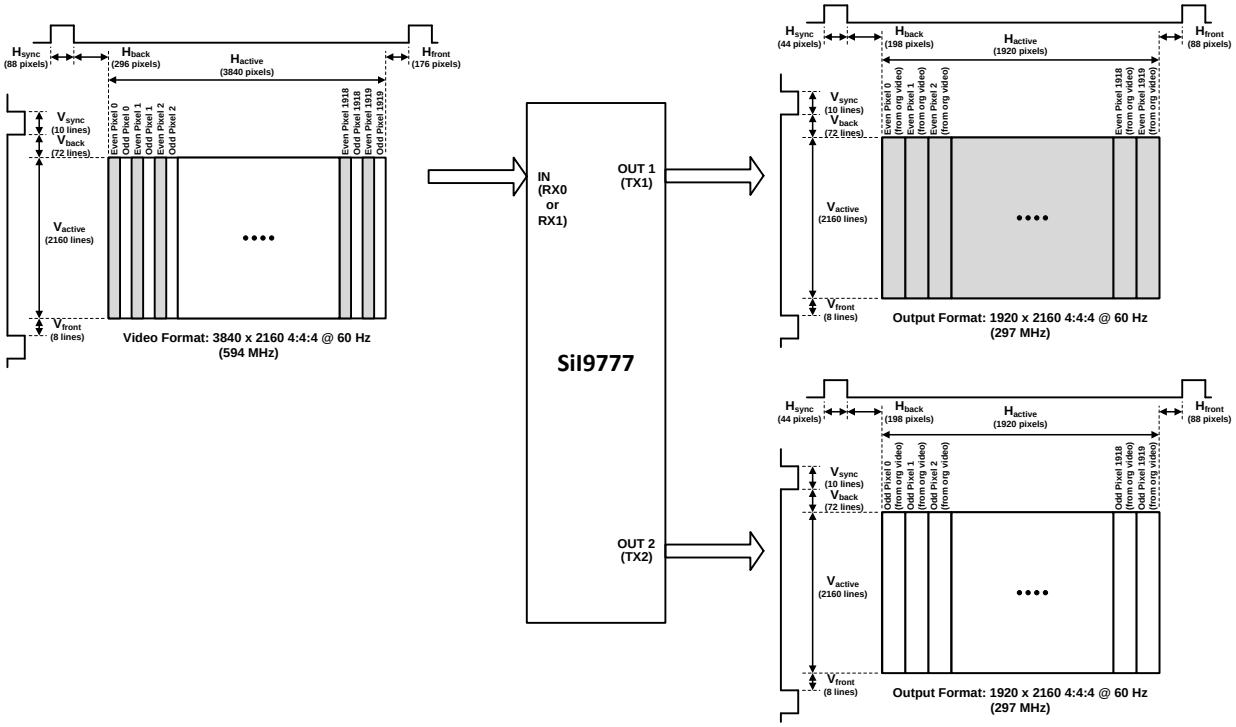


Figure 3.3. Even/Odd Pixel Split Operation on a 4K × 2K 4:4:4 @ 60 Hz Video Signal

3.7.2. Left/Right Frame Split Mode

In Left/Right Frame split mode, the horizontal active pixels are divided into two segments of equal size. Pixels from the beginning of the line to the center of the line are mapped to the left frame while pixels from the center of the line to the end of the line are mapped to the right frame. The left frame is then sent to Transmitter Port 1 output port while the right frame is sent to Transmitter Port 2 output port. As in the Even/Odd Pixel mode, the pixels of the left and right frames are driven out by a clock that is one half the frequency of the pixel clock rate of the input signal. The Vsync and Hsync signals are duplicated on both outputs and the horizontal parameters such as the front porch, sync pulse width, and the back porch are half that of the input signal.

The output streams are synchronized with a maximum skew of three pixel clocks.

Figure 3.4 on the next page shows the operation of the Left/Right Frame split mode for a 600 Mcsc pixel frequency 4K × 2K input signal.

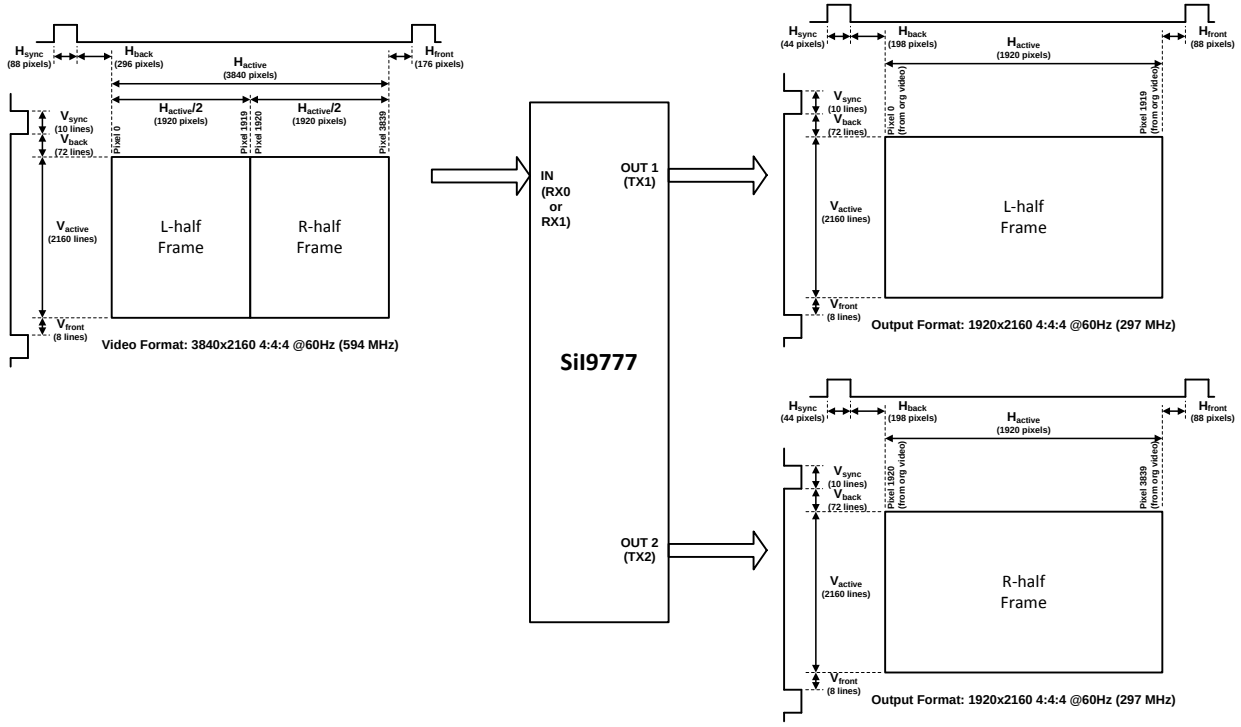


Figure 3.4. Left/Right Frame Split Operation on a 4K × 2K 4:4:4 @ 60 Hz Video Signal

3.8. Video Test Patterns

The Video Test Pattern Generator (VTPG) generates the test patterns described below.

3.8.1. Solid Patterns

Eight solid patterns with the following RGB configurations are provided:

- Solid Red (255, 0, 0)
- Solid Green (0, 255, 0)
- Solid Blue (0, 0, 255)
- Solid Cyan (0, 255, 255)
- Solid Magenta (255, 0, 255)
- Solid Yellow (255, 255, 0)
- Solid Black (0, 0, 0)
- Solid White (255, 255, 255)

3.8.2. 256 Gray Pattern

- 256 vertical bars of equal width.
- Value of first bar: RGB (0, 0, 0).
- Value of last bar: RGB (255, 255, 255).
- Increment of each bar: One RGB value. For example (1, 1, 1), (2, 2, 2), (3, 3, 3), and so on.

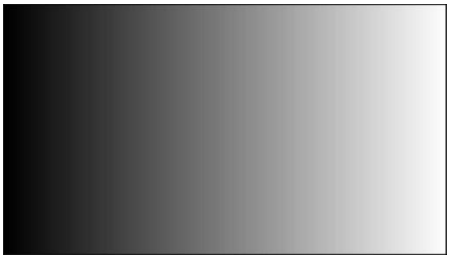


Figure 3.5. 256 Gray Pattern

3.8.3. Checkerboard Pattern

- 8 columns by 6 rows of alternating black and white squares.
- Value of black: RGB (0, 0, 0).
- Value of white: RGB (255, 255, 255).

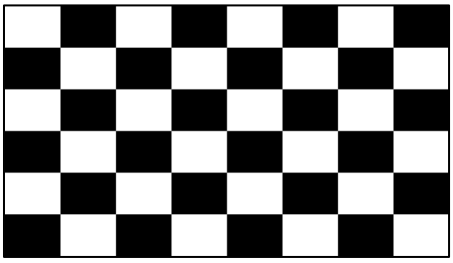


Figure 3.6. 8 × 6 Checkerboard Pattern

3.8.4. RGB Color Bars Pattern

- Eight vertical bars.
- RGB format with pixel values listed in Table 3.8.

Table 3.8. Color Bars Pixel Values

Component	Color							
	White	Yellow	Cyan	Green	Magenta	Red	Blue	Black
R	255	255	0	0	255	255	0	0
G	255	255	255	255	0	0	0	0
B	255	0	255	0	255	0	255	0

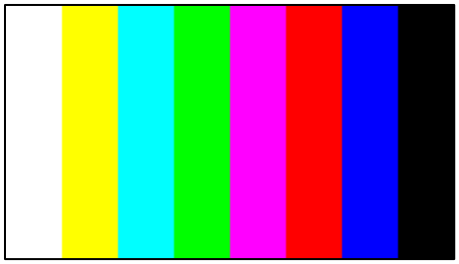


Figure 3.7. Color Bars Pattern

3.9. TMDS Pin Order Inverting

The SiI9777 transmitter/port processor supports inverting the order of the TMDS pins on all three transmitter ports. This option allows wiring of the TMDS output pins to an on-board HDMI receiver IC. Table 3.9 shows the TMDS output connections before and after inverting the pin order.

Table 3.9. TMDS Output Pin Order before and after Inverting

Transmitter Port	Pin Number	Normal Pin out	Pin out after Inverting
0	18	No Connect	TX0_TXCP
	17	No Connect	TX0_TXCN
	15	TX0_TX2P	TX0_TX0P
	14	TX0_TX2N	TX0_TX0N
	12	TX0_TX1P	TX0_TX1P
	11	TX0_TX1N	TX0_TX1N
	9	TX0_TX0P	TX0_TX2P
	8	TX0_TX0N	TX0_TX2N
	6	TX0_TXCP	No Connect
	5	TX0_TXCN	No Connect
1	202	TX1_TX2P	TX1_TXCN
	201	TX1_TX2N	TX1_TXCP
	199	TX1_TX1P	TX1_TX0N
	198	TX1_TX1N	TX1_TX0P
	197	TX1_TX0P	TX1_TX1N
	196	TX1_TX0N	TX1_TX1P
	194	TX1_TXCP	TX1_TX2N
	193	TX1_TXCN	TX1_TX2P
2	189	TX2_TX2P	TX2_TXCN
	188	TX2_TX2N	TX2_TXCP
	186	TX2_TX1P	TX2_TX0N
	185	TX2_TX1N	TX2_TX0P
	184	TX2_TX0P	TX2_TX1N
	183	TX2_TX0N	TX2_TX1P
	181	TX2_TXCP	TX2_TX2N
	180	TX2_TXCN	TX2_TX2P

Note: For Inverted pin case on TX0 port, this is intended for on-board applications only and not configurations over cables that require compliance.

3.10. Color Space Conversion

The SiI9777 port processor supports many different color space conversion options. These are performed in individual small steps; this modular concept allows the most flexibility in order to support different standards. A simplified block diagram of color space conversion module is shown in Figure 3.8 and Figure 3.9 below.

The individual modules are described in the following sections. If color space conversion is not needed, the module can be bypassed.

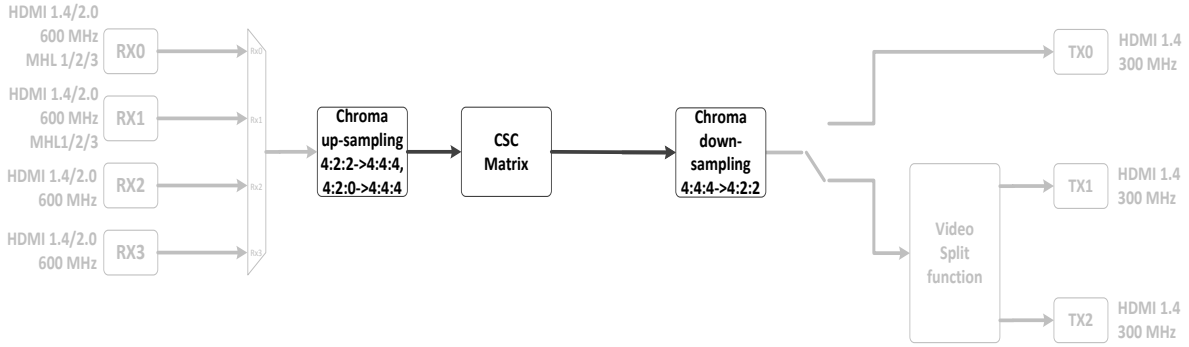


Figure 3.8. SiI9777 Color Space Conversion in Receiver Mode

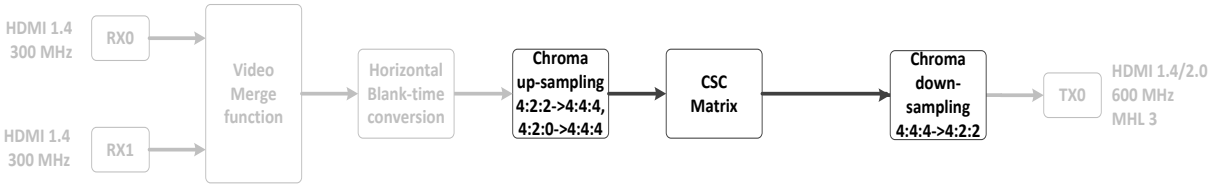


Figure 3.9. SiI9777 Color Space Conversion in Transmitter Mode

3.10.1. Chroma Up/Subsampling

In order to perform color space conversions, all input signals must first be converted to 4:4:4. This means 4:2:0 input signals need to be vertically upsampled first to a 4:2:2 signal. The 4:2:2 input signals or converted signals then need to be horizontally upsampled to 4:4:4.

On the output side, the 4:4:4 signal can be horizontally subsampled to 4:2:2. Vertical subsampling to 4:2:0 is not supported.

3.10.2. CSC Matrix

This function is used for any linear conversion of gamma corrected signals, such as cross conversions between R'G'B' and Y'Cb'Cr', or linear expansion or compression of individual signals.

The Multi-CSC matrix supports the following colorimetry conversions, in any combination:

- Y'Cb'Cr' ↔ R'G'B' (BT.601)
- Y'Cb'Cr' ↔ R'G'B' (BT.709)
- Y'Cb'Cr' ↔ R'G'B' (BT.2020), only the non-constant luminance portion of BT.2020 is supported
- Dynamic Range Expansion (Video levels → PC levels)
- Dynamic Range Compression (PC levels → Video levels)

3.11. Local Host Interface

The host controller can communicate with the SiI9777 transmitter/port processor either through the local I^2C bus, or through the local SPI slave interface. Below is a description of both interfaces.

3.11.1. Local I^2C Interface

The host controller communicates with the SiI9777 transmitter/port processor through a local I^2C bus interface. The local I^2C interface uses pins CSCL and CSDA and is a slave interface that can run up to 400 kHz.

The I^2C master that is used to control the transmitter must be able to support SCL clock line stretching by the transmitter.

The device address of the local I^2C interface can be set to one of two values by strapping the GPIO0 pin LOW or HIGH at reset. Table 3.10 shows the device address selected for each state of the GPIO0 pin at reset. Also, the upper 6 bits of the base address can be changed in the boot loader configuration to a value other than 0x40. See Sii9777 firmware reference for details.

Table 3.10. Control of Local I^2C Device Address with GPIO0 Pin

Device Address	GPIO0 = LOW	GPIO0 = HIGH
Local I^2C	0x40	0x42

3.11.2. SPI Slave interface

Alternatively, the host can communicate with the SiI9777 transmitter/port processor through the SPI slave interface.

4. Electrical Specifications

Not Final: Specifications are subject to change.

4.1. Target Absolute Maximum Conditions

Table 4.1. Target Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
LPSBV	Low-power Standby Power Supply Voltage	–0.3	—	5.7	V	1, 2
SBVCC5	Standby Power Supply Voltage	–0.3	—	5.7	V	1, 2
RX*n*_PWR5V	HDMI +5 V Power Signal Input Voltage	–0.3	—	5.7	V	1, 2
IO_VDD33	I/O Pin 3.3 V Supply Voltage	–0.3	—	4.0	V	1, 2
RX_AVDD33	TMDS Receiver Analog 3.3 V Supply Voltage	–0.3	—	4.0	V	1, 2
PVDD33	PLL 3.3 V supply	–0.3	—	4.0	V	1, 2
TX0_AVDD33	TMDS Transmitter Port 0 Analog 3.3 V Supply Voltage	–0.3	—	4.0	V	1, 2
XTAL_VDD33	Crystal Oscillator Power	–0.3	—	4.0	V	1, 2
AVDD_PLL	TMDS Receiver Analog 1.0 V Supply Voltage	–0.3	—	1.5	V	1, 2
RX_AVDD10	TMDS Receiver Analog 1.0 V Supply Voltage	–0.3	—	1.5	V	1, 2
TX*n*_AVDD10	TMDS Transmitter Analog Supply Voltage	–0.3	—	1.5	V	1, 2
TX*n*_PVDD10	TMDS Transmitter PLL Supply Voltage	–0.3	—	1.5	V	1, 2
PVDD10	PLL 1.0V Supply Voltage	–0.3	—	1.5	V	1, 2
CVDD10	Digital Core Supply Voltage	–0.3	—	1.5	V	1, 2
CG*n*_PVDD10	Clock Generator PLL Supply Voltage	–0.3	—	1.5	V	1, 2
XTAL_VDD10	Crystal Oscillator PLL Supply Voltage	–0.3	—	1.5	V	1, 2
V_I	Input Voltage	–0.3	—	IO_VDD33 + 0.3	V	1, 2
$V_{5V\text{-}Tolerant}$	Input Voltage on 5 V Tolerant Pins	–0.3	—	5.7	V	1, 2
T_J	Junction Temperature	0	—	125	°C	1, 2
T_{STG}	Storage Temperature	–65	—	150	°C	1

Notes:

1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described in the Target Normal Operating Conditions section on the next page.

ESD Specifications

Refer to the SiI9777 Qualification report for detailed information on ESD performance.

4.2. Target Normal Operating Conditions

Table 4.2. Target Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
LPSBV	Low-power Standby Power Supply Voltage	4.5	5.0	5.5	V	—
RX*n*_PWR5V	HDMI +5 V Power Signal Input Voltage	4.5	5.0	5.5	V	—
SBVCC5	Standby Power Supply Voltage	4.5	5.0	5.5	V	1
IO_VDD33	I/O Pin 3.3 V Supply Voltage	3.14	3.3	3.46	V	—
RX_AVDD33	TMDS Receiver Analog 3.3 V Supply Voltage	3.14	3.3	3.46	V	—
TX0_AVDD33	TMDS Transmitter 0 Analog 3.3 V Supply Voltage	3.14	3.3	3.46	V	—
RX_AVDD10	TMDS Receiver Analog 1.0 V Supply Voltage	0.95	1.0	1.05	V	—
TX*n*_AVDD10	TMDS Transmitter Analog Supply Voltage	0.95	1.0	1.05	V	—
TX*n*_PVDD10	TMDS Transmitter PLL Supply Voltage	0.95	1.0	1.05	V	—
CVDD10	Digital Core Supply Voltage	0.95	1.0	1.05	V	—
CG*n*_PVDD10	Clock Generator PLL Supply Voltage	0.95	1.0	1.05	V	—
RX_PVDD10	Receiver PLL Supply Voltage	0.95	1.0	1.05	V	—
T_A	Ambient Temperature	0	+25	+70	°C	2
Θja	Ambient Thermal resistance (Theta JA)	—	—	18.0	°C/W	3, 4
Θjc	Junction to Case Resistance (Theta JC)	—	—	8.5	°C/W	4

Notes:

1. SBVCC5 Voltage is measured at SBVCC5TP as shown in Figure 4.1.
2. With power applied.
3. Airflow at 0 m/s.
4. The thermal resistance figures are based on a 4-layer PCB.

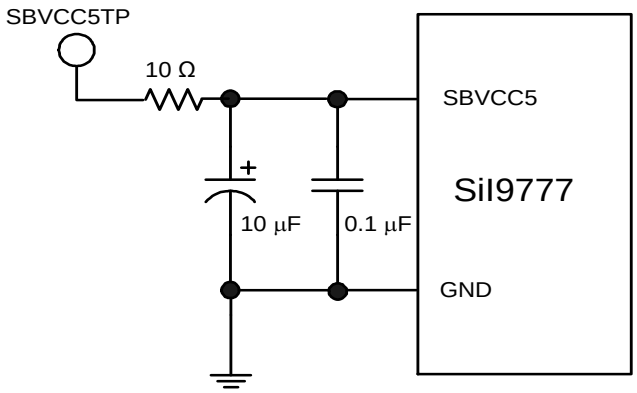


Figure 4.1. Test Point SBVCC5TP for SBVCC5 Measurement

4.3. Target DC Specifications

Table 4.3.Target Digital I/O Specifications

Symbol	Parameter	Pin Type[1]	Conditions	Min	Typ	Max	Units	Note
V_{IH}	HIGH-level Input Voltage	LVTTL	—	2.0	—	—	V	—
V_{IL}	LOW-level Input Voltage	LVTTL	—	—	—	0.8	V	—
V_{TH+} RESET_N	LOW-to-HIGH threshold RESET_N pin	Schmitt	—	2.0	—	—	V	2
V_{TH-} RESET_N	HIGH-to-LOW threshold RESET_N pin	Schmitt	—	—	—	0.8	V	2
V_{TH+DDC}	LOW-to-HIGH Threshold, DDC Bus	Schmitt	—	3.0	—	—	V	2
V_{TH-DDC}	HIGH-to-LOW Threshold, DDC Bus	Schmitt	—	—	—	1.5	V	2
V_{TH+I2C}	LOW-to-HIGH Threshold, Local I^2C Bus	Schmitt	—	2.0	—	—	V	2
V_{TH-I2C}	HIGH-to-LOW Threshold, Local I^2C Bus	Schmitt	—	—	—	0.8	V	2
V_{OH}	HIGH-level Output Voltage	LVTTL	I_{OH} = 8 mA	2.4	—	—	V	—
V_{OL}	LOW-level Output Voltage	LVTTL	I_{OL} = –8 mA	—	—	0.4	V	—
V_{OL_DDC}	LOW-level Output Voltage	Open-drain	I_{OL} = –3 mA	—	—	0.4	V	—
V_{OL_I2C}	LOW-level Output Voltage	Open-drain	I_{OL} = –3 mA	—	—	0.4	V	—
V_{OL_INT}	LOW-level Output Voltage	Open-drain	I_{OL} = –3 mA	—	—	0.4	V	—
I_{IL}	Input Leakage Current	—	High impedance	–10	—	10	µA	—
		With R_{PD}	High impedance	–10	—	100	µA	3
I_{OL}	Output Leakage Current	—	High impedance	–10	—	10	µA	—
		With R_{PD}	High impedance	–10	—	100	µA	4
I_{OD}	8 mA Digital Output Drive	LVTTL	V_{OUT} = 2.4 V	8	—	—	mA	—
			V_{OUT} = 0.4 V	8	—	—	mA	—
R_{PD}	Internal Pull Down Resistor	—	—	—	46	—	kΩ	4

Notes:

1. See the Pin Descriptions section on page 41 for pin type designations for all package pins.
2. Schmitt trigger input pin thresholds V_{TH+} and V_{TH-} correspond to V_{IH} and V_{IL}, respectively.
3. Some input pins on the device have internal pull-down resistor. In high-impedance state, these pins draw a pull-down current according to this specification when the signal is driven HIGH by another device.
4. Some output pins on the device have internal pull-down resistor. In high-impedance state, these pins draw a pull-down current according to this specification when the signal is driven HIGH by another device.
5. Applies to the GPIO2, GPIO3, and AI_SPDIF and AO_SPDIF signal pins.

Table 4.4. Target Power Requirements

Symbol	Parameter	Min	Typ	Max	Unit
I_{IO_VDD33}	Supply Current for IO_VDD33	—	—	9	mA
I_{RX_AVDD33}	Supply Current for RX_AVDD33	—	—	3	mA
I_{PVDD33}	Supply Current for PVDD33	—	—	1	mA
I_{XTAL_VDD33}	Supply Current for XTAL_VDD33	—	—	5.5	mA
I_{TX0_VDD33}	Supply Current for TX0_AVDD33	—	—	3	mA
I_{RX_AVDD10}	Supply Current for RX_AVDD10	—	—	223	mA
I_{TX0_AVDD10}	Supply Current for TX0_AVDD10	—	—	40	mA
I_{TX1_AVDD10}	Supply Current for TX1_AVDD10	—	—	37	mA
I_{TX2_AVDD10}	Supply Current for TX2_AVDD10	—	—	37	mA
I_{TX0_PVDD10}	Supply Current for TX0_PVDD10	—	—	21	mA
I_{TX1_PVDD10}	Supply Current for TX2_PVDD10	—	—	9	mA
I_{PVDD10}	Supply Current for PVDD10	—	—	22	mA
I_{CVDD10}	Supply Current for CVDD10	—	—	1712	mA
I_{CG0_PVDD10}	Supply Current for CG0_PVDD10	—	—	14	mA
I_{SBVCC5}	Supply Current for SBVCC5	—	—	30	mA
I_{LPSBV}	Supply Current for LPSBV	—	—	1.0	mA
Total	Total Power Dissipation	—	—	2.64	W

Note: Maximum supply currents are measured at maximum operating voltages, and 70 °C ambient temperature with all input and output ports switching at the maximum supported clock frequency.

Table 4.5. Target TMDS Input DC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDF}	Differential Mode Input Voltage	—	150	—	1200	mV
V_{IDC}	Single-ended Input DC Voltage	—	150	—	1200	mV
V_{ICM}	Common Mode Input Voltage	—	AVDD33 – 400	—	AVDD33 +10	mV

Table 4.6. Target TMDS Input DC Specifications – MHL 1 and 2 Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDC}	Single-ended Input DC Voltage	—	V_{TERM} – 1200	—	V_{TERM} – 300	mV
V_{IDF}	Differential Mode Input Swing Voltage	—	200	—	1000	mV
V_{ICM}	Common Mode Input Swing Voltage	—	170	—	Min (720, 0.85 V_{IDF})	mV

Table 4.7. Target TMDS Input DC Specifications – MHL 3 Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IDC}	Single-ended Input DC Voltage	—	V_{TERM} – 1200	—	V_{TERM} – 300	mV
V_{IDF}	Differential Mode Input Swing Voltage	—	200	—	1000	mV
V_{ICM}	Common Mode Input Swing Voltage	—	170	—	Min (720, 0.85 V_{IDF})	mV

Table 4.8. Target TMDS Output DC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{SWING(Data)}$	Single-ended Output Swing Voltage data	R_{LOAD} = 50 Ω	400	—	600	mV
$V_{SWING(Clock)}$	Single-ended Output Swing Voltage clock	R_{LOAD} = 50 Ω, 300 MHz	200	—	600	mV
		R_{LOAD} = 50 Ω, 300 MHz	200	—	600	mV
V_H	Single-ended HIGH-level Output Voltage	300 MHz	AVDD33 – 400	—	AVDD33 + 10	mV
V_L	Single-ended LOW-level Output Voltage	300 MHz	AVDD33 – 700	—	AVDD33 – 400	mV
V_H	Single-ended HIGH-level Output Voltage	600 Mcsc	AVDD33 – 400	—	AVDD33 + 10	mV
$V_{L(Data)}$	Single-ended LOW-level Output Voltage data	600 Mcsc	AVDD33 – 1000	—	AVDD33 – 400	mV
$V_{L(Clock)}$	Single-ended LOW-level Output Voltage clock	600 Mcsc	AVDD33 – 1000	—	AVDD33 – 200	mV

Table 4.9. Target DC MHL 3 oCBUS Specifications

Symbol	Parameter	Signal Type	Conditions	Min	Typ	Max	Units
V_{TERM_CBUS}	CBUS Termination Voltage	oCBUS	—	1.7	—	1.9	V
V_{IH_CBUS}	HIGH-level Input Voltage		—	1.0	—	—	V
V_{IL_CBUS}	LOW-level Input Voltage		—	—	—	0.6	V
V_{OH_CBUS}	HIGH-level Output Voltage		IOVCC18 = 1.8 V, 85 °C	1.5	—	—	V
V_{OL_CBUS}	LOW-level Output Voltage		IOVCC18 = 1.8 V, 85 °C	—	—	0.2	V
I_{OH_CBUS}	HIGH-level Output Drive Current		V_{OH} = 1.5 V	2	—	—	mA
I_{OL_CBUS}	LOW-level Output Drive Current		V_{OL} = 0.2 V	300	—	—	µA
I_{IL}/I_{IH}	Input Leakage Current		High impedance	–1.0	—	1.0	µA
$Z_{CBUS\_SRC\_DISCOVER}$	Pull-up Resistance – Discovery		—	9	10	11	kΩ
$Z_{CBUS\_SRC\_ON}$	Pull-up Resistance – ON		—	4	5	6	kΩ
$Z_{RID\_MHL\_ACCEPT}$	R_ID range identified as MHL		—	800	1000	1200	Ω
$Z_{RID\_MHL\_REJECT}$	R_ID identified as not MHL		—	<500	—	>1600	Ω

4.4. Target MHL CBUS I/O Specification

Table 4.10. Target Digital CBUS I/O Specifications

Symbol	Parameter	Signal	Conditions	Min	Typ	Max	Units
V_{IH_CBUS}	LOW to HIGH Threshold, CBUS pin	CBUS	—	1.0	—	—	V
V_{IL_CBUS}	HIGH to LOW Threshold, CBUS pin	CBUS	—	—	—	0.6	V
V_{OH_CBUS}	Output HIGH Voltage, CBUS pin	CBUS	85°C, I_{OH} = 300 µA	1.5	—	—	V
$V_{OH\_CBUS\_DISCOVERY}$	Output HIGH Voltage, CBUS pin during Discovery	CBUS	85°C, I_{OH} = 300 µA	1.4	—	—	V
V_{OL_CBUS}	Output LOW Voltage, CBUS pin	CBUS	85°C, I_{OL} = 300 µA	—	—	0.2	V
I_{IL}	Input Leakage Current	CBUS	High impedance	–1.0	—	1.0	µA
$Z_{CBUS\_SINK\_DISCOVER}$	Pull down resistance – Discovery	CBUS	—	800	1000	1200	Ω
$Z_{CBUS\_SINK\_ON}$	Pull down resistance – ON	CBUS	—	90	100	110	kΩ

4.5. Target MHL3 eCBUS-S I/O Specification

Table 4.11. Target DC MHL3 eCBUS-S Sink Specifications

Symbol	Parameter	Signal	Conditions	Min	Typ	Max	Units
$V_{IDC\_SE\_MHL\_CLK}$, $V_{IDC\_SE\_eCBUS\_FWD}$	Input DC Voltage: Single-Ended MHL CLK, eCBUS-S Forward	eCBUS	—	95	—	230	mV
$V_{ISE\_SWING\_SE\_MHL\_CLK}$, $V_{ISE\_SWING\_SE\_eCBUS\_FWD}$	Single-Ended input swing voltage: Single-Ended MHL CLK, eCBUS-S Forward	eCBUS	—	200	—	400	mV
$V_{SE\_HIGH\_SE\_eCBUS\_BWD}$	Single-Ended high level output voltage: eCBUS-S Backward	eCBUS	—	220	—	430	mV
$V_{SE\_LOW\_SE\_eCBUS\_BWD}$	Single-Ended low level output voltage: eCBUS-S Backward	eCBUS	—	-30	—	+30	mV
$V_{SE\_SWING\_SE\_eCBUS\_BWD}$	Single-Ended output swing voltage: eCBUS-S Backward	eCBUS	—	250	—	400	mV

Table 4.12. Target Single Mode Audio Return Channel Input DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IS_ARC}	Input Swing Amplitude	—	160	—	600	mV

Table 4.13. Target Single Mode Audio Return Channel Output DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{el}	Operating DC Voltage	—	0	—	5	V
$V_{el\ swing}$	Swing Amplitude	—	400	—	600	mV

4.6. Target AC Specifications

Table 4.14. Target TMDS Input Timing AC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra Pair Differential Input Skew	—	—	—	$0.15T_{BIT} + 112$	ps
T_{CCS}	Inter Pair Differential Input Skew	—	—	—	$0.2T_{PIXEL} + 1.78$	ns
F_{RXC}	Differential Input Clock Frequency	—	25	—	340	MHz
T_{RXC}	Differential Input Clock Period	—	2.94	—	40	ns
T_{IJIT}	Differential Input Clock Jitter Tolerance	340 MHz	—	—	0.3	T_{BIT}

Table 4.15. Target TMDS Input Timings – MHL 1 and 2 Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$T_{INTRA\text{-}PAIR\_SKEW}$	Input Intra Pair Skew Tolerance	—	—	—	93	ps
F_{RXC}	Differential Input Clock Frequency	—	25	—	75	MHz
T_{RXC}	Differential Input Clock Period	—	13.3	—	40	ns

Table 4.16. Target TMDS Input Timings – MHL 3 (eCBUS-S) Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$T_{INTRA-PAIR\_SKEW}$	Input Intra Pair Skew Tolerance	—	—	—	93	ps
F_{RXC}	Differential Input Clock Frequency	—	74.9625	75	75.0375	MHz
T_{RXC}	Differential Input Clock Period	—	13.32	13.33	13.34	ns

Table 4.17. Target TMDS Output Timing AC Specifications – HDMI Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{TXDPS}	Intra Pair Differential Output Skew	—	—	—	0.15	T_{BIT}
T_{TXRTFT}	Data Rise/Fall Time	20%–80%, 300 MHz	75	—	—	ps
		20%–80%, 600 Mcsc	42.5	—	—	ps
T_{TXFTRT}	Clock Fall/Rise Time	80%–20%	75	—	—	ps
F_{TXC}	Differential Output Clock Frequency	—	25	—	300	MHz
T_{TXC}	Differential Output Clock Period	—	3.33	—	40	ns
T_{DUTY}	Differential Output Clock Duty Cycle	—	40%	—	60%	T_{TXC}
T_{OJIT}	Differential Output Clock Jitter	—	—	—	0.30	T_{BIT}

Table 4.18. Target I^2S Input Port AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{S_I2S}	Sample Rate	—	32	—	192	kHz	—	—
T_{SCKCYC}	I^2S Cycle Time	C_L = 10 pF	—	—	1.0	UI	Figure 4.2	1
$T_{SCKDUTY}$	I^2S Duty Cycle	C_L = 10 pF	90%	—	110%	UI	Figure 4.2	—
T_{I2SSU}	I^2S Setup Time	C_L = 10 pF	15	—	—	ns	Figure 4.2	2
T_{I2SHD}	I^2S Hold Time	C_L = 10 pF	0	—	—	ns	Figure 4.2	2

Notes:

1. Proportional to unit time (UI) according to sample rate. Refer to the I^2S Specification or the S/PDIF Specification.
2. Setup and hold minimum times are based on 13.388 MHz sampling, which is adapted from Figure 3 of the Philips I^2S Specification.

Table 4.19. Target I^2S Output Port AC Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{TR}	SCK Clock Period (TX)	C_L = 10 pF	1.00	—	—	T_{TR}	Figure 4.4	1
T_{SU}	Setup Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR} - 5$	—	—	ns		1
T_{HD}	Hold Time, SCK to SD/WS	C_L = 10 pF	$0.4T_{TR} - 5$	—	—	ns		1
$T_{SCKDUTY}$	SCK Duty Cycle	C_L = 10 pF	40%	—	60%	T_{TR}		1
T_{SCK2SD}	SCK to SD or WS Delay	C_L = 10 pF	–5	—	+5	ns		2

Notes:

1. Meets timings in Philips I^2S Specification, see Figure 4.4 on page 37.
2. Applies also to SD-to-WS delay.

Table 4.20.Target S/PDIF Input Port AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
F_{I_SPDIF}	Sample Rate	—	32	—	192	kHz	—
T_{I_SPCYC}	Cycle Time	—	—	—	1.0	UI	1, 2
T_{I_SPDUTY}	Duty Cycle	—	90	—	110	%UI	1, 2

Notes:
1. Proportional to unit time (UI), according to sample rate. Refer to the S/PDIF Specification.
2. Refer to Figure 4.3 below.

Table 4.21. Target S/PDIF Output Port AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
T_{SPCYC}	SPDIF Cycle Time	C_L = 10 pF	—	1.0	—	UI	1
F_{SPDIF}	SPDIF Frequency	—	4.0	—	24.0	MHz	—
T_{SPDUTY}	SPDIF Duty Cycle	C_L = 10 pF	90.0	—	110.0	% T_{SPCYC}	2
$T_{MCLKCYC}$	MCLK Cycle Time	C_L = 10 pF	20.0	—	250	ns	3
F_{MCLK}	MCLK Frequency	C_L = 10 pF	4.0	—	50.0	MHz	3
$T_{MCLKDUTY}$	MCLK Duty Cycle	C_L = 10 pF	45	—	65	% $T_{MCLKCYC}$	—

Notes:
2. Proportional to unit time (UI), according to sample rate. Refer to the S/PDIF Specification.
2. Refer to Figure 4.5 on the next page.
3. Refer to Figure 4.6 on the next page.

4.6.1. Digital Audio Input Timing

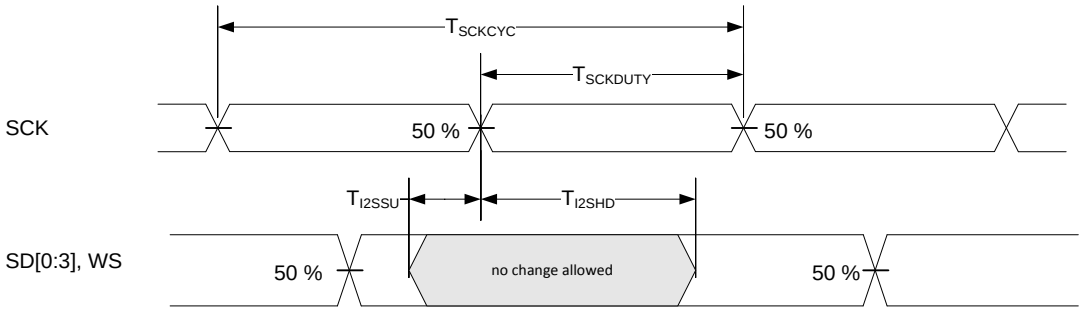


Figure 4.2. I²S Input Timing

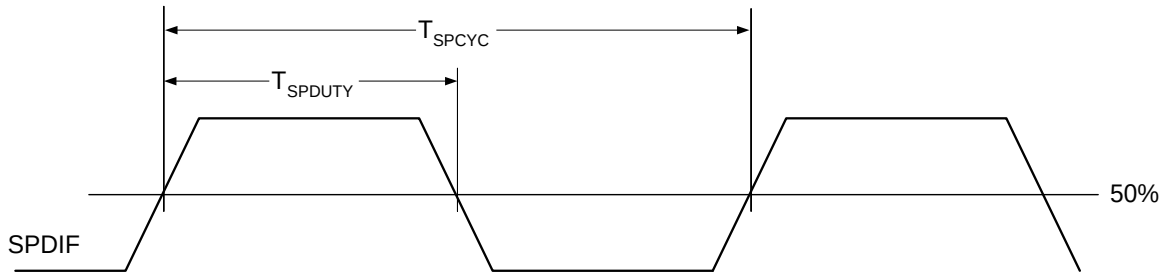


Figure 4.3. S/PDIF Input Timing

4.6.2. Digital Audio Output Timing

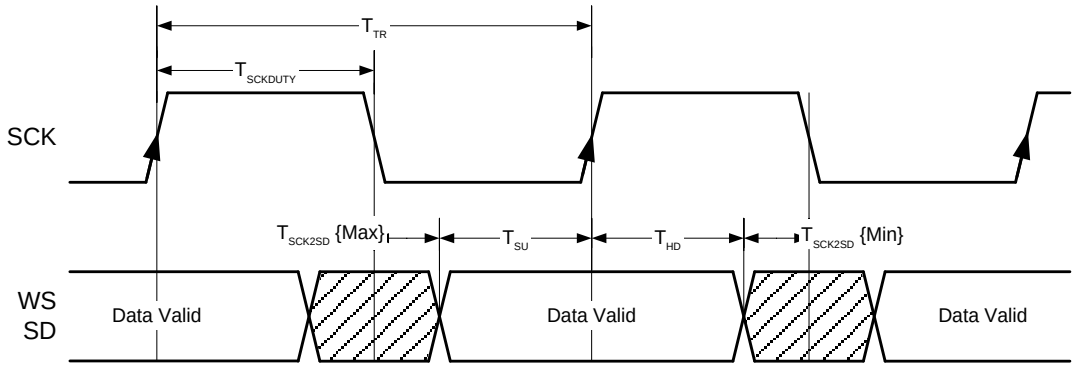


Figure 4.4. I²S Output Timing

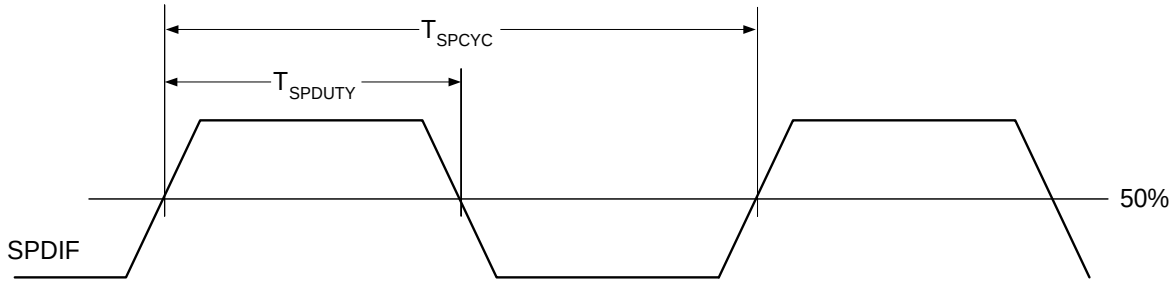


Figure 4.5. S/PDIF Output Timing

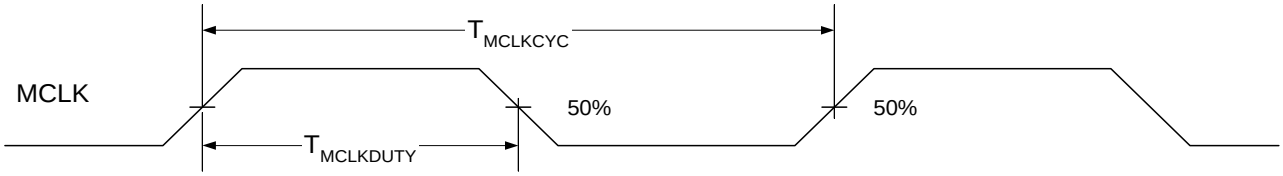


Figure 4.6. MCLK Timing

Table 4.22. Target Crystal Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{XTAL}	External Crystal Frequency	—	—	27	—	MHz

4.7. Target Control Timing Specifications

Table 4.23. Target Reset Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
T_{RESET}	RESET_N Signal LOW Time for Valid Reset	—	200	—	—	µs	Figure 4.7
$T_{RESET\_TO\_I2C\_ACTIVE}$	Delay from Reset deasserted to Local I²C bus active*	—	50	—	—	µs	—

***Note:** Local I²C interface requires initialization after reset, an I²C master device should not start a bus transaction until after this time delay is met.

Figure 4.7 shows the minimum timing interval for RESET_N. RESET_N must be driven LOW for at least the period of T_{RESET} before accessing registers.

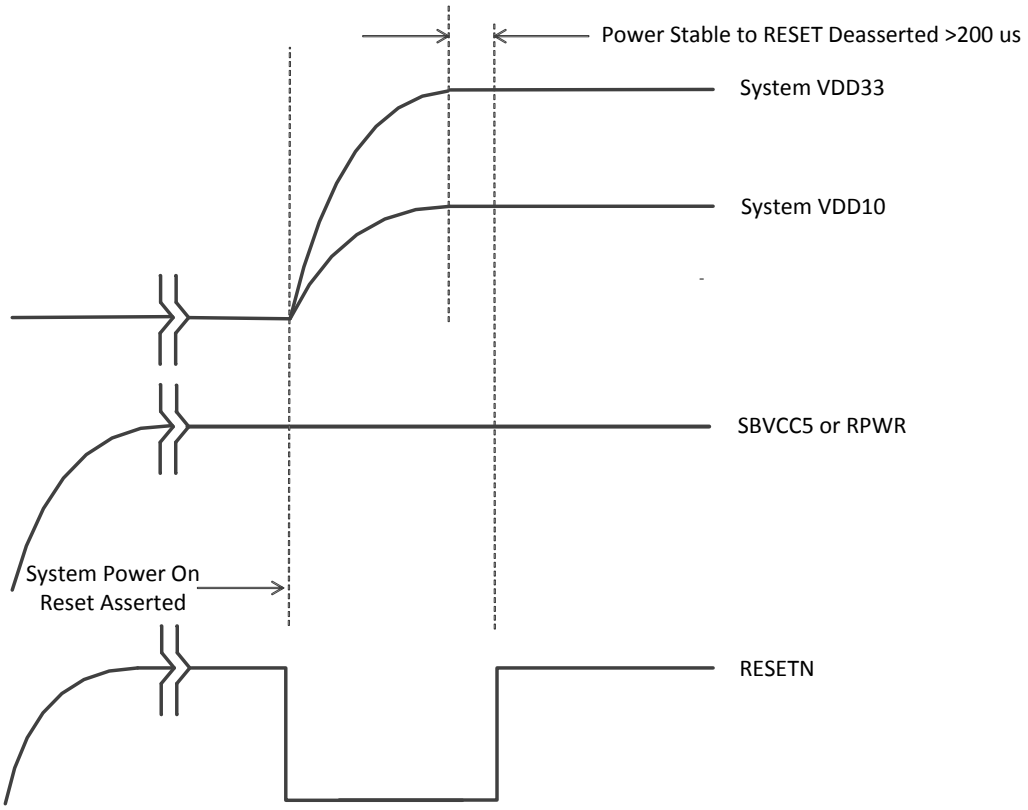


Figure 4.7. RESET_N Minimum Timing

Table 4.24. Target I²C Control Signal Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{I2CDVD}	SDA Data Valid Delay from SCL Falling Edge	C_L = 400 pF	—	—	700	ns	Figure 4.8	—
F_{RXDDC}	Clock Rate on Receiver DDC Port	C_L = 400 pF	—	—	100	kHz	—	1
F_{TXDDC}	Clock Rate on Transmitter DDC Port	C_L = 400 pF	—	—	100	kHz	—	1
F_{I2C}	Clock Rate on Local I²C Port	C_L = 400 pF	—	—	400	kHz	—	2

Notes:
1. DDC ports are limited to 100 kHz by the HDMI Specification, and meet I²C standard mode timings.
2. Local I²C port (CSCL/CSDA) meets standard mode I²C timing requirements to 400 kHz.

Figure 4.8 shows the I²C data valid delay, driving read cycle data.

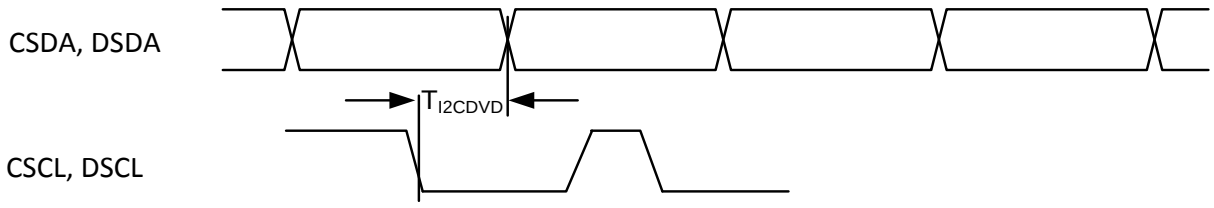


Figure 4.8. I²C Data Valid Delay

Table 4.25. Target Flash Memory and SPI Slave Interface Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
tCLKfreq	SPI Master (SPIM) CLK Frequency	ISP	2.12	—	2.88	MHz	—
		Boot Loading	4.25	—	5.75	MHz	—
	SPI Slave (SPIS) CLK Frequency		—	—	10	MHz	—
tCSs	SPI_CS# Setup Time to SPI_CLK Rising Edge	—	86	—	—	ns	Figure 4.9, Figure 4.10
tCSh	SPI_CS# Hold Time from SPI_CLK Falling Edge	—	86	—	—	ns	Figure 4.9, Figure 4.10
tTXod	SPI_MOSI Output Time from SPI_CLK Falling Edge	—	0	—	8	ns	Figure 4.9, Figure 4.10
tRXs	SPI_MISO Setup Time to SPI_CLK Rising Edge	—	6	—	—	ns	Figure 4.10
tRXh	SPI_MISO Hold Time to SPI_CLK Rising Edge	—	6	—	—	ns	Figure 4.10

Figure 4.9 and Figure 4.10 show the Serial Peripheral Interface write and read timings, respectively.

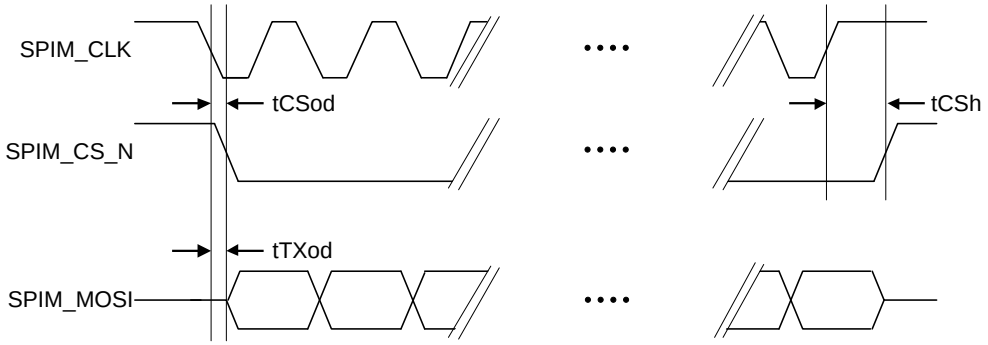


Figure 4.9. SPI Write Timings

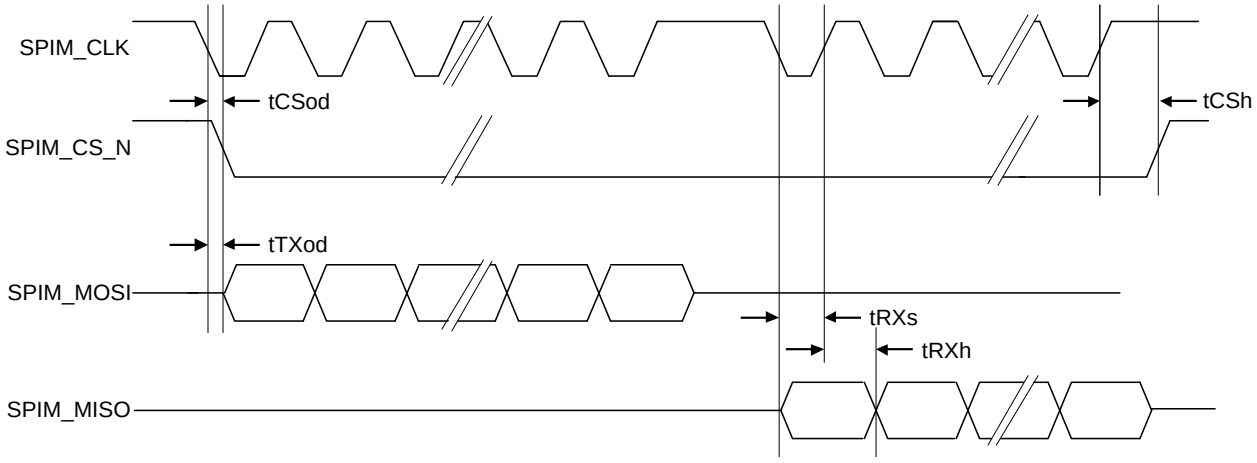


Figure 4.10. SPI Read Timings

5. Pin Diagram and Descriptions

5.1. Pin Diagram

Not Final: Pin assignments are subject to change.

Figure 5.1 shows the pin assignments of the SiI9777 device. The Pin Descriptions section beginning on the next page describes the pin functions. The package is a 28 mm × 28 mm 208-pin LQFP with an ePad. The ePad ***must*** be soldered to a pad on the PC board that is electrically connected to ground.

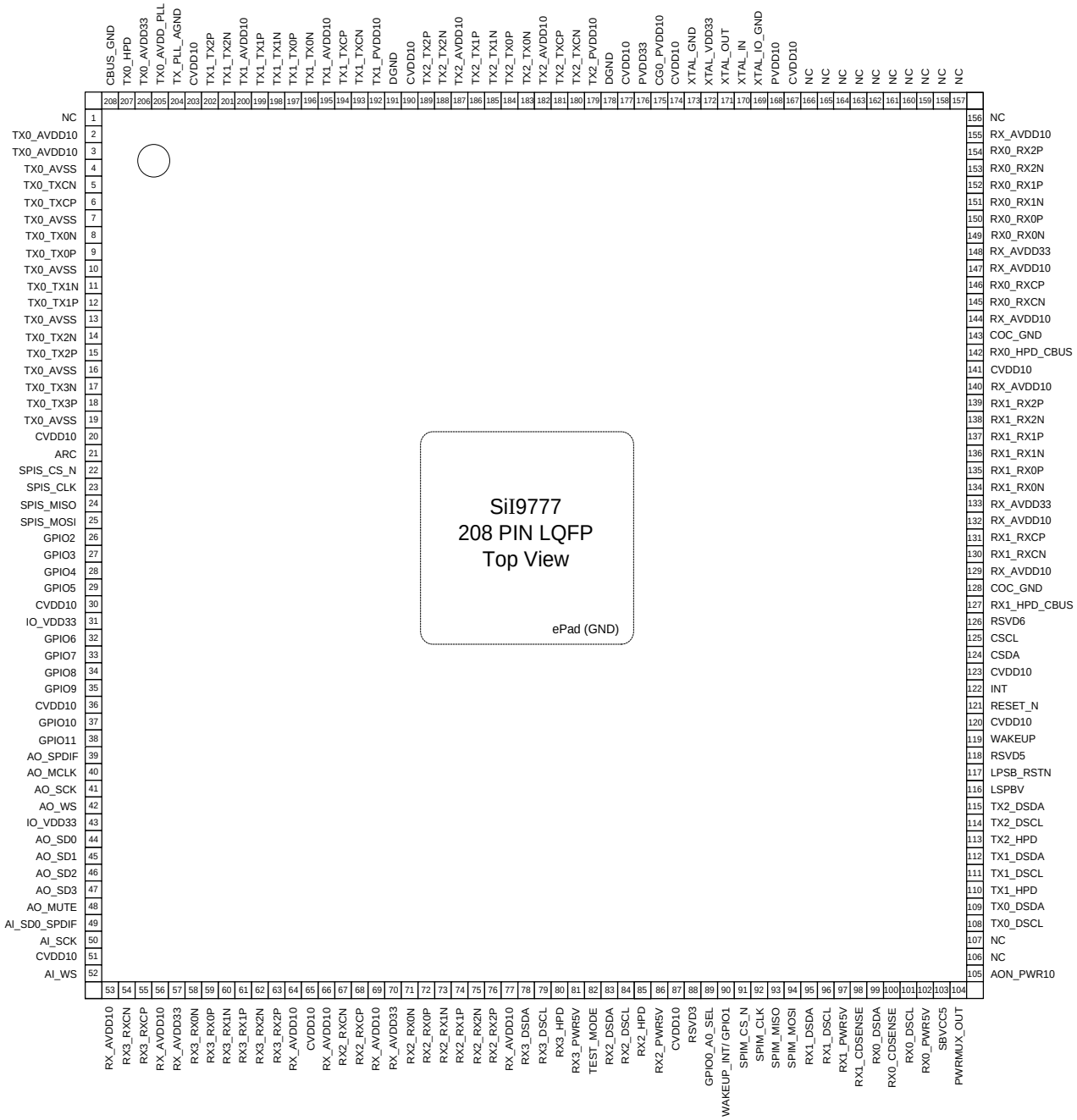


Figure 5.1. Pin Diagram

5.2. Pin Descriptions

Not Final: Pin assignments are subject to change.

5.2.1. HDMI/MHL Transmitter Port TMDS Pins

Pin Name	Pin	Type	Dir	Description
TX0_TXCP	6	TMDS	Output	Transmitter Port 0 TMDS Clock Pair. The transmitter clock pair transmits an HDMI 2.0 or 1.4 differential clock. The maximum link rate supported on this port is 600 Mcsc in HDMI 2 mode.
TX0_TXCN	5			
TX0_TX0P	9	TMDS	Output	Transmitter Port 0 TMDS Data Pairs. HDMI/MHL TMDS output data pairs. This transmitter port supports both HDCP 1.4 and HDCP 2.2 encryption. The TX3P/N pair is used for alternate mapping of reverse connections in an on-board application see Table 3.9.
TX0_TX0N	8			
TX0_TX1P				
TX0_TX1N				
TX0_TX2P				
TX0_TX2N				
TX0_TX3P	18			
TX0_TX3N				
TX1_TXCP	194	TMDS	Output	Transmitter Port 1 TMDS Clock Pair. HDMI 1.4 transmitter TMDS output clock pair. The maximum link frequency supported on this port is 300 MHz.
TX1_TXCN	193			
TX1_TX0P	197	TMDS	Output	Transmitter Port 1 TMDS Data Pairs. HDMI 1.4 transmitter TMDS output data pairs. This transmitter port supports HDCP 1.4 encryption only.
TX1_TX0N				
TX1_TX1P				
TX1_TX1N				
TX1_TX2P				
TX1_TX2N				
TX2_TXCP	181	TMDS	Output	Transmitter Port 2 TMDS Clock Pair. HDMI 1.4 transmitter TMDS output clock pair. The maximum link frequency supported on this port is 300 MHz.
TX2_TXCN	180			
TX2_TX0P	184	TMDS	Output	Transmitter Port 2 TMDS Data Pairs. HDMI transmitter TMDS output data pairs. This transmitter port does not support encryption.
TX2_TX0N				
TX2_TX1P				
TX2_TX1N				
TX2_TX2P				
TX2_TX2N	188			

5.2.2. HDMI Transmitter Port Control Signal Pins

Pin Name	Pin	Type	Dir	Description
TX0_HPD	207	LVTTL Schmitt 5 V tolerant	Input/ Output	Hot Plug Detect for Transmitter Port 0. The HDMI transmitter uses this pin to detect when a Sink is connected.
TX0_DSCL	108	DDC Compliant	Input/ Output	DDC I^2C Clock for Transmitter Port 0. The DDC port provides the communication channel for the HDMI Source device to read the EDID of the Sink and to perform HDCP authentication with the Sink. The DDC port is also used by the Source and Sink devices to exchange data over the Status and Control Data Channel as described in the HDMI Specification. This pin does not present a current path to GND when the device is not powered. A pull-up resistor between 1.5 kΩ to 2.0 kΩ is required on this signal as specified in the HDMI Specification.
TX0_DSDA	109	DDC Compliant	Input/ Output	DDC I^2C Data for Transmitter Port 0. The DDC port provides the communication channel for the HDMI Source device to read the EDID of the Sink and to perform HDCP authentication with the Sink. The DDC port is also used by the Source and Sink devices to exchange data over the Status and Control Data Channel as described in the HDMI Specification. This pin does not present a current path to GND when the device is not powered. A pull-up resistor between 1.5 kΩ to 2.0 kΩ is required on this signal as specified in the HDMI Specification.
TX1_HPD	110	LVTTL Schmitt 5 V tolerant	Input	Hot Plug Detect Input for Transmitter Port 1. The HDMI transmitter uses this pin to detect when a Sink is connected.
TX1_DSCL	111	DDC Compliant	Input/ Output	DDC I^2C Clock for Transmitter Port 1. The DDC port provides the communication channel for the HDMI Source device to read the EDID of the Sink and to perform HDCP authentication with the Sink. This pin does not present a current path to GND when the device is not powered. A pull-up resistor between 1.5 kΩ to 2.0 kΩ to DDC 5 V is required on this signal as specified in the HDMI Specification.
TX1_DSDA	112	DDC Compliant	Input/ Output	DDC I^2C Data for Transmitter Port 1. The DDC port provides the communication channel for the HDMI Source device to read the EDID of the Sink and to perform HDCP authentication with the Sink. This pin does not present a current path to GND when the device is not powered. A pull-up resistor between 1.5 kΩ to 2.0 kΩ to DDC 5 V is required on this signal as specified in the HDMI Specification.
TX2_HPD	113	LVTTL Schmitt 5 V tolerant	Input	Hot Plug Detect Input for Transmitter Port 2. The HDMI transmitter uses this pin to detect when a Sink is connected.
TX2_DSCL	114	DDC Compliant	Input/ Output	DDC I^2C Clock for Transmitter Port 2. The DDC port provides the communication channel for the HDMI Source device to read the EDID of the Sink and to perform HDCP authentication with the Sink. This pin does not present a current path to GND when the device is not powered. A pull-up resistor between 1.5 kΩ to 2.0 kΩ to DDC 5 V is required on this signal as specified in the HDMI Specification.
TX2_DSDA	115	DDC Compliant	Input/ Output	DDC I^2C Data for Transmitter Port 2. The DDC port provides the communication channel for the HDMI Source device to read the EDID of the Sink and to perform HDCP authentication with the Sink. This pin does not present a current path to GND when the device is not powered. A pull-up resistor between 1.5 kΩ to 2.0 kΩ to DDC 5 V is required on this signal as specified in the HDMI Specification.

5.2.3. HDMI/MHL Receiver Port TMDS Pins

Pin Name	Pin	Type	Dir	Description
RX0_RXCP	146	TMDS	Input	Receiver Port 0 TMDS Clock Pair.
RX0_RXCN	145			The receiver clock pair accepts HDMI differential clock.
RX0_RX0P	150	TMDS	Input	Receiver Port 0 Channel 0 TMDS Data Pair.
RX0_RX0N	149			In HDMI, this data pair carries the TMDS Channel 0 data.
RX0_RX1P	152	TMDS	Input	Receiver Port 0 Channel 1 TMDS Data Pair.
RX0_RX1N	151			This data pair carries the TMDS Channel 1 data.
RX0_RX2P	154	TMDS	Input	Receiver Port 0 Channel 2 TMDS Data Pair.
RX0_RX2N	153			This data pair carries the TMDS Channel 2 data.
RX1_RXCP	131	TMDS	Input	Receiver Port 1 TMDS Clock Pair.
RX1_RXCN	130			The receiver clock pair accepts HDMI differential clock.
RX1_RX0P	135	TMDS	Input	Receiver Port 1 Channel 0 TMDS Data Pair.
RX1_RX0N	134			This data pair carries the TMDS Channel 0 data.
RX1_RX1P	137	TMDS	Input	Receiver Port 1 Channel 1 TMDS Data Pair.
RX1_RX1N	136			This data pair carries the TMDS Channel 1 data.
RX1_RX2P	139	TMDS	Input	Receiver Port 1 Channel 2 TMDS Data Pair.
RX1_RX2N	138			This data pair carries the TMDS Channel 2 data.
RX2_RXCP	68	TMDS	Input	Receiver Port 2 TMDS Clock Pair.
RX2_RXCN				The receiver clock pair accepts HDMI differential clock.
RX2_RX0P	72	TMDS	Input	Receiver Port 2 Channel 0 TMDS Data Pair.
RX2_RX0N	71			In HDMI, this data pair carries the TMDS Channel 0 data.
RX2_RX1P	74	TMDS	Input	Receiver Port 2 Channel 1 TMDS Data Pair.
RX2_RX1N	73			This data pair carries the TMDS Channel 1 data.
RX2_RX2P	76	TMDS	Input	Receiver Port 2 Channel 2 TMDS Data Pair.
RX2_RX2N	75			This data pair carries the TMDS Channel 2 data.
RX3_RXCP	55	TMDS	Input	Receiver Port 3 TMDS Clock Pair.
RX3_RXCN	54			The receiver clock pair accepts HDMI differential clock.
RX3_RX0P	59	TMDS	Input	Receiver Port 3 Channel 0 TMDS Data Pair.
RX3_RX0N	58			This data pair carries the TMDS Channel 0 data.
RX3_RX1P	61	TMDS	Input	Receiver Port 3 Channel 1 TMDS Data Pair.
RX3_RX1N				This data pair carries the TMDS Channel 1 data.
RX3_RX2P	63	TMDS	Input	Receiver Port 3 Channel 2 TMDS Data Pair.
RX3_RX2N	62			This data pair carries the TMDS Channel 2 data.

5.2.4. HDMI Receiver Port Control Signal Pins

Pin Name	Pin	Type	Dir	Description
RX0_HPD_CBUS	142	5 V tolerant	Input/ Output	Receiver Port 0 Hot Plug Detect Output and CBUS Input/Output. This is a 5 V tolerant signal with 1 kΩ output impedance. In HDMI mode it indicates that the EDID is readable, in MHL mode this provides the CBUS interface signaling
RX0_DSCL	101	DDC Compliant	Input/ Output	DDC I^2C Clock for Receiver Port 0. The receiver DDC port provides the communication channel for the HDMI Source device to read the EDID of the sink device and to perform HDCP authentication with the Sink device. The DDC port is also used by the Source and Sink devices, to exchange data over the Status and Control Data Channel as defined in the HDMI 2.0 Specification. This pin does not present a current path to GND when the device is not powered. A 47 kΩ pull-up resistor to DDC 5 V is required on this signal as specified in the HDMI Specification.
RX0_CDSENSE	100	Schmitt 5 V tolerant	Input	Receiver Port 0 MHL Cable Detect
RX0_DSDA	99	DDC Compliant	Input/ Output	DDC I^2C Data for Receiver Port 0. The receiver DDC port provides the communication channel for the HDMI Source to read the EDID of the Sink device and to perform HDCP authentication with the Sink device. The DDC port is also used by the Source and Sink devices, to exchange data over the Status and Control Data Channel as defined in the HDMI 2.0 Specification. This pin does not present a current path to GND when the device is not powered.
RX1_HPD_CBUS	127	5 V tolerant	Input/ Output	Receiver Port 1 Hot Plug Detect Output and CBUS Input/Output. This is a 5 V tolerant signal with 1 kΩ output impedance. In HDMI mode it indicates the EDID is readable, in MHL mode this provides the CBUS interface signaling
RX1_DSCL	96	DDC Compliant	Input/ Output	DDC I^2C Clock for Receiver Port 1. The DDC port provides the communication channel for the HDMI Source device to read the EDID of the Sink device and to perform HDCP authentication with the Sink device. The DDC port is also used by the Source and Sink devices, to exchange data over the Status and Control Data Channel as described in the HDMI 2.0 Specification. This pin does not present a current path to GND when the device is not powered. A 47 kΩ pull-up resistor to DDC 5 V is required on this signal as specified in the HDMI Specification.
RX1_CDSENSE	98	Schmitt 5 V tolerant	Input	Receiver Port 1 MHL Cable Detect
RX1_DSDA	95	DDC Compliant	Input/ Output	DDC I^2C Data for Receiver Port 1. The DDC port provides the communication channel for the HDMI Source to read the EDID of the Sink device and to perform HDCP authentication with the Sink device. The DDC port is also used by the Source and Sink devices, to exchange data over the Status and Control Data Channel as described in the HDMI 2.0 Specification. This pin does not present a current path to GND when the device is not powered.
RX2_HPD	85	5 V tolerant	Output	Receiver Port 2 Hot Plug Detect Output and CBUS Input/Output. This is a 5 V signal with 1 kΩ output impedance. It indicates that EDID is readable.

HDMI Receiver Port Control Signal Pins *(continued)*

Pin Name	Pin	Type	Dir	Description
RX2_DSCL	84	DDC Compliant	Input/ Output	DDC I^2C Clock for Receiver Port 2. The receiver DDC port provides the communication channel for the HDMI Source device to read the EDID of the Sink device and to perform HDCP authentication with the Sink device. The DDC port is also used by the Source and Sink devices, to exchange data over the Status and Control Data Channel as defined in the HDMI 2.0 Specification. This pin does not present a current path to GND when the device is not powered. A 47 kΩ pull-up resistor to DDC 5 V is required on this signal as specified in the HDMI Specification.
RX2_DSDA	83	DDC Compliant	Input/ Output	DDC I^2C Data for Receiver Port 2. The receiver DDC port provides the communication channel for the HDMI Source to read the EDID of the Sink device and to perform HDCP authentication with the Sink device. The DDC port is also used by the Source and Sink devices, to exchange data over the Status and Control Data Channel as defined in the HDMI 2.0 Specification. This pin does not present a current path to GND when the device is not powered.
RX3_HPD	80	5 V tolerant	Output	Receiver Port 3 Hot Plug Detect Output. This is a 5 V signal with 1 kΩ output impedance. It indicates that EDID is readable.
RX3_DSCL	79	DDC Compliant	Input/ Output	DDC I^2C Clock for Receiver Port 3. The receiver DDC port provides the communication channel for the HDMI Source device to read the EDID of the Sink device and to perform HDCP authentication with the Sink device. The DDC port is also used by the Source and Sink devices, to exchange data over the Status and Control Data Channel as described in the HDMI 2.0 Specification. This pin does not present a current path to GND when the device is not powered. A 47 kΩ pull-up resistor to DDC 5 V is required on this signal as specified in the HDMI Specification.
RX3_DSDA	78	DDC Compliant	Input/ Output	DDC I^2C Data for Receiver Port 3. The DDC port provides the communication channel for the HDMI Source to read the EDID of the Sink device and to perform HDCP authentication with the Sink device. The DDC port is also used by the Source and Sink devices, to exchange data over the Status and Control Data Channel as described in the HDMI 2.0 Specification. This pin does not present a current path to GND when the device is not powered.

5.2.5. Audio Pins

Pin Name	Pin	Type	Dir	Description
ARC	21	Analog	Input/ Output	Audio Return Channel. In ARC receiver mode, this pin receives an S/PDIF signal from an ARC transmitter-capable Sink and outputs it on the AO_SPDIF pin. In ARC transmitter mode, this pin sends an S/PDIF audio stream from the S/PDIF input to an upstream HDMI device.
AI_SD0_SPDIF	49	LVTTL Schmitt 5 V tolerant	Input	S/PDIF Audio Input, or SD0 input in I^2S mode. This pin has a weak internal pull-down resistor.
AI_SCK	50	LVTTL Schmitt 5 V tolerant	Input	I^2S Audio Input Serial Clock. This pin has a weak internal pull-down resistor.
AI_WS	52	LVTTL Schmitt 5 V tolerant	Input	I^2S Audio Input Word Select. This pin has a weak internal pull-down resistor.
AO_SPDIF	39	LVTTL Schmitt 5 V tolerant	Output	S/PDIF Audio Output
AO_MCLK	40	LVTTL Schmitt 5 V tolerant	Output	I^2S Audio Output MCLK Audio clock reference
AO_SCK	41	LVTTL 5 V tolerant	Output	I^2S Audio Output Serial Clock
AO_WS	42		Output	I^2S Audio Output Word Select
AO_SD0	44		Output	I^2S Audio Output Serial Data Channel 0
AO_SD1	45		Output	I^2S Audio Output Serial Data Channel 1
AO_SD2	46		Output	I^2S Audio Output Serial Data Channel 2
AO_SD3	47		Output	I^2S Audio Output Serial Data Channel 3
AO_MUTE	48		Output	I^2S Audio Output Mute Signal

5.2.6. Control and Configuration Pins

Control and configuration pins are 5 V tolerant.

Pin Name	Pin	Type	Dir	Description
RESET_N	121	LVTTL Schmitt 5 V tolerant	Input	External Reset. Active LOW reset signal to the device. See Figure 4.7 for reset timing requirements.
XTAL_IN	170	LVTTL Schmitt	Input	Crystal or Oscillator Input*
XTAL_OUT	171	LVTTL	Output	Crystal Feedback Output*
INT	122	LVTTL 5 V tolerant	Output	Interrupt Output. The INT pin can be programmed to be an open-drain output (default) or a push-pull LVTTL output. The polarity can be set to negative (default) or positive asserted.
GPIO0_A0_SEL	89	LVTTL 5 V tolerant Schmitt	Input/ Output	Programmable GPIO pins. During chip reset, the level on the GPIO0 pin is latched during AON reset to set the local I^2C device address: • LOW – Set device address to 0x40 • HIGH – Set device address to 0x42 GPIO0 derives its power from the Standby (AON) power domain. This pin has a weak pull-down resistor internally. When left open the default I^2C address will be 0x40. When using the pin as a GPIO, ensure that external circuitry does not interfere with the intended state of the pin during AON reset. During reset, the logic level on the pin is sampled to determine the local I^2C address.
WAKEUP_INT/GPIO1	90			WAKEUP_INT/ GPIO1 –The power on default of this pin is the WAKEUP_INT signal from the LPSB (Low Power Standby) Logic. Alternately, the pin can be configured as a GPIO. The functionality of this pin is configured through the *gl_int_wakeup_config* register 0x07F. GPIO1 derives its power from the Standby power domain.
GPIO2	26			GPIO2-11 – These pins can be used as General Purpose Input and Output functions. Refer to the API Reference for details on how to access the control registers for these pins.
GPIO3	27			
GPIO4	28			
GPIO5	29			
GPIO6	32			
GPIO7	33			
GPIO8	34			
GPIO9	35			
GPIO10	37			
GPIO11	38			
CSCL	125	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	Local Configuration/Status I^2C Clock. Chip configuration and status are accessed using this I^2C port. This pin requires an external pull-up resistor. A value of 4.7 kΩ or lower is suggested.
CSDA	124	LVTTL Schmitt Open-drain 5 V tolerant	Input/ Output	Local Configuration/Status I^2C Data. Chip configuration and status are accessed using this I^2C port. This pin requires an external pull-up resistor. A value of 4.7 kΩ or lower is suggested.
WAKEUP	119	LVTTL Open-drain 5 V tolerant	Output	WAKEUP output to system power management controller. Active HIGH wakeup signal to signal a wakeup event to system power management controller. This pin should be pulled up through a 10K resistor to the LPSBV supply pin (Pin 116).

***Note**: A 27 MHz crystal or oscillator clock source is required for operation. Refer to Figure 5.2 on page 50.

Control and Configuration Pins *(continued)*

Pin Name	Pin	Type	Dir	Description
LPSB_RSTN	117	LVTTL 3.3 V tolerant	Input	Low Power Standby Active Low Reset Input. This pin should be connected to system power controller through an open drain output to provide an active low reset signal. The input should be pulled high through a voltage divider to LBSPV_5V supply. See Figure 5.3 on page 51.
SPIM_CS_N	91	LVTTL Schmitt 5 V tolerant	Output	Flash Memory Interface Chip Select.
SPIM_CLK	92	LVTTL Schmitt 5 V tolerant	Output	Flash Memory Interface Clock Output Signal.
SPIM_MISO	93	LVTTL Schmitt 5 V tolerant	Input	Flash Memory Interface Data Input Signal.
SPIM_MOSI	94	LVTTL Schmitt 5 V tolerant	Output	Flash Memory InterfaceData Output.
SPIS_CS_N	22	LVTTL Schmitt 5 V tolerant	Input	SPI Host Slave Interface Chip Select.
SPIS_CLK	23	LVTTL Schmitt 5 V tolerant	Input	SPI Host Slave Interface CLK Input Signal.
SPIS_MISO	24	LVTTL Schmitt 5 V tolerant	Output	SPI Host Slave Interface Data Output Signal.
SPIS_MOSI	25	LVTTL Schmitt 5 V tolerant	Input	SPI Host Slave Interface Data Input Signal.

5.2.7. Power and Ground Pins

Pin Name	Pin	Type	Description	Supply
SBVCC5	103	Power	Always On local power system power	5.0 V
AON_PWR10	105	Power	AON internal 1.0 V regulator This pin requires a 330 Ω resistor connected from this pin to PWRMUX_OUT (Pin 104), see Figure 5.4 on page 51. Note: For Revision 1.1 Silicon, no resistor connection is required, leave pin open.	1.0V
LPSBV	116	Power	Low power standby voltage. Always-On, ultra-low standby power used for MHL input detection to cause a wakeup event. This pin should either be connected to a 5 V ultra-low power supply (if available in the system) or connected to SBVCC5.	5.0 V
RX0_PWR5V	102	Power	RX0 5 V DDC power input	5.0 V
RX1_PWR5V	97	Power	RX1 5 V DDC power input	5.0 V
RX2_PWR5V	86	Power	RX2 5 V DDC power input	5.0 V
RX3_PWR5V	81	Power	RX2 5 V DDC power input	5.0 V
IO_VDD33	31, 43	Power	I/O power supply	3.3 V
RX_AVDD33	57, 70, 133, 148	Power	TMDS receiver analog 3.3 V power supply	3.3 V
PWRMUX_OUT	104	Power	On-Chip 3.3 V regulator power output. This pin requires an external 2.2 µF capacitor to ground. Maximum output current is 30 mA.	3.3 V
PVDD33	176	Power	PLL 3.3 V supply	3.3 V
XTAL_VDD33	172	Power	Crystal oscillator 3.3 V power supply	3.3 V
TX0_AVDD33	206	Power	TMDS transmitter 0 3.3 V analog power supply	3.3 V
TX0_AVDD_PLL	205	Power	PLL 1.0 V analog supply voltage	1.0 V
RX_AVDD10	53, 56, 64, 66, 69, 77, 129, 132, 140, 144, 147, 155	Power	TMDS receiver analog 1.0 V power supply	1.0 V
TX0_AVDD10	2, 3	Power	TMDS Transmitter 0 analog power supply	1.0 V
TX1_AVDD10	195, 200	Power	TMDS Transmitter 1 analog power supply	1.0 V
TX2_AVDD10	182, 187	Power	TMDS Transmitter 2 analog power supply	1.0 V
TX2_PVDD10	179	Power	TMDS Transmitter 0 PLL power supply	1.0 V
TX1_PVDD10	192	Power	TMDS Transmitter 1 PLL power supply	1.0 V
PVDD10	168	Power	PLL 1.0 V supply	1.0 V
CVDD10	20, 30, 36, 51, 65, 87, 120, 123, 141, 167, 174, 177, 190, 203	Power	Digital core power supply	1.0 V
CG0_PVDD10	175	Power	Clock generator 0 PLL power supply	1.0 V
XTAL_GND	173	Ground	Crystal Ground. Connect directly to ground plane.	Ground
XTAL_IO_GND	169	Ground	Crystal I/O Ground. Connect directly to ground plane.	Ground
TX_PLL_AGND	204	Ground	PLL Ground. Connect directly to ground plane.	Ground
TX0_AVSS	4, 7, 10, 13, 16, 19	Ground	TX0 Signal Ground. Connect directly to ground plane.	Ground
CBUS_GND	208	Ground	MHL CBUS ground return. Connect directly to ground plane.	Ground

Power and Ground Pins (*continued*)

Pin Name	Pin	Type	Description	Supply
COC_GND	128, 143	Ground	Analog Ground for MHL3 RX0, RX1 COC. Connect directly to ground plane.	Ground
DGND	178, 191	Ground	TX PLL Ground. Connect directly to ground plane.	Ground
GND	ePad	Ground	The ePad ***must*** be soldered to ground.	Ground

5.2.8. Reserved Pins

Pin Name	Pin	Type	Description
NC	1, 106, 107, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166	Reserved	No Connect. These pins have no internal connection on the device and should be left open in the system.
TEST_MODE	82	Reserved Input	Factory Test Only. Connect this signal to ground through a 10K resistor.
RSVD3	88	Reserved Input	Reserved for future use. Connect this signal to ground through a 10K resistor.
RSVD5	118	Reserved Output Open-Drain	Reserved for future use. No Connect
RSVD6	126	Reserved Input	Reserved for future use. No Connect

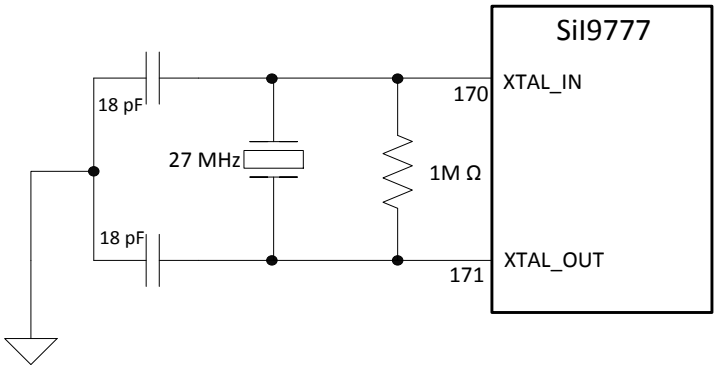


Figure 5.2 27 MHz Crystal Circuit

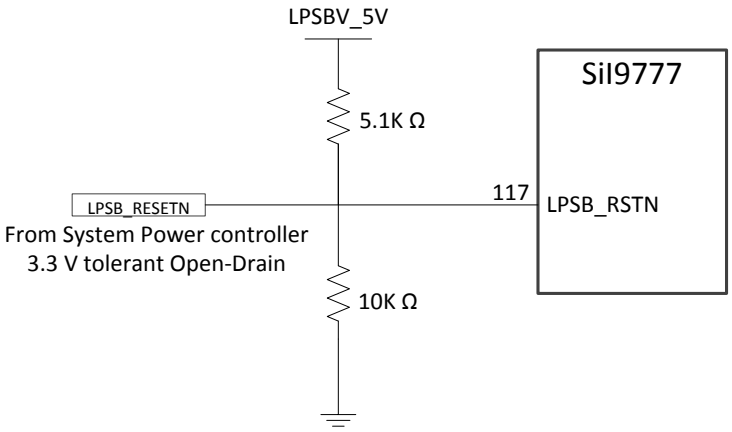


Figure 5.3 LPSB_RSTN Circuit

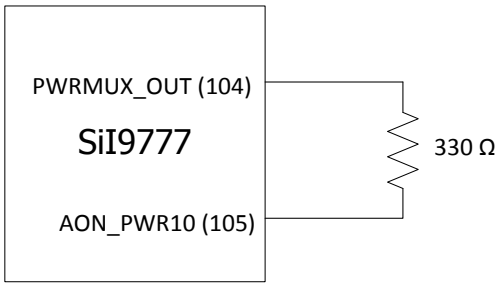


Figure 5.4 External Resistor for AON _PWR10

6. Design Recommendations

6.1. Power Supply Decoupling

Designers should include decoupling and bypass capacitors at each power signal in the layout. These are shown schematically in Figure 6.1. Connections in one group (such as AVDD10) can share C2, C3, and the ferrite, with each pin having a separate C1 placed as close to the pin as possible. Figure 6.2 shows an option for implementing power connections on the transmitter.

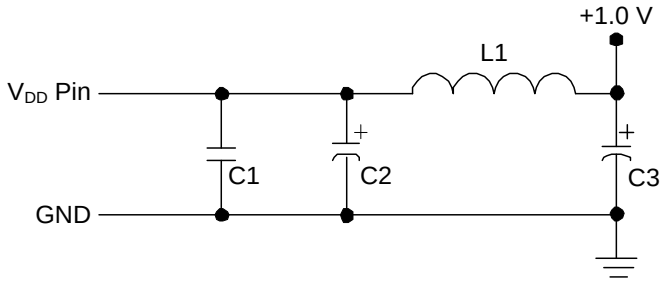


Figure 6.1. Decoupling and Bypass Schematic

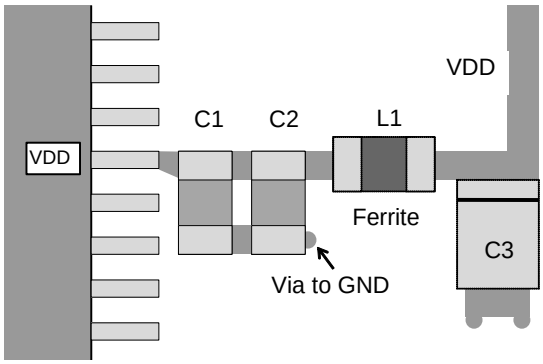


Figure 6.2. Decoupling and Bypass Capacitor Placement

6.2. Layout Guidelines

To ensure signal integrity of the system, Silicon Image recommends these design guidelines:

- Place the input and output connectors that carry the TMDS signals as close as possible to the chip.
- Route the TMDS differential pairs together and as directly as possible from the connector to the device.
- Route each TMDS differential pair with controlled differential impedance of 100 Ω.
- Avoid routing the TMDS signal lines through vias.
- Place external ESD devices, if used, close to the HDMI connector.
- Series resistors included on the receiver TMDS signal lines for impedance matching should be placed as close as possible to the device.
- Serpentine traces are not recommended to compensate for intra- and inter-pair trace skew of the TMDS signal lines.

6.3. Electrostatic Discharge Protection

The SiI9777 device can withstand electrostatic discharges (ESD) due to handling during manufacture. In applications where higher protection levels are required, ESD-limiting components can be placed on the differential lines of the chip. These components typically have a capacitive effect that reduces the signal quality at higher clock frequencies. Use the lowest capacitance devices possible. ESD components must be placed as close as possible to the input or output connector. In no case can the capacitance value of these components exceed 1 pF.

6.4. Electromagnetic Interference Considerations

Electromagnetic interference (EMI) is a function of board layout, shielding, receiver component operating voltage, frequency of operation, and other factors. When attempting to control emissions, it is important not to place any passive components on the differential signal lines, except the common-mode chokes and ESD protection described earlier. The differential signaling used in HDMI is inherently low in EMI if the routing recommendations noted in the Layout Guidelines section are followed.

The PCB ground plane should extend unbroken under as much of the transmitter chip and associated circuitry as possible, with all ground pins of the chip using a common ground.

7. Package Information

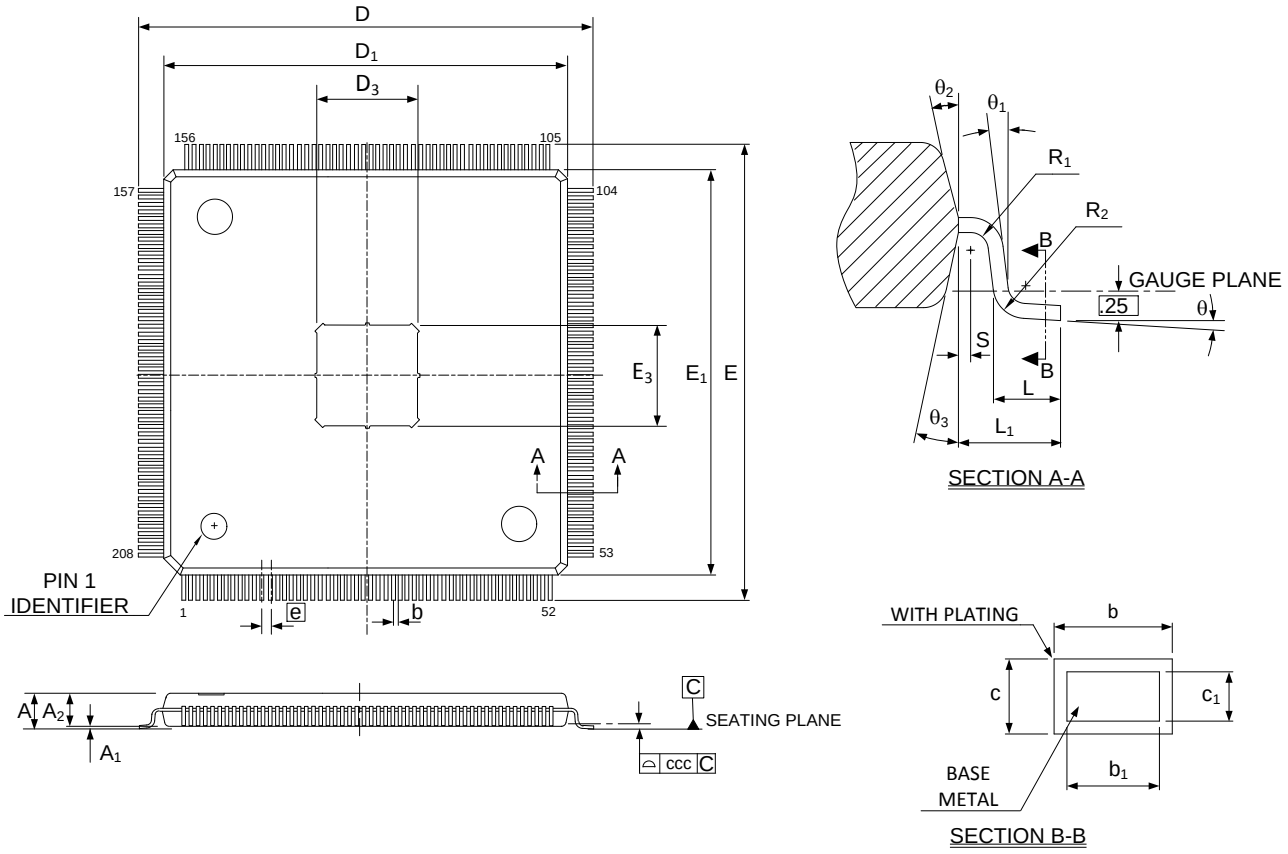
7.1. ePad Requirements

The SiI9777 transmitter/port processor is packaged in a 208-pin, 28 mm × 28 mm LQFP package with an exposed pad (ePad) that is used for the electrical ground of the device and for improved thermal transfer characteristics. The ePad dimensions are 7.2 mm × 7.2 mm (±0.15 mm). Soldering the ePad to the ground plane of the PCB is **required** to meet package power dissipation requirements at full speed operation, and to correctly connect the chip circuitry to electrical ground. As a general guideline, a clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical shorts.
Figure 7.1 on the next page shows the package dimensions of the SiI9777 transmitter/port processor.

7.2. Package Dimensions

These drawings are not to scale. Dimensions are in millimeters.

Not Final: Package diagram or dimensions are subject to change.



JEDEC Package Code MS-026

Item	Description	Min	Typ	Max
A	Thickness	—	—	1.60
A_1	Stand-off	0.05	—	0.15
A_2	Body thickness	1.35	1.40	1.45
b	Lead width (with plating)	0.17	0.22	0.27
b_1	Lead width (base metal)		0.20 REF	
c	Lead thickness (with plating)	0.12	—	0.20
c_1	Lead thickness (base metal)		0.13 REF	
D	Footprint	29.85	30.00	30.15
D_1	Body size	27.90	28.00	29.10
E	Footprint	29.85	30.00	30.15
E_1	Body size	27.90	28.00	28.10
D_3/E_3	Exposed pad size		7.2 REF	

Item	Description	Min	Typ	Max
e	Lead pitch		0.50 BSC	
L	Lead foot length	0.45	0.60	0.75
L_1	Total lead length		1.00 REF	
R_1	Lead radius, inside		0.15	
R_2	Lead radius, outside		0.15	
S	Lead horizontal run		0.21	
Θ	—	0°	3.5°	7°
$Θ_1$	—		7° REF	
$Θ_2$	—		12° REF	
$Θ_3$	—		12° REF	
ccc	—		0.08	

Figure 7.1. Package Diagram

7.3. Marking Specification

Not Final: Marking diagram is subject to change.

Figure 7.2 shows the markings of the SiI9777 package. This drawing is not to scale.

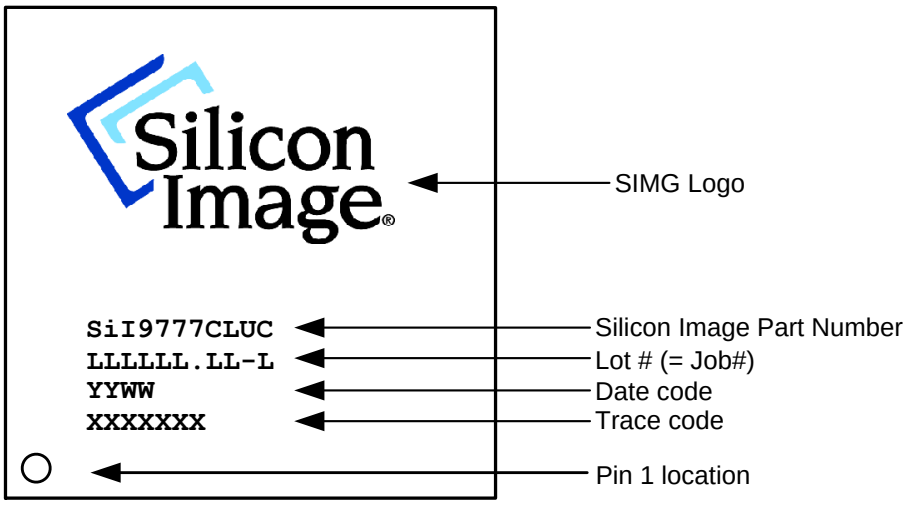


Figure 7.2. Marking Diagram

7.4. Ordering Information

Production Part Numbers:

Device	Part Number
SiI9777 18 Gb/s Transmitter and Port Processor for HDMI 2.0 and MHL 3 with HDCP 2.2	SiI9777CLUC

References

Standards Documents

This is a list of the standards abbreviations appearing in this document.

Abbreviation	Standards Publication, Organization, and Date
CEA-861-F	*A DTV Profile for Uncompressed High Speed Digital Interfaces*, EIA/CEA, May 2013
DVI	*Digital Visual Interface,* Revision 1.0, Digital Display Working Group, April 1999
EDDC	*Enhanced Display Data Channel Standard*, Version 1.1, VESA, September 1999
E-EDID	*Enhanced Extended Display Identification Data Standard*, Release A Revision 1, VESA, February 2000
E-DID IG	*VESA EDID Implementation Guide*, VESA, June 2001
HCTS	*HDMI Compliance Test Specification,* Revision 1.4b, HDMI Licensing, LLC, October 2011
HDCP	*High-bandwidth Digital Content Protection,* Revision 1.4, Digital Content Protection, LLC, July 2009
HDMI	*High Definition Multimedia Interface*, Revision 2.0, HDMI Consortium; September 2013 *High Definition Multimedia Interface*, Revision 1.4b, HDMI Licensing, LLC, October 2011
MHL	*MHL (Mobile High-Definition Link) Specification*, Version 3.0, MHL, LLC, September 2013

For information on the specifications that apply to this document, contact the responsible standards groups appearing on this list.

Standards Group	Web URL	e-mail	Phone
ANSI/EIA/CEA	http://global.ihs.com	global@ihs.com	800-854-7179
DVI	http://www.ddwg.org	ddwg.if@intel.com	—
HDCP	http://www.digital-cp.com	info@digital-cp.com	—
HDMI	http://www.hdmi.org	admin@hdmi.org	—
MHL	http://www.mhlconsortium.org	info@mhlconsortium.org	408-962-4269
VESA	http://www.vesa.org	—	408-957-9270

Silicon Image Documents

This is a list of the related documents that are available from your Silicon Image sales representative.

Document	Title
UG-1131	CP9777 HDCP 2.2 Transmitter and Port Processor for HDMI 2.0 and MHL 3 Starter Kit User Guide
TBD	Sil9777 Transmitter/Port Processor Driver API Reference

Revision History

Revision 0.80, September 2014

First preliminary release.

1. Updated Figure 2.1. Functional Block Diagram.
2. Added new Power Domains section.
3. Added new Video Stream Splitting section.
4. Updated HDCP Cores section.
5. Updated Boot Loader section.
6. Updated Microcontroller Unit section.
7. Updated Host Interface section to include SPI slave bus.
8. Updated Video Input Format Support section with rules to implement support for a particular video format.
9. Updated Table 3.9. TMDS Output Pin Order before and after Inverting, added table note.
10. Added Local Host Interface section.
11. Updated information on I^2C address boot loader configuration in Local I2C Interface section.
12. Updated Min values of LPSBV, RXn_PWR5V, SBVCC5, and Max values of Θja, Θjc in Table 4.2. Target Normal Operating Conditions.
13. Updated Max values in Table 4.4. Target Power Requirements.
14. Added $V_{OH\_CBUS\_DISCOVERY}$ to Table 4.10. Target Digital CBUS I/O Specifications, updated Min value of V_{OH_CBUS}.
15. Added new Table 4.18. Target I2S Input Port AC Specifications and Table 4.19. Target I2S Output Port AC Specification.
16. Updated Min value of T_{RESET} in Table 4.23. Target Reset Timings, added $T_{RESET\_TO\_I2C\_ACTIVE}$.
17. Added new Figure 4.7. RESET_N Minimum Timing.
18. Added SPI Slave (SPIS) CLK Frequency to Table 4.25. Target Flash Memory and SPI Slave Interface Timing.
19. Added TX0_TX3P and TX0_TX3N to HDMI/MHL Transmitter Port TMDS Pins.
20. Updated TX0_HPD in HDMI Transmitter Port Control Signal Pins.
21. Updated RX1_HPD_CBUS in HDMI Receiver Port Control Signal Pins.
22. Updated AI_SCK, AI_WS, AO_SPDIF, AO_MCLK, and AO_WS in Audio Pins.
23. Updated RESET_N, XTAL_OUT, GPIO0_A0_SEL, WAKEUP_INT/GPIO1, CSCL, WAKEUP, SPIM_CLK, SPIM_MOSI, SPIS_CS_N, SPIS_CLK, SPIS_MISO and SPIS_MOSI, and added LPSB_RSTN to Control and Configuration Pins.
24. Added AON_PWR10 and TX0_AVSS to Power and Ground Pins, updated LPSBV and PWRMUX_OUT.
25. Updated Reserved Pins.
26. Added new Figure 5.4 External Resistor for AON _PWR10, Figure 5.3 LPSB_RSTN Circuit, and Figure 5.2 27 MHz Crystal Circuit.

Revision 0.70, May 2014

First advance release.

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