SiI9134 HDMI Deep Color Transmitter

Data Sheet

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Revision History

Revision	Date	Comment
A	11/2006	Tables of AC and DC specification were updated.
B	12/2006	Updated DC specifications and overall matting.
B01	2/2007	UpdatedI CCT and ISTBY specifications.
C	4/2007	Added Audio Down-sampler inmation and HDMI design considerations
D	10/2007	Corrected DC and Digital I/O specifications, hot plug inmation, and other content
E	8/2009	Updated to include 3D provided in the HDMI 1.4 Standard.
E01	5/2010	Updated page 1 and layout to prepare Data Brief; minor editing throughout.
F	7/2010	Updated Table 22; clarified 3D inmation.

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General Description

The SiI9134 HDMI Deep Color Transmitter is a third-generation High Definition Multimedia Interface (HDMI®) transmitter that provides a simple method of sending protected digital audio and video that provides end rs with a truly all-digital experience. A/V receivers, along with Blu-ray Disc™ and HD DVD players and recorders, can provide high quality digital audio and video over a simple, low cost cable. The SiI9134 transmitter extends the family of HDMI transmitters by supporting 30-bit and 36-bit Deep Color video, and incorporates a flexible audio and video interface. It is software and pin-compatible with the SiI9034 transmitter.

The transmitter performs the 10- or 12-bit to 8-bit conversion of the 10/12-bit Deep Color video input data by increasing the TMDS™ clock frequency and packing the extra bits into the next byte. An

225 MHz to support Deep Color and 1080p integrated color-space converter allows direct connection to all major MPEG decoders, including those that provide an ITU.656 output. Pre-programmed High Bandwidth Content Protection

(HDCP) keys provide the highest level of key security; which simplifies manufacturing and lowers cost.

HDMI Output

- Supports Deep Color and High-Bitrate Audio
- Supports all the mandatory and several optional 3D mats described in the HDMI 1.4 Specification
- s the latest generation of TMDS core , which operates from 25 MHz to

resolution

- Backward compatibility with the DVI Specification allows HDMI systems to connect to DVI displays.

Digital Video Interface

- Supports DVD and HD MPEG decoders
- 24-bit, 30-bit, and 36-bit RGB/YCbCr 4:4:4 (Deep Color)
- 16-bit, 20-bit, and 24-bit YCbCr 4:2:2
- 8-bit, 10-bit, and 12-bit YCbCr 4:2:2 (ITU.601 and ITU.656)
- 12-bit, 15-bit and 18-bit dual-edge clocking input modes
- YCbCr-to-RGB color space conversion
- BTA-T1004 video input mat
- Input clock divider or multiplier (input clock frequencies of 0.5x, 2x, 4x).
- Programmable Data Enable generator and sync extraction.

Digital Audio Interface

- DTS HD and Dolby True HD high bit rate audio support
- A dedicated 4-pin Direct Stream Digital (DSD) 8-channel input provides Super Audio CD (SACD) and decoded

  Dolby Digital applications
- Four I²S inputs with flexible channel mapping support

  High Bit-Rate audio and accept Dolby Digital and DVD-Audio input (2-channel 192 kHz, 8-channel 192 kHz)
- S/PDIF input supports PCM, Dolby Digital, and DTS

  digital audio transmission (32–192 kHz sample rate)
- IEC60958 or IEC61937 compatible
- 2:1 and 4:1 down-sampling handles 96 kHz and 192 kHz audio streams

Control Capability

- Monitor Detection supported through Hot Plug and Receiver Detection
- Master I²C interface DDC connection simplifies board layout and lowers cost.

- HDCP encryption engine transmitting protected audio and video content
- Flexible power management.

Package

- 100-pin14 mm by 14 mm TQFP package

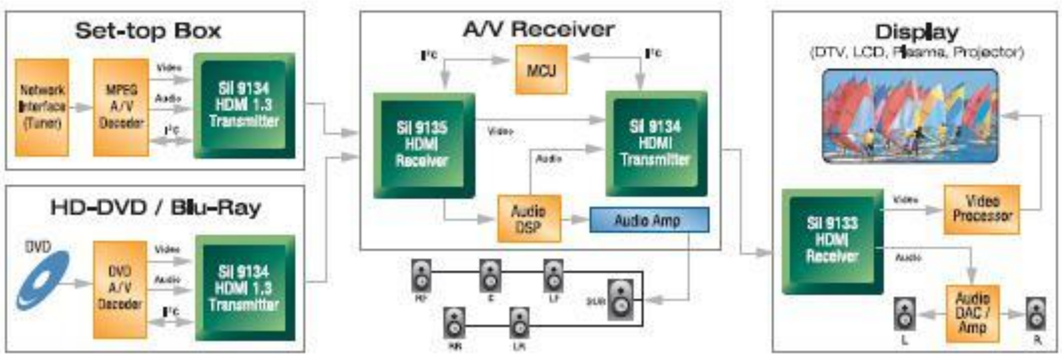


Figure 1. SiI9134 System Diagram

SiI9134 Transmitter Compared with SiI9030 and SiI9034 Devices

Table 1 summarizes the differences among the SiI9030, the SiI9034, and the SiI9134 HDMI transmitters.

Table 1. Summary of New Features

Transmitter	SiI9030	SiI9034	SiI9134
Video Input			
Digital Video Input Ports	1	1	1
I/O Voltage	3.3 V	3.3 V	3.3 V
Input Pixel Clock Multiply/Divide	0.5x, 2x, 4x	0.5x, 2x, 4x	0.5x, 2x, 4x
Maximum Pixel Input Clock Rate	150 MHz	165 MHz	165 MHz
Maximum TMDS Output Clock	150 MHz	165 MHz	225 MHz
BTA-T1004 mat Support	Yes	Yes	Yes
Video mat Conversion			
36-Bit and 30-Bit Deep Color	No	No	Yes
YCbCr → RGB CSC	Yes	Yes	Yes
RGB → YCbCr CSC	No	Yes	Yes
4:2:2 → 4:4:4 Upsampling	Yes	Yes	Yes
4:4:4 → 4:2:2 Decimation	No	Yes	Yes
16-235 → 0-255 Expansion	Yes	Yes	Yes
0-255 → 16-235 Compression	No	Yes	Yes
One-bit Audio (DSD/SACD)	No	Yes	Yes
16-235/240 Clipping	No	Yes	Yes
Audio Input			
S/PDIF Input Ports	1	1	1
I²S Input Bits	4 (8-channel)	4 (8-channel)	4 (8-channel)
High Bit Rate Audio Support	No	No	Yes
Compressed DTS-HD and Dolby True-HD			
2-Channel Maximum Sample Rate	192 kHz on I²S 96 kHz on S/PDIF	192 kHz on I²S 192 kHz on S/PDIF	192 kHz on I²S 192 kHz on S/PDIF
8-Channel Maximum Sample Rate	96 kHz	192 kHz	192 kHz
Down Sampling	96 kHz to 48 kHz	96 kHz to 48 kHz	96 kHz to 48 kHz
[redacted]			
I²C Address Bus			
Device Address Select	CI2CA Pin	CI2CA Pin	CI2CA Pin
Master DDC Bus	Yes	Yes	Yes
Other	—	—	—
3D Support	No	No	Yes
HDCP Reset	Software Register	Software Register	Software Register
Package	80-pin TQFP ePad	100-pin TQFP	100-pin TQFP

Pin Diagram

Figure 2 shows the pin connections the SiI9134 transmitter in the 100-pin TQFP package. Individual pin functions are described in the Pin Descriptions section beginning on page 25.

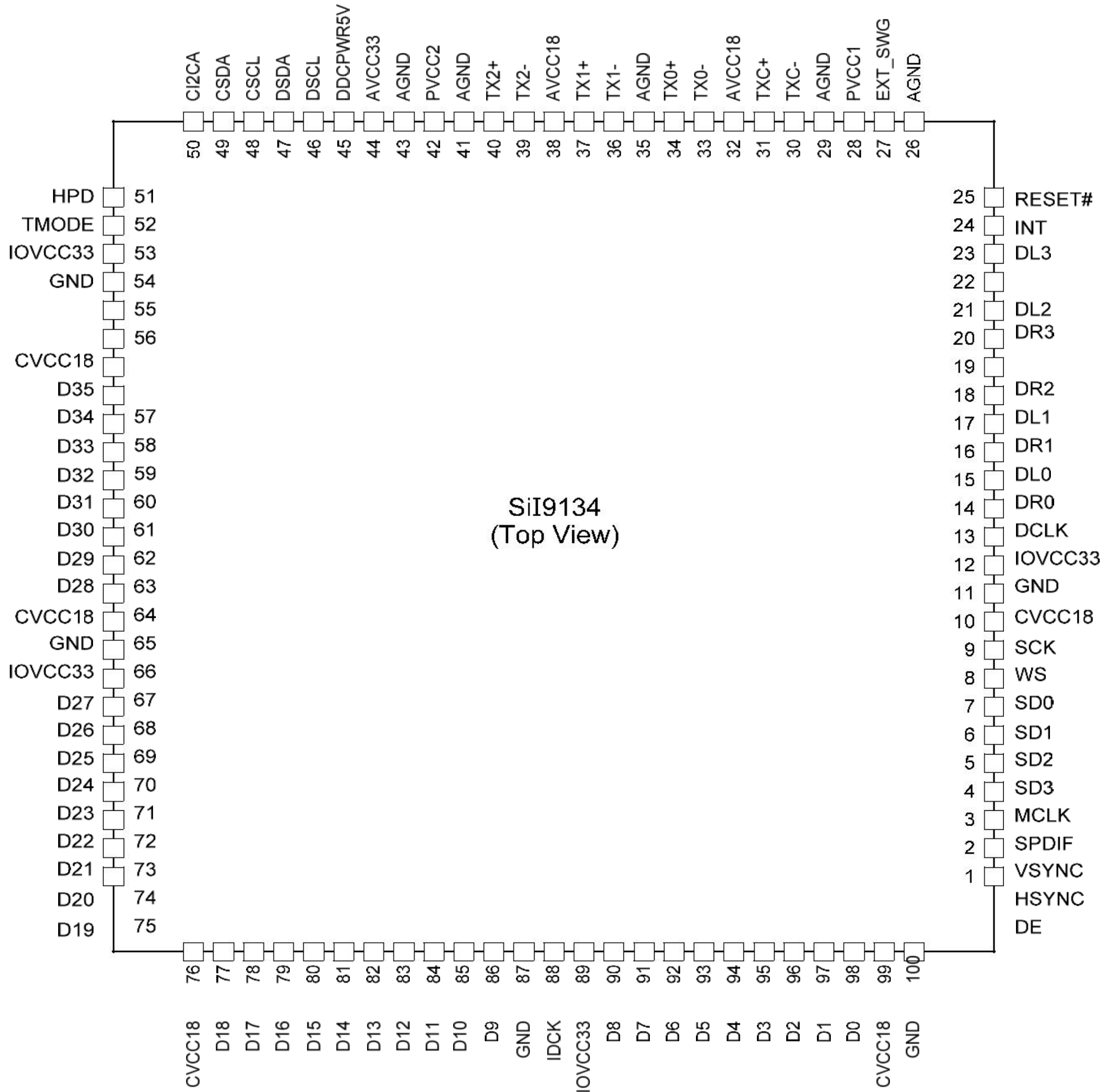


Figure 2. Pin Diagram

Description

The SiI9134 transmitter provides a complete solution transmitting HDMI digital audio or video. Specialized audio and video processing available within the transmitter adds HDMI capability to consumer electronics devices easily and cost effectively. Figure 3 shows the functional blocks of the device. Pin descriptions begin on page 25.

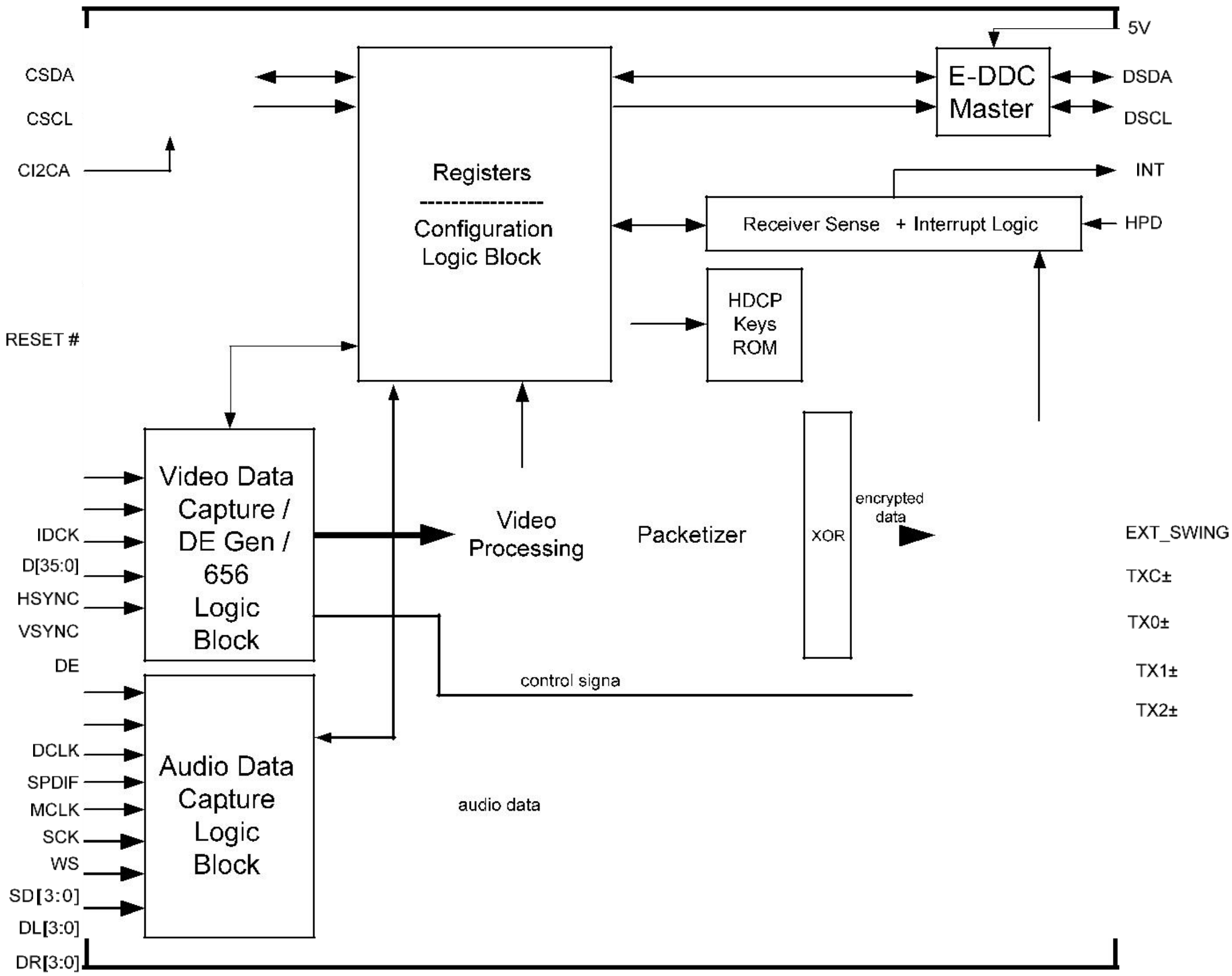


Figure 3 Functional Block Diagram

Video Data Input and Conversion

Video Processing Pipeline

Figure 4 shows the video data processing stages. Each of the processing blocks can be bypassed by setting the appropriate register bits. The HSYNC and VSYNC input signals are required except in embedded sync modes. The DE input signal is optional; the DE generator can create this signal using the HSYNC and VSYNC pulses.

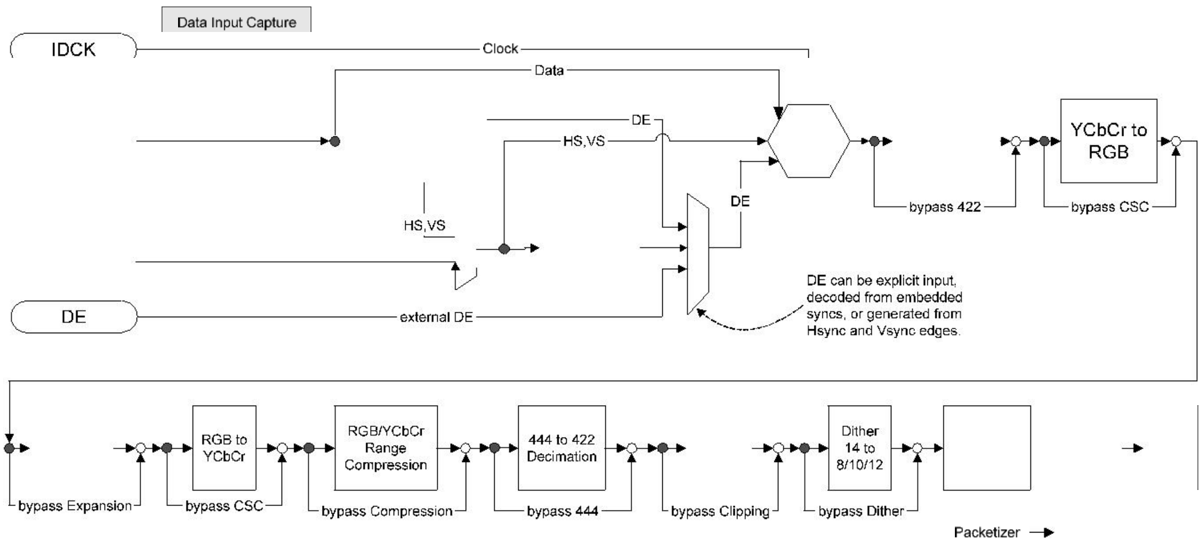


Figure 4. Transmitter Video Data Processing Path

Input Clock Multiplier/Divider

The input pixel clock can be multiplied by 0.5, 1, 2, or 4. Video input mats that a 2x clock (such as YC Mux mode) can then be transmitted across the HDMI link with a 1x clock; similarly with 1x to 2x, 1x to 4x and 2x to 4x.

Video Data Capture Logic

The video data capture logic receives uncompressed digital video through an 8-bit to-24 bit wide interface. The three 8/10/12-bit data channels of the interface can be configured 17 different video mats (see Table 2 on page 6). It provides a direct connection to major A/V processors. Register settings configure the interface bus width, mat (8/10/12/16/20/24-bit), and rising or falling edge latching. The appropriate registers must be configured to describe which mat of video is being sent to the SiI9134 transmitter. This inmation travels over the HDMI link in CEA-861D Active Video Inmation (AVI) packets. The transmitter also supports dual-edge clocking using 12 data pins.

Configuration to Support Deep-color

The SiI9134 transmitter provides support Deep Color video data up to the maximum specified link speed of 2.25 Gbps (225 MHz clock rate the Deep Color packetized data). It supports both 30-bit (10 -bits per pixel component) and 36-bit (12-bits per pixel component) video input mats, and converts the data to 8-bit packets encryption and TMDS encoding transferring across the TMDS link.

When the input data width is wider than desired, the device can be programmed to dither or truncate the video data to the desired size. instance, if the input data width is 12 bits per pixel component, but the sink device supports 10 bits, the transmitter can be programmed either to dither or to truncate the 12-bit input data to the desired 10-bit output data. Dither processing is the final block in the video processing path and occurs after all other video processing has been permed.

Common Video Input mats

Table 2 lists the video input mats that the SiI9134 transmitter supports.

Table 2. Video Input mats Example

Data Enable Generator

Color Space	Video mat	Input Channels	Bus Width[1, 2]	HSYNC/ VSYNC[4]	Input Pixel Clock (MHz)								Notes
					480i[5]	VGA/480p	XGA	720p	1080i	SXGA	1080p	UXGA	
RGB	4:4:4	3	36	Separate	27	25/27	—	74.25	74.25	108	148.5	—	—
		3	30	Separate	27	25/27	—	74.25	74.25	108	148.5	—	—
		3	24	Separate	27	25/27	65	74.25	74.25	108	148.5	162	—
		1.5	12	Separate	27	25/27	65	74.25	74.25	—	—	—	3
		1.5	15	Separate	27	25/27	65	74.25	74.25	—	—	—	3
		1.5	18	Separate	27	25/27	65	74.25	74.25	—	—	—	3
YCbCr	4:4:4	3	36	Separate	27	27	—	74.25	74.25	—	148.5	—	—
		3	30	Separate	27	27	—	74.25	74.25	—	148.5	—	—
		3	24	Separate	27	27	—	74.25	74.25	—	148.5	—	—

		1.5	12	Separate	27	27	—	74.25	74.25	—	—	—	3
		1.5	15	Separate	27	25/27	65	74.25	74.25	—	—	—	3
		1.5	18	Separate	27	25/27	65	74.25	74.25	—	—	—	3
	4:2:2		16/20/24	Separate	27	27	—	74.25	74.25	—	148.5	—	—
		2											
				Embedded	27	27	—	74.25	74.25	—	148.5	—	4
		1	8/10/12	BTA-T1004	—	54	—	—	—	—	—	—	4 , 6

Notes:
1. Bus widths of 8, 10, or 12 bits one channel. Bus widths of 16, 20, or 24 bits with 4:2:2 data sequences two data channels.
2. Latching edge is programmable.
3. These mats dual-edge clocking.
4. If embedded syncs are provided, then DE is generated ly from SAV/EAV sequences. Embedded syncs
The transmitter includes logic toconstruct a DE signal from the incoming HSYNC, VSYNC, and clock. Registers are
656 SAV/EAV sequences of FF, 00, 00, XY.

5. 480i must be input at 27 MHz using pixel replication to be transmitted across the HDMI link.
6. BTA-T1004 mat is defined a single-channel (8/10/12-bit) bus with encoded syncs.

Embedded Sync Decoding

The SiI9134 transmitter can create DE, HSYNC, and VSYNC signals from the Start of Active Video (SAV) and End of Active Video (EAV) codes within the 656 video stream. HDCP is not supported in this mode.

programmed to enable the DE signal to define the size of the active display region. This feature is ful when interfacing to MPEG decoders that do not provide a specific DE output signal.

Re-sampling

Re-sampling (up-sampling/decimation) blocks allow conversion of 4:4:4 data to 4:2:2 and of 4:2:2 data to 4:4:4 transmission over the HDMI link.

Color Space Converters (CSC)

Two color space converters (CSCs) (YCbCr to RGB and RGB to YCbCr) are available to interface to the many video mats supplied by A/V processors and to provide full DVI backward compatibility. The CSC can be adjusted to perm standard-definition conversions (ITU.601) or high-definition conversions (ITU.709) by setting the appropriate registers.

RGB to YCbCr The RGB→YCbCr color space converter can convert from video data RGB to standard definition or to high definition YCbCr mats. The HDMI AVI packet defines the color space of the incoming video.

Table 3. Color Space versus Video mat

Video mat	Conversion	mulas
		CE Mode 16-235 RGB
640 x 480	ITU-R BT.601	Y = 0.299R′ + 0.587G′ + 0.114B′ Cb = –0.172R′ – 0.339G′ + 0.511B′ + 128 Cr = 0.511R′ – 0.428G′ – 0.083B′ + 128
480i	ITU-R BT.601	
576i	ITU-R BT.601	
480p	ITU-R BT.601	
576p	ITU-R BT.601	
240p	ITU-R BT.601	
288p	ITU-R BT.601	
720p	ITU-R BT.709	Y = 0.213R′ + 0.715G′ + 0.072B′ Cb = –0.117R′ – 0.394G′ + 0.511B′ + 128 Cr = 0.511R′ – 0.464G′ – 0.047B′ + 128
1080i	ITU-R BT.709	
1080p	ITU-R BT.709	

YCbCr to RGB The YCbCr→RGB color space converter allows MPEG decoders to interface with RGB- inputs. The CSC can convert from YCbCr in standard-definition (ITU.601) or high-definition (ITU.709) to RGB. Refer to the detailed mulas in Table 4. Note the difference between RGB range CE modes and PC modes.

Table 4. YCbCr-to-RGB Color Space Conversion mula

mat change	Conversion	YCbCr Input Color Range 2, 3
YCbCr 16-235 Input[2, 3] to RGB 16-235 Output[2, 3]	**601[1]**	R′ = Y + 1.371(Cr – 128) G′ = Y– 0.698(Cr – 128) – 0.336(Cb – 128) B′ = Y + 1.732(Cb – 128)
Notes:	**709[1]**	R′ = Y + 1.540(Cr – 128) B′ = Y + 1.816(Cb – 128)
YCbCr 16-235 Input[2, 3] to RGB 0-255 Output[2, 3]	**601**	R′ = 1.164((Y-16) + 1.371(Cr – 128)) G′ = 1.164((Y-16) – 0.698(Cr – 128) – 0.336(Cb – 128)) B′ = 1.164((Y-16) + 1.732(Cb – 128))
	709	R′ = 1.164((Y-16) + 1.540(Cr – 128)) G′ = 1.164((Y-16) – 0.459(Cr – 128) – 0.183(Cb – 128)) B′ = 1.164((Y-16) + 1.816(Cb – 128))

1. No clipping can be
2. 10-bit deepby 4.
3. 12-bit deepby 16.done.color,alloccurrencesofthevalues16,128,235,and255shouldbemultiplied color,alloccurrencesofthevalues16,128,235,and255shouldbemultiplied

14-to-8/10/12-Dither

The 14-to-8/10/12-dither block dithers ly processed, 14-bit data to 8, 10, or 12 bits output on the HDMI link. It can be bypassed to output 10/12-bit modes when supplied by the A/V processor or converted in the decimator and CSC.

Color Range Scaling

The SiI9134 transmitter can scale the input color range from limited-range into full-range or vice versa through the range expansion and compression blocks. When enabled by itself, the range expansion block expands 16–235 (64–943 to 256–3775 30/36-bit color depth) limited-range data into 0–255 (0–1023 to 0–4095 30/36-bit color depth) full-range data each video channel. When range expansion and the YCbCr to RGB converter are both enabled, the input conversion range Cb and Cr channels is 16–240 (64–963 to 256–3855 30/36-bit color depth). Similarly, the range compression block compresses 0–255/0–1023/0–4095 full-range data into 16–235/64–943/256–3775 limited-range data each video channel when enabled by itself. When enabled with the RGB to YCbCr converter, this block compresses to 16–240/64–963/256–3855 the Cb and Cr channels. The color range scaling is linear.

Clipping

The clipping block, when enabled, clips the values of the output video to 16–235 RGB video or the Y channel, and to 16–240 the Cb and Cr channels.

HDCP Encryption Engine/XOR Mask

The HDCP encryption engine contains the logic necessary to encrypt the incoming audio and video data and includes support HDCP authentication and repeater checks. The system microcontroller or microprocessor controls the encryption process by using a set sequence of register reads and writes. An algorithm s HDCP keys and a Key Selector Value (KSV) stored in the on-board ROM to calculate a number that is then applied to an XOR mask. This process encrypts the audio and video data on a pixel-by-pixel basis during each clock cycle.

3D Video mats

TMDS Digital Core

The TMDS digital core perms 8-to- 10-bit TMDS encoding on the data received from the HDCP XOR mask. This data is sent to three TMDS differential data lines, along with a TMDS differential clock line. A resistor tied to the EXT_SWING pin controls the TMDS swing amplitude.

The SiI9134 transmitter supports the 3D video modes described in the HDMI Specification. All modes support RGB

prevented as it may resultin visible artifacts.

4:4:4, YCbCr 4:4:4, and YCbCr 4:2:2 color mats and 8-, 10-, and 12-bit data-width per color component. External separate HSYNC, VSYNC, and DE signals can be supplied, or these signals can be supplied as embedded EAV/SAV Furthermore, a frame rate of 24 Hz also means that a framerateof 23.98 Hz is supported and a frame rate of 60 Hz also means a frame rate of 59.94 Hz is supported. Input pixel clock changes accordingly.

sequences in the video stream. Table 5 shows the maximum possible resolution with a given frame rate; example, Side- by-Side (Half) mode is defined 1080p60, which implies that 720p60 and 480p60 are also supported.

When using Side-by-Side mat, the of 4:2:2 to 4:4:4: up - sampling and 4:4:4 to 4:2:2 down-sampling should be

Video processing should be bypassed in the case of *L + depth* mat.
Transmission of the HDMI Vendor Specific InfoFrame, which carries 3D inmation to the receiver, is supported by the SiI9134 device.

Table 5. Supported 3D Video mats

3D mat	Extended Definition	Resolution	Frame Rate (Hz)	Input Pixel Clock (MHz)
	—	1080p	24	

Frame Packing		720p	50/60	148.5
Frame Packing	interlaced	1080i	50/60	148.5
L + depth	—	1080p	24	148.5
L + depth	—	720p	50/60	148.5
Side-by-Side	full	1080p	24	148.5
Side-by-Side	full	720p	50/60	148.5
Side-by-Side	half	1080p	50/60	148.5
Side-by-Side	half	1080i	50/60	74.25
Top-and-Bottom	—	1080p	24	74.25
Top-and-Bottom	—	720p	50/60	74.25

3D Video Limitations

Frame Packing mat: Frame packing mat requires Vact_space, which must have constant video data. Dithering should be disabled when transmitting the frame packing mat.

In the case of 1080p 24 Hz mat, this video mat has a total of 2295 lines. However, the VRES counter (0x72. 0x3C,0x3D) of the SiI9134 device has 11 bits, which means a maximum of 2047 lines. In this case, the VRES counter overflows and shows a value of 0.

The DE generator is supported except the 1080p 24 Hz mat. The DE_LIN register (0x72.0x38,0x39) has 11 bits (maximum 2047), but the 1080p 24 Hz mat requires 2205 lines.

Side-by-Side mat: L frame and R frame are concatenated without a border. Since 4:4:4 to 4:2:2 down-sampling and 4:2:2 dithering and upsampling to 4:4:4 has a decimation filter which looks at adjacent pixels, those features should not be d to avoid visible artifacts.

L + Depth mat: Any video processing should be bypassed.

Top-and-Bottom mat: There are no limitations.

Audio Data Capture Logic

The SiI9134 transmitter accepts digital audio over an S/PDIF interface, four I^2S inputs, or eight one-bit audio inputs.

S/PDIF

The S/PDIF stream can carry 2-channel uncompressed PCM data (IEC 60958) or a compressed bit stream multi-
channel (IEC 61937) mats. The audio data capture logic ms the audio data into packets described in the HDMI Specification. The S/PDIF input supports audio sampling (Fs) rates from 32 to 192 kHz. A separate master clock input (MCLK), coherent with the S/PDIF input, is required time-stamping purposes. *Coherent* means that the MCLK and
S/PDIF have been created from the same clock source. This step usually s the original MCLK to strobe out the

S/PDIF from the sourcing chip. There is no setup or hold timing requirement on an input with respect to MCLK.

I^2S

Four I^2S inputs allow transmission of DVD-Audio or decoded Dolby Digital to A/V receivers and high-end displays. The interface supports up to 8-channels at 192 kHz. The I^2S pins must also be coherent with MCLK.

Register control allows the audio data to be downsampled by one-half or one-fourth. This control allows the transmitter

to share the audio bus with a high-sample-rate audio DAC, while downsampling audio an attached display that
128 4.096 MHz 5.645 MHz6.144 MHz11.290 MHz 12.288 MHz 22.579 MHz 24.576 MHz
supports lower rates. Conversions from 192 to 48 kHz, from 176.4 to 44.1 kHz, from 96 to 48 kHz, and from 88.2 to 44.1 kHz are supported. Audio data can be downsampled on 2-channel audio.

The appropriate registers must be configured to describe the audio mat provided to the SiI9134 transmitter. This inmation is passed over the HDMI link in the CEA-861D Audio Info (AI) packets.

Table 5 shows the MCLK frequencies that support the seven audio sample rates.

Table 5. Supported MCLK Frequencies

Multiple of Fs	I^2S and S/PDIF Supported MCLK Rates						
	Audio Sample Rate, Fs						
	32 kHz	44.1 kHz	48 kHz	88.2 kHz	96 kHz	176.4 kHz	192 kHz
192	6.144 MHz	8. 467 MHz	9.216 MHz	16.934 MHz	18.432 MHz	33.868 MHz	36.864 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.864 MHz	36.864 MHz	67.737 MHz	73.728 MHz
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz	—	—
768	24.576 MHz	33.869 MHz	36.864 MHz	67.738 MHz	73.728 MHz	—	—
1024	32.768 MHz	45.158 MHz	49.152 MHz	—	—	—	—
1152	36.864 MHz	50.803 MHz	55.296 MHz	—	—	—	—

One-Bit Audio Input (DSD/SACD)

Direct Stream Digital (DSD) is an audio data mat defined Super Audio CD (SACD) applications. A clock and four data inputs, each left and right channels, provide support up to 8 channels. One-bit audio sources provide MCLK and support 64 · Fs, with Fs being either 44.1 kHz or 88.2 kHz.

The one-bit audio inputs are sampled on the positive edge of the DSD clock, assembled into 56-bit packets, and mapped to the appropriate FIFO. The Audio InfoFrame, instead of the Channel Status bits, carries the sampling inmation one-bit audio.

High-Bit Rate Audio on HDMI

The new high-bit-rate compression standards, such as MLP and DTS-HD, transmit data at bit rates as high as 18 or 24 Mbps. Beca these bit rates are so high, DVD decoders and HDMI transmitters (as source devices), and DSP and HDMI receivers (as sink devices) must carry the data using four I^{2}S lines rather than using a single very-high-speed S/PDIF interface or I^{2}S bus (see Figure 5 on the next page).

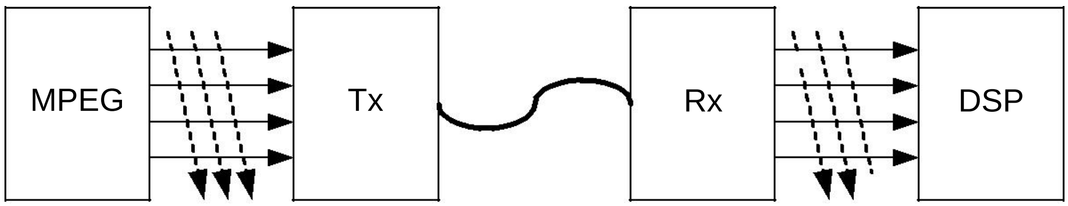


Figure 5. HighSpeed Data Transmission

The high-bit-rate audio stream is originally encoded as a single stream. To send the stream over four I^{2}S lines, the DVD decoder splits it into four streams. Figure 6 shows the high-bit-rate stream bee it has been split into four I^{2}S lines. Figure 7 shows the same audio stream after being split. Each sample requires 16 cycles of the I^{2}S clock (SCK).

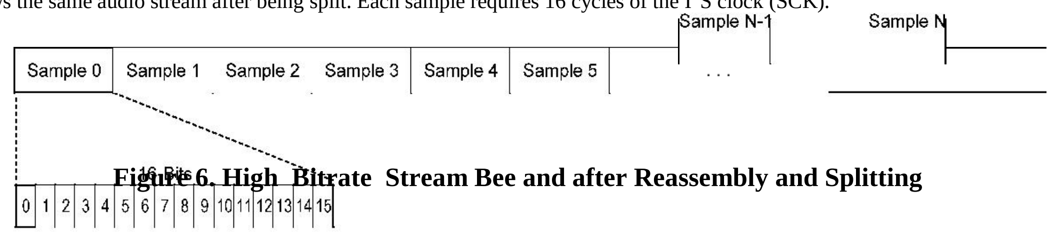


Figure 6. High Bitrate Stream Bee and after Reassembly and Splitting

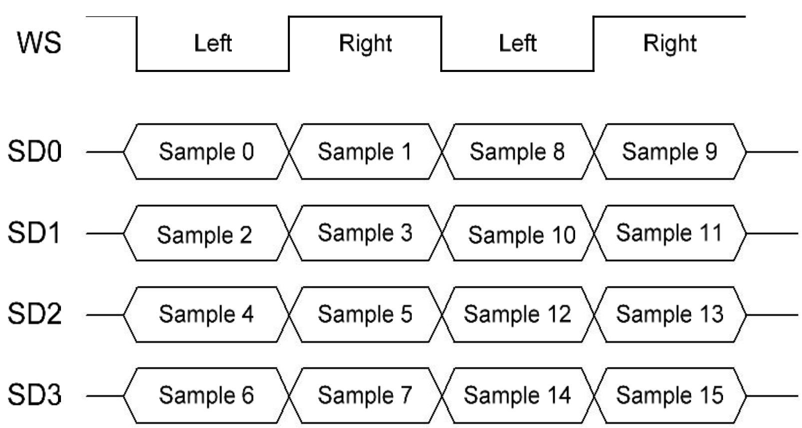


Figure 7. High Bit Rate Stream After Splitting

, Inc.

Audio Downsampler Limitations

The SiI9134 transmitter has an audio downsampler function that can down sample the incoming two-channel audio data and output the result over the HDMI link. The audio data can be downsampled by one-half or one-fourth with register control. Conversions from 192 to 48 kHz, 176.4 to 44.1 kHz, 96 to 48 kHz, and 88.2 to 44.1 kHz are supported. Some limitations in the audio sample word length when using this feature may need special consideration in a real application.

When enabling the audio downsampler, the Channel Status registers the audio sample word lengths sent over the HDMI link always indicate the maximum possible length. example, if the input S/PDIF stream was in 20-bit mode with 16 bits valid, after enabling the downsampler the Channel Status indicates 20-bit mode with 20 bits valid.

Audio sample word length is carried in bits 33 through 35 of the Channel Status register over the HDMI link, as shown in Table 6. These bits are always set to 0b101 when enabling the down-sampler feature. Audio data is not affected beca 0s are placed into the LSBs of the data, and the wider word length is sent across the HDMI link.

Table 6. Channel Status Bits d Word Length

202, 4

Bit				Sample word length, bits	Note
Audio sample word length			Max. word length[1]		
35	34	33	32		
0	0	0	0	Not indicated	—
0	0	1	0	16	2
0	1	0	0	18	2
1	0	0	0	19	2
1	1	0	0	17	2
0	0	0	1	Not indicated	3
0	0	1	1	20	3
0	1	0	1	22	3
1	0	0	1	23	3
1	0	1	1	24	3, 4
1	1	0	1	21	3

length (MAXLEN) is 20its if MAXLEN = 0, 24 bits if MAXLEN = 1.

Notes:

2. Maximum audio sample word length is 20.
3. Maximum audio sample word length is 24.
4. Bits [35:33] are always 0b101 when the down-sampler is enabled

HDCP Key ROM

The SiI9134 transmitter comes pre-programmed with a set of production HDCP keys stored in an ROM. System manufacturers do not need to purchase key sets from the Digital-Content Protection LLC.   handles all purchasing, programming, and security the HDCP keys. The pre- programmed HDCP keys provide the highest level of security beca there is no way to read the keys once the devices are programmed. Customers must sign the HDCP license agreement (www.digital-cp.com) or be under a specific NDA with   bee receiving samples of the transmitter.

Interrupt Out

The INT pin provides an interrupt signal to the system microcontroller when any of the following occur:

- Monitor Detect (HPD input) changes
- VSYNC (ful synchronizing a microcontroller to the vertical timing interval)

0xFF on each page in the I2C protocol. Beca thereare more than 255 bytes of registers in the transmitter, it is

- Error in the audio mat
- DDC FIFO status change

The Register/Configuration Logicblock incorporates all the registers required configuring and managing the SiI9134

- HDCP authentication error

Control and Configuration

All functions of the transmitter are monitored and controlled with I²C registers. Register addresses range from 0x00 to

transmitter. These registers are d to perm HDCP authentication, audio/video mat processing, CEA-861D info-packet

matting, and power-down control.

accessed using one of two I²C device addresses, which can be altered with the CI2CA pin. The level on the CI2CA pin is
not latched ly and theree must not be changed during any active I²C operations.

Table 7. Control of I²C Address with CI2CA Pin

Device Address	CI2CA = HIGH	CI2CA = LOW
First Device Address	0x76	0x72
Second Device Address	0x7E	0x7A

Registers/Configuration Logic

Microcontroller Slave I²C Interface

The controller slave I²C interface on the transmitter (pins CSCL and CSDA) is capable of running up to 400 kHz. This bus is d to configure the transmitter by reading and writing to various registers and is 5 V tolerant. Figure 8 shows the host I²C ports.

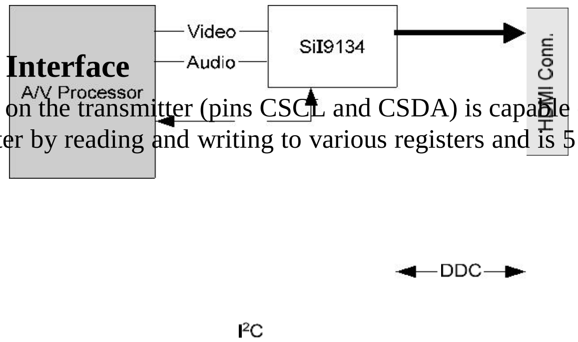


Figure 8. Simplified I²C Ports

DDC Master I²C Interface

The transmitter includes two I²C ports: a master port to connect directly to the HDMI cable and a port to connect to the system microcontroller or processor. Both are shown in Figure 8. DDC reads and writes are executed by reading and writing registers in the SiI9134 transmitter.

The master DDC block supports I²C transactions specified by VESA Enhanced Display Data Channel Standard (Section 3.1.2), and it supports an I²C write transaction needed HDCP. The Master DDC block complies with the Standard Mode timing of the I²C specification (100 kHz) and supports slave clock stretching as required by E-DDC. Section 8.4.1 of the HDMI Specification limits the speed allowed on the DDC bus to 100 kHz.

Figure 8 provides inmation about the transactions supported by the master I²C interface.

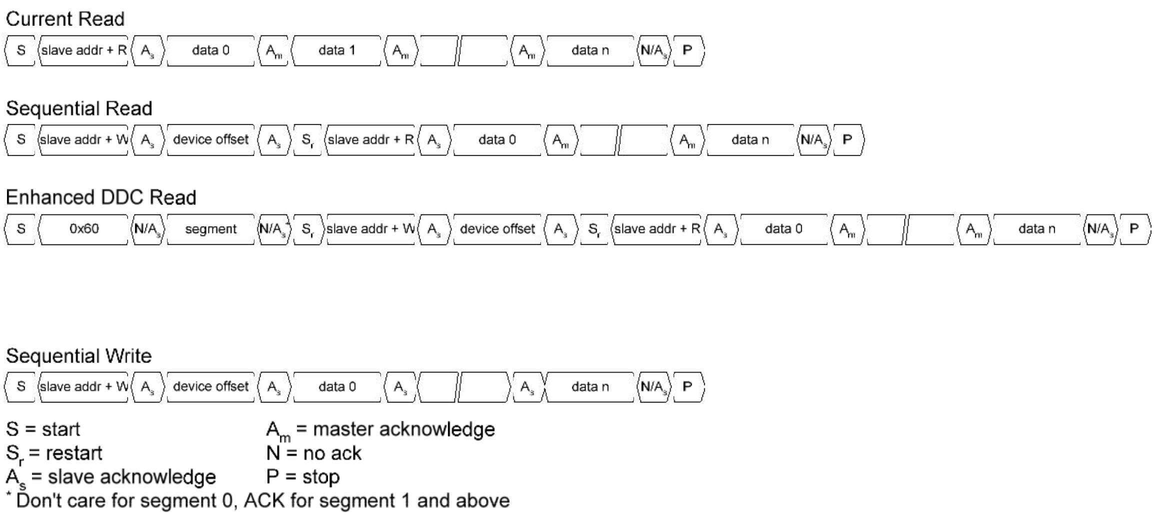


Figure 8. Master I²C Supported Transactions

Electrical Specifications

The following tables provide electrical specifications the SiI9134 transmitter.

Absolute Maximum Conditions

Table 9. Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O pin supply voltage 3.3 V	–0.3	—	4.0	V	3
PVCC1	TMDS PLL supply voltage	–0.3	—	2.5	V	—
PVCC2	TMDS PLL supply voltage	–0.3	—	2.5	V	—
AVCC18	TMDS analog supply voltage	–0.3	—	2.5	V	—
AVCC33	TMDS analog supply voltage 3.3 V	–0.3	—	4.0	V	3
CVCC18	Digital Core supply voltage	–0.3	—	2.5	V	3
DDCPWR5V	DDC I^2C I/O reference voltage	–0.3	—	5.5	V	—
V_I	Input voltage	–0.3	—	5.5	V	—
V_O	Output voltage	–0.3	—	IOVCC33 + 0.3	V	—
T_A	Ambient temperature (with power applied)	–25	—	105	°C	—
T_J	Junction temperature (with power applied)	—	—	125	°C	—
T_{STG}	Storage temperature	–65	—	150	°C	—

Notes:

1. Permanent device damage can occur if absolute maximum conditions are exceeded.

IOVCC33I/O pin supply voltage 3.3 V 2.973.33.63V1

2. Restrict functional operation to the conditions described in the Normal Operating Conditions section below.
3. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.

4. Refer to the SiI9134 HDMI Deep Color Transmitter Qualification Report inmation on ESD permance.

Normal Operating Conditions

Table 10. Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
Θ_{jc}	Junction thermal resistance(Theta JC)	—	—	17.5	°C/W	—
PVCC1	TMDS PLL supply voltage	1.62	1.8	1.98	V	2
PVCC2	TMDS PLL supply voltage	1.62	1.8	1.98	V	2
AVCC18	TMDS analog supply voltage 1.8 V	1.62	1.8	1.98	V	—
AVCC33	TMDS analog supply voltage 3.3 V	2.97	3.3	3.63	V	5
CVCC18	Digital core supply voltage	1.62	1.8	1.98	V	—
DDCPWR5V	DDC I^2C I/O reference voltage	4.50	5.0	5.50	V	4

DIFF3318	(VCC33–VCC18)	–1.0	—	2.0	V	3, 4
Θ_{ja}	Ambient thermal resistance (Theta JA)	—	—	55	°C/W	6

Notes:

1. Power to IOVCC33 and AVCC33 pins should be controlled from one source.
2. Power to PVCC1 and PVCC2 pins should be regulated.
3. Applies to all 3.3 V and 1.8 V power supplies. Power supply sequencing must guarantee that power pins stay within these limits of each other. See Figure 19.
4. No power sequencing is required on other supply voltages.
5. The HDMI Specification requires termination voltage to be controlled to 3.3 V ±5%. The SiI9134 HDMI Deep Color Transmitter tolerates a wider range of ±300 mV.
6. Airflow at 0 m/s.
7. See page 42 schematics showing decoupling and power supply regulation.

DC Specifications

Digital I/O Specifications

Under normal operating conditions, unless otherwise specified.

Table 11. Digital I/O Specifications

Symbol	Parameter	Pin Type[3]	Conditions	Min	Typ	Max	Units	Notes
V_{IH}	HIGH-level input voltage	LVTTL	—	2.0	—	—	V	1
V_{IL}	LOW-level input voltage	LVTTL	—	—	—	0.825	V	1
V_{OH}	HIGH-level output voltage	LVTTL	—	2.4	—	—	V	1
V_{OL}	LOW-level output voltage	LVTTL	—	—	—	0.4	V	1
I_{OH}	Output minimum source DC current	LVTTL	VOUT = 2.4 V	6.2	12.4	19	mA	2, 7, 8
I_{OL}	Output minimum sink current	LVTTL	VOUT = 0.4 V	4.5	6.6	7.6	mA	2, 7, 8
V_{TH+I2L}	LOW to HIGH threshold, local I^2C bus	Schmitt	—	1.9	—	—	V	1, 4
V_{TH-I2L}	HIGH to LOW threshold, local I^2C bus	Schmitt	—	—	—	0.7	V	1, 4
V_{TH+I2D}	LOW to HIGH threshold, DDC I^2C Bus	Schmitt	—	2.3	—	—	V	1
V_{TH-I2D}	HIGH to LOW threshold, DDC I^2C bus	Schmitt	—	—	—	1.5	V	1
V_{CINL}	Input clamp voltage	All	ICL = –18 mA	—	—	GND – 0.8	V	1, 5
V_{CIPL}	Input clamp voltage	All	ICL = 18 mA	—	—	V_{CC} + 0.8	V	1, 5
I_{IL}	Input leakage Current	All	High impedance	–10	—	10	µA	1, 6

Notes:

1. Guaranteed by characterization.
2. Guaranteed by design.
3. LVTTL inputs except CI2CA have no pull-up or pull-down resistors. All und input pins should be tied LOW.
4. When no VCC is applied to the chip, the CSCL and CSDA pins can continue to draw a small current and prevent the I^2C masterfrom communicating with other deviceson the I^2C bus. Theree, do not remove VCC from the transmitter unless the attached I^2C bus is completely idle.
5. Guaranteed by design. Voltage undershoot or overshoot cannot exceed absolute maximum conditions a pulse of greater than 3 ns or more than one third of the clock cycle, whichever is less. Exceeding the Clamp Current I_{CL} listed can result in permanent damage to the chip.
6. Limits defined by HDMI Specification.
7. Output drive specification applies to INT, DSCL, DSDA, and CSDA pins.
8. Minimum output drive specified at ambient = 70 °C and IOVCC = 3.0 V. Typical drive specified at ambient = 25 °C and IOVCC = 3.3 V. Maximum output drive specified at ambient = 0 °C and IOVCC = 3.6 V.

TMDS I/O Specifications

Table 12. TMDS DC Specifications— Source Termination On

source termination and leakage bias (STERM and LVBIAS in TMDS Control Register #1 bits 0 and 2 respectively) are turned on in the chip. External source termination components must be removed. LVBIAS should be set to 1 after reset.

Symbol	Parameter	Pin Type	Conditions	Min	Typ	Max	Units	Notes
V_{DOH}	Differential HIGH level output voltage	TMDS	—	AVCC33 – 150	AVCC33 – 130	AVCC33 –110	mV	1
V_{DOL}	Differential LOW level output voltage	TMDS	—	AVCC33 – 600	AVCC33	AVCC33 – 400	mV	1
V_{OD}	Differential Outputs single ended swing amplitude	TMDS	REXT_SWING = 698 Ω 1%	400	450	600	mV	1, 3
V_{ODD}	Differential Outputs differential swing amplitude	TMDS	REXT SWING = 698 Ω 1%	800	900	1200	mV	1, 3
I_{DOS}	Differential output short circuit	TMDS	VOUT = 0 V	—	—	5	μA	2

–

voltage – 600– 500– 400

Notes: current

1. Guaranteed by characterization.
2. Guaranteed by design.
3. Minimum output drive specified at ambient = 70 °C and IOVCC = 3.0 V. Typical drive specified at ambient = 25 °C

Pin

and IOVCC = 3.3 V. Maximum output drive specified at ambient = 0 °C and IOVCC = 3.6 V.

Table 13. TMDS DC Specifications— Source Termination Off

source termination and leakage bias (STERM and LVBIAS in TMDS Control Register #1 bits 0 and 2 respectively) are turned off in the chip. External source termination components are required and the chip must be set accordingly upon power up.

Symbol	Parameter	Type	Conditions	Min	Typ	Max	Units	Notes
V_{DOH}	Differential HIGH level output voltage	TMDS	—	AVCC33 – 10	AVCC33	AVCC33 + 10	mV	1
V_{DOL}	Differential LOW level output	TMDS	—	AVCC33	AVCC33	AVCC33	mV	1

3. Minimum output drive specifiedat ambient = 70 °C and IOVCC = 3.0 V. Typical drive specified at ambient = 25 °C

V_{OD}	Differential Outputs single ended swing amplitude	TMDS	= 850 Ω 1%	400	500	600	mV	1, 3
V_{ODD}	Differential Outputs differential swing amplitude	TMDS	REXT SWING = 850 Ω 1%	800	1000	1200	mV	1, 3
I_{DOS}	Differential output short circuit current	TMDS	VOUT = 0 V	—	—	5	μA	2

Notes:

1. Guaranteed by characterization.
2. Guaranteed by design.

and IOVCC = 3.3 V. Maximum output drive specified at ambient = 0 °C and IOVCC = 3.6 V.

DC Power Supply Pin Specifications

Table 14. Power-Down Modes

Symbol	Parameter	Mode	Frequency	Maximum[3] 1.8 V	Maximum[3] 3.3 V	Units	Notes
I_{PDQ3}	Complete power-down current	A	No input	1	5	mA	1, 2
I_{PDQ}	Quiet power-down current	B	clock	8	5	mA	1
I_{PD}	Power-down current @ 225 MHz	C	Clocking	30	5	mA	1

Notes:

1. Power is not related to input pixel clock (IDCK) frequency.
2. Most registers are accessible with no input pixel clock. Exceptions include Packet Control and ROM test. Stopping the input pixel clock (IDCK) is equivalent to setting PDIDCK# = 0 to minimize power.
3. Maximum power limits measured with all supplies at maximum normal operating conditions, minimum normal operating ambient temperature, and a single pixel checkerboard pattern.

Table 15. Total Power Mode

3. Typical valuesare specified full functional mode,not power-down modes.

Symbol	Parameter	Mode	Frequency	Typical[1] 1.8 V	Typical[1] 3.3 V	Maximum[2] 1.8 V	Maximum[2] 3.3 V	Units	Notes
I_{STBY}	Standby current	D	27 MHz	—	—	20	5	mA	3
			74.25 MHz	—	—	44	5	mA	
			150 MHz	—	—	77	5	mA	
			225 MHz	—	—	94	5	mA	
I_{CCT}	current	E	27 MHz	87	5	102	5	mA	—
			150 MHz	221	5	230	5	mA	—
			225 MHz	251	5	276	5	mA	—

Notes:

1. Typical power specifications measured with supplies at typical normal operating conditions and an SMPTE133 video pattern.
2. Maximum power limits measured with all supplies at maximum normal operating conditions, minimum normal operating ambient temperature, and a single pixel checkerboard pattern.

Table 16. Power Operating Modes

clock trees

	Mode	Bit States PDTOT#	PD#	PDIDCK#	PDOSC	Input Switching	Description	Comment
A	Complete Power Down	1	0	0	1	No	Minimum power.	Lowest power mode.
B	Quiet Power Down	1	0	0	0	No	Master DDC available.	Access DDC bus
C	Power Down	1	0	0	0	Yes	Upstream chip still active.	while minimizing transmit power.
D	Standby	1	0	1	0	Yes	active.	Power-reset mode.

E	Full Power	1	1	1	0	Yes	Full-function.	Functional mode.

AC Specifications

TMDS AC Timing Specifications

Under normal operating conditions, unless otherwise specified.

Table 17. TMDS AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
T_{DDF}	VSYNC and HSYNC Delay from DE falling edge	—	1	—	—	T_{CIP}	Figure 12
T_{DDR}	VSYNC and HSYNC Delay to DE rising edge	—	1	—	—	T_{CIP}	Figure 12
T_{HDE}	DE HIGH Time	—	—	—	8191	T_{CIP}	Figure 13
T_{LDE}	DE LOW Time [3]		138	—	—	T_{CIP}	Figure 13
S_{LHT}	Differential Swing LOW-to-HIGH Transition Time [4]	R_{EXT_SWING} = 698 Ω Source Termination On	75	—	144	ps	Figure 20
S_{HLT}	Differential Swing HIGH-to-LOW Transition Time [4]		75	—	144	ps	Figure 20

Notes:

1. Guaranteed by design.
2. Guaranteed by characterization.
3. T_{LDE} (DE LOW Time) minimum is defined HDMI mode carrying 480p video with 192 kHz audio, which requires at least 138 pixel clocks of blanking to carry the audio packets. If HDCP is running, minimum DE LOW time is 58 clocks (according to the HDCP Specification). If both HDCP and audio are not running, minimum DE LOW time is 12 clocks TMDS. moredetails, refer to Figure 13 on page 22. Minimum vertical blanking time is 3 horizontal line times.
4. Limits are defined by the HDMI Specification.

Audio AC Timing Specifications

Table 18. S/PDIF Input Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
F_{S_SPDIF}	Sample Rate	2 Channel	32	—	192	kHz	—
T_{SPCYC}	SPDIF Cycle Time [1]	C_L = 10 pF	—	—	1.0	UI	Figure 15
T_{SPDUTY}	SPDIF Duty Cycle [1]	C_L = 10 pF	90%	—	110%	UI	Figure 15
$T_{MCLKCYC}$	MCLK Cycle Time [3]	C_L = 10 pF	13.3	—	—	ns	Figure 15
F_{MCLK}	MCLK Frequency [3]	C_L = 10 pF	—	—	75	MHz	Figure 15
$T_{MCLKDUTY}$	MCLK Duty Cycle [3]	C_L = 10 pF	40%	—	60%	$T_{MCLKCYC}$	Figure 15
T_{AUDDLY}	Audio Pipeline Delay [4]	—	—	30	70	µs	—

Table 19. I²S Input Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
F_{S_I2S}	Sample Rate	—	32	—	192	kHz	—
T_{SCKCYC}	I²S Cycle Time [1]	C_L = 10 pF	—	—	1.0	UI	Figure 16
$T_{SCKDUTY}$	I²S Duty Cycle [1]	C_L = 10 pF	90%	—	110%	UI	Figure 16
T_{I2SSU}	I²S Setup Time [2]	C_L = 10 pF	15	—	—	ns	Figure 16
T_{I2SHD}	I²S Hold Time [2]	C_L = 10 pF	0	—	—	ns	Figure 16

Table 20. DSD Input Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure
F_{S_DSD}	Sample Rate	—	—	44.1	88.2	kHz	—
T_{DCKCYC}	DSD Cycle Time[1]	C_L = 10 pF	—	—	1.0	UI	Figure 17
$T_{DCKDUTY}$	DSD Duty Cycle[1]	C_L = 10 pF	90%	—	110%	UI	Figure 17
T_{DSDSU}	DSD Setup Time	C_L = 10 pF	20	—	—	ns	Figure 17
T_{DSDHD}	DSD Hold Time	C_L = 10 pF	20	—	—	ns	Figure 17

Notes:
1. Proportional to unit time (UI) according to sample rate. Refer to the I^2S or S/PDIF Specifications.
2. Setup and hold minima are based on 13.388 MHz sampling, which is adapted from Fig. 3 of Philips I^2S Specification.
3. A separate master clock input (MCLK) is required; refer to the S/PDIF section on page 9.
4. Audio pipeline delay is measured from the transmitter input pins to TMDS output. The video path delay is insignificant.

Single-edge

T_{HIDF} 0.8——ns Figure 10

Video AC Timing Specifications

Under normal operating conditions, unless otherwise specified.

Table 21. Video Input AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
T_{CIP}	IDCK period, one pixel per clock	—	6.1	—	40	ns	Figure 9	1
F_{CIP}	IDCK frequency, one pixel per clock	—	25	—	165	MHz	Figure 9	2
T_{CIP12}	IDCK period, dual-edge clock	—	12.3	—	40	ns	Figure 11	2
F_{CIP12}	IDCK frequency, dual-edge clock	—	25	—	82.5	MHz	Figure 11	2
T_{DUTY}	IDCK duty cycle	—	40%	—	60%	T_{CIP}	Figure 9	—
T_{IJIT}	Worst case IDCK clock jitter	—	—	—	1.0	ns	Figure 9	3, 4
T_{SIDF}	Setup time to IDCK falling edge (EDGE = 0)	clocking mode	1.0	—	—	ns	Figure 10	5
	Hold time to IDCK falling edge (EDGE = 0)							
T_{SIDR}	Setup time to IDCK rising edge (EDGE = 1)		1.0	—	—	ns	Figure 10	
T_{HIDR}	Hold time to IDCK rising edge (EDGE = 1)		0.5	—	—	ns	Figure 10	
T_{SIDD}	Setup time to IDCK rising or falling edge	12-bit dual-edge clocking mode	1.0	—	—	ns	Figure 11	6
T_{HIDD}	Hold time to IDCK rising or falling edge		1.0	—	—	ns	Figure 11	

2. T_{CIP12} and F_{CIP12} apply in dual-edgemode. T_{CIP12} is not a controlling specification.

Notes:
1. T_{CIP} and F_{CIP} apply in single-edge clocking modes. T_{CIP} is the inverse of F_{CIP} and is not a controlling specification.

3. Input clock jitter is estimated by triggering a digital scope at the rising edge of input clock and measuring the peak-to-peak time spread of the rising edge of the input clock one microsecond after the trigger.
4. Actual jitter tolerance can be higher depending on the frequency of the jitter.
5. Setup and hold time specifications apply to Data, DE, VSYNC, and HSYNC input pins, relative to IDCK input clock.
6. Setup and hold limits are not affected by EDGE bit setting 12/15/18-bit, dual-edge clocking mode.

Control Timing Specifications

Under normal operating conditions, unless otherwise specified.

Table 22. Control Signal Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Note
TRESET	RESET# signal LOW time required reset	—	50	—		µs	Figure 14	1, 5
TI2CDVD	SDA Data Valid Delay from SCL falling edge on READ command	C_L = 400pF	—	—	700	ns	Figure 21	2
THDDAT	I^2C data hold time	0–400 kHz	7.0	—	—	ns	—	3
THDSTA	I^2C Hold time (repeated) START condition	0–400 kHz	–7.0	—	—	ns	—	—
TINT	Response time INT output pin from change in input condition (HPD, Receiver Sense, VSYNC change, etc.).	RESET# = HIGH	–	—	100	µs	Figure 22[2]	—
FSCL	Frequency on master DDC SCL signal	—	40	70	100	kHz	—	—

Notes:

1. Reset on RESET# pin can be LOW as the supply becomes stable, or pulled LOW at least TRESET.
2. All standard-mode (100 kHz) I^2C timing requirements are guaranteed by design. These timings apply to the slave I^2C port (pins CSDA and CSCL) and to the master I^2C port (pins DSDA and DSCL).
3. This minimum hold time is required by CSCL and CSDA pins as an I^2C slave. The device does not include the 300 ns delay required by the I^2C Specification (Version 2.1, Table 5, note 2).
4. The master DDC block provides an SCL signal the E-DDC bus. The HDMI Specification limits this to I C Standard Mode or 100 kHz. of the Master DDC block does not require an active IDCK.
5. Not a Schmitt trigger.

Timing Diagrams

Input Timing Diagrams

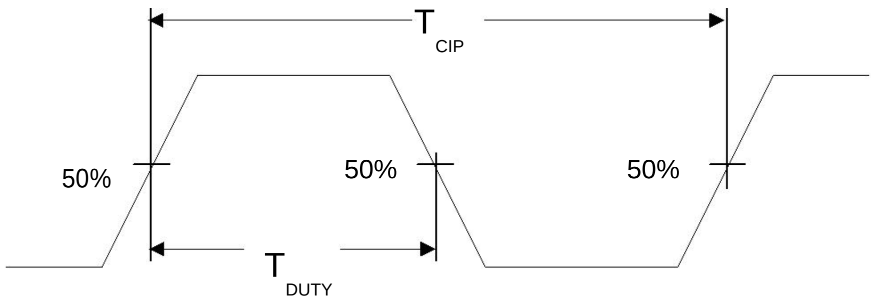


Figure 9. IDCK Clock Cycle/HIGH/LOW Times

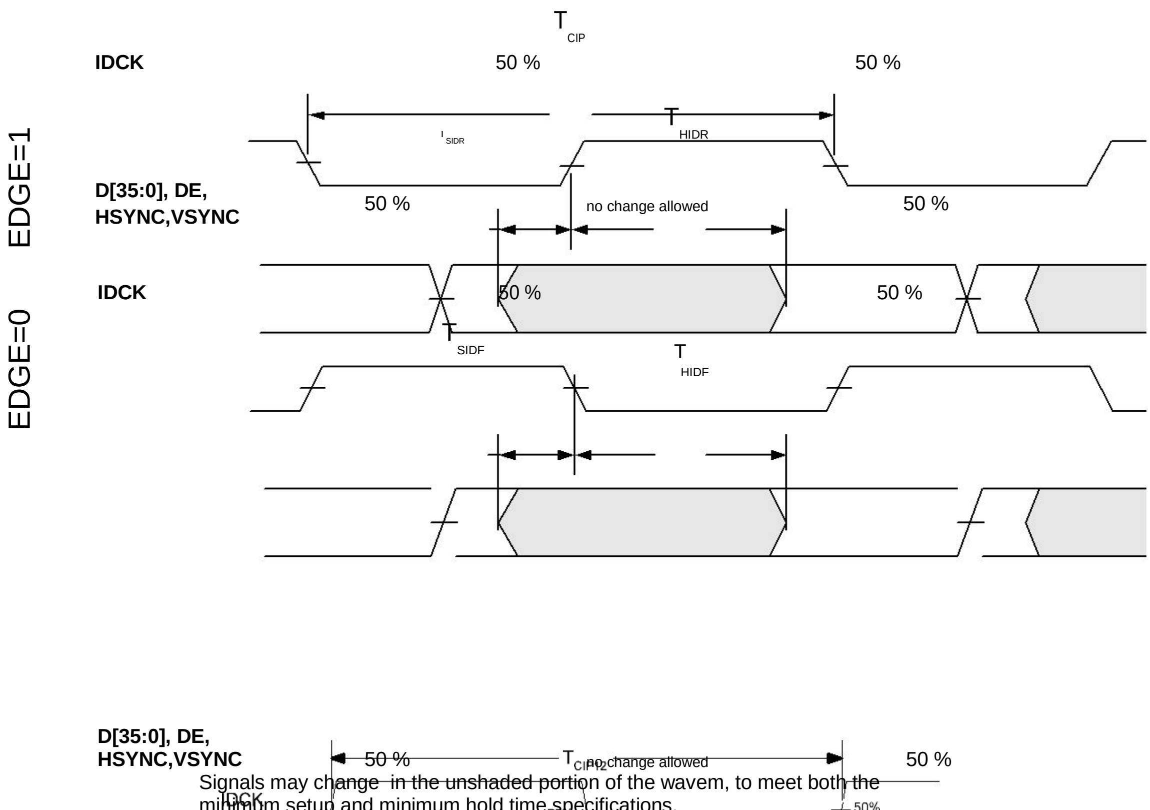


Figure 10. Control and Data Single-Edge Setup/Hold Times to IDCK

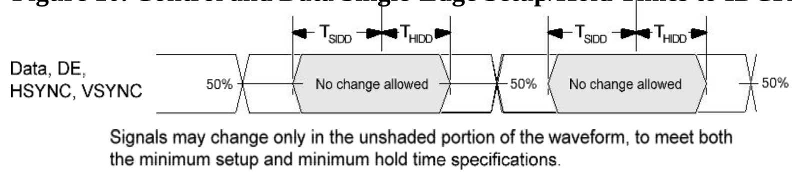


Figure 11. Dual-Edge Setup/Hold Times to IDCK

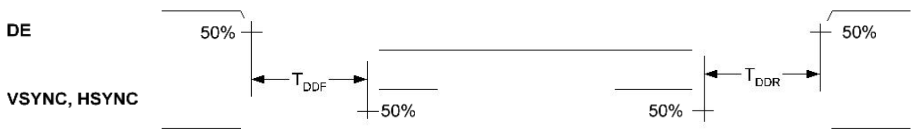


Figure 12. VSYNC and HSYNC Delay Times from/to DE

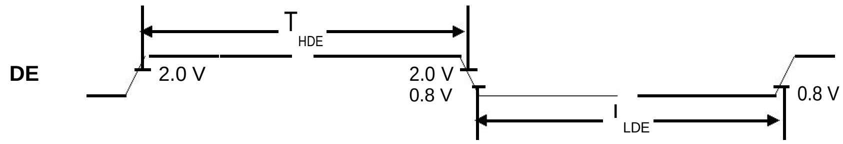
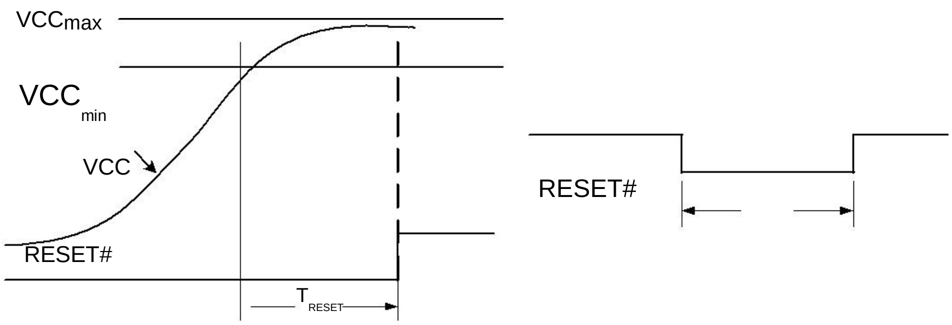


Figure 13. DE HIGH/LOW Times



Note: VCC must be stable between its limits Normal Operating Conditions T_{RESET} bee RESET# is HIGH.

RESET# must be pulled LOW T_{RESET} bee accessing registers. This can be done by holding RESET# LOW until T_{RESET} after stable power (as shown to the left above) or by pulling RESET# LOW from a HIGH state (as shown to the right) at least T_{RESET}.

Figure 14. RESET# Minimum Timings

Audio Timing Diagrams

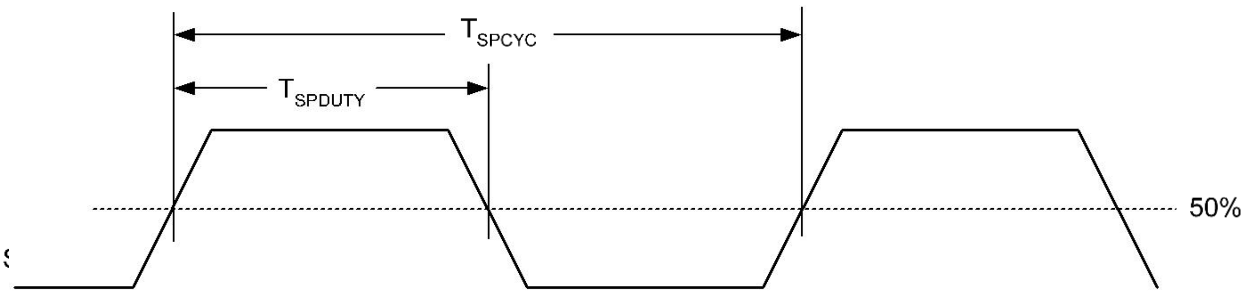


Figure 15. S/PDIF Input Timings

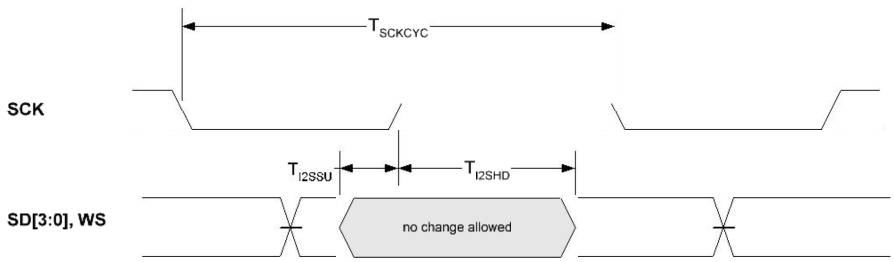


Figure 16. I²S Input Timings

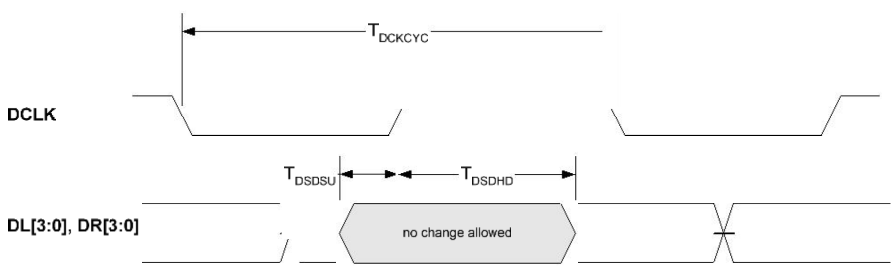


Figure 17. DSD Input Timings

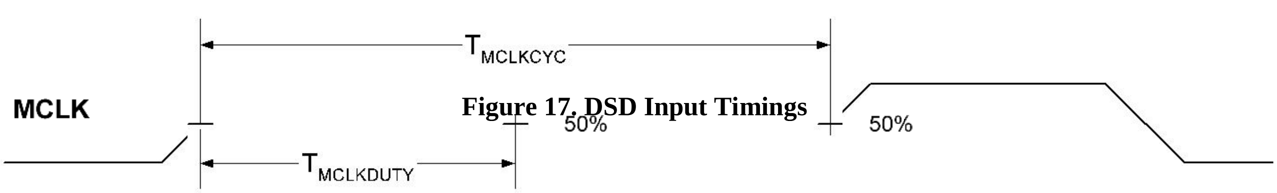


Figure 18. MCLK Timings

Power Supply Sequencing

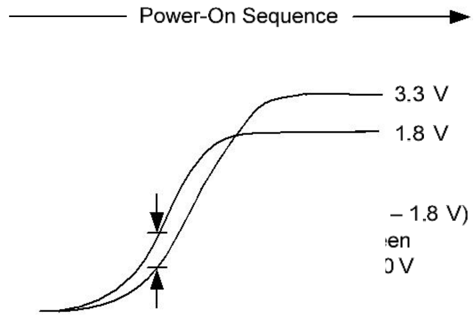


Figure 19. Power Supply Sequencing

Output Timing Diagrams

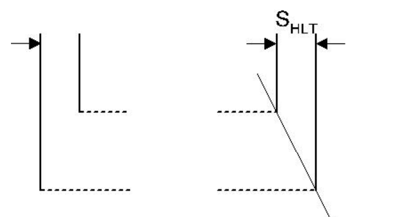


Figure 20. Differential Transition Times

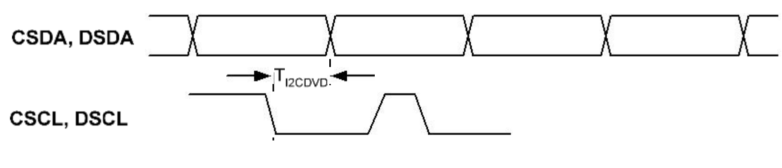


Figure 21. I C Data Valid Delay (Driving Read Cycle Data)

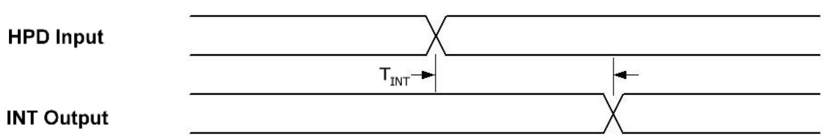


Figure 22. INT Output Pin Response to HPD Input Change

Pin Descriptions

The following tables provide pin descriptions the SiI9134 transmitter

Video Input Pins

Pin Name	Pin	Type	Dir	Description
D0	98	LVTTL	Input	These are the lower 12 bits of the 36-bit pixel bus. These pins are highly configurable, and support multiple RGB and YCbCr mats. Refer to Data Bus Mappings on page 27 complete inmation.
D1	97	LVTTL	Input	
D2	96	LVTTL	Input	
D3	95	LVTTL	Input	
D4	94	LVTTL	Input	
D5	93	LVTTL	Input	
D6	92	LVTTL	Input	
D7	91	LVTTL	Input	
D8	90	LVTTL	Input	
			Input	
D9	86	LVTTL	Input	
D10	85	LVTTL	Input	
D11	84	LVTTL	Input	
D12	83	LVTTL	Input	These are the middle 12 bits of the 36-bit pixel bus.
D13	82	LVTTL	Input	
D14	81	LVTTL	Input	
D15	80	LVTTL	Input	
D16	79	LVTTL	Input	
D17	78	LVTTL	Input	
D18	77	LVTTL	Input	
D19	75	LVTTL	Input	
D20	74	LVTTL	Input	
D21	73	LVTTL	Input	
D22	72	LVTTL	Input	
[redacted]				
D24	70	LVTTL	Input	These are the upper 12 bits of the 36-bit pixel bus.
D25	69	LVTTL	Input	
D26	68	LVTTL	Input	
D27	67	LVTTL	Input	
D28	63	LVTTL	Input	
D29	62	LVTTL	Input	
D30	61	LVTTL	Input	
D31	60	LVTTL	Input	
D33	58	LVTTL	Input	
D34	57	LVTTL	Input	

D35	56	LVTTL	Input	
IDCK	88	LVTTL	Input	Input data clock
DE	1	LVTTL	Input	Data enable
HSYNC	2	LVTTL	Input	Horizontal sync input control signal
VSYNC	3	LVTTL	Input	Vertical sync input control signal

Audio Input Pins

Pin Name	Pin	Type	Dir	Description
SCK	11	LVTTL	Input	I^2S serial clock
WS	10	LVTTL	Input	I^2S Word Select
SD0	9	LVTTL	Input	I^2S serial data
SD1	8	LVTTL	Input	I^2S serial data
SD2	7	LVTTL	Input	I^2S serial data
SD3	6	LVTTL	Input	I^2S serial data
DL0	17	LVTTL	Input	One-bit audio data left 0
DR0	16	LVTTL	Input	One-bit audio data right 0
DL1	19	LVTTL	Input	One-bit audio data left 1
DR1	18	LVTTL	Input	One-bit audio data right 1
DL2	21	LVTTL	Input	One-bit audio data left 2
DR2	20	LVTTL	Input	One-bit audio data right 2

Control Pins

DL3	23	LVTTL	Input	One-bit audio data left 3
DR3	22	LVTTL	Input	One-bit audio data right 3
DCLK	15	LVTTL	Input	One-bit audio clock input
MCLK	5	LVTTL	Input	Audio input master clock
SPDIF	4	LVTTL	Input	S/PDIF audio input

Configuration/Programming Pins

Pin Name	Pin	Type	Dir	Description
HPD	51	LVTTL	Input	Hot Plug Detect input
RSVDL	52	LVTTL	Input	Reserved by and must be tied LOW.
INT	24	LVTTL	Output	Interrupt output

		Open drain	Output	
Pin Name	**Pin**	**Type**	**Dir**	**Description**
CI2CA	50	LVTTL	Input	I^2C device address select (see page 12)
RESET#	25	LVTTL	Input	Reset pin (active LOW)
		Schmidt		5 V tolerant
CSCL	48	Schmitt	Input	I^2C Clock
CSDA	49	Schmitt	Input	I^2C Data (open drain output.)
		Open drain	Output	
DSCL	46	Schmitt	Input	DDC Clock (open drain output)
DSDA	47	Schmitt	Input	DDC Data (open drain output.)

The DSCL pin is bi-directional. The transmitter monitors the state of DSCL so that it can accommodate I^{2}C clock stretching by the slave device. The level on the CI2CA pin is not latched ly and **must not** be changed during any active I^{2}C operations.

Differential Signal Data Pins

Pin Name	Pin	Type	Dir	Description
TX0+	34	TMDS	Output	TMDS output data pairs.
TX0-	33	TMDS	Output	—
TX1+	37	TMDS	Output	—
TX1-	36	TMDS	Output	—
TX2+	40	TMDS	Output	—
TX2-	39	TMDS	Output	—
TXC+	31	TMDS	Output	TMDS output clock pair.
TXC-	30	TMDS	Output	—
EXT_SWING	27	Analog	Input	Voltage Swing Adjust. A resistor is tied from this pin to AVCC18. This resistor determines the amplitude of the voltage swing. recommends a value of 698 Ω 1%.

Power and Ground Pins

Pin Name	Pin	Type	Description	Supply
CVCC18	12, 55, 64, 76, 99	Power	Digital Core VCC.	1.8 V
IOVCC33	14, 53, 66, 89	Power	IO Pin VCC.	3.3 V
AVCC33	44	Power	Analog VCC.	3.3 V
AVCC18	32, 38,	Power	Analog VCC.	1.8 V
AGND	26, 29, 35, 41,43	Ground	Analog GND.	Ground
PVCC1	28	Power	TMDS Core PLL Power.	1.8 V
PVCC2	42	Power	Filter PLL Power.	1.8 V
DDCPWR5V	45	Power	Power reference signal. Supplies power to the DDC I^2C pads when chip is powered off.	5 V
GND	13, 54, 65, 87,100	Ground	Digital ground	Ground

Data Bus Mappings

The SiI9134 transmitter supports multiple input data mappings. Some have explicit control signals, and some have embedded control signals. The selection of data mapping mode should be consistent at the pins and in the corresponding register settings.

Table 23. Input Video mats

Input Mode	Data Widths	Clock Mode	Syncs	Page	Notes
RGB 4:4:4	24, 30, 36	1x	Explicit	28	3, 6
YCbCr 4:4:4	24, 30, 36	1x	Explicit	28	1, 3, 6
YC 4:2:2	16, 20, 24	1 x	Explicit	—	2, 1
YC 4:2:2	16, 20, 24	1 x	Embedded	31	2, 1
YC Mux 4:2:2	16, 20, 24	1 x	Explicit	—	—
YC Mux 4:2:2	16, 20, 24	1 x	Embedded	—	—
RGB 4:4:4	12, 15, 18	dual-edge	Explicit	38	8
YCbCr 4:4:4	12, 15, 18	dual-edge	Explicit	38	1, 8

every HDMI source to transmitan accurate AVI InfoFrame. Even in therare cases where an AVI is not absolutely transmitting audio.In addition, the HDMI Specification andthe EIA/CEA-861D Specification require virtually

Notes:

1. 4:4:4 data contains one Cr, one Cb, and one Y value every pixel.
2. 4:2:2 data contains one Cr and one Cb value every two pixels, and one Y value every pixel.
3. these mats can be carried across the HDMI link. Refer to the HDMI Specification, Section 6.2.3. The link clock must be within the specified range of the HDMI receiver.
4. In YC MUX mode data is input on one 8/10/12-bit channel. A 2x clock is required.
5. Embedded sync decoding extracts the syncs. A 2x clock is required. The DE generator may be needed to convert extracted sync timings to CEA-861D compliant timings.
6. A 2x clock can also be sent with 4:4:4 data. This is necessary the receiver to remat such a stream into 4:2:2 data or into a multiplexed YC MUX output mat.
7. When sending a 2x clock the HDMI source must also send AVI InfoFrames with an accurate pixel replication field. Refer to the HDMI Specification, Section 6.4.
8. Dual-edge clocking is allowed these video mappings.
9. The HDMI Specification requires that every HDMI source transmit an accurate Audio InfoFrame whenever it is

required,   strongly recommends transmitting an AVI during every vertical blanking interval.

RGB and YCbCr 4:4:4 mats with Separate Syncs

The pixel clock runs at the pixel rate and a complete definition of each pixel is input on each clock. The same timing mat is d YCbCr 4:4:4.

Table 24. 4:4:4 Mappings

Pin Name	24-bit RGB	24-bit YCbCr	30-bit RGB	30-bit YCbCr	36-bit RGB	36-bit YCbCr
D0	GND	GND	GND	GND	B0	Cb0
D1	GND	GND	GND	GND	B1	Cb1
D2	GND	GND	B0	Cb0	B2	Cb2
D3	GND	GND	B1	Cb1	B3	Cb3
D4	B0	Cb0	B2	Cb2	B4	Cb4
D5	B1	Cb1	B3	Cb3	B5	Cb5
D6	B2	Cb2	B4	Cb4	B6	Cb6
D7	B3	Cb3	B5	Cb5	B7	Cb7
D8	B4	Cb4	B6	Cb6	B8	Cb8
D9	B5	Cb5	B7	Cb7	B9	Cb9
D10	B6	Cb6	B8	Cb8	B10	Cb10
D11	B7	Cb7	B9	Cb9	B11	Cb11
D12	GND	GND	GND	GND	G0	Y0
D13	GND	GND	GND	GND	G1	Y1
D14	GND	GND	G0	Y0	G2	Y2
D15	GND	GND	G1	Y1	G3	Y3
D16	G0	Y0	G2	Y2	G4	Y4
D17	G1	Y1	G3	Y3	G5	Y5
D18	G2	Y2	G4	Y4	G6	Y6
D19	G3	Y3	G5	Y5	G7	Y7
D21	G5	Y5	G7	Y7	G9	Y9
D22	G6	Y6	G8	Y8	G10	Y10
D33	R5	Cr5		R7Cr7	R9	Cr9
D24	GND	GND	GND	GND	R0	Cr0
D25	GND	GND	GND	GND	R1	Cr1
D26	GND	GND	R0	Cr0	R2	Cr2
D27	GND	GND	R1	Cr1	R3	Cr3
D28	R0	Cr0	R2	Cr2	R4	Cr4
D29	R1	Cr1	R3	Cr3	R5	Cr5
D30	R2	Cr2	R4	Cr4	R6	Cr6
D32	R4	Cr4	R6	Cr6	R8	Cr8
D34	R6	Cr6	R8	Cr8	R10	Cr10
D35	R7	Cr7	R9	Cr9	R11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

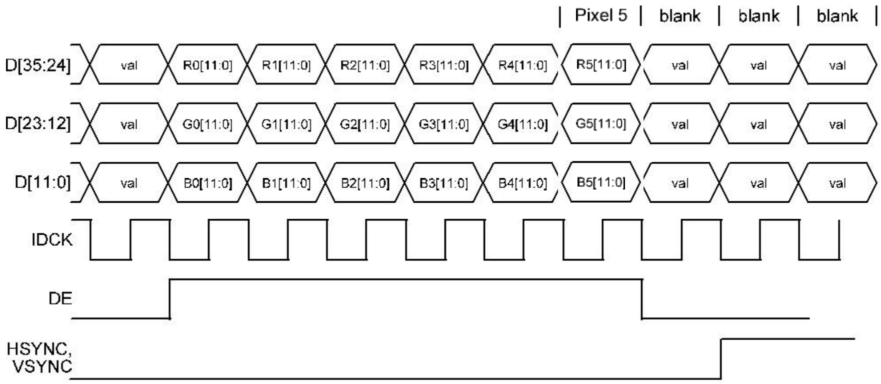


Figure 23. 4:4:4 RGB 36-Bit Timing Diagram

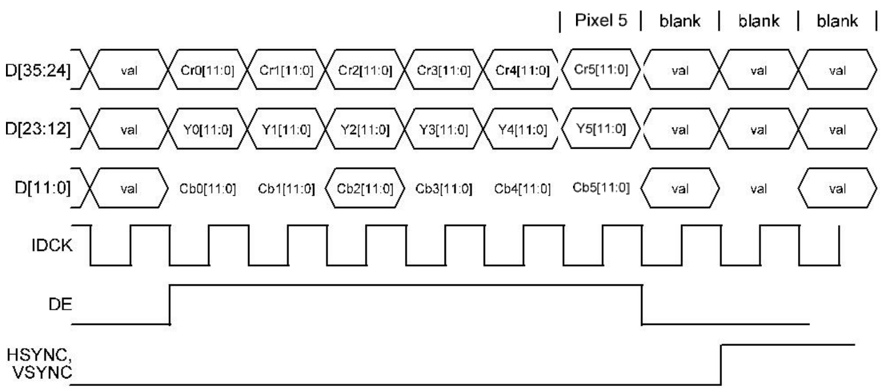


Figure 24. 4:4:4 YCbCr 36 -Bit Timing Diagram

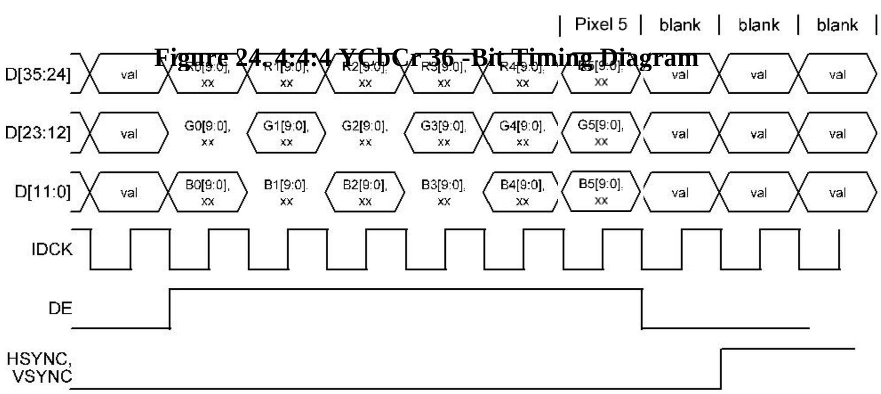


Figure 25. 4:4:4 RGB 30-Bit Timing Diagram

, Inc.

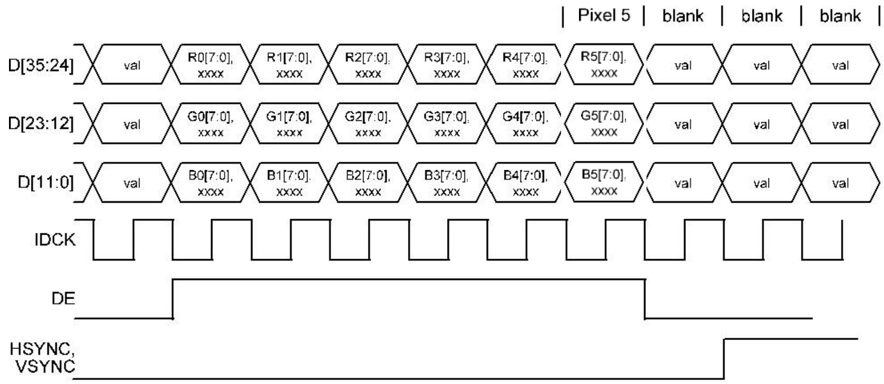


Figure 26. 4:4:4 YCbCr 30-Bit Timing Diagram

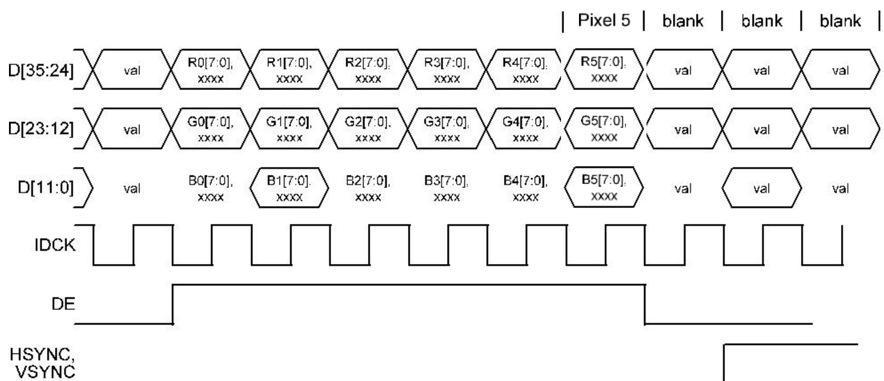


Figure 27. 4:4:4 RGB 24-Bit Timing Diagram

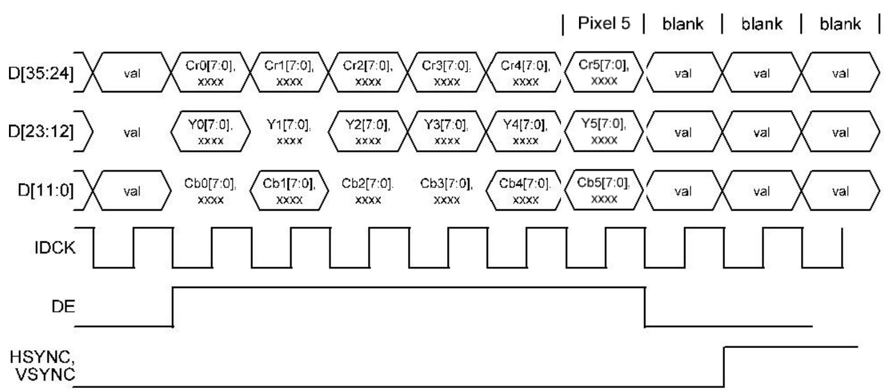


Figure 28. Figure 24. 4:4:4 YCbCr 24-Bit Timing Diagram

YC 4:2:2 mats with Separate Syncs

The YC 4:2:2 mats input one pixel every pixel clock period. A luma (Y) value is input every pixel, but the chroma values (Cb and Cr) change every second pixel. Pixel data can be 16-bit, 20-bit or 24- bit. HSYNC and VSYNC are input explicitly on their own pins. The DE high time must contain an even number of pixel clocks.

Table 25. YC 4:2:2 Separate Sync Pin Mappings

Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
D0	GND	GND	GND	GND	GND	GND
D1	GND	GND	GND	GND	GND	GND
D2	GND	GND	GND	GND	GND	GND
D3	GND	GND	GND	GND	GND	GND
D4	GND	GND	GND	GND	Y0	Y0
D5	GND	GND	GND	GND	Y1	Y1
D6	GND	GND	Y0	Y0	Y2	Y2
D7	GND	GND	Y1	Y1	Y3	Y3
		Y6	Y8Y8Y10			
D8	GND	GND	GND	GND	Cb0	Cr0
D9	GND	GND	GND	GND	Cb1	Cr1
D10	GND	GND	Cb0	Cr0	Cb2	Cr2
D17	Y1	Y1	Y3	Y3	Y5	Y5
D11	GND	GND	Cb1	Cr1	Cb3	Cr3
D12	GND	GND	GND	GND	GND	GND
D13	GND	GND	GND	GND	GND	GND
D15	GND	GND	GND	GND	GND	GND
D16	Y0	Y0	Y2	Y2	Y4	Y4
D18	Y2	Y2	Y4	Y4	Y6	Y6
D19	Y3	Y3	Y5	Y5	Y7	Y7
D20	Y4	Y4	Y6	Y6	Y8	Y8
D21	Y5	Y5	Y7	Y7	Y9	Y9
D23	Y7	Y7	Y9	Y9	Y11	Y11
D24	GND	GND	GND	GND	GND	GND
D25	GND	GND	GND	GND	GND	GND

D26	GND	GND	GND	GND	GND	GND
D27	GND	GND	GND	GND	GND	GND
D28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
D29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
D31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
D32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
D33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
D34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
D35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

YC 4:2:2 mats with Embedded Sync

Table 26. YC 4:2:2 Embedded Sync Pin Mappings

Pin Name	16-bit YC		20-bit YC		24-bit YC	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
D0	GND	GND	GND	GND	GND	GND
D1	GND	GND	GND	GND	GND	GND
D2	GND	GND	GND	GND	GND	GND
D3	GND	GND	GND	GND	GND	GND
D4	GND	GND	GND	GND	Y0	Y0
D5	GND	GND	GND	GND	Y1	Y1
D6	GND	GND	Y0	Y0	Y2	Y2
D7	GND	GND	Y1	Y1	Y3	Y3
D8	GND	GND	GND	GND	Cb0	Cr0
D9	GND	GND	GND	GND	Cb1	Cr1
D10	GND	GND	Cb0	Cr0	Cb2	Cr2
D11	GND	GND	Cb1	Cr1	Cb3	Cr3
D12	GND	GND	GND	GND	GND	GND
D13	GND	GND	GND	GND	GND	GND
D14	GND	GND	GND	GND	GND	GND
D15	GND	GND	GND	GND	GND	GND
D16	Y0	Y0	Y2	Y2	Y4	Y4
D17	Y1	Y1	Y3	Y3	Y5	Y5
D18	Y2	Y2	Y4	Y4	Y6	Y6
D19	Y3	Y3	Y5	Y5	Y7	Y7
D21	Y5	Y5	Y7	Y7	Y9	Y9
D23	Y7	Y7	Y9	Y9	Y11	Y11
D24	GND	GND	GND	GND	GND	GND
D35	Cb7	Cr7		Cb9Cr9	Cb11	Cr11
D26	GND	GND	GND	GND	GND	GND
D27	GND	GND	GND	GND	GND	GND
D28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
D29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
D30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
D31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
D32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
D34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
HSYNC	GND	GND	GND	GND	GND	GND
VSYNC	GND	GND	GND	GND	GND	GND
DE	GND	GND	GND	GND	GND	GND

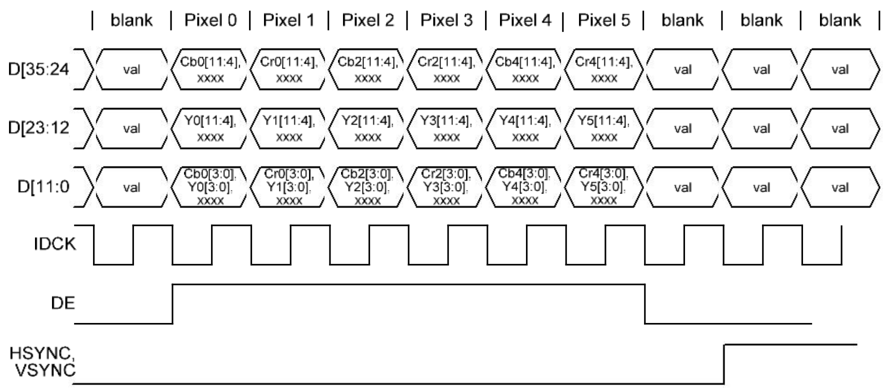


Figure 29. YC 4:2:2 12-Bit per Pixel Timing Diagram

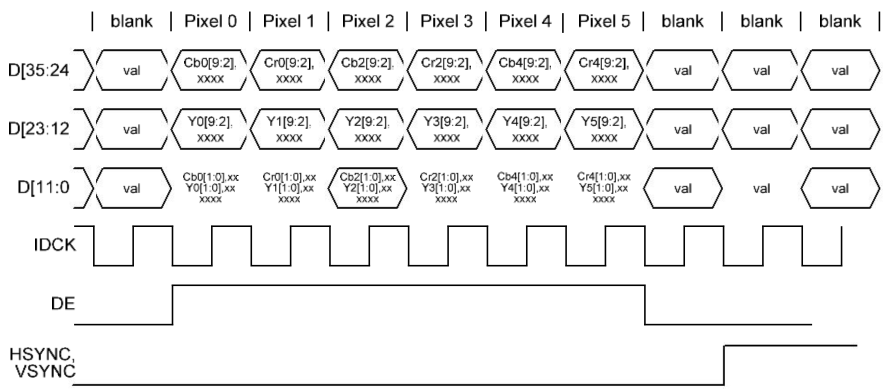


Figure 30. YC 4:2:2 10-Bit per Pixel Timing Diagram

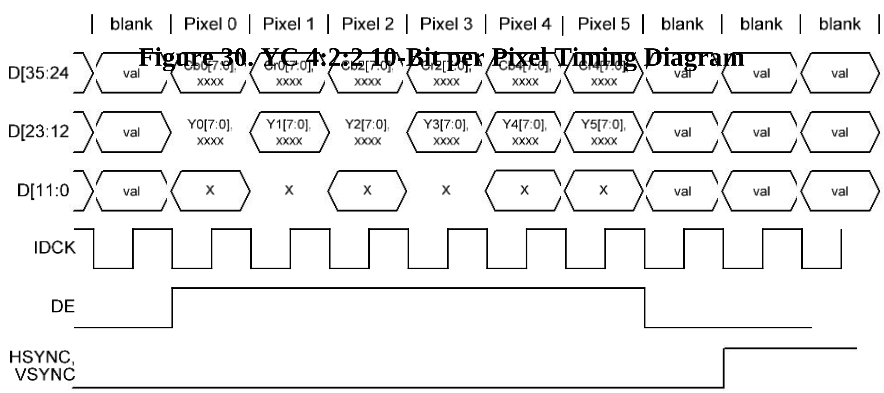


Figure 31. YC 4:2:2 8-Bit per Pixel Timing Diagram

Note: The *val* data is defined in various specifications to specific values.

YC Mux 4:2:2 mats with Separate Syncs

The video data is multiplexed onto fewer pins than the mapping in Table 25, but a luma (Y) is provided each pixel, and either a Cb or a Cr value each pixel, since the clock rate is doubled. Figure 32 shows the 12-bit mode. The 10-and 8-bit mappings fewer input pins the pixel data. Note the explicit syncs.

Table 27. YC Mux 4:2:2 Mappings

Pin Name	8-bit		10-bit		12-bit	
	1st Clk	2nd Clk	1st Clk	2nd Clk	1st Clk	2nd Clk
D0	GND	GND	GND	GND	GND	GND
D1	GND	GND	GND	GND	GND	GND
D2	GND	GND	GND	GND	GND	GND
D3	GND	GND	GND	GND	GND	GND
D4	GND	GND	GND	GND	C0	Y0
D5	GND	GND	GND	GND	C1	Y1
D6	GND	GND	C0	Y0	C2	Y2
D7	GND	GND	C1	Y1	C3	Y3
			Y6C8		Y8C10	
D8	GND	GND	GND	GND	GND	GND
D9	GND	GND	GND	GND	GND	GND
D10	GND	GND	GND	GND	GND	GND
D17	C1	Y1	C3	Y3	C5	Y5
D11	GND	GND	GND	GND	GND	GND
D12	GND	GND	GND	GND	GND	GND
D13	GND	GND	GND	GND	GND	GND
D15	GND	GND	GND	GND	GND	GND
D16	C0	Y0	C2	Y2	C4	Y4
D18	C2	Y2	C4	Y4	C6	Y6
D19	C3	Y3	C5	Y5	C7	Y7
D20	C4	Y4	C6	Y6	C8	Y8
D21	C5	Y5	C7	Y7	C9	Y9
D23	C7	Y7	C9	Y9	C11	Y11
D24	GND	GND	GND	GND	GND	GND
D25	GND	GND	GND	GND	GND	GND

D26	GND	GND	GND	GND	GND	GND
D27	GND	GND	GND	GND	GND	GND
D28	GND	GND	GND	GND	GND	GND
D29	GND	GND	GND	GND	GND	GND
D31	GND	GND	GND	GND	GND	GND
D32	GND	GND	GND	GND	GND	GND
D33	GND	GND	GND	GND	GND	GND
D34	GND	GND	GND	GND	GND	GND
D35	GND	GND	GND	GND	GND	GND
HSYNC	HSYNC		HSYNC		HSYNC	
VSYNC	VSYNC		VSYNC		VSYNC	
DE	DE		DE		DE	

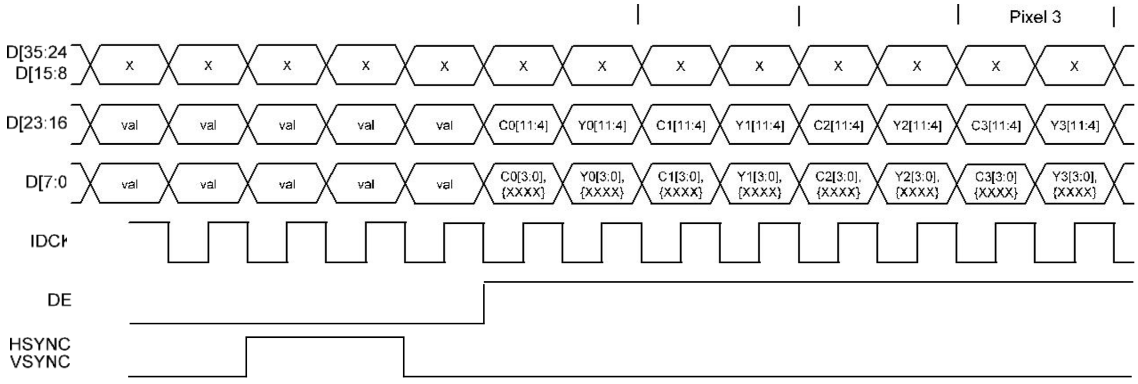


Figure 32. YC Mux 4:2:2 Timing Diagram

Note: The *val* data is defined in various specifications to specific values.

YC Mux 4:2:2 Embedded Sync mats

This mode is similar to the one on page 34, but with embedded syncs. It is similar to SMTPE 293 in embedding the syncs, but also multiplexes the luma (Y) and chroma (Cb and Cr) onto the same pins on alternating pixel clock cycles. Normally this mode is d 480i, 480p, 576i, and 576p modes. Input clock rate is twice the pixel clock rate. SAV code is shown bee rise of DE. EAV follows fall of DE. 480p 54 MHz input can be achieved if the input clock is 54 MHz.

Table 28. YC Mux 4:2:2 Embedded Sync Pin Mapping

Pin Name	8-bit		10-bit		12-bit	
	1st Clk	2nd Clk	1st Clk	2nd Clk	1st Clk	2nd Clk
D0	GND	GND	GND	GND	GND	GND
D1	GND	GND	GND	GND	GND	GND
D2	GND	GND	GND	GND	GND	GND
D3	GND	GND	GND	GND	GND	GND
D4	GND	GND	GND	GND	C0	Y0
D5	GND	GND	GND	GND	C1	Y1
D6	GND	GND	C0	Y0	C2	Y2
D7	GND	GND	C1	Y1	C3	Y3
D8	GND	GND	GND	GND	GND	GND
D9	GND	GND	GND	GND	GND	GND
D10	GND	GND	GND	GND	GND	GND
D11	GND	GND	GND	GND	GND	GND
D12	GND	GND	GND	GND	GND	GND
D13	GND	GND	GND	GND	GND	GND
D14	GND	GND	GND	GND	GND	GND
D15	GND	GND	GND	GND	GND	GND
D16	C0	Y0	C2	Y2	C4	Y4
D17	C1	Y1	C3	Y3	C5	Y5
D18	C2	Y2	C4	Y4	C6	Y6
D19	C3	Y3	C5	Y5	C7	Y7
D20	C4	Y4	C6	Y6	C8	Y8
D21	C5	Y5	C7	Y7	C9	Y9
D22	C6	Y6	C8	Y8	C10	Y10
D23	C7	Y7	C9	Y9	C11	Y11
D24	GND	GND	GND	GND	GND	GND
D25	GND	GND	GND	GND	GND	GND
D26	GND	GND	GND	GND	GND	GND
D27	GND	GND	GND	GND	GND	GND
D28	GND	GND	GND	GND	GND	GND
D30	GND	GND	GND	GND	GND	GND
D31	GND	GND	GND	GND	GND	GND
D32	GND	GND	GND	GND	GND	GND
D33	GND	GND	GND	GND	GND	GND

D34	GND	GND	GND	GND	GND	GND
D35	GND	GND	GND	GND	GND	GND
HSYNC	GND		GND		GND	
VSYNC	GND		GND		GND	
DE	GND		GND		GND	

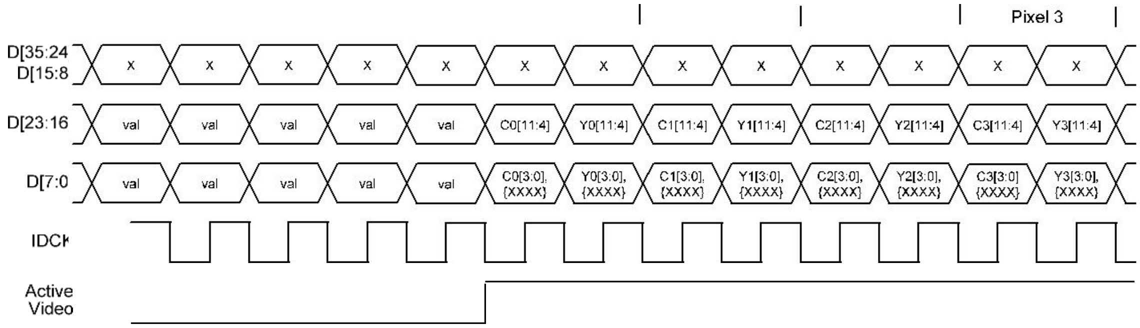


Figure 33. YC Mux 4:2:2 Embedded Sync Encoding Timing Diagram

Note: The val data is defined in various specifications to specific values. The DE generator may be needed to convert extracted sync timings to CEA-861D timings. See the ITU-R BT656 Specification.

12/15/18-Bit DMO RGB and YCbCr mats

The pixel clock runs at the pixel rate and a complete definition of each pixel is input on each clock. One clock edge latches in half the pixel data on 12, 15, or 18 pins (depending on the input data width). The opposite clock edge latches in the remaining half of the pixel data on the same 12, 15, or 18 pins. Figure 34 shows RGB data. The same timing mat is d YCbCr 4:4:4, as listed in Table 24. Control signals (DE, HSYNC, and VSYNC) must change state to meet the setup and hold times with respect to the first edge of IDCK. Figure 34 shows IDCK latching input data when the EDGE bit is set to 1. DE, VSYNC, and HSYNC must change state while meeting the setup and hold times specified 12-bit, dual-edge mode. Refer to page 18 more details.

Table 29. 12/15/18-Bit Input 4:4:4 Mappings

Pin Name	24-bit				30-bit				36-bit			
	RGB		YCbCr		RGB		YCbCr		RGB		YCbCr	
	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge	First Edge	Second Edge
D0	GND	GND	GND	GND	GND	GND	GND	GND	B0	G6	Cb0	Y6
D1	GND	GND	GND	GND	GND	GND	GND	GND	B1	G7	Cb1	Y7
D2	GND	GND	GND	GND	B0	G5	Cb0	Y5	B2	G8	Cb2	Y8
		R5Y1		Cr5	G3		R8hnologyY3Cr8G5					
D3	GND	GND	GND	GND	B1	G6	Cb1	Y6	B3	G9	Cb3	Y9
D4	B0	G4	Cb0	Y4	B2	G7	Cb2	Y7	B4	G10	Cb4	Y10
D5	B1	G5	Cb1	Y5	B3	G8	Cb3	Y8	B5	G11	Cb5	Y11
D6	B2	G6	Cb2	Y6	B4	G9	Cb4	Y9	B6	R0	Cb6	Cr0
D7	B3	G7	Cb3	Y7	B5	R0	Cb5	Cr0	B7	R1	Cb7	Cr1
D8	B4	R0	Cb4	Cr0	B6	R1	Cb6	Cr1	B8	R2	Cb8	Cr2
D9	B5	R1	Cb5	Cr1	B7	R2	Cb7	Cr2	B9	R3	Cb9	Cr3
D10	B6	R2	Cb6	Cr2	B8	R3	Cb8	Cr3	B10	R4	Cb10	Cr4
D11	B7	R3	Cb7	Cr3	B9	R4	Cb9	Cr4	B11	R5	Cb11	Cr5
D12	GND	GND	GND	GND	GND	GND	GND	GND	G0	R6	Y0	Cr6
D13	GND	GND	GND	GND	GND	GND	GND	GND	G1	R7	Y1	Cr7
D14	GND	GND	GND	GND	G0	R5	Y0	Cr5	G2	R8	Y2	Cr8
D15	GND	GND	GND	GND	G1	R6	Y1	Cr6	G3	R9	Y3	Cr9
D16	G0	R4	Y0	Cr4	G2	R7	Y2	Cr7	G4	R10	Y4	Cr10
D18	G2	R6	Y2	Cr6	G4	R9	Y4	Cr9	GND	GND	GND	GND
D19	G3	R7	Y3	Cr7	GND	GND	GND	GND	GND	GND	GND	GND

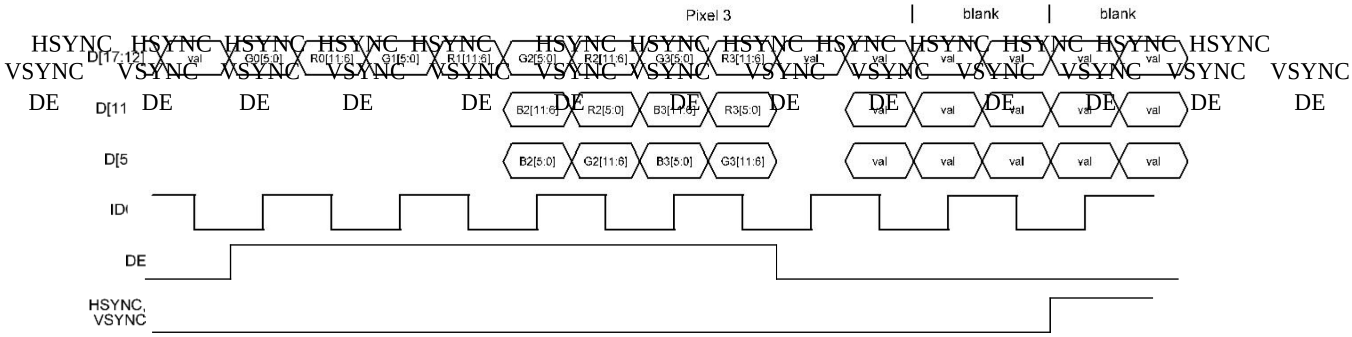


Figure 34. 12-Bit Input DMO Timing Diagram

Design Guidelines

Power Supplies

Voltage Ripple Regulation

Excessive noise on PVCC1 or PVCC2 can ca improper PLL operation as it tries to stay locked on the incoming video clock. Make sure to keep PVCC1 and PVCC2 noise below the maximum allowable value of 100 mV. If the ripple on PVCC1 or PVCC21 is higher than 100 mV,   recommends that a separate power source be d to supply these pins. A voltage regulator that can supply 50 mA is sufficient PVCC1 and PVCC2. Refer to the schematic on page 42.

Decoupling

Designers should include decoupling and bypass capacitors at each power pin in the layout. These capacitors are shown schematically in Figure 35. Place them as close as possible to the SiI9134 device pins, and avoid routing through vias if possible, as shown in Figure 36, which represents the various types of power pins on the transmitter.

Note: Figure 36 shows the decoupling and bypass capacitor placement the TQFP package.

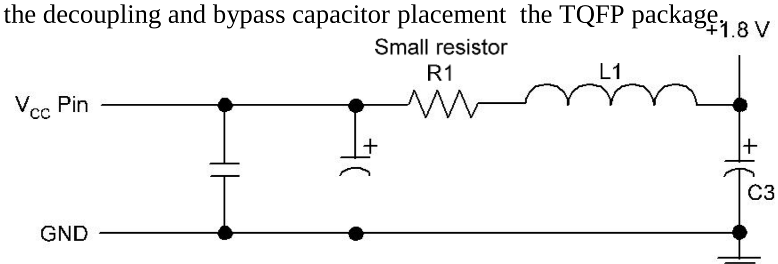


Figure 35. Decoupling and Bypass Schematic

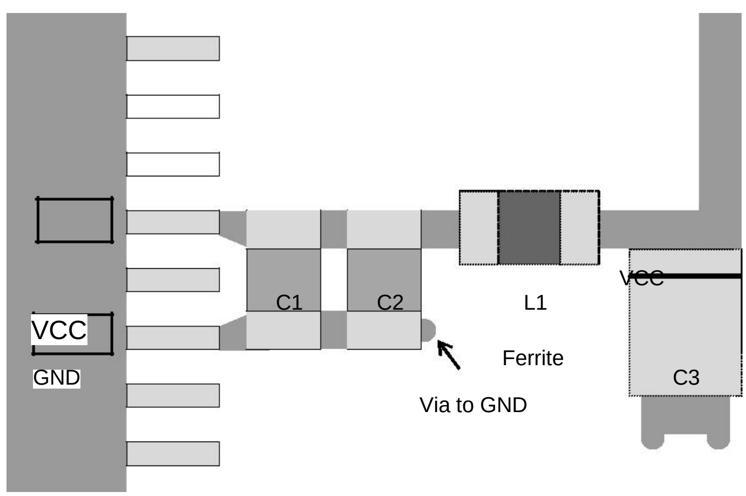


Figure 36. Decoupling and Bypass Capacitor Placement

Pins in each of the groups AVCC33, AVCC18, CVCC18, and IOVCC33 can share C2, C3, and L1, with each pin having a separate C1 placed as close to the pin as possible.

High-Speed TMDS Signals

ESD Protection

The transmitter chip can withstand electrostatic discharge to 2kV HBM. In applications where higher protection levels are required, ESD-limiting components can be placed on the differential lines coming out of the chip. These components typically have a capacitive effect, reducing the signal quality at higher clock frequencies on the link. the lowest capacitance devices possible. In no case should the capacitance value exceed 5 pF.

Transmitter Layout Guidelines

The layout guidelines below help to ensure signal integrity, and   encourages the board designer to follow them if possible. An example of routing is shown in Figure 37.

- Place the output connector that carries the TMDS signals as close as possible to the chip.
- Route the differential lines as directly as possible from the connector to the device.

- Route the two traces of each differential pair together.
- Minimize the number of vias through which the signal lines are routed.

- Lay out the two traces of each differential pair with a controlled differential impedance of 100 Ω.

Beca   HDMI transmitters are tolerant of skews between differential pairs, spiral skew compensation path length differences is not required.

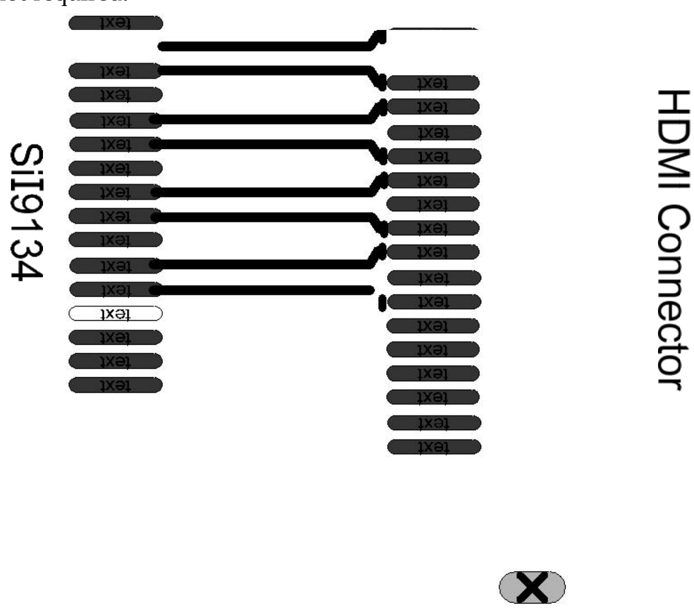


Figure 37. Transmitter to HDMI Connector Routing–Top View

Protection I^2C Port

Both the local (CSCL/CSDA) and master DDC (DSCL/DSDA) I^2C pins on the transmitter chip are 5 V tolerant, although the CSCL and CSDA pins are typically tied to 3.3 V. When no VCC is applied to the chip, the CSCL and CSDA pins can continue to draw a small current and prevent the 1^2C master from communicating with other devices on the I^2C bus. Theree, do not remove VCC unless the local I^2C bus is completely idle. The same requirement does not

apply to the DSCL and DSDA pins, which have true open- drain connections that enter a high-impedance state when the chip is powered off, as long as the 5 volt reference voltage signal these I/Os, DDCPWR5V, continues to be supplied.

Hot Plug Signal Conditioning

The HDMI interface provides a hot plug signal back to the host side from the display. This signal is generated by routing a 5 V source from the host through the cable to the display, and back. The specification defines the minimum HIGH level the hot plug as 2.0 volts at the connector pin. The HPD pin is 5 V tolerant and can be directly connected to the SiI9134 transmitter. However, an external pull-down resistor of 47 kΩ is required to guarantee that this CMOS input is not floating, as shown in Figure 39 on page 43.

HDMI Design Considerations

HDMI CTS Test ID 7-4: TMDS Differential Rise and Fall Time

The HDMI CTS requires that the differential rise and fall time of the TMDS signals be ≥ 75 ps, with all measurements taken at the highest supported TMDS clock frequency. The HDMI CTS Specification lists three different oscilloscopes that can be d to measure this parameter.

SiI9134 transmitter passes with rise and fall times greater than 75 ps. However, when using the Agilent DSO80000B

- Tektronix TDS7404 (can bedupto148.5MHz.)
- Tektronix DPO70804 (no frequency limitation)
- Agilent DSO80000B (no frequency limitation)

The Tektronix TDS7404scopeisthesamescope listed in the previous HDMI 1.2 CTS. When this scope is d, the adding a discrete capacitor of approximately 1 pF from the signal to ground can also solve this compliance issue. The

scope, has found the rise and fall time of the transmitter can be faster than 75 ps. The difference is due to the higher bandwidth of the Agilent DSO80000B, giving a more accurate measurement. has done no testing with Tektronix DPO70804.

Recommendation to pass Test ID 7-4

Adding common components, such as common-mode filters and ESD suppression devices, increase the capacitance slightly, slowing down the rise and fall time to well within the specification. If these devices are not in your design, following external components have been tested on the CP9034/9134 reference design and proven to comply with the HDMI CTS Specification:

- Common Mode Filter: TDK ACM2012H
- ESD Suppression Diode: Semtech Rclamp 0514M. Calinia Micro Devices (CMD) also makes a similar device

Components with similar characteristics can also be d.

Electromagnetic interference is a functionofboardlayout,shielding,receiver component operating voltage, frequency of operation, and other factors. When attempting to control emissions, it is important not to place any passive components on the differential signal lines other than any essential ESD protection, as described earlier. The differential signaling d in HDMI is inherently low in EMI, as long as the routing recommendations noted in the Transmitter Layout Guidelines section on page 40 are followed.

which has not tested but from which we expect similar compliance permance.

EMI Considerations

The PCB ground plane should extend unbroken under as much of the transmitter chip and associated circuitry as possible, with all ground pins of the chip using a common ground.

Typical Circuit

Representative circuits applications of the SiI9134 transmitter chip are shown in Figure 38 through Figure 41. a detailed review of your intended circuit implementation, contact your representative.

Power Supply Decoupling

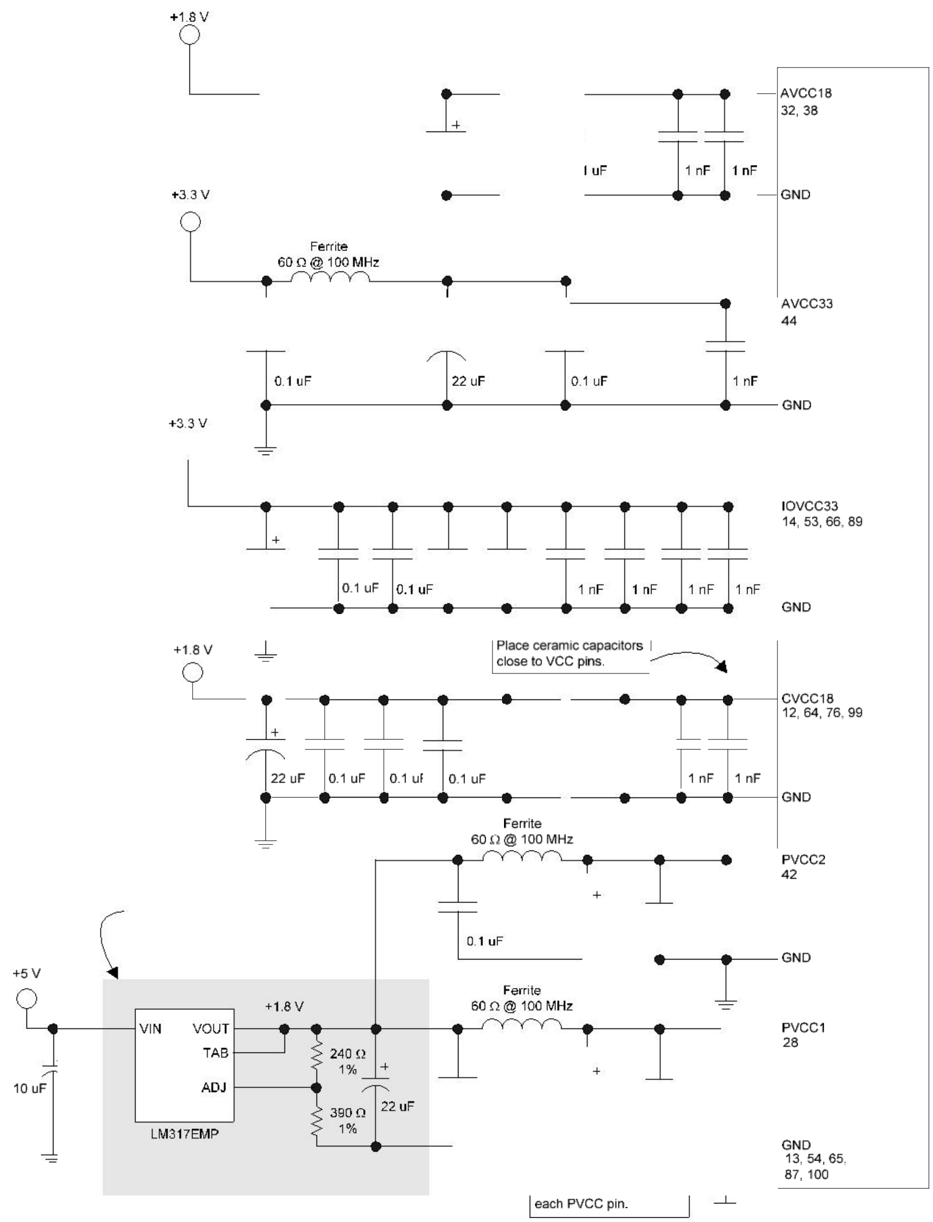


Figure 38. Power Supply Decoupling and PLL Filtering Schematic

The ferrites shown in Figure 38 should have an impedance of 10 Ω or more in the frequency range 1–2 MHz.

HDMI Port TMDS Connections

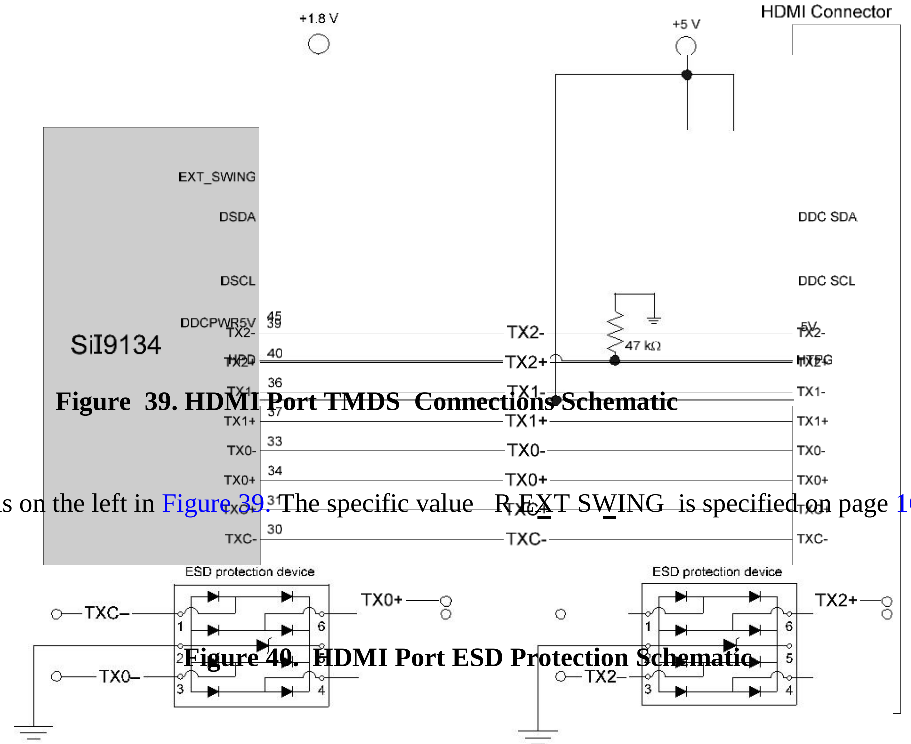


Figure 39. HDMI Port TMDS Connections Schematic

The transmitter is on the left in Figure 39. The specific value R EXT SWING is specified on page 16.

Figure 40. HDMI Port ESD Protection Schematic

Control Signal Connections

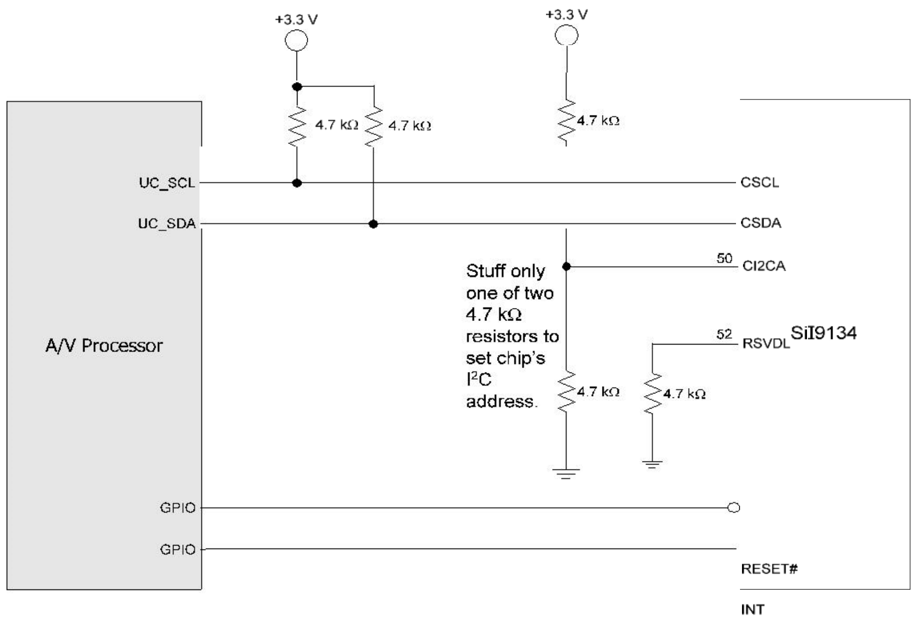
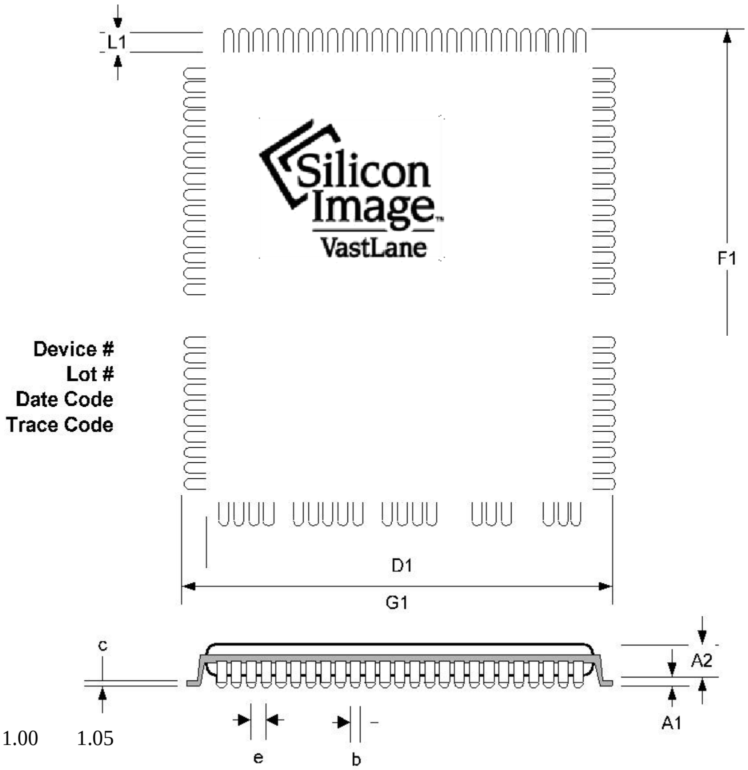


Figure 41. Controller Connections Schematic

Packaging

100-pin TQFP Package Dimensions and Marking Specification



Body thickness 1.00 1.05

Item	Description	typ	max
A	Thickness	—	1.20
A1	Stand-off	—	0.15
A2			
D1	Body size	14.00	—
E1	Body size	14.00	—
F1	Footprint	16.00	—
G1	Footprint	16.00	—
L1	Lead length	1.00	—
L	Foot length	0.60	0.75
b	Lead width	0.22	0.27
c	Lead thickness	—	0.20
e	Lead pitch	0.50	—

Package: SiI9134CTU	
Legend	**Description**
LLLLLL.LLLL	Lot number
YY	Yearof manufacture
WW	Week of manufacture
TTTTTT	Trace code
M	Maturity code = 0: engineering samples = 1: pre-production > 1: production

Figure 42. Package Diagram

Ordering Inmation

Production Part Numbers:

—

Device	Part Number
Standard	SiI9134CTU

References

Standards Documents

Table 30 lists the abbreviations d in this document. Contact the responsible standards groups listed in Table 31 more inmation on these specifications.

Table 30. Referenced Documents

Abbreviation	Standards Publication, Organization, and Date
HDMI	*High Definition Multimedia Interface, Revision 1.4*, HDMI Consortium, June 2009
HCTS	*HDMI Compliance Test Specification, Revision 1.3a*, HDMI Consortium, November 2006
HDCP	*High-bandwidth Digital Content Protection, Revision 1.3*, Digital Content Protection, LLC, December 2006
E-EDID	*Enhanced Extended Display Identification Data Standard*, Release A Revision 1, VESA, Feb. 2000
E-DID IG	*VESA EDID Implementation Guide*, VESA, June 2001
CEA-861-D	*A DTV Profile Uncompressed High Speed Digital Interfaces*, EIA/CEA, July 2006
EDDC	*Enhanced Display Data Channel Standard*, Version 1.1, VESA, March 2004

Table 31. Standards Groups Contact Inmation

Standards Group	Web URL	e-mail	Phone
ANSI/EIA/CEA	http://global.ihs.com	global@ihs.com	800-854-7179
VESA	http://www.vesa.org	—	408-957-9270
HDCP	http://www.digital-cp.com	info@digital-cp.com	—
DVI	http://www.ddwg.org	ddwg.if@intel.com	—
HDMI	http://www.hdmi.org	admin@hdmi.org	—

Documents

Table 32 lists   documents that are available from your   sales representative.

Table 32.   Publications

Document	Title	
[redacted]		
SiI-PR-0039	*SiI9034/9134 HDMI Transmitter Programmer's Reference*	

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