Single-Chip 10/100M Ethernet PHYceiver with Auto MDIX

General Description

The SR8201F-VB-CG, SR8201FL-VB-CG, and SR8201FN-VB-CG are single-chip/single-port 10/100Mbps Ethernet PHYceivers that support:

- MII (Media Independent Interface)
- RMII (Reduced Media Independent Interface)

The SR8201F/FL/FN implement all 10/100M Ethernet Physical-layer functions including the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Twisted Pair Physical Medium Dependent Sublayer (TP-PMD), 10Base-TX Encoder/Decoder, and Twisted-Pair Media Access Unit (TPMAU). The SR8201F/FL/FN support auto MDIX.

A PECL (Pseudo Emitter Coupled Logic) interface is supported to connect with an external 100Base-FX fiber optical transceiver. The chip utilizes an advanced CMOS process to meet low voltage and low power requirements. With on-chip DSP (Digital Signal Processing) technology, the chip provides excellent performance under all operating conditions.

Application

- MAU (Media Access Unit)
- DTV (Digital TV)
- CNR (Communication and Network Riser)
- Game Console
- Printer and Office Machine
- DVD Player and Recorder
- Ethernet Hub
- Ethernet Switch

In addition, the SR8201F/FL/FN can be used in any embedded system with an Ethernet MAC that needs a UTP physical connection or Fiber PECL interface to an external 100Base-FX optical transceiver module

Features

- Supports IEEE 802.3az-2010 (EEE)
- 100Base-TX IEEE 802.3u Compliant
- 10Base-T IEEE 802.3 Compliant
- Supports MII mode
- Supports RMII mode
- Full/half duplex operation
- Twisted pair or fiber mode output
- Supports Auto-Negotiation
- Supports power down mode
- Supports Link Down Power Saving
- Supports Base Line Wander (BLW) Compensation
- Supports auto MDIX
- Supports Interrupt function
- Support Wake-On_LAN(WOL)
- Adaptive Equalization
- Automatic Polarity Correction
- LEDs
  - SR8201F and SR8201FL provide two network status LEDs
  - SR8201FN provide three network status LEDs
- Supports 25MHz external crystal or OSC
- Supports 50MHz external OSC Clock input for RMII
- Provides 50MHz clock source for MAC
- Low power supply 1.1V and 3.3V; 1.1V is generated by an internal regulator
- 0.11μm CMOS process
- Packages:
  - 32-pin MII/RMII QFN ‘Green’ package (SR8201F)
  - 48-pin MII/RMII LQFP ‘Green’ package (SR8201FL)
  - 48-pin MII/RMII QFN ‘Green’ package (SR8201FN)

Application Diagram

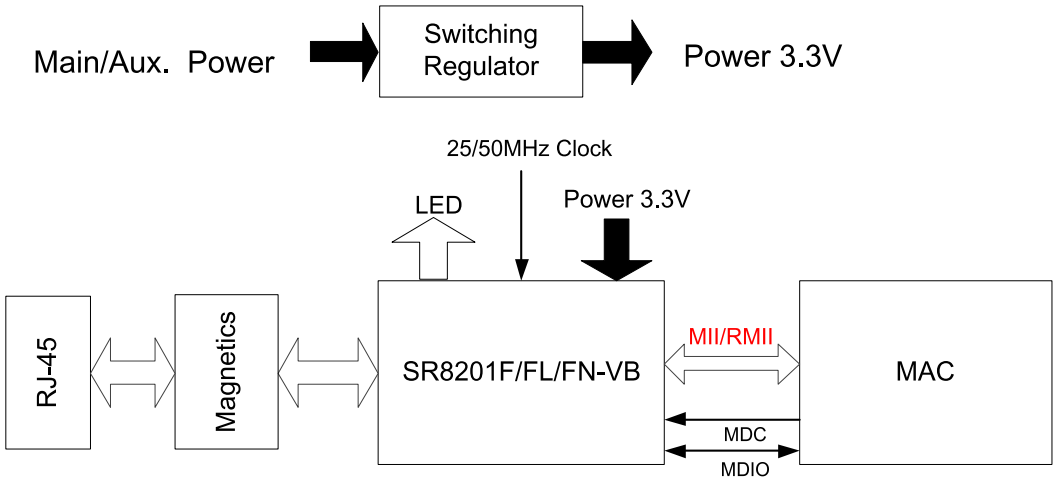


Figure 1. Application Diagram

Block Diagram

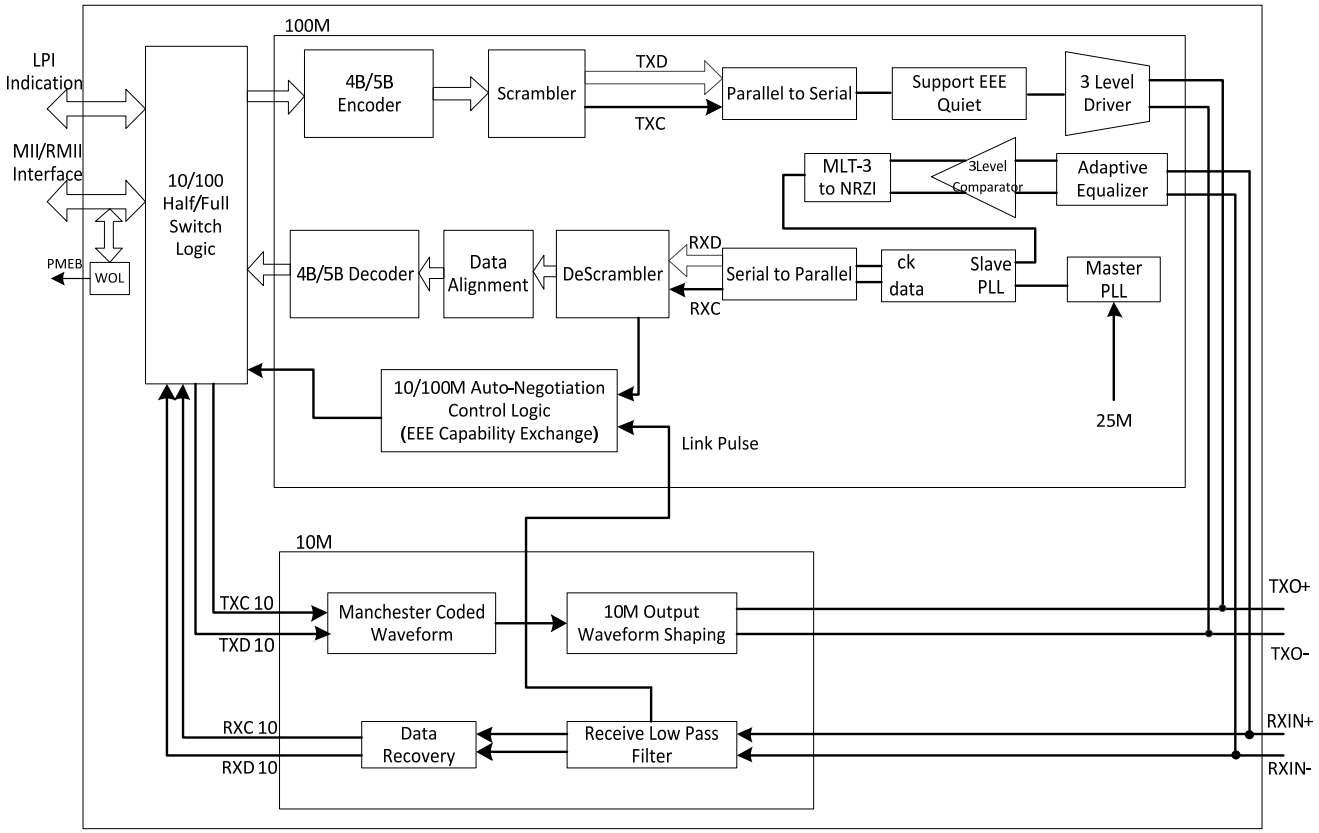


Figure 2. Block Diagram

Pin Assignment

SR8201F (32-Pin)

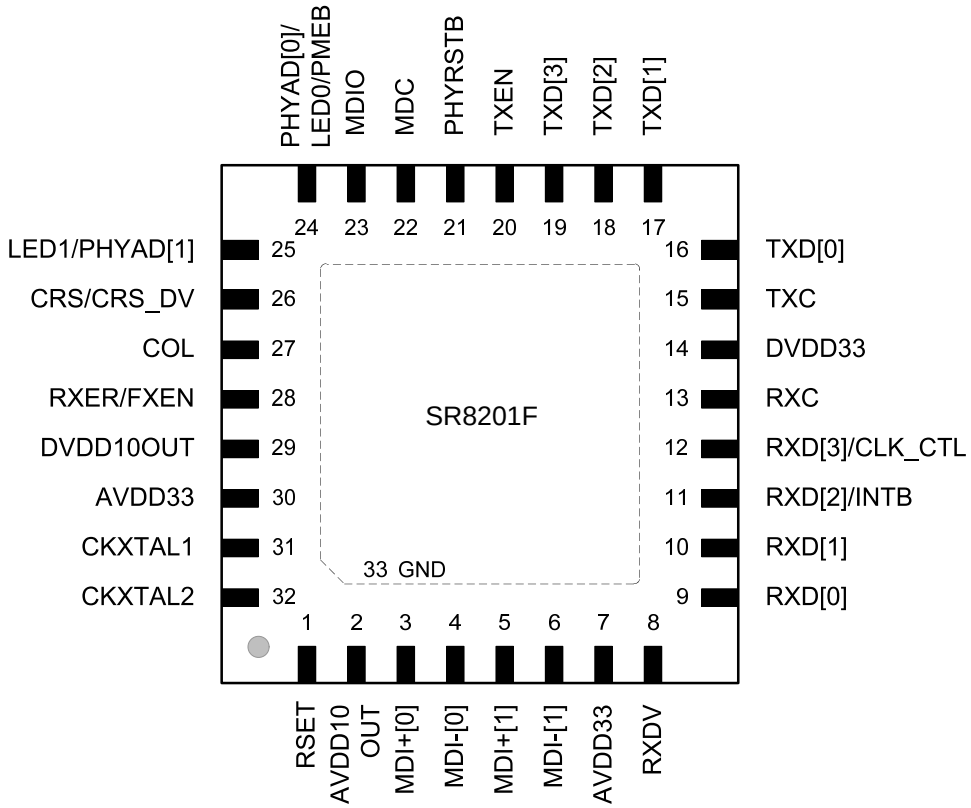


Figure. SR8201F QFN-32 Pin Assignments

SR8201FN (48-Pin)

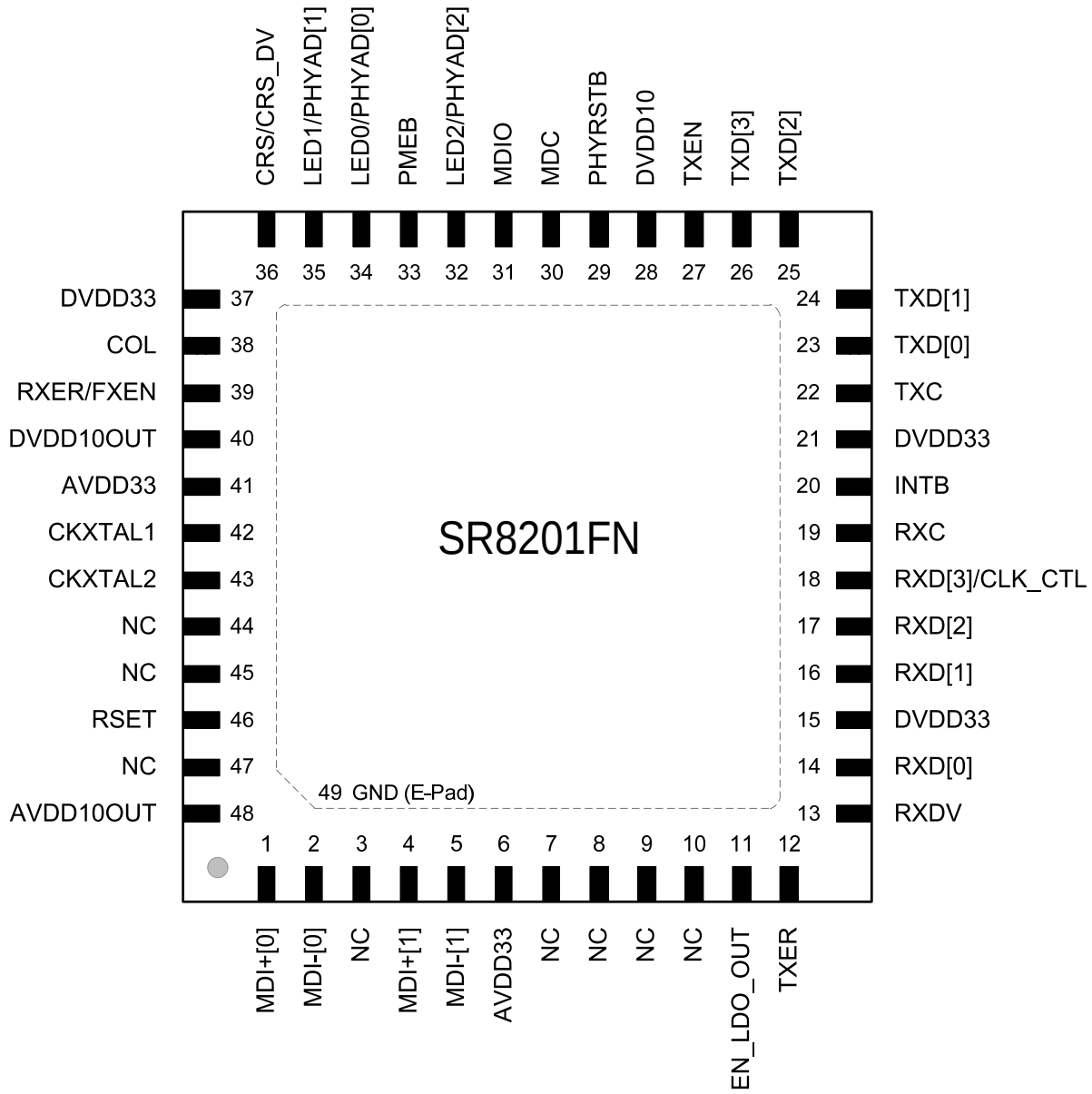


Figure 4. SR8201FN QFN-48 Pin Assignments

SR8201FL (48-Pin)

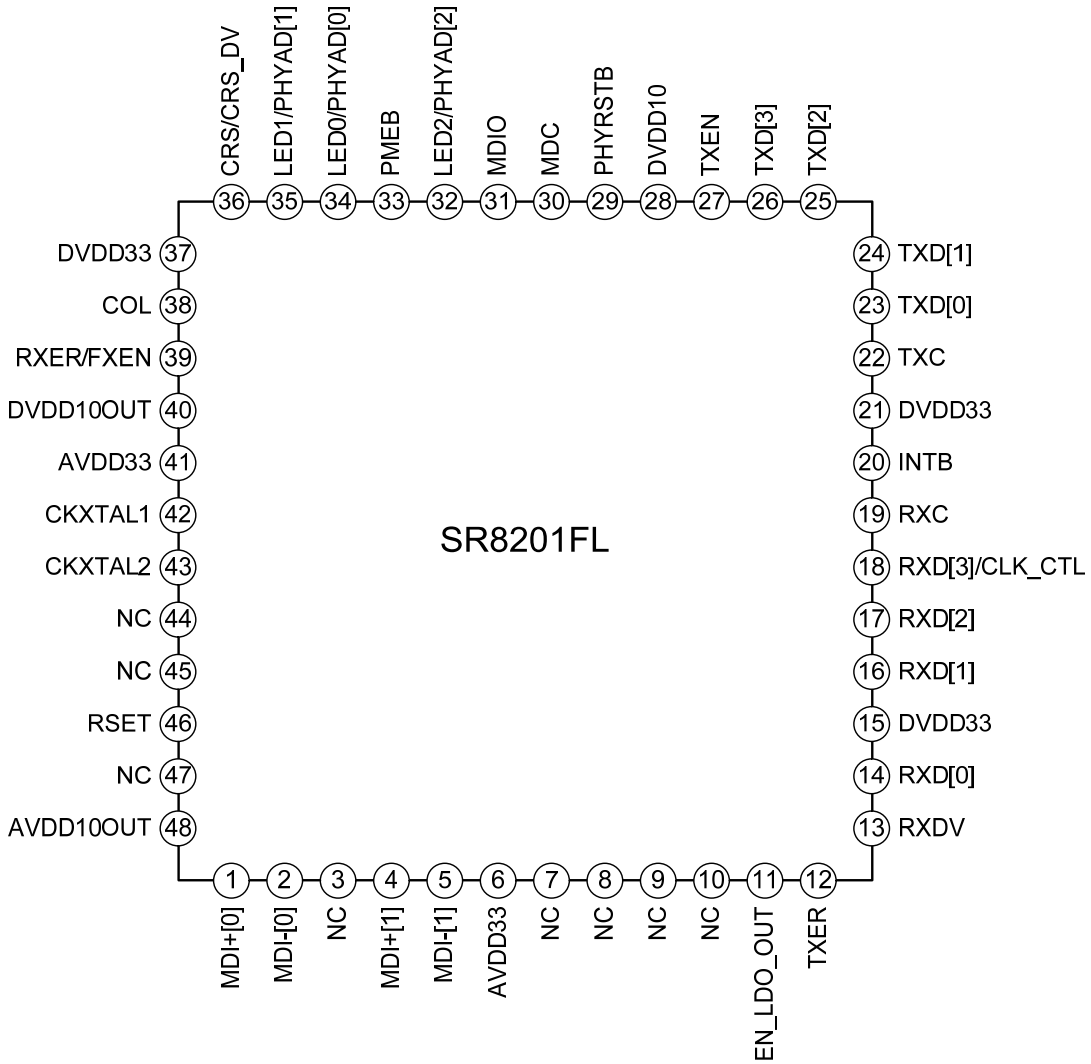


Figure 5. SR8201FL LQFP-48 Pin Assignment

Pin Descriptions

1. MII Interface

Table 1. MII Interface

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	Symbol	Type	Description
15	22	22	TXC	O/PD	Transmit Clock. This pin provides a continuous clock as a timing reference for TXD [3:0] and TXEN signals. TXC is 25MHz in 100Mbps mode and 2.5MHz in 10Mbps mode.
20	27	27	TXEN	I/PD	Transmit Enable. The input signal indicates the presence of valid nibble data on TXD [3:0]. An internal weakly pulled low resistor prevents the bus floating.
-	12	12	TXER	I/PD	Transmit Error.
16 17 18 19	23 24 25 26	23 24 25 26	TX[0] TXD[1] TXD[2] TXD[3]	I/PD I/PD I/PD I/PD	Transmit Data. The MAC will source TXD [0:3] synchronous with TXC when TXEN is asserted. An internal weakly pulled low resistor prevents the bus floating.
13	19	19	RXC	O/PD	Receive Clock. This pin provides a continuous clock reference for RXDV and RXD [0:3] signals. RXC is 25MHz in 100Mbps mode and 2.5MHz in 10Mbps mode.
27	38	38	COL	O/PD	Collision Detect. COL is asserted high when a collision is detected on the media.
26	36	36	CRS/ CRS_DV	O/PD	Carrier Sense. This pin's signal is asserted high if the media is not in Idle state.
8	13	13	RXDV	LI/O/PD	Receive Data Valid. This pin's signal is asserted high when received data is present on the RXD[3:0] lines. The signal is de-asserted at the end of the packet. The signal is valid on the rising edge of the RXC. This pin should be pulled low when operating in MII mode. 0: MII mode 1: RMII mode An internal weakly pulled low resistor sets this to the default of MII mode. It is possible to use an external 4.7KΩ pulled high resistor to enable RMII mode. After power on, the pin operates as the Receive Data Valid pin.

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	Symbol	Type	Description
9 10 - 11	14 16 17 -	14 16 17 -	RXD[0] RXD[1] RXD[2] RXD[2]/ INTB	O/PD LI/O/PD O/PD O/PD	Receive Data. These are the four parallel receive data lines aligned on the nibble boundaries driven synchronously to the RXC for reception by the external physical unit (PHY). Note 1: An internal weakly pulled low resistor sets RXD[1] to the LED function (default). Use an external 4.7KΩ pulled high resistor to enable the WOL function for the SR8201F. Note 2: The SR8201F Pin11 is named RXD[2]/INTB. When in RMII mode, this pin is used for the interrupt function. See Table 9. Reset and Other Pins, page 12 for INTB descriptions.
12	18	18	RXD[3]/ CLK_CTL	LI/O/PD	Receive Data. This is the parallel receive data line aligned on the nibble boundaries driven synchronously to the RXC for reception by the external physical unit (PHY). RXD[3]/CLK_CTL pin is the Hardware strap in RMII Mode. 1: REF_CLK input mode 0: REF_CLK output mode Note: An internal weakly pulled low resistor sets RXD[3]/CLK_CTL to REF_CLK output mode (default).
28	39	39	RXER/ FXEN	LI/O/PD	Receive Error. If a 5B decode error occurs, such as invalid /J/K/, invalid /T/R/, or invalid symbol, this pin will go high. Fiber/UTP Enable. This pin's status is latched at power on reset to determine the media mode to operate in. 1: Fiber mode 0: UTP mode An internal weakly pulled low resistor sets this to the default of UTP mode. It is possible to use an external 4.7KΩ pulled high resistor to enable fiber mode. After power on, the pin operates as the Receive Error pin.

2. RMII Interface

Table 2. RMII Interface

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	Symbol	Type	Description
15	22	22	TXC	IO/PD	Synchronous 50MHz Clock Reference for Receive, Transmit, and Control Interface. The direction is decided by Page 7, Register 16. The default direction is reference clock output mode if RXD[3]/CLK_CTL pin floating.
26	36	36	CRS/ CRS_DV	O/PD	Carrier Sense/Receive Data Valid. CRS_DV shall be asserted by the PHY when the receive medium is non-idle.
20	27	27	TXEN	I/PD	Transmit Enable.
16, 17	23, 24	23, 24	TXD[0:1]	I/PD	Transmit Data.

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	Symbol	Type	Description
9, 10	14, 16	14, 16	RXD[0:1]	O/PD	Receive Data.
28	39	39	RXER/ FXEN	LI/O/PD	Receive Error. RX_ER is a required output of the PHY, but is an optional input for the MAC.

3. Serial Management Interface

Table 3. Serial Management Interface

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	Symbol	Type	Description
22	30	30	MDC	I/PU	Management Data Clock. This pin provides a clock synchronous to MDIO, which may be asynchronous to the transmit TXC and receive RXC clocks. The clock rate can be up to 2.5MHz. Use an internal weakly pulled high resistor to prevent the bus floating.
23	31	31	MDIO	IO/PU	Management Data Input/Output. This pin provides the bi-directional signal used to transfer management information.

4. Clock Interface

Table 4. Clock Interface

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	Symbol	Type	Description
32	43	43	CKXTAL2	IO	25MHz Crystal Output. This pin provides the 25MHz crystal output. If an external 25MHz/50MHz oscillator or clock is used, connect CKXTAL2 to the oscillator or clock output (Oscillator Requirements, page 51).
31	42	42	CKXTAL1	I	25MHz Crystal Input. This pin provides the 25MHz crystal input. Must be shorted to GND when an external 25MHz/50MHz oscillator or clock drives CKXTAL2.

5. 10M/100M Network Interface

Table 5. 10M/100M Network Interface

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	Symbol	Type	Description
3 4	1 2	1 2	MDI+[0] MDI-[0]	IO	Transmit Output. Differential transmit output pair shared by 100Base-TX, 100Base-FX, and 10Base-T modes. When configured as 100Base-TX, output is an MLT-3 encoded waveform. When configured as 100Base-FX, the output is pseudo- ECL level.
5 6	4 5	4 5	MDI+[1] MDI-[1]	IO	Receive Input. Differential receive input pair shared by 100Base-TX, 100Base-FX, and 10Base-T modes.

6. Transmit Bias Interface

Table 6. Transmit Bias Interface

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	Symbol	Type	Description
1	46	1	RSET	I	Transmit Bias Resistor Connection. This pin should be pulled to GND by a 2.49KΩ (1%) resistor to define driving current for the transmit DAC.

7. Device Configuration Interface

Table 7. Device Configuration Interface

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	Symbol	Type	Description
8	13	13	RXDV	LI/O/PD	Receive Data Valid. This pin's signal is asserted high when received data is present on the RXD [3:0] lines. The signal is de-asserted at the end of the packet. The signal is valid on the rising edge of the RXC. This pin should be pulled low when operating in MII mode. 0: MII mode 1: RMII mode An internal weakly pulled low resistor sets this to the default of MII mode. It is possible to use an external 4.7KΩ pulled high resistor to enable RMII mode. After power on, the pin operates as the Receive Data Valid pin.
10	16	16	RXD[1]	LI/O/PD	An internal weakly pulled low resistor sets RXD[1] to the LED function (default). Use an external 4.7KΩ pulled high resistor to enable the WOL function for the SR8201F.
12	18	18	RXD[3]/ CLK_CTL	LI/O/PD	Receive Data. This is the parallel receive data line aligned on the nibble boundaries driven synchronously to the RXC for reception by the external physical unit (PHY). RXD [3]/CLK_CTL pin is the Hardware strap in RMII Mode. 1: REF_CLK input mode 0: REF_CLK output mode Note: An internal weakly pulled low resistor sets RXD[3]/CLK_CTL to REF_CLK output mode (default).
28	39	39	RXER/ FXEN	LI/O/PD	Fiber/UTP Interface. This pin's status is latched at power on reset to determine the media mode to operate in. 1: Fiber mode 0: UTP mode An internal weakly pulled low resistor sets this to the default of UTP mode. It is possible to use an external 4.7KΩ pulled high resistor to enable fiber mode.

<table>
<tr><th>Pin No (8201F)</th><th>Pin No (8201FL)</th><th>Pin No (8201FN)</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>-</td><td>34</td><td>34</td><td>LED0/
PHYAD[0]</td><td>LI/O/PU
LI/O/PU</td><td>PHY Address and Customized LED Settings. The default available PHY addresses are: SR8201F: 00000~00011.
SR8201FL:
00100~00111 (when PMEB pin is pulled high)
00000~00011 (when PMEB pin is pulled low)
SR8201FN: 00000~00111.
Traditional LED Function Selection
<table>
<tr><td>LED _Sel</td><td>00</td><td>01</td><td>10</td><td>11</td></tr>
<tr><td>LED0</td><td>ACT_{ALL}</td><td>$Link_{ALL}$/ ACT_{ALL}</td><td>$Link_{10}$ / ACT_{ALL}</td><td>$LINK_{10}$ /ACT_{10}</td></tr>
<tr><td>LED1</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$/ ACT_{100}</td></tr>
<tr><td>LED2</td><td>Reserved</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
</table>
Note 1: For Customized LED Settings, see section 7.17, page 22.
Note 2: LED_Sel default is 11. Refer to section 7.19, page 23.

An internal weakly pulled low resistor sets RXD[1] to the LED function for SR8201F (default).
Use an external 4.7KΩ pulled high resistor to enable the WOL function for SR8201F.
Traditional LED Function Selection for the SR8201F with WOL Enabled
With the SR8201F WOL function enabled, the PHY address must be 00001 or 00011.
<table>
<tr><td>LED _Sel</td><td>00</td><td>01</td><td>10</td><td>11</td></tr>
<tr><td>LED1</td><td>LINK100</td><td>LINK100</td><td>LINK100</td><td>LINK100/ ACT100</td></tr>
</table></td></tr>
<tr><td>24</td><td>-</td><td>-</td><td>LED0/
PHYAD[0]/
PMEB</td><td>LI/O/PD
LI/O/PD</td><td></td></tr>
<tr><td>25</td><td>35</td><td>35</td><td>LED1/
PHYAD[1]</td><td></td><td></td></tr>
<tr><td>-</td><td>-</td><td>32</td><td>LED2/
PHYAD[2]</td><td></td><td></td></tr>
</table>

8. Power and Ground Pins

Table 8. Power and Ground Pins

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	Symbol	Type	Description
7, 30	6, 41	6, 41	AVDD33	P	3.3V Analog Power Input. 3.3V power supply for analog circuit; should be well decoupled.
14	15, 21, 37	15, 21, 37	DVDD33	P	3.3V Digital Power Input. 3.3V power supply for digital circuit.
-	28	28	DVDD10	P	1.1V Digital Power.
2	48	48	AVDD10OUT	O	Power Output. Be sure to connect a 0.1μF ceramic capacitor for decoupling purposes. The connection method is outlined in section 8.8 3.3V Power Supply and Voltage Conversion Circuit, page 37.

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	Symbol	Type	Description
29	40	40	DVDD10 OUT	O	Power Output. Be sure to connect a 0.1μF ceramic capacitor for decoupling purposes. The connection method is outlined in section 8.8 3.3V Power Supply and Voltage Conversion Circuit, page 37.
E-PAD	7, 20,33,47	E-PAD	GND	P	Ground. Should be connected to a larger GND plane. Exposed Pad (E-Pad) is Analog and Digital Ground.

9. Reset and Other Pins

Table 9. Reset and Other Pins

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	Symbol	Type	Description
7, 30	6, 41	21	PHYRSTB	I/HZ	RESETB. Set low to reset the chip. For a complete reset, this pin must be asserted low for at least 10ms. Note: When the WOL function is enabled, keep the pin high (SR8201FN only).
14	15, 21, 37	-	INTB	O/OD	Interrupt. Set low if link status changed, duplex changed, or auto negotiation failed. Active Low. This pin is an open-drain design, and for default value should be pulled high by an external 4.7KΩ. If not used, keep floating.
-	28	11	RXD[2]/INTB	O/PD	Interrupt. Set low if link status changed, duplex changed, or auto negotiation failed. Active Low. This pin is an open-drain design, and for default value should be pulled high by an external 4.7KΩ. If not used, keep floating. Note: This pin is used for the interrupt function only when in the RMII mode.
2	48	24	PMEB	O/OD	Power Management Enable. Set low if received a magic packet or wake up frame; active low.

10. NC (Not Connected) Pins

Table 10. NC (Not Connected) Pins

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	Symbol	Type	Description
-	3,8,9,11, 44,45	3, 7, 8, 9, 10,44, 45, 47	NC	-	Not Connected.

I=Input, O=Output, IO= Bi-directional input and output, PD=Internal Pull down, PU=Internal Pull up,

LI=Latched Input during Power up or Reset, OD= Open Drain Output, P=Power

Register Descriptions

This section describes the functions and usage of the registers available in this file. In this section the following abbreviations are used.

RW:	Read/Write	RW/LI:	Read/Write/Latch In
RO:	Read Only	RW/SC:	Read/Write/Self-Clearing
RC:	Read Clear	SC:	Self-Clear

Table 11. Register 0 Basic Mode Control Register

Address	Name	Description	Mode	Default
0:15	Reset	This bit sets the status and control registers of the PHY in the default state. This bit is self-clearing. 1: Software reset 0: Normal operation Register 0 and register 1 will return to default values after a software reset (set Bit15 to 1). This action may change the internal PHY state and the state of the physical link associated with the PHY.	RW/ SC	0
0:14	Loopback	This bit enables loopback of transmit data nibbles TXD3:0 to the receive data path. 1: Enable loopback 0: Normal operation	RW	0
0:13	Speed Selection	This bit sets the network speed. 1: 100Mbps 0: 10Mbps After completing auto negotiation, this bit will reflect the speed status. 1: 100Base-T 0: 10Base-T When 100Base-FX mode is enabled, this bit=1 and is read only.	RW	1
0:12	Auto Negotiation Enable	This bit enables/disables the NWay auto-negotiation function. 1: Enable auto-negotiation; bits 0:13 and 0:8 will be ignored 0: Disable auto-negotiation; bits 0:13 and 0:8 will determine the link speed and the data transfer mode, respectively When 100Base-FX mode is enabled, this bit=0 and is read only.	RW	1

Address	Name	Description	Mode	Default
0:10	Isolate	1: Electrically isolate the PHY from MII/GMII/RGMII/RSGMII. PHY is still able to respond to MDC/MDIO. 0: Normal operation	RW	0
0:11	Power Down	This bit turns down the power of the PHY chip, including the internal crystal oscillator circuit. The MDC, MDIO is still alive for accessing the MAC. 1: Power down 0: Normal operation	RW	0
0:9	Restart Auto Negotiation	This bit allows the NWay auto-negotiation function to be reset. 1: Re-start auto-negotiation 0: Normal operation	RW/ SC	0
0:8	Duplex Mode	This bit sets the duplex mode if auto-negotiation is disabled (bit 0:12=0). 1: Full duplex0: Half duplex After completing auto-negotiation, this bit will reflect the duplex status. 1: Full duplex0: Half duplex	RW	1
0:7	Collision Test	Collision Test. 1: Collision test enabled 0: Normal operation When set, this bit will cause the COL signal to be asserted in response to the TXEN assertion within 512-bit times. The COL signal will be de-asserted within 4-bit times in response to the TXEN de-assertion.	RW	0
0:6~0	Reserved	Reserved.	-	-

Table 12. Register 1 Basic Mode Status Register

Address	Name	Description	Mode	Default
1:15	100Base-T4	1: Enable 100Base-T4 support 0: Suppress 100Base-T4 support	RO	0
1:14	100Base_TX_FD	1: Enable 100Base-TX full duplex support 0: Suppress 100Base-TX full duplex support	RO	1
1:13	100Base_TX_HD	1: Enable 100Base-TX half duplex support 0: Suppress 100Base-TX half duplex support	RO	1

Address	Name	Description	Mode	Default
1:12	10Base_T_FD	1: Enable 10Base-T full duplex support 0: Suppress 10Base-T full duplex support	RO	1
1:11	10_Base_T_HD	1: Enable 10Base-T half duplex support 0: Suppress 10Base-T half duplex support	RO	1
1:10~7	Reserved	Reserved.	-	-
1:6	MF Preamble Suppression	The SR8201F/FL/FN will accept management frames with preamble suppressed. A minimum of 32 preamble bits are required for the first management interface read/write transaction after reset. One idle bit is required between any two management transactions as per IEEE 802.3u specifications.	RO	1
1:5	Auto Negotiation Complete	1: Auto-negotiation process completed 0: Auto-negotiation process not completed	RO	0
1:4	Remote Fault	1: Remote fault condition detected (cleared on read) 0: No remote fault condition detected When in 100Base-FX mode, this bit means an in-band signal Far-End-Fault has been detected (see 8.10 Far End Fault Indication, page 37).	RC	0
1:3	Auto-Negotiation Ability	1: PHY is able to perform auto-negotiation 0: PHY is not able to perform auto-negotiation	RO	1
1:2	Link Status	1: Valid link established 0: No valid link established This bit indicates whether the link was lost since the last read. For the current link status, read this register twice.	RO	0
1:1	Jabber Detect	1: Jabber condition detected 0: No jabber condition detected	RO	0
1:0	Extended Capability	1: Extended register capable (permanently=1) 0: Not extended register capable	RO	1

Table 13. Register 2 PHY Identifier Register 1

Address	Name	Description	Mode	Default
2:15~0	OUI	Composed of the 6th to 21st bits of the Organizationally Unique Identifier (OUI), respectively.	RO	001Ch

Table 14. Register 3 PHY Identifier Register 2

Address	Name	Description	Mode	Default
3:15~10	OUI_LSB	Assigned to the 0 through 5th bits of the OUI.	RO	110010
3:9~4	Model Number	Model Number	RO	000001
3:3~0	Revision Number	Revision Number	RO	0110

Table 15. Register 4 Auto-Negotiation Advertisement Register (ANAR)

This register contains the advertised abilities of this device as they will be transmitted to its link partner during auto-negotiation.

Address	Name	Description	Mode	Default
4:15	Next Page	Next Page Bit. 0: Transmitting the primary capability data page 1: Transmitting the protocol specific data page	RW	0
4:14	Acknowledge	1: Acknowledge reception of link partner capability data word 0: Do not acknowledge reception	RO	0
4:13	Remote Fault	1: Advertise remote fault detection capability 0: Do not advertise remote fault detection capability	RW	0
4:12	Reserved	Reserved.	-	-
4:11	Asymmetric PAUSE	1: Advertise asymmetric pause support 0: No support of asymmetric pause	RW	0
4:10	Pause	Reserved.	RW	0
4:9	100Base-T4	1: 100Base-T4 is supported by local node 0: 100Base-T4 not supported by local node	RO	0
4:8	100Base-TX-FD	1: 100Base-TX full duplex is supported by local node 0: 100Base-TX full duplex not supported by local node	RW	1
4:7	100Base-TX	1: 100Base-TX is supported by local node 0: 100Base-TX not supported by local node	RW	1
4:6	10Base-T-FD	1: 10Base-T full duplex supported by local node 0: 10Base-T full duplex not supported by local node	RW	1
4:5	10Base-T	1: 10Base-T is supported by local node 0: 10Base-T not supported by local node	RW	1
4:4~0	Selector Field	Binary Encoded Selector Supported by This Node. Currently only CSMA/CD 00001 is specified. No other protocols are supported.	RO	00001

Table 16. Register 5 Auto-Negotiation Link Partner Ability Register (ANLPAR)

This register contains the advertised abilities of the Link Partner as received during auto-negotiation. The content changes after a successful auto-negotiation if Next-pages are supported.

Address	Name	Description	Mode	Default
5:15	Next Page	Next Page Bit. 0: Transmitting the primary capability data page 1: Transmitting the protocol specific data page	RO	0
5:14	Acknowledge	1: Link partner acknowledges reception of local node's capability data word 0: No acknowledgement	RO	0
5:13	Remote Fault	1: Link partner is indicating a remote fault 0: Link partner is not indicating a remote fault	RO	0
5:12	Reserved	Reserved.	-	-
5:11	Asymmetric Pause	1: Asymmetric Flow control supported by Link Partner 0: No Asymmetric flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability.	RO	0
5:10	Pause	1: Flow control supported by Link Partner 0: No flow control supported by Link Partner When auto-negotiation is enabled, this bit reflects Link Partner ability (read only).	RO	0
5:9	100Base-T4	1: 100Base-T4 is supported by link partner 0: 100Base-T4 not supported by link partner	RO	0
5:8	100Base-TX-FD	1: 100Base-TX full duplex is supported by link partner 0: 100Base-TX full duplex not supported by link partner	RO	0
5:7	100Base-TX	1: 100Base-TX is supported by link partner 0: 100Base-TX not supported by link partner This bit will also be set if the link in 100Base-TX is established by parallel detection.	RO	0
5:6	10Base-T-FD	1: 10Base-T full duplex is supported by link partner 0: 10Base-T full duplex not supported by link partner	RO	0
5:5	10Base-T	1: 10Base-T is supported by link partner 0: 10Base-T not supported by link partner This bit will also be set if the link in 10Base-T is established by parallel detection.	RO	0
5:4~0	Selector Field	Link Partner's Binary Encoded Node Selector. Currently only CSMA/CD 00001 is specified.	RO	00001

Table 17. Register 6 Auto-Negotiation Expansion Register (ANER)

This register contains additional status for NWay auto-negotiation.

Address	Name	Description	Mode	Default
6:15~5	Reserved	Reserved.	-	-
6:4	Parallel Detection Fault	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	RC	0
6:3	Link Partner Next Page Ability	1: Link Partner is Next Page able 0: Link Partner is not Next Page able	RO	0
6:2	Local Next Page Ability	1: Next Page is able 0: Not Next Page able	RO	0
6:1	Page Received	1: A New Page has been received 0: A New Page has not been received	RC	0
6:0	Link Partner Auto-Negotiation Ability	If Auto-Negotiation is Enabled, This Bit Means: 1: Link Partner is Auto-Negotiation able 0: Link Partner is not Auto-Negotiation able	RO	0

Table 18. Page 0 Register 13 MACR (MMD Access Control Register; Address 0x0D)

Bits	Name	RW	Default	Description
13.15:14	Function	WO	0	00: Address 01: Data; no post increment 10: Data; post increment on reads and writes 11: Data; post increment on writes only
13.13:5	Reserved	RO	000000000	Reserved.
13.4:0	DEVAD	WO	0	Device Address.

Note 1: Used in conjunction with the MAADR (Register 14) to provide access to the MMD address space.

Note 2: If the access of MAADR is for address (Function=00) then it is directed to the address register within the MMD associated with the value in the DEVAD field.

Note 3: If the access of MAADR is for data (Function!=00) then both the DEVAD field and the MMD address register direct the MAADR data accesses to the appropriate registers within the MMD.

Table 19. Page 0 Register 14 MAADR (MMD Access Address Data Register; Address 0x0E)

Bits	Name	RW	Default	Description
14.15:0	Address Data	RW	0x0000	13.15:14=00 **à** MMD DEVAD's address register 13.15:14=01, 10, or 11 **à** MMD DEVAD's data register as indicated by the contents of its address register

Note: Used in conjunction with the MACR (Register 13) to provide access to the MMD address space.

Table 20. Register 24 Power Saving Mode Register (PSMR)

Address	Name	Description	Mode	Default
15	Enpwrsave	Enable Power Saving Mode. The bit will return to default value by software reset.	RW	1
14~0	Reserved	Reserved	-	-

Note: If the REF_CLK output is needed in RMII output mode, LDPS (Link Down Power Saving) must be disabled (see Table 43, page 36).

Table 21. Register 28 Fiber Mode and Loopback Register

Address	Name	Description	Mode	Default
28:15~6	Reserved	Reserved.	-	-
28:5	Fxmode	Enable Fiber Mode.	RW	0
28:4~3	Reserved	Reserved.	-	-
28:2	En_autoMDIX	Enable Auto MDIX Function.	RW	1
28:1	Force_MDI	Force MDI/MDIX Mode. If enable auto MDIX function is disabled: 1: Force MDI 0: Force MDIX	RW	1
28:0	Reserved	Reserved.	-	-

Table 22. Register 30 Interrupt Indicators and SNR Display Register

Address	Name	Description	Mode	Default
30:15	Anerr	Auto-Negotiation Error Interrupt. 1: Enable 0: Disable	RC	0
30:14	Spdchg	Speed Mode Change Interrupt. 1: Enable 0: Disable	RC	0
30:13	Duplexchg	Duplex Mode Change Interrupt. 1: Enable 0: Disable	RC	0
30:12	Reserved	Reserved.	-	-
30:11	Linkstatuschg	Link Status Change Interrupt. 1: Enable 0: Disable	RC	0
30:10~4	Reserved	Reserved.	-	-
30:3~0	SNR_O	These 4-Bits Show the Signal to Noise Ratio Value.	RO	0000

Table 23. Register 31 Page Select Register

Address	Name	Description	Mode	Default
31:15~8	Reserved	Reserved for Internal Testing.	-	-
31:7~0	PAGE SEL	Select Page Address: 00000000~11111111.	RW	00000000

Table 24. Page 4 Register 16 EEE Capability Enable Register

Address	Name	Description	Mode	Default
16:15~14	Reserved	Reserved.	-	-
16:13	EEE_10_cap	Enable EEE 10M Capability.	RW	1
16:12	EEE_nway_en	Enable Next Page Exchange in NWay for EEE 100M.	RW/ EFUS	1
16:11~10	Reserved	Reserved.	-	-
16:9	Tx_quiet_en	Enable Ability to Turn Off Power 100TX when TX in Quiet State. This bit is recommended to be set to 1 when EEE is enabled.	RW/ EFUS	1
16:8	Rx_quiet_en	Enable Ability to Turn Off Power 100RX when RX in Quiet state. This bit is recommended to be set to 1 when EEE is enabled.	RW/ EFUS	1
16:7:0	Reserved	Reserved.	-	-

Table 25. Page 4 Register 21 EEE Capability Register

Address	Name	Description	Mode	Default
21:15~13	Reserved	Reserved.	-	-
21:12	Rg_dis_ldvt	Set to 1 to Disable the Line Driver of the Analog Circuit.	RW	0
21:11~1	Reserved	Reserved.	-	-
21:0	EEE_100_cap	NWay Result to Indicate Link Partner Supports EEE 100M.	RO	0

Table 26. Page 7 Register 16 RMII Mode Setting Register (RMSR)

Address	Name	Description	Mode	Default
16:15~13	Reserved	Reserved.	-	-
16:12	Rg_rmii_clkdir	This Bit Sets the Type of TXC in RMII Mode. 0: Output 1: Input	RW/LI	0
16:11~8	Rg_rmii_tx_offset	Adjust RMII TX Interface Timing.	RW/EFUS	1111
16:7~4	Rg_rmii_rx_offset	Adjust RMII RX Interface Timing.	RW/EFUS	1111
16:3	Reserved	Reserved.	RW/LI	0

Address	Name	Description	Mode	Default

16:2	Rg_rmii_rxdv_sel	0: CRS/CRS_DV pin is CRS_DV signal 1: CRS/CRS_DV pin is RXDV signal	RW/EFUS	0
16:1	Rg_rmii_rxdsel	0: RMII data only 1: RMII data with SSD Error	RW/EFUS	1
16:0	Reserved	Reserved.	-	-

Table 27. Page 7 Register 17 Customized LEDs Setting Register

This register is for setting customized LEDs. Table below shows the customized LED matrix table.

Table27.1 Customized LED Matrix Table

	LINK		ACT
	10M	100M	
LED0	Bit0	Bit1	Bit3
LED1	Bit4	Bit5	Bit7
LED2	Bit8	Bit9	Bit11

LED Pin	ACT=0	ACT=1
LINK=0	Floating	All Speed ACT
LINK>0	Selected Speed LINK	Selected Speed LINK+ACT

Note: The SR8201F/FL only supports LED0 and LED1. The SR8201FN supports LED0, LED1, and LED2.

Table 27.2. Page7 Register 17 Customized LEDs Setting Register

Address	Name	Description	Mode	Default
17:15~12	Reserved	Reserved.	-	-
17:11~8	LED_sel2	Customized LED2 Setting. Set Bit3 (Page7 Register 19; Table 30, page 24) to 1 to enable customized LED function.	RW/ EFUS	0000
17:7~4	LED_sel1	Customized LED1 Setting. Set Bit3 (Page7 Register 19; Table 30, page 24) to 1 to enable customized LED function.	RW/ EFUS	0000
17:3~0	LED_sel0	Customized LED0 Setting. Set Bit3 (Page7 Register 19; Table 30, page 24) to 1 to enable customized LED function.	RW/ EFUS	0000

Table 28. Page 7 Register 18 EEE LEDs Enable Register

Address	Name	Description	Mode	Default
18:15~3	Reserved	Reserved.	-	-
18:2	EEE_LED_en2	Enable LED2 in EEE/LPI Mode.	RW	0
18:1	EEE_LED_en1	Enable LED1 in EEE/LPI Mode.	RW	0
18:0	EEE_LED_en0	Enable LED0 in EEE/LPI Mode.	RW	0

Table 29. Page 7 Register 19 Interrupt, WOL Enable, and LEDs Function Registers

<table>
<tr><th>Address</th><th>Name</th><th>Description</th><th>Mode</th><th>Default</th></tr>
<tr><td>19:15~14</td><td>Reserved</td><td>Reserved.</td><td>-</td><td>-</td></tr>
<tr><td>19:13</td><td>Int_linkchg</td><td>Link Change Interrupt Mask.
1: Interrupt pin Enable
0: Interrupt pin Disable
This bit set to 0 only masks the link change interrupt event in the INTB pin. Reg30 Bit11 always reflects the link change interrupt behavior (see register 30, page 21).</td><td>RW</td><td>0</td></tr>
<tr><td>19:12</td><td>Int_dupchg</td><td>Duplex Change Interrupt Mask.
1: Interrupt pin Enable
0: Interrupt pin Disable
This bit set to 0 only masks the duplex change interrupt event in the INTB pin. Reg30 Bit13 always reflects the duplex change interrupt behavior (see register 30, page 21).</td><td>RW</td><td>0</td></tr>
<tr><td>19:11</td><td>Int_anerr</td><td>NWay Error Interrupt Mask.
1: Interrupt pin Enable
0: Interrupt pin Disable
This bit set to 0 only masks the NWay Error interrupt event in the INTB pin.Reg30 Bit15 always reflects the NWay Error interrupt behavior (see register 30, page 21).</td><td>RW</td><td>0</td></tr>
<tr><td>19:10</td><td>Rg_led0_wol_sel</td><td>LED and Wake-On-LAN Function Selection (SR8201F Only).
1: Wake-On-LAN Function Enable
0: LED Function Enable
An internal weakly pulled low resistor sets RXD[1] to the LED function (default). Use an external 4.7KΩ pulled high resistor to enable the WOL function for the SR8201F.</td><td>RW/LI</td><td>0</td></tr>
<tr><td>19:9~6</td><td>Reserved</td><td>Reserved.</td><td>-</td><td>-</td></tr>
<tr><td>19:5~4</td><td>LED_sel[1:0]</td><td>Traditional LED Function Selection.
<table>
<tr><td>LED_sel</td><td>LED0</td><td>LED1</td><td>LED2</td></tr>
<tr><td>00</td><td>ACT_{ALL}</td><td>$Link_{100}$</td><td>Reserved</td></tr>
<tr><td>01</td><td>$Link_{ALL}/ACT_{ALL}$</td><td>$Link_{100}$</td><td>Reserved</td></tr>
<tr><td>10</td><td>$Link_{10}/ACT_{ALL}$</td><td>$Link_{100}$</td><td>Reserved</td></tr>
<tr><td>11</td><td>$Link_{10}/ACT_{10}$</td><td>$Link_{100}/ACT_{100}$</td><td>Reserved</td></tr>
</table></td><td>RW/
EFUS</td><td>11</td></tr>
<tr><td>19:3</td><td>Customized_LED</td><td>Customized LED Enable.
1: Customized LED function enable
0: Customized LED function disable
See the section 4.7 Customized LED, page 33 for detail.</td><td>RW/
EFUS</td><td>0</td></tr>
<tr><td>19:2~1</td><td>Reserved</td><td>Reserved.</td><td>-</td><td>-</td></tr>
<tr><td>19:0</td><td>En10mlpi</td><td>Enable 10M LPI LED Function.</td><td>RW</td><td>0</td></tr>
</table>

Table 30. Page 7 Register 20 MII TX Isolate Register

Address	Name	Description	Mode	Default
20:15	Rg_tx_isolate_en	Isolate MII TX Path Signals when TX Idle.	RW	0
20:14~0	Reserved	Reserved.	-	-

Table 31. Page 7 Register 24 Spread Spectrum Clock Register

Address	Name	Description	Mode	Default
24:15~1	Reserved	Reserved.	-	-
24:0	Rg_dis_ssc	0: SSC function is enabled 1: SSC function is disabled	RW	0

Table 32. MMD Register Mapping and Definition

Note: MMD registers are placed at Page 0 Register 13 and Register 14.

Device	Offset	Access	Name	Description
3	0	RW	EEEPC1R	EEE PCS Control 1 Register
3	1	RO/RO, LH	EEEPS1R	EEE PCS Status Control 1 Register
3	20	RO	EEECR	EEE Capability Register
3	22	RC	EEEWER	EEE Wake Error Register
7	60	RW	EEEAR	EEE Advertisement Register
7	61	RO	EEELPAR	EEE Link Partner Ability Register

Note: LH: Latching High

Table 33. EEEPC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)

Bits	Name	RW	Default	Description
3:0:15~11	Reserved	RW	0	Reserved.
3:0:10	Clock Stop Enable	RW	0	1: PHY stops RXC in LPI 0: RXC not stoppable
3:0:9~0	Reserved	RW	0	Reserved.

Table 34. EEEPS1R (PCS Status 1 Register, MMD Device 3, Address 0x01)

Bits	Name	RW	Default	Description
3:1:15~12	Reserved	RO	0	Reserved.
3:1:11	TX LPI Received	RO, LH	0	1: TX PCS has received LPI 0: LPI not received
3:1:10	RX LPI Received	RO, LH	0	1: RX PCS has received LPI 0: LPI not received

Bits	Name	RW	Default	Description
3:1:9	TX LPI Indication	RO	0	1: TX PCS is currently receiving LPI 0: TX PCS is not currently receiving LPI
3:1:8	RX LPI Indication	RO	0	1: RX PCS is currently receiving LPI 0: RX PCS is not currently receiving LPI
3:1:7	Reserved	RO	0	Reserved.
3:1:6	Clock Stop Capable	RO	1	1: MAC stops TXC in LPI 0: TXC not stoppable
3:1:5~0	Reserved	RO	0	Reserved.

Table 35. EEECR (EEE Capability Register, MMD Device 3; Address 0x14)

Bits	Name	RW	Default	Description
3:20:15~2	Reserved	RO	0	Reserved.
3:20:1	100Base-TX EEE	RO	1	1: EEE is supported for 100Base-TX EEE 0: EEE is not supported for 100Base-TX EEE
3:20:0	Reserved	RO	1	Reserved.

Table 36. EEECR (EEE Capability Register, MMD Device 3; Address 0x14)

Bits	Name	RW	Default	Description
3:22:15~0	EEE Wake Error Counter	RC	0	Used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type.

Table 37. EEEAR (EEE Advertisement Register, MMD Device 7; Address 0x3c)

Bits	Name	RW	Default	Description
7:60:15~3	Reserved	RW	0	Reserved.
7:60:1	100Base-TX EEE	RW	1	Advertise 100Base-TX EEE Capability. 1: Advertise 0: Do not advertise
7:60:0	Reserved	RW	0	Reserved.

Table 38. EEELPAR (EEE Link Partner Ability Register, MMD Device 7; Address 0x3d)

Bits	Name	RW	Default	Description
7:61:15~3	Reserved	RO	0	Reserved.
7:61:1	LP 100Base-TX EEE	RO	0	1: Link Partner is capable of 100Base-TX EEE 0: Link Partner is not capable of 100Base-TX EEE
7:61:0	Reserved	RO	0	Reserved.

Functional Description

The SR8201F/FL/FN PHYceiver is a physical layer device that integrates 10Base-T and 100Base-TX/100Base-FX functions, and some extra power management features. This device supports the following functions:

- MII interface with MDC/MDIO management interface to communicate with the MAC
- IEEE 802.3u clause 28 Auto-Negotiation ability
- Speed, duplex, auto-negotiation ability configurable by hard wire or MDC/MDIO
- Power Down mode support
- 4B/5B transform
- Scrambling/De-scrambling
- NRZ to NRZI, NRZI to MLT-3
- Manchester Encode and Decode for 10Base-T operation
- Clock and Data recovery
- Adaptive Equalization
- Automatic Polarity Correction
- Far End Fault Indication (FEFI) in fiber mode
- Network status LEDs
- Wake-On-LAN (WOL)
- Energy Efficient Ethernet (EEE)
- Spread Spectrum Clock (SSC) for RMII REF_CLK output mode

1. MII and Management Interface

1.1. Data Transition

The MII (Media Independent Interface) is an 18-signal interface (as described in IEEE 802.3u) supplying a standard interface between the PHY and MAC layer.

This interface operates at two frequencies; 25MHz and 2.5MHz, to support 100Mbps/10Mbps bandwidth for both transmit and receive functions.

Transmission

The MAC asserts the TXEN signal. It then changes byte data into 4-bit nibbles and passes them to the PHY via TXD[3:0]. The PHY will sample TXD[3:0] synchronously with TXC – the transmit clock signal supplied by the PHY – during the interval TXEN is asserted.

Reception

The PHY asserts the RXDV signal. It passes the received nibble data RXD[3:0] clocked by RXC. CRS and COL signals are used for collision detection and handling.

In 100Base-TX mode, when the decoded signal in 5B is not IDLE, the CRS signal will assert. When 5B is recognized as IDLE it will be de-asserted. In 10Base-T mode, CRS will assert when the 10M preamble has been confirmed and will be de-asserted when the IDLE pattern has been confirmed.

The RXDV signal will be asserted when decoded 5B are /J/K/ and will be de-asserted if the 5B are /T/R/ or IDLE in 100Mbps mode. In 10Mbps mode, the RXDV signal is the same as the CRS signal.

The RXER (Receive Error) signal will be asserted if any 5B decode errors occur, e.g., an invalid J/K, invalid T/R, or invalid symbol. This pin will go high for one or more clock periods to indicate to the reconciliation sublayer that an error was detected somewhere in the frame.

1.2. Serial Management Interface

The MAC layer device can use the MDC/MDIO management interface to control a maximum of 4 (SR8201F/FL) or 8 (SR8201FN) devices, configured with different PHY addresses (00b to 11b for the SR8201F/FL; 000b to 111b for the SR8201FN). Frames transmitted on the MDC/MDIO Management Interface should have the frame structure shown in table as below.

Table 39. Management Frame Format

	Management Frame Fields							
	Preamble	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Read	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

During a hardware reset, the logic levels of pins 20(PHYAD[0]) and 10(PHYAD[1]) are latched to be set as the PHY address for management communication via the serial interface. The read and write frame structure for the management interface is illustrated in Figure show as below.

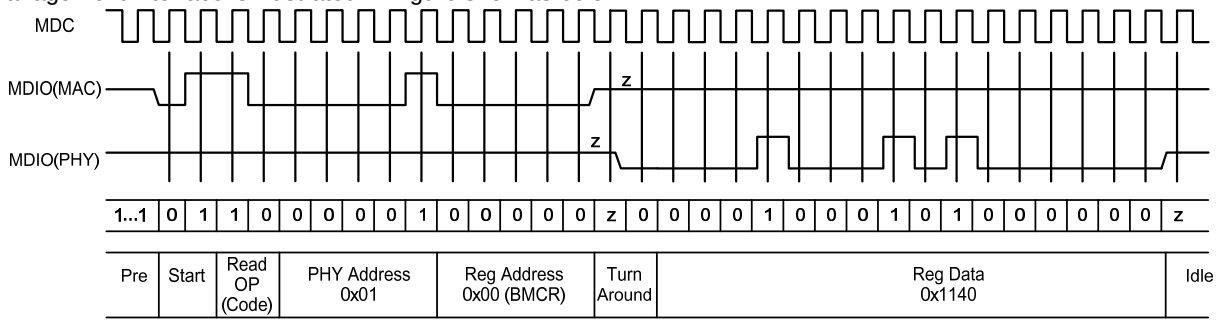


Figure 6. Read Cycle

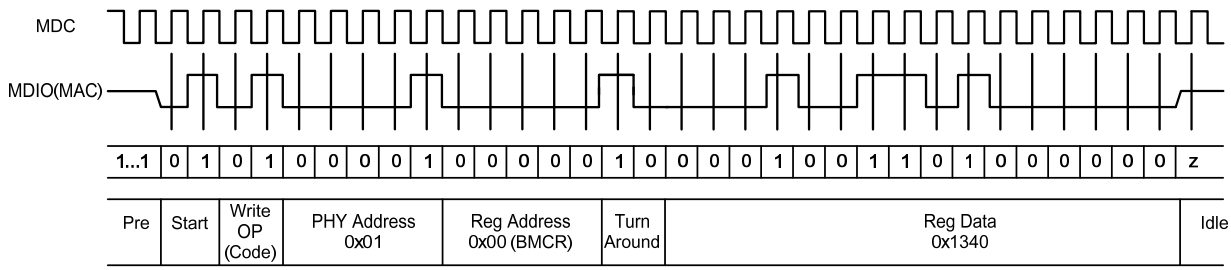


Figure 7. Write Cycle

Table 40. Serial Management

Name	Description
Preamble	32 Contiguous Logical 1's Sent by the MAC on MDIO, along with 32 Corresponding Cycles on MDC. This provides synchronization for the PHY.
ST	Start of Frame. Indicated by a 01 pattern.
OP	Operation Code. Read: 10 Write: 01

Name	Description
PHYAD	PHY Address. Up to 4 PHYs can be connected to one MAC. This 2-bit field selects which PHY the frame is directed to.
REGAD	Register Address. This is a 5-bit field that sets which of the 32 registers of the PHY this operation refers to.
TA	Turnaround. This is a 2-bit-time spacing between the register address and the data field of a frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY remain in a high-impedance state for the first bit time of the turnaround. The PHY drives a zero bit during the second bit time of the turnaround of a read transaction.
DATA	Data. These are the 16 bits of data.
IDLE	Idle Condition. Not truly part of the management frame. This is a high impedance state. Electrically, the PHY's pull-up resistor will pull the MDIO line to a logical '1'.

2. Interrupt

Whenever there is a status change on the media detected by the SR8201F, the correspond interrupt status registers (page0 register14) will be set, and the interrupt pin (LED1/INTB Pin21) will be drived to low to issue an interrupt event. The MAC senses the status change and accesses the page0 register14 through the MDC/MDIO interface in response.

Once these status registers page0 register30 have been read by the MAC through the MDC/MDIO, the INTB is de-asserted. The SR8201FN/FL interrupt function removes the need for continuous polling through the MDC/MDIO management interface.

Note 1: The SR8201F RXD[2]/INTB pin (Pin11) is used for the interrupt function only when in the RMII mode.

Note2: The Interrupt function is disabled by default. To enable this function, refer to Interrupt Enable Function Register

3. Auto-Negotiation and Parallel Detection

The SR8201F supports IEEE 802.3u clause 28 Auto-negotiation for operation with other transceivers supporting auto-negotiation.The SR8201F can auto-detect the link partner's abilities and determine the highest speed/duplex configuration possible between the two devices. If the link partner does not support auto-negotiation, then the SR8201F will enable half-duplex mode and enter parallel detection mode.The SR8201F will default to transmitting FLP (Fast Link Pulse) and wait for the link partner to respond. If the SR8201F receives a FLP, then the auto-negotiation process will continue. If it receives an NLP (Normal Link Pulse), then the SR8201F will change to 10Mbps and half-duplex mode. If it receives a 100Mbps IDLE pattern, it will change to 100Mbps and half-duplex mode.

3.1 Setting the Medium Type and Interface Mode to MAC

Table 41. Setting the Medium Type and Interface Mode to MAC

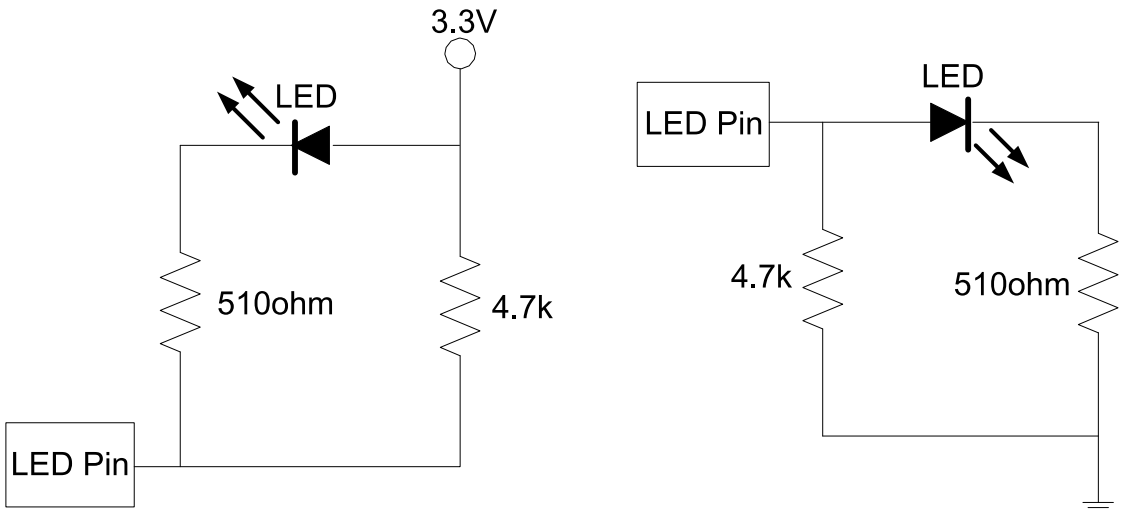
FXEN	RXDV	Operation Mode
H	L	Fiber Mode and MII Mode
H	H	Fiber Mode and RMII Mode
H	X	Fiber Mode and MII Mode
L	L	UTP Mode and MII Mode
L	H	UTP Mode and RMII Mode
L	X	UTP Mode and MII Mode

4. LED Functions

The SR8201FN supports three LED signals, and the SR8201F and SR8201FL support two LED signals, in four configurable operation modes. The following sections describe the various LED actions.

4.1. LED and PHY Address

As the PHYAD[0] strap options share the LED output pins, the external combinations required for strapping and LED usage must be considered in order to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding PHYAD input upon power-up/reset. For example,as Figure (left-side) shows, if a given PHYAD input is resistively pulled high then the corresponding output will be configured as an active low driver. On the right side, we can see that if a given PHYAD input is resistively pulled low then the corresponding output will be configured as an active high driver. The PHY address configuration pins should not be connected to GND or VCC directly, but must be pulled high or low through a resistor (e.g.,4.7KΩ).If no LED indications are needed,the components of the LED path (LED+510Ω) can be removed.



PHY Address[x] = Logical 1
LED Indication = Active low

PHY Address[x]= Logical 0
LED Indication= Active high

Figure 8. LED and PHY Address Configuration

4.2. Link Monitor

The Link Monitor senses link integrity,such as LINK10,LINK100,LINK10/ACT,or LINK100/ACT. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected,the link LED pin is driven high, indicating that no network connection exists.

4.3. RX LED

In 10/100M mode, blinking of the RX LED indicates that receive activity is occurring.

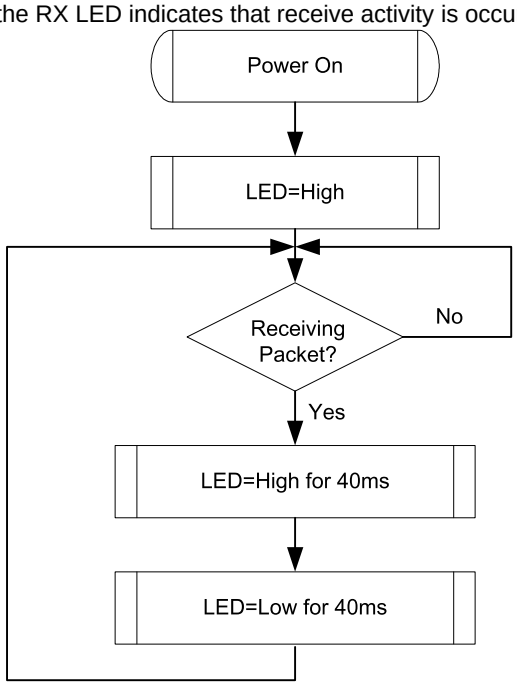


Figure 9. RX LED

4.4. TX LED

In 10/100M mode, blinking of the TX LED indicates that transmit activity is occurring.

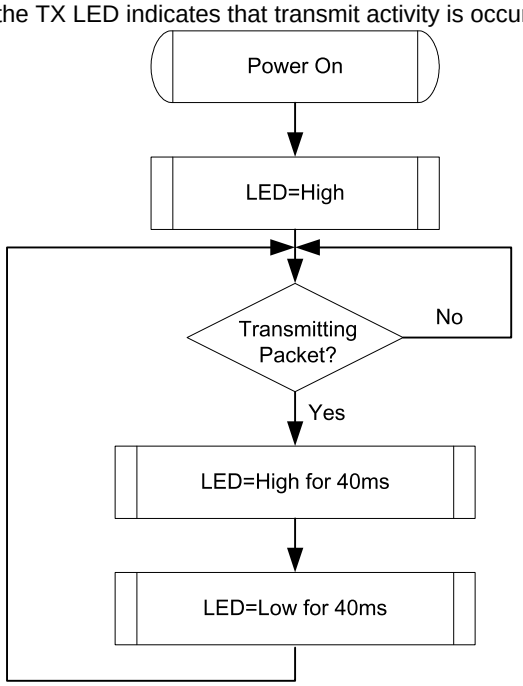


Figure 10. TX LED

4.5. TX/RX LED

In 10/100M mode, blinking of the TX/RX LED indicates that both transmit and receive activity is occurring.

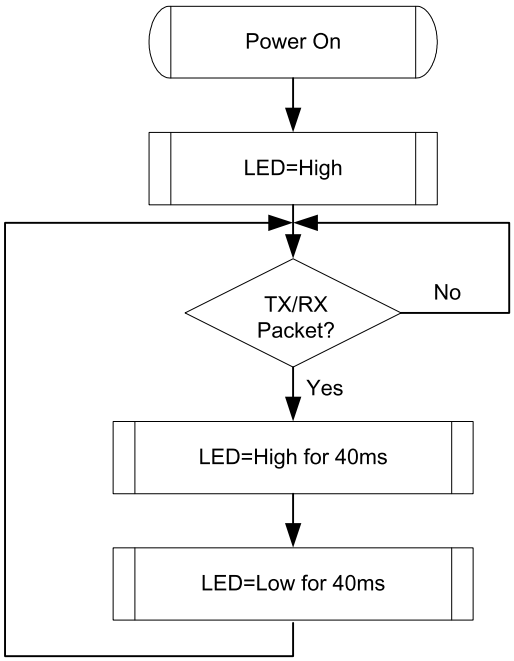


Figure 11. TX/RX LED

4.6. LINK/ACT LED

In 10/100M mode, blinking of the LINK/ACT LED indicates that the SR8201F is linked and operating properly. When this LED is high for extended periods, it indicates that a link problem exists.

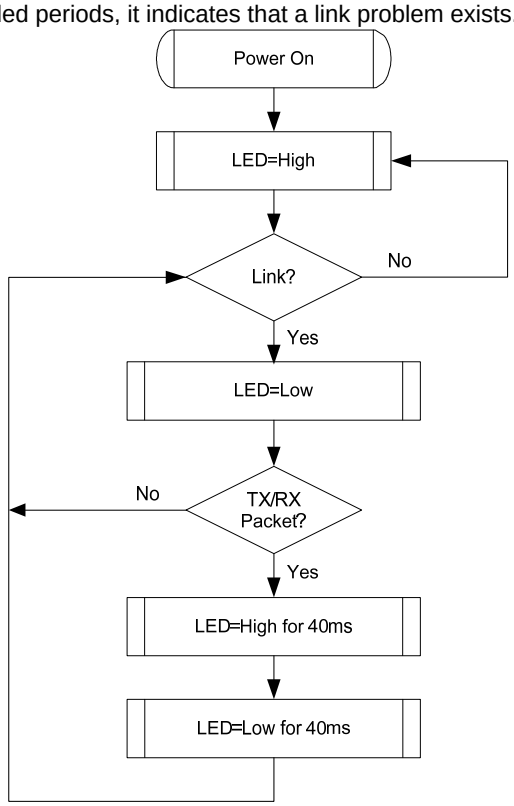


Figure 12. LINK/ACT LED

4.7 Customized LED

The SR8201F/FL/FN supports programmable LEDs in 10/100Mbps mode. This function can be enabled/disabled via page7, reg19[3] register (Figure below).

Refer to page7 register17, page 23 for customized LED register setting.

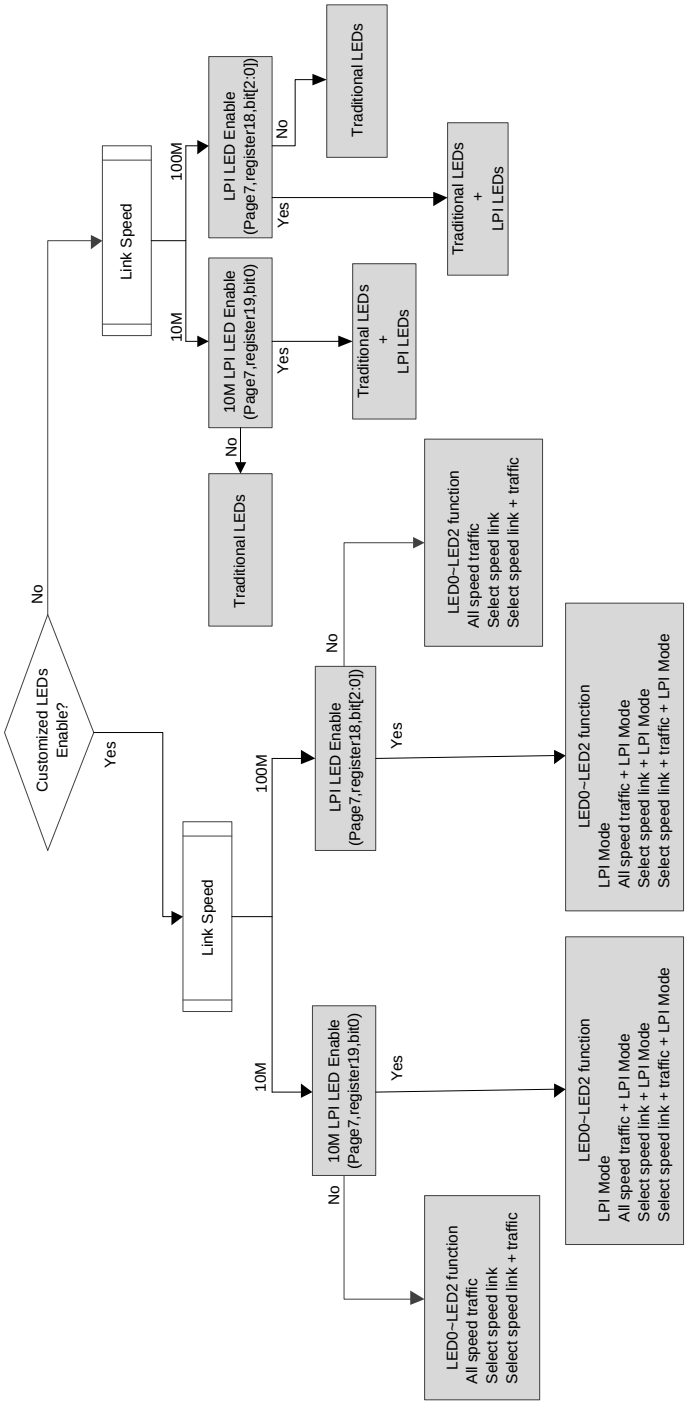


Figure 13. Customized LED with/without LPI LED Mode

4.8 EEE LED Behavior

EEE Idle mode: LED continuous slow blinking.

EEE Active mode: LED fast and slow blinking (on packet transmission and reception). Refer to page7 register18, page 23 for EEE LED enable setting.

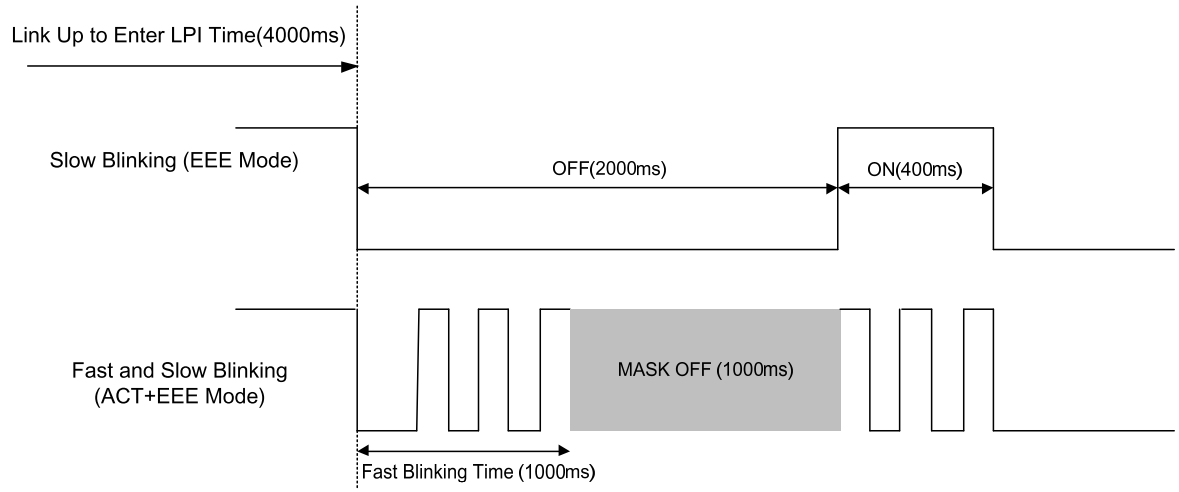


Figure 14. EEE LED Behavior

5. Power Down and Link Down Power Saving Modes

Two types of Power Saving mode operation are supported. This section describes how to implement each mode through software.

Table 42. Power Saving Mode Pin Settings

Mode	Description
PWD	Setting bit 11 of register 0 to 1 puts the SR8201F/FL/FN into Power Down Mode (PWD). This is the maximum power saving mode while the SR8201F/FL/FN is still 'live'. In PWD mode, the SR8201F/FL/FN will turn off all analog/digital functions except the MDC/MDIO management interface. Therefore, if the SR8201F/FL/FN is put into PWD mode and the MAC wants to recall the PHY, it must create the MDC/MDIO timing by itself (this is done by software).
LDPS	Setting bit 15 of register 24 to 1 will put the SR8201F/FL/FN into LDPS (Link Down Power Saving) mode. In LDPS mode, the SR8201F/FL/FN will detect the link status to decide whether or not to turn off the transmit function. If the link is off, FLP or 100Mbps IDLE/10Mbps NLP will not be transmitted. However, some signals similar to NLP will be transmitted. Once the receiver detects leveled signals, it will stop the signal and transmit FLP or 100Mbps IDLE/10Mbps NLP again. This can cut power used by 60%~80% when the link is down.

6. 10M/100M Transmit and Receive

6.1. 100Base-TX Transmit and Receive Operation

100Base-TX Transmit

Transmit data in 4-bit nibbles (TXD[3:0]) clocked at 25MHz (TXC) is transformed into 5B symbol code (4B/5B encoding). Scrambling, serializing, and conversion to 125MHz,and NRZ to NRZI then takes place. After this process, the NRZI signal is passed to the MLT-3 encoder, then to the transmit line driver. The transmitter will first

assert TXEN. Before transmitting the data pattern, it will send a /J/K/ symbol (Start-of-frame delimiter), the data symbol,and finally a /T/R/ symbol known as the End-Of-Frame delimiter. For better EMI performance, the seed of the scrambler is based on the PHY address. In a hub/switch environment, each SR8201F will have different scrambler seeds and so spread the output of the MLT-3 signals.

100Base-TX Receive

The received signal is compensated by the adaptive equalizer to make up for signal loss due to cable attenuation and Inter Symbol Interference (ISI). Baseline Wander Correction monitors the process and dynamically applies corrections to the process of signal equalization. The Phase Locked Loop (PLL) then recovers the timing information from the signals and from the receive clock. With this, the received signal is sampled to form NRZI (Non-Return-to-Zero Inverted) data. The next steps are the NRZI to NRZ (Non- Return-to-Zero) process, unscrambling of the data, serial to parallel and 5B to 4B conversion, and passing of the 4B nibble to the MII interface.

6.2. 100Base-FX Fiber Transmit and Receive Operation

The SR8201F/FL/FN can be configured to 100Base-FX mode via hardware configuration. The hardware 100Base-FX setting takes priority over NWay settings. A scrambler is not required in 100Base-FX.

100Base-FX Transmit

Di-bits of TXD are processed as 100Base-TX except without a scrambler before the NRZI stage. Instead of converting to MLT-3 signals, as in 100Base-TX, the serial data stream is driven out as NRZI PECL signals, which enter the fiber transceiver in differential-pair form.

100Base-FX Receive

The signal is received through PECL receiver inputs from the fiber transceiver and directly passed to the clock recovery circuit for data/clock recovery. The scrambler/de-scrambler is bypassed in 100Base-FX.

6.3. 10Base-T Transmit and Receive Operation

10Base-T Transmit

Transmit data in 4-bit nibbles (TXD[3:0]) clocked at 2.5MHz (TXC) is first fed to a parallel-to-serial converter, then the 10Mbps NRZ signal is sent to a Manchester encoder.The Manchester encoder converts the 10Mbps NRZ data into a Manchester Encoded data stream for the TP transmitter and adds a Start of Idle pulse (SOI) at the end of the packet as specified in IEEE 802.3. Finally, the encoded data stream is shaped by a band-limited filter embedded in the SR8201F and then transmitted.

10Base-T Receive

In 10Base-T receive mode, the Manchester decoder in the SR8201F/FL/FN converts the Manchester encoded data stream into NRZ data by decoding the data and stripping off the SOI pulse. The serial NRZ data stream is then converted to a parallel 4-bit nibble signal (RXD[0:3]).

7. Reset and Transmit Bias

There are two SR8201F/FL/FN reset types:

1. Hardware Reset: Pull the PHYRSTB pin high for at least 150ms to access the SR8201F/FL/FN registers. Pull the PHYRSTB pin low for at least 10ms and then pull high. All registers will return to default values after a hardware reset. The media interface will disconnect and restart the auto-negotiation/parallel detection process.
2. Software Reset: Set register 0 bit 15 to 1 for at least 20ms to access the SR8201F/FL/FN registers. A Software reset will only partially reset the registers, and will reset the chip status to ‘initializing’.

The RSET pin must be pulled low by a 2.49KΩ resistor with 1% accuracy to establish an accurate transmit bias. This will affect the signal quality of the transmit waveform. Keep its circuitry away from other clock traces and transmit/receive paths to avoid signal interference.

8. 3.3V Power Supply and Voltage Conversion Circuit

The SR8201F/FL/FN is fabricated in a 0.11μm process. The core circuit needs to be powered by 1.1V, however, the digital IO and DAC circuits need a 3.3V power supply. Regulators are embedded in the SR8201F/FL/FN to convert 3.3V to 1.1V.

Note: The internal linear regulator output voltage is 1.1V. A 1.05V is supplied when using external core power. The external 1.05V power supply is not suggested for the SR8201F/FL as the internal regulators cannot be disabled (the SR8201F/FL does not have an EN_LDO_OUT pin to disable the internal 1.1V power supply), and the internal and external power sources may conflict.

As with many commercial voltage conversion devices, the 1.1V output pin of this circuit requires the use of an output capacitor (0.1μF X5R low-ESR ceramic capacitor) as part of the device frequency compensation.

The analog and digital ground planes should be as large and intact as possible. If the ground plane is large enough, the analog and digital grounds can be separated, which is the ideal configuration. However, if the total ground plane is not sufficiently large, partition of the ground plane is not a good idea. In this case, all the ground pins can be connected together to a larger single and intact ground plane.

Note: The embedded 1.1V LDO is designed for PHYceiver device internal use only. Do not provide this power to other devices.

9. Automatic Polarity Correction

The SR8201F automatically corrects polarity errors on the receive pairs in 10Base-T mode (polarity is irrelevant in 100Base-TX mode). In 10Base-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. Detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link goes down.

10. Far End Fault Indication

The MII Reg.1.4 (Remote Fault) is the Far End Fault Indication (FEFI) bit when 100FX mode is enabled, and indicates when a FEFI has been detected. FEFI is an alternative in-band signaling method that is composed of 84 consecutive ‘1’s followed by one ‘0’. When the SR8201F/FL/FN detects this pattern three times, Reg.1.4 is set, which means the transmit path (the Remote side’s receive path) has a problem. On the other hand, if an incoming signal fails to cause a ‘Link OK’, the SR8201F/FL/FN will start sending this pattern, which in turn causes the remote side to detect a Far End Fault. This means that the receive path has a problem from the point of view of the SR8201F/FL/FN. The FEFI mechanism is used only in 100Base-FX mode.

11. Wake-On-LAN (WOL)

11.1 Magic Packet and Wake-Up Frame Format

The SR8201F/FL/FN can monitor the network for a Wake-Up Frame or a Magic Packet, and notify the system via the PMEB (Power Management Event; ‘B’ means low active) pin when such a packet or event occurs. The system can then be restored to a normal state to process incoming jobs. The PMEB pin mustbe connected with a 4.7k-ohm resistor and pulled up to 3.3V. When the Wake-Up Frame or a Magic Packet is sent to the PHY, the PMEB pin will be set low to notify the system to wake up. Refer to the WOL application note for details.

Magic Packet Wake-Up occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the SR8201F/FL/FN, e.g., a broadcast, multicast, or unicast packet addressed to the current SR8201F/FL/FN.
- The received Magic Packet does not contain a CRC error.
- The Magic Packet pattern matches; i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wake-Up Frame event occurs only when the following conditions are met:

- The destination address of the received Wake-Up Frame is acceptable to the SR8201F/FL/FN, e.g., a broadcast, multicast, or unicast address to the current SR8201F/FL/FN.
- The received Wake-Up Frame does not contain a CRC error.
- The 16-bit CRC of the received Wake-Up Frame matches the 16-bit CRC of the sample Wake-Up Frame pattern given by the local machine's OS. Or, the SR8201F/FL/FN is configured to allow direct packet wake up, e.g., a broadcast, multicast, or unicast network packet.

Note 1: 16-bit CRC: The SR8201F/FL/FN supports eight long-Wake-Up frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet). CRC16 polynomial=x16+x12+x5+1.

Note 2: Refer to the WOL Application Note for detailed Wake-On-LAN register settings and waveform timings.

11.2 Active Low Wake-On-LAN

When the PHY receives a Wake-Up Frame or a Magic Packet from the link partner, the PMEB pin will go low and the MAC will wake up after a T cycle. The PMEB pin will be reset to high via the system or MAC (Two figures below).

Refer to the WOL Application Note for details.

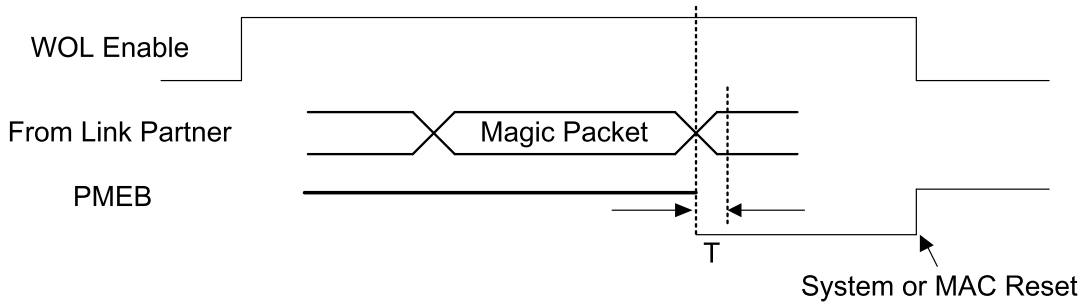


Figure 15. Active Low When Receiving a Magic Packet

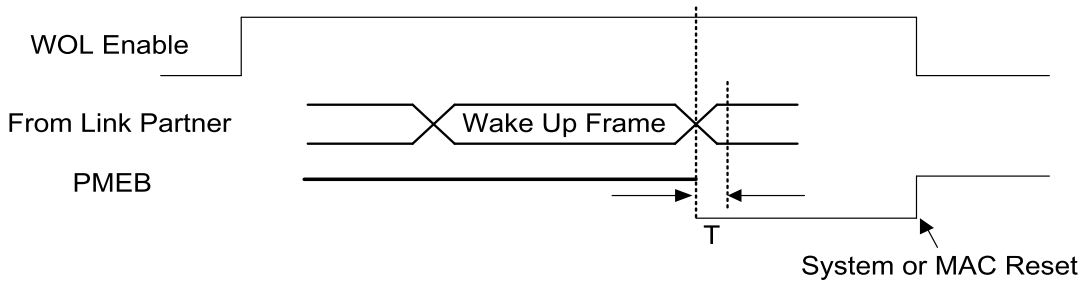


Figure 16. Active Low When Receiving a Wake-Up Frame

11.3. Pulse Low Wake-On-LAN

When the PHY receives a Wake-Up Frame or a Magic Packet from the link partner, the PMEB pin will go low for a period (84ms, 168ms (default), 336ms, or 672ms; set through the MDC/MDIO), and will wake up after a T cycle (Two figures below).

Refer to the WOL Application Note for details.

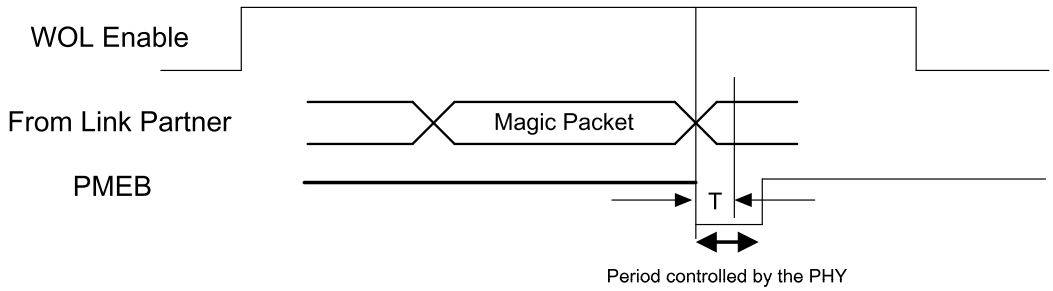


Figure 17. Pulse Low When Receiving a Magic Packet

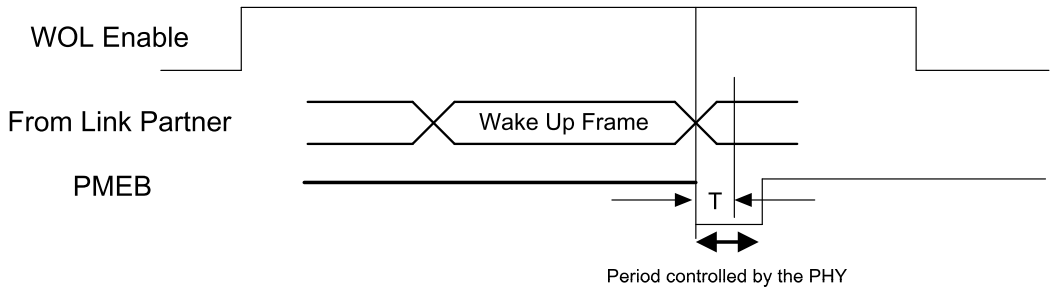


Figure 18. Pulse Low When Receiving a Wake-Up Frame

11.4 Wake-On-LAN Pin Types (MII Mode)

Table 43. Wake-On-LAN Pin Types (MII Mode)

Name	Type	Normal			WOL Enable
		100M	10M	Idle	
TXC	O/PD	25M CLK Output	2.5M CLK Output	2.5M CLK Output	O (2.5M/25M)/L/PD1
TXEN	I/PD	I	I	I	I/PD
TXD[0:3]	I/PD	I	I	I	I/PD
RXC	O/PD	25M CLK Output	2.5M CLK Output	2.5M CLK Output	O (2.5M/25M)/PD2
COL	LI/O/PD	O	O	O	O or PD2
CRS	LI/O/PD	O	O	O	O or PD2
RXDV	LI/O/PD	O	O	O	O or PD2
RXD[0:2]	O/PD	O	O	O	O or PD2
RXD[3]	LI/O/PD	O	O	O	O or PD2
RXER	LI/O/PD	O	O	O	O or PD2
MDC	I/PU	I	I	I	I/PU
MDIO	IO/PU	IO	IO	IO	IO/PU

Note 1: If TX Isolate=1, the TXC is halted and the pin type is 'L'.Set page0, register0, and bit10=1 to change the TXC pin type to 'PD'.

Note 2: If RX Isolate=1, all the MII RX interfaces are halted and the pin types are 'PD'.

11.5 Wake-On-LAN Pin Types (RMII Mode)

Table 44. Wake-On-LAN Pin Types (RMII Mode)

Name	Type	Normal			WOL Enable
		100M	10M	Idle	
TXC (REF_CLK)1	IO/PD	50M CLK Input/Output	50M CLK Input/Output	50M CLK Input/Output	I/O (50M)2
TXEN	I/PD	I	I	I	I/PD
TXD[0:1]	I/PD	I	I	I	I/PD
CRS_DV	LI/O/PD	O	O	O	O or PD3
RXD[0:1]	O/PD	O	O	O	O or PD3
RXER	LI/O/PD	O	O	O	O or PD3
MDC	I/PU	I	I	I	I/PU
MDIO	IO/PU	IO	IO	IO	IO/PU

Note 1: If TXC (REF_CLK) is in input mode (MAC to PHY), the REF_CLK cannot halt at WOL Enable.

Note 2: When REF_CLK is in output mode (PHY to MAC), the REF_CLK cannot halt (always toggles 50MHz out). To set the TXC pin type to 'PD', set page0, register0, bit10=1.

Note 3: If RX Isolate=1, all RMII RX interfaces are halted and the pin types are 'PD'.

12. Energy Efficient Ethernet (EEE)

The SR8201F/FL/FN supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE), at 10Mbps and 100Mbps. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. When packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled; however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported. Refer to http://www.ieee802.org/3/az/index.html for more details.

Refer to the 'SR8201(F_FL_FN)_Ethernet_Transceiver_(R)MII_EEE_App_Note' for EEE MII/RMII power saving mode register settings.

13. Spread Spectrum Clock (SSC)

The RMII REF_CLK path can be a source of EMI noise. Spread Spectrum Clock (SSC) spreads the REF_CLK signal across a wider bandwidth, reducing the peak radiated energy at any one frequency, and lowering unwanted EMI noise.

The SSC function is enabled by default when using RMII REF_CLK output mode (see Page 7 Register 24 Spread Spectrum Clock Register, page 25).

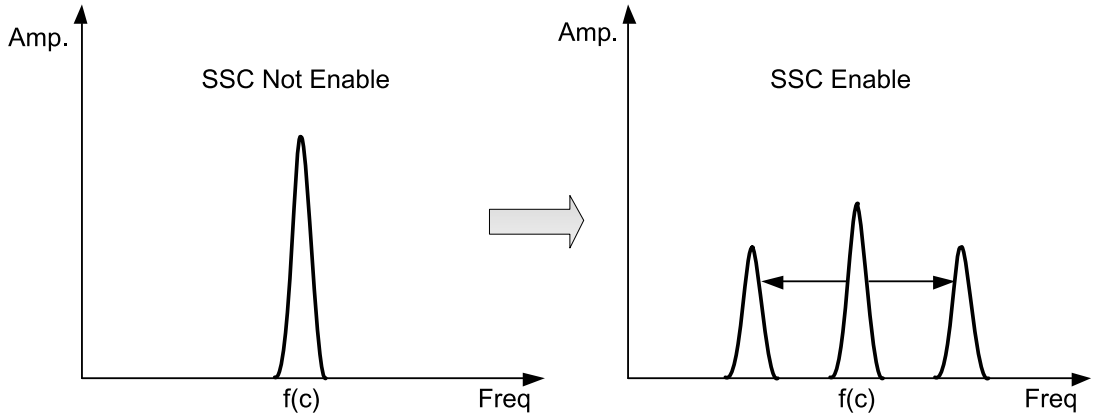


Figure 19. Spectrum Spread Clock

Electrical Characteristics

1. DC Characteristics

1.1 Absolute Maximum Ratings

Table 45. Absolute Maximum Ratings

Parameter	Symbol	Range	Units
Supply Voltage 3.3V	DVDD33, AVDD33	-0.4 ~ 3.7	V
Supply Voltage 1.05V*	DVDD10, DVDD10OUT, AVDD10OUT	-0.1 ~ 1.26	V
Input Voltage	DC Input	-0.3 ~ Corresponding Supply Voltage +0.5V	V
Output Voltage	DC Output	-0.3 ~ Corresponding Supply Voltage +0.5V	V
Storage Temperature	N/A	-55 ~ 125	^{o}C

Note: The internal linear regulator output voltage is 1.1V.

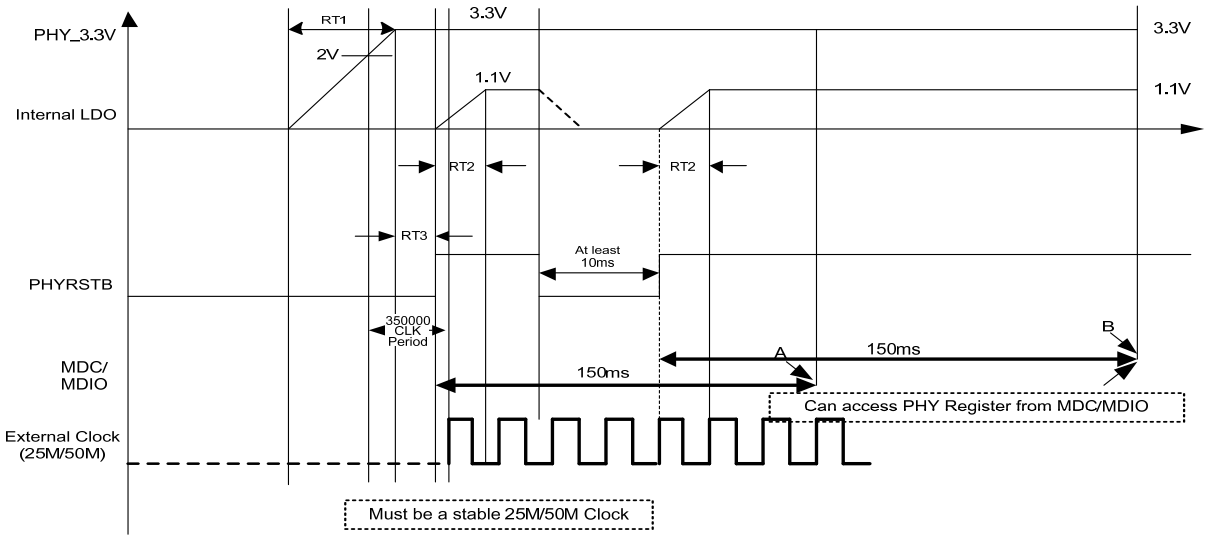
1.2 Recommend Operation Conditions

Table 46. Recommend Operation Conditions

Parameter	Pins	Range	Typical	Units
Supply Voltage VDD	DVDD33, AVDD33	2.97 ~ 3.63	3.63	V
	DVDD10, DVDD10OUT, AVDD10OUT	1.00 ~ 1.16*	1.16	V
Ambient Operating Temperature T_A		0 ~70	70	^{o}C
Maximum Junction Temperature	-	- ~125	125	^{o}C

1.3 Power On and PHY Reset Sequence

The SR8201F/FL/FN needs 150ms power on time. After 150ms it can access the PHY register from MDC/MDIO



Note1: If there is no PHY Reset sequence, the MAC can access the PHY Register at point A.
Note2: If there is a PHY Reset sequence, the MAC can access the PHY Register at point B.
Note3: The Internal LDO (Linear Regulator) output voltage is 1.1V.

Figure 20. Power On and PHY Reset Sequence

Table 47. Power On and PHY Reset Sequence

Symbol	Description	Minimum	Maximum
Rt1	3.3V Rise Time@ Power On Sequence	100μs	-
Rt2	1.05V Rise Time@ Power On and PHY Reset Sequence	100μs	-
Rt3	PHYRSTB De-Assert after PHY_3.3V Stable	80μs	-

Note: Rt2 requires 100μs Rise Time only when using an external 1.05V power supply.

1.4 RMII Input Mode Power Dissipation

The whole system power dissipation (including regulator loss) is shown in Table below.

Table 48. RMII Input Mode Power Dissipation (Whole System)

Symbol	Condition	SR8201F	SR8201FN	SR8201FL	Unit
P_{10IDLE}	10Base-T Idle (EEE not Enabled)	36.3	36.3	36.3	mW
P_{10F}	10Base-T Full Duplex	108.9	118.8	108.9	mW
$P_{100IDLE}$	100Base-T Idle (EEE not Enabled)	148.5	151.8	155.1	mW
$P_{100IDLEEEE}$	100Base-T Idle with EEE	56.1	56.1	62.7	mW
P_{100F}	100Base-T Full Duplex	174.9	178.2	178.2	mW
P_{LDPS}	Link Down Power Saving	20.328	17.985	23.1	mW
P_{PHYRST}	PHY Reset	3.3	3.3	3.3	mW

Note: Setting page 4 register 21 bit12 to '1' will reduce power consumption when the system is idle.

1.5 Input Voltage: Vcc

Table 49. Input Voltage: Vcc

Symbol	Condition		Minimum	Maximum
TTL V_{IH}	Input High Voltage	-	0.5*Vcc	Vcc+0.5V
TTL V_{IL}	Input Low Voltage	-	-0.5V	0.7V
TTL V_{OH}	Output High Voltage	IOH=-8mA	0.65*Vcc	Vcc
TTL V_{OL}	Output Low Voltage	IOL=8mA	-	0.7V
TTL I_{OZ}	Tri-State Leakage	Vout=Vcc or GND	-110μA	10μA
I_{IN}	Input Current	Vin=Vcc or GND	-1μA	10μA
I_{PL}	Input Current with Internal Weakly Pulled Low Resistor	Vin=Vcc or GND	-1μA	100μA
I_{PH}	Input Current with Internal Weakly Pulled High Resistor	Vin=Vcc or GND	-110μA	10μA
PECL V_{IH}	PECL Input High Voltage	-	Vdd-1.16V	Vdd-0.88V
PECL V_{IL}	PECL Input Low Voltage	-	Vdd-1.81V	Vdd-1.47V
PECL V_{OH}	PECL Output High Voltage	-	Vdd-1.02V	-
PECL V_{OL}	PECL Output Low Voltage	-	-	Vdd-1.62V

2. AC Characteristics

All output timing assumes equivalent loading between 10pF and 25pF that includes PCB layout traces and other connected devices (e.g., MAC).

2.1 MII Transmission Cycle Timing

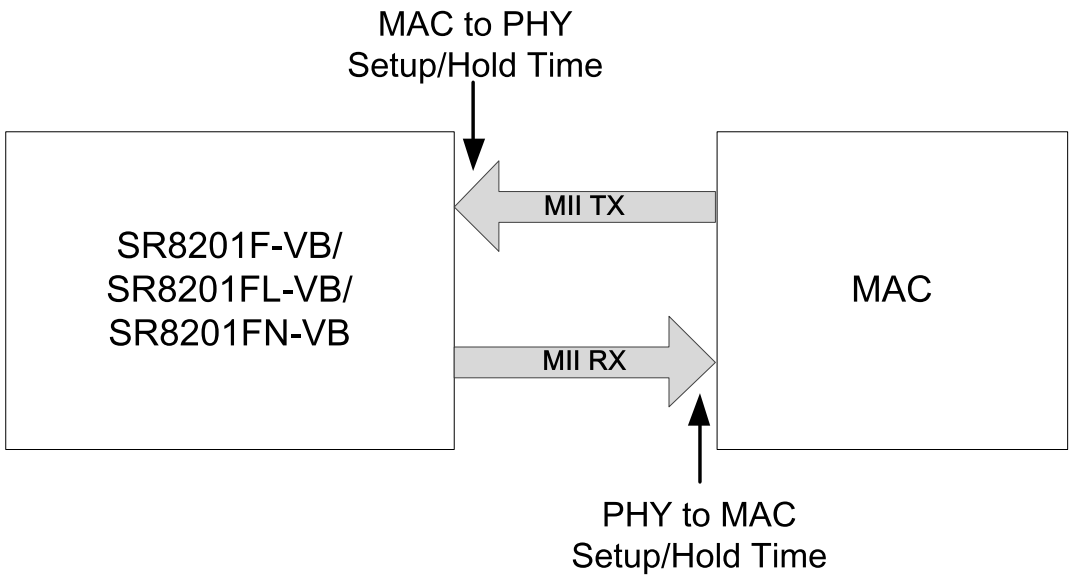


Figure 21. MII Interface Setup/Hold Time Definitions

Figures below show show an example of a packet transfer from MAC to PHY on the MII interface.

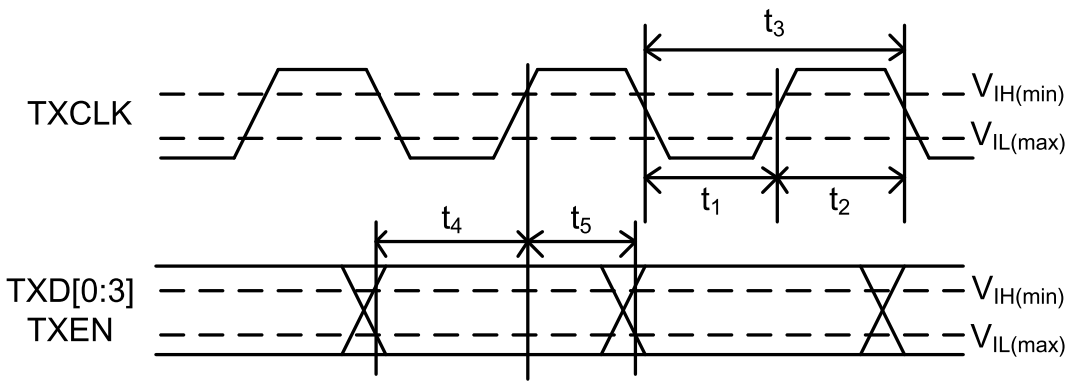


Figure 22. MII Transmission Cycle Timing-1

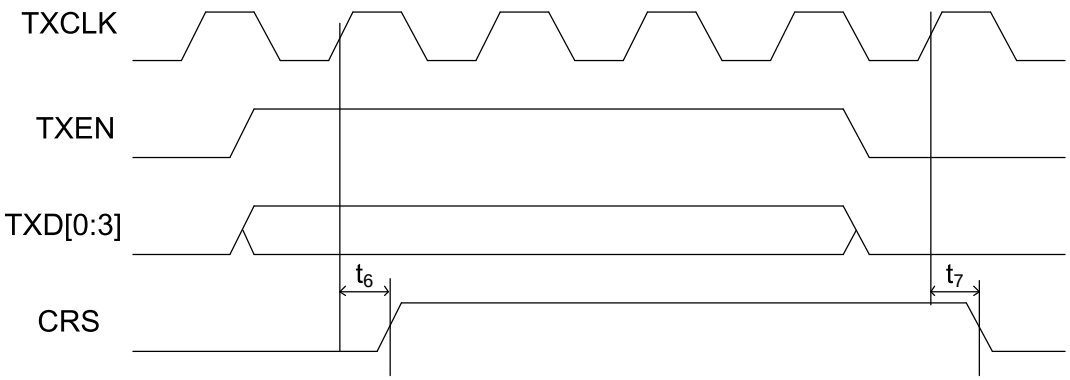


Figure 23. MII Transmission Cycle Timing-2

Table 50. MII Transmission Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
t_1	TXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t2	TXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t3	TXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t4	TXEN, TXD[0:3]	100Mbps	10	-	-	ns
	Setup to TXCLK Rising Edge	10Mbps	5	-	-	ns
t5	TXEN, TXD[0:3]	100Mbps	0	-	-	ns
	Hold After TXCLK Rising Edge	10Mbps	0	-	-	ns
t6	TXEN Sampled to CRS High	100Mbps	-	-	40	ns
		10Mbps	-	-	400	ns
t7	TXEN Sampled to CRS Low	100Mbps	-	-	160	ns
		10Mbps	-	-	2000	ns

2.2 MII Reception Cycle Timing

Figures below show an example of a packet transfer from PHY to MAC on the MII interface.

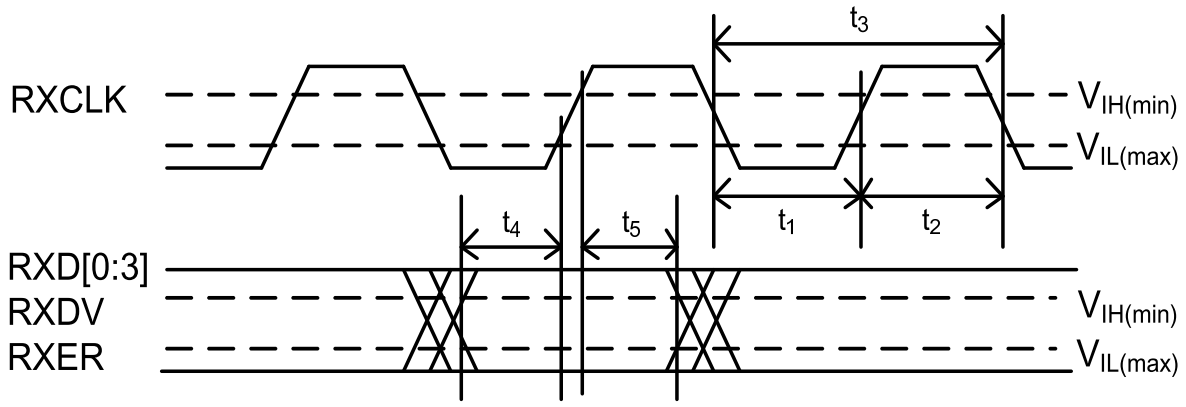


Figure 24. MII Reception Cycle Timing-1

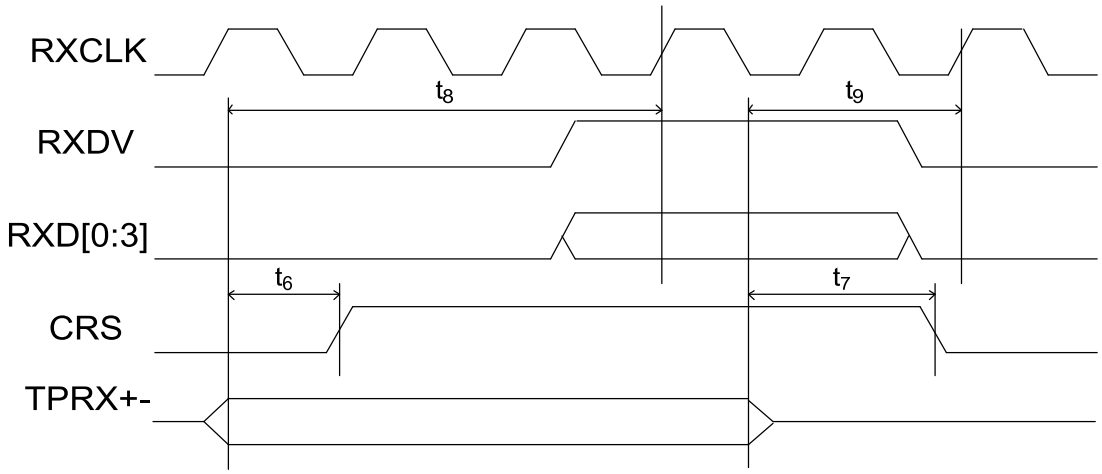


Figure 25. MII Reception Cycle Timing-2

Table 51. MII Reception Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
t1	RXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t2	RXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t3	RXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t4	RXER, RXDV, RXD[0:3] Setup to RXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	10	-	-	ns
t5	RXER, RXDV, RXD[0:3] Hold After RXCLK Rising Edge	100Mbps	10	-	-	ns
		10Mbps	10	-	-	ns
t6	Receive Frame to CRS High	100Mbps	-	-	130	ns
		10Mbps	-	-	2000	ns
t7	End of Receive Frame to CRS Low	100Mbps	-	-	240	ns
		10Mbps	-	-	1000	ns
t8	Receive Frame to Sampled Edge of RXDV	100Mbps	-	-	150	ns
		10Mbps	-	-	3200	ns
t9	End of Receive Frame to Sampled Edge of RXDV	100Mbps	-	-	120	ns
		10Mbps	-	-	1000	ns

2.3 RMII Transmission and Reception Cycle Timing

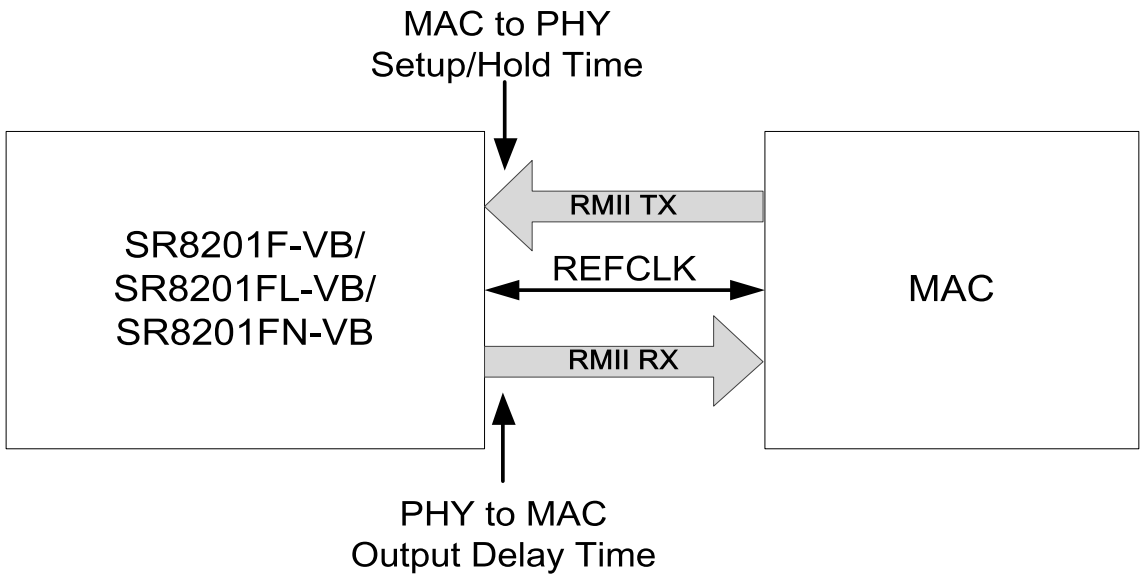


Figure 26. RMII Interface Setup, Hold Time, and Output Delay Time Definitions

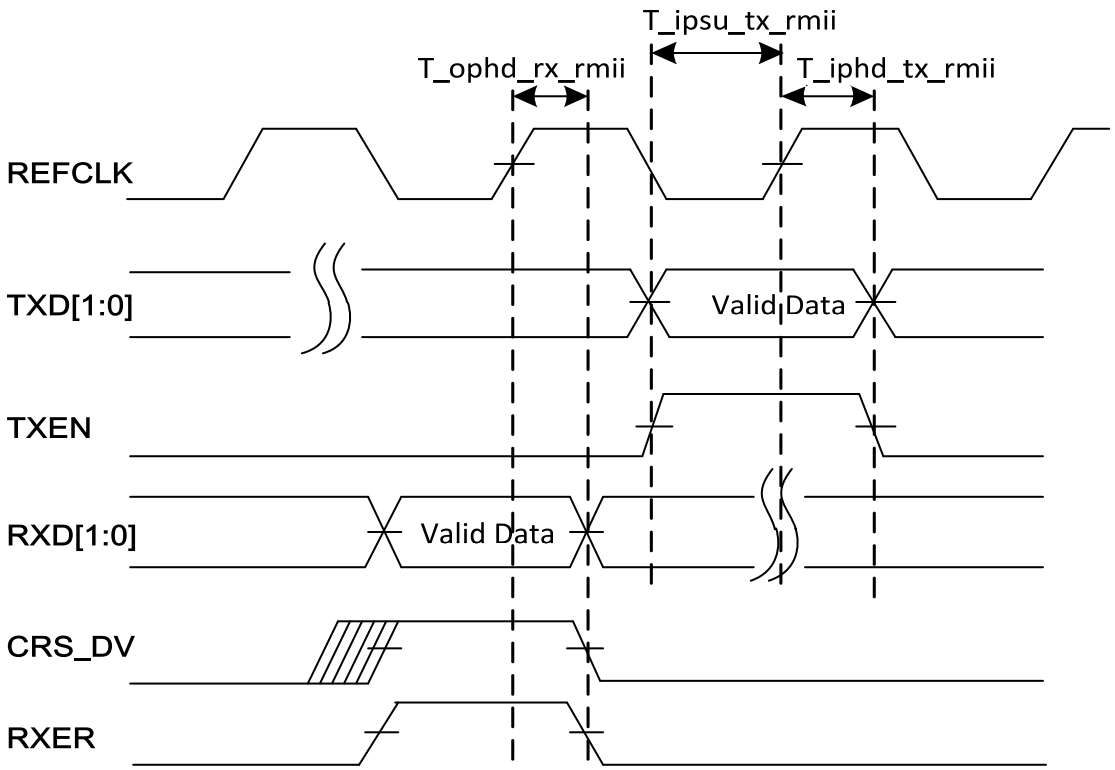


Figure 27. RMII Transmission and Reception Cycle Timing

Table 52. RMII Transmission and Reception Cycle Timing

Symbol	Description	Minimum	Typical	Maximum	Unit
REFCLK Frequency	Frequency of Reference Clock	-	50	-	MHz
REFCLK Duty Cycle	Duty Cycle of Reference Clock	35	-	65	%
T_ipsu_tx_rmii	TXD[1:0]/TXEN Setup Time to REFCLK	4	-	-	ns
T_iphd_tx_rmii	TXD[1:0]/TXEN Hold Time from REFCLK	2	-	-	ns
T_ophd_rx_rmii	RXD[1:0]/CRS_DV/RXER Output Delay Time from REFCLK	2	-	-	ns

Note 1: RMII TX timing can be adjusted by setting page7, register16[11:8]; the minimum adjustable resolution is 2ns. Any changes for these bits are not recommended as the default value is the optimum setting.

Note 2: RMII RX timing can be adjusted by setting page7, register16[7:4]; the minimum adjustable resolution is 2ns. Any changes for these bits are not recommended as the default value is the optimum setting.

2.4 MDC/MDIO Timing

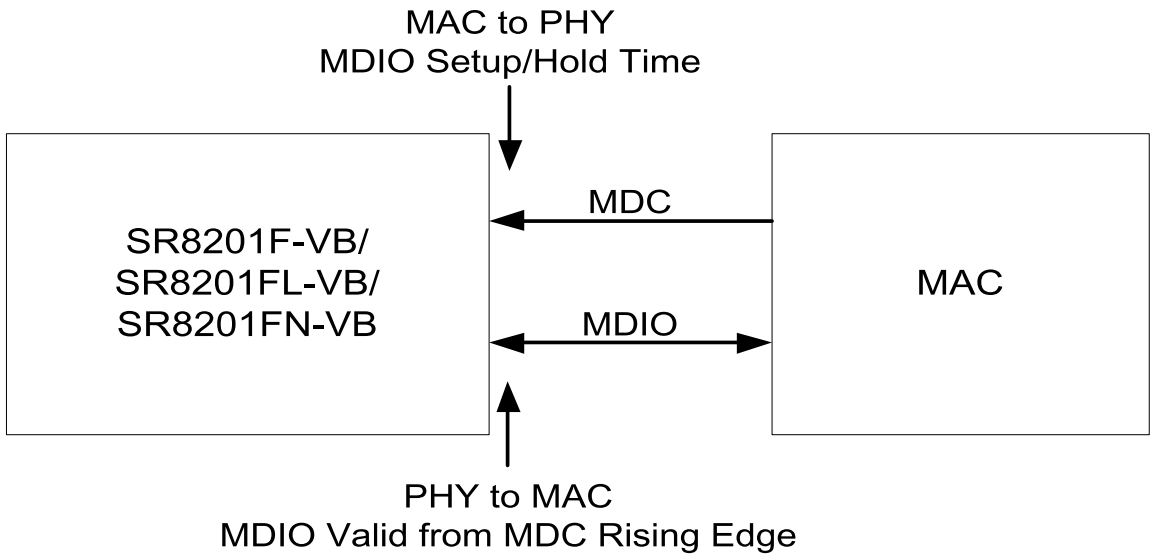


Figure 28. MDC/MDIO Interface Setup, Hold Time, and Valid from MDC Rising Edge Time Definitions

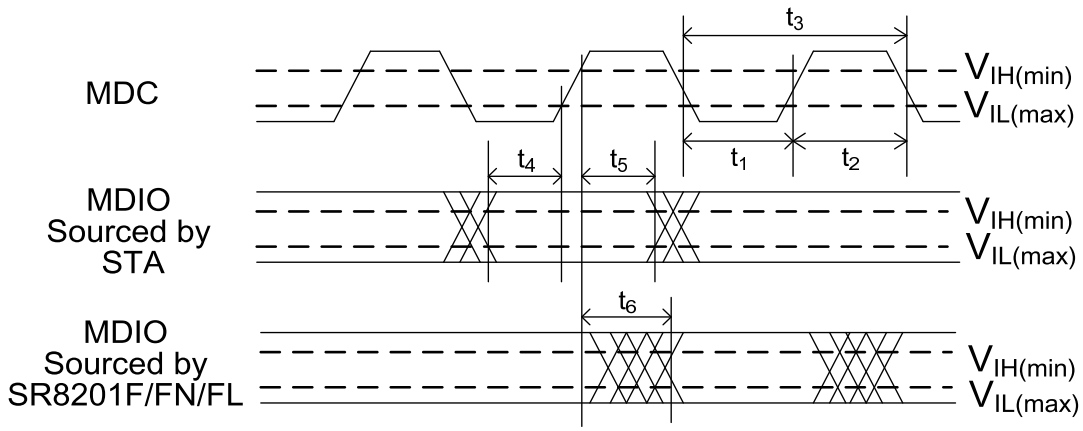


Figure 29. MDC/MDIO Timing

Table 53. MDC/MDIO Timing

Symbol	Description	Minimum	Maximum	Unit
t_1	MDC High Pulse Width	160	-	ns
t_2	MDC Low Pulse Width	160	-	ns
t_3	MDC Period	400	-	ns
t_4	MDIO Setup to MDC Rising Edge	10	-	ns
t_5	MDIO Hold Time from MDC Rising Edge	10	-	ns
t_6	MDIO Valid from MDC Rising Edge	0	300	ns

2.5 Transmission without Collision

Figure below shows an example of a packet transfer from MAC to PHY.

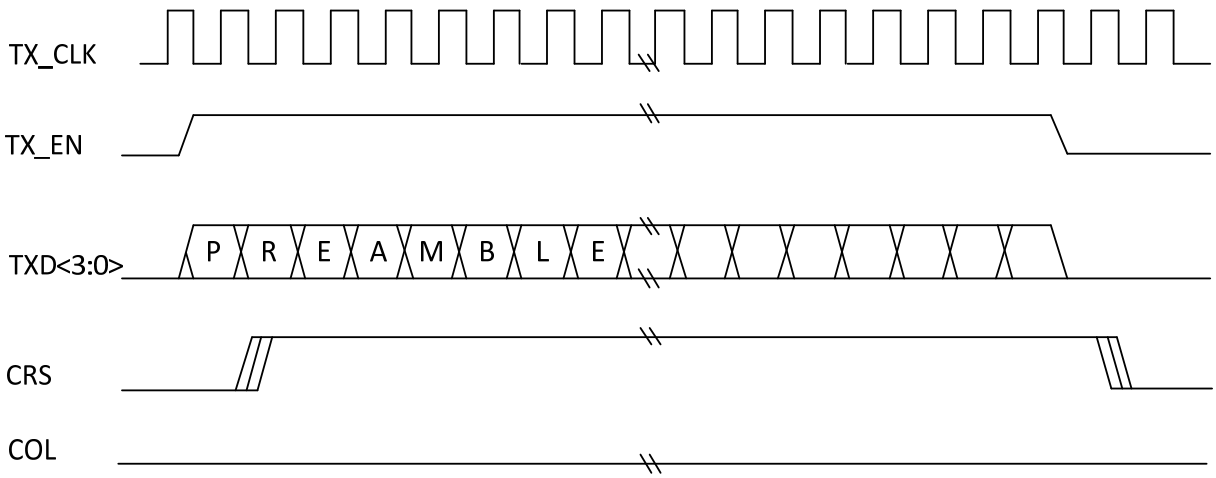


Figure 30. MAC to PHY Transmission without Collision

2.6 Reception without Error

Figure below shows an example of a packet transfer from PHY to MAC.

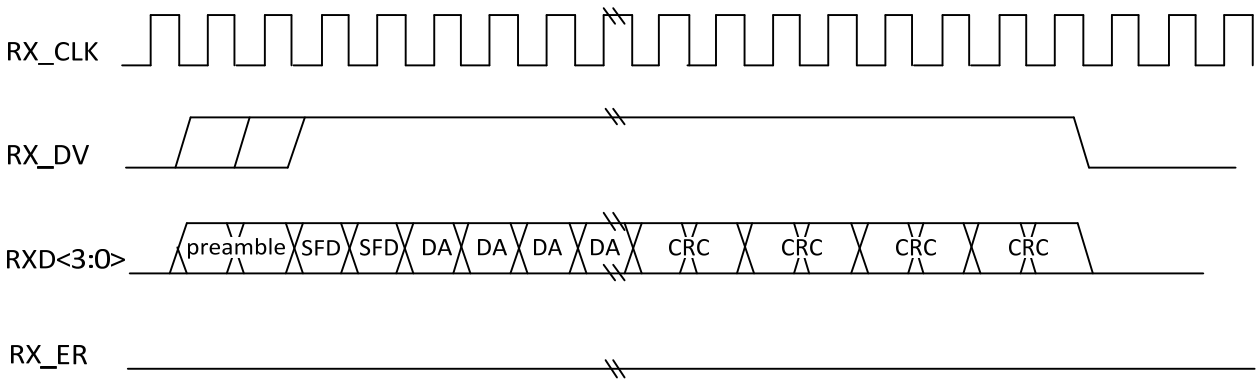


Figure 31. PHY to MAC Reception Without Error

3. Crystal Characteristics

Table 54. Crystal Characteristics

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
Fref	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	-	25	-	MHz
Fref Stability	Parallel Resonant Crystal Frequency Stability, Fundamental Mode, AT-Cut Type. T_a=0°C~70°C.	-30	-	+30	ppm
Fref Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=25°C.	-50	-	+50	ppm
Fref Duty Cycle	Reference Clock Input Duty Cycle.	40	-	60	%
ESR	Equivalent Series Resistance.	-	-	30	Ω
DL	Drive Level.	-	-	0.3	mW
Jitter	Broadband Peak-to-Peak Jitter[1, 2]	-	-	500	ps

Note 1: 25KHz to 25MHz RMS < 3ps.
Note 2: Broadband RMS < 9ps.

4. Oscillator Requirements

Table 55. Oscillator Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	-	25/50	-	MHz
Frequency Stability	Ta = 0°C~+70°C	-30	-	30	ppm
Frequency Tolerance	Ta = 25°C	-50	-	50	ppm
Duty Cycle	-	40	-	60	%
Broadband Peak-to-Peak Jitter[1, 2]	-	-	-	500	ps
Vpeak-to-peak	-	3.15	3.3	3.45	V
Rise Time (10%~90%)	-	-	-	10	ns
Fall Time (10%~90%)	-	-	-	10	ns
Operating Temperature Range	-	0	-	70	°C

Note 1: 25KHz to 25MHz RMS < 3ps.

Note 2: Broadband RMS < 9ps.

5. Clock Requirements

Table 56. Clock Requirements

Parameter	Minimum	Typical	Maximum	Unit
Frequency	-	25/50	-	MHz
Frequency Stability	-30	-	30	ppm
Frequency Tolerance	-50	-	50	ppm
Duty Cycle	40	-	60	%
Broadband Peak-to-Peak Jitter[1, 2]	-	-	500	ps
Vpeak-to-peak	3.15	3.3	3.45	V
Rise Time (10%~90%)	-	-	10	ns
Fall Time (10%~90%)	-	-	10	ns

Note 1: 25KHz to 25MHz RMS < 3ps.
Note 2: Broadband RMS < 9ps.

6. Transformer Characteristics

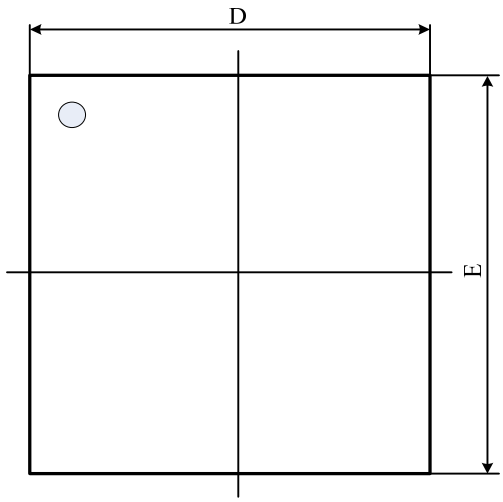
Table 57. Transformer Characteristics

Parameter	Transmit End	Receive End
Turn Ratio	1:1 CT	1:1 CT
Inductance (min.)	350μH @ 8mA	350μH @ 8mA

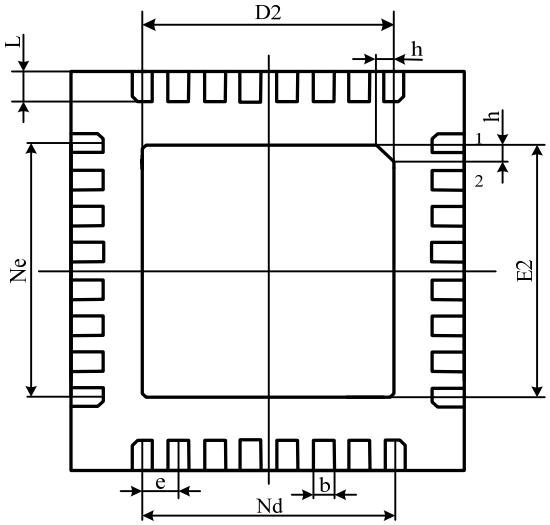
Package Diagram

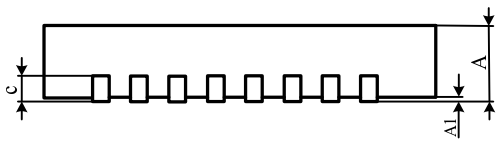
QFN-32-5×5-0.50 **Unit: mm**

TOP VIEW



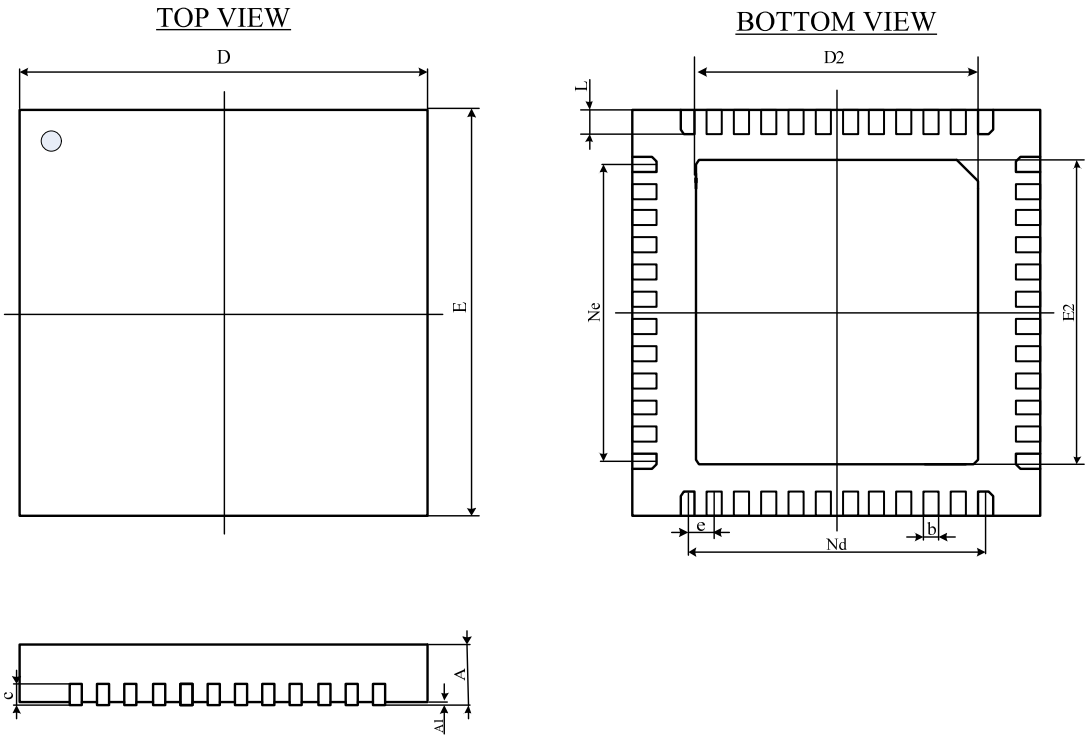
BOTTOM VIEW





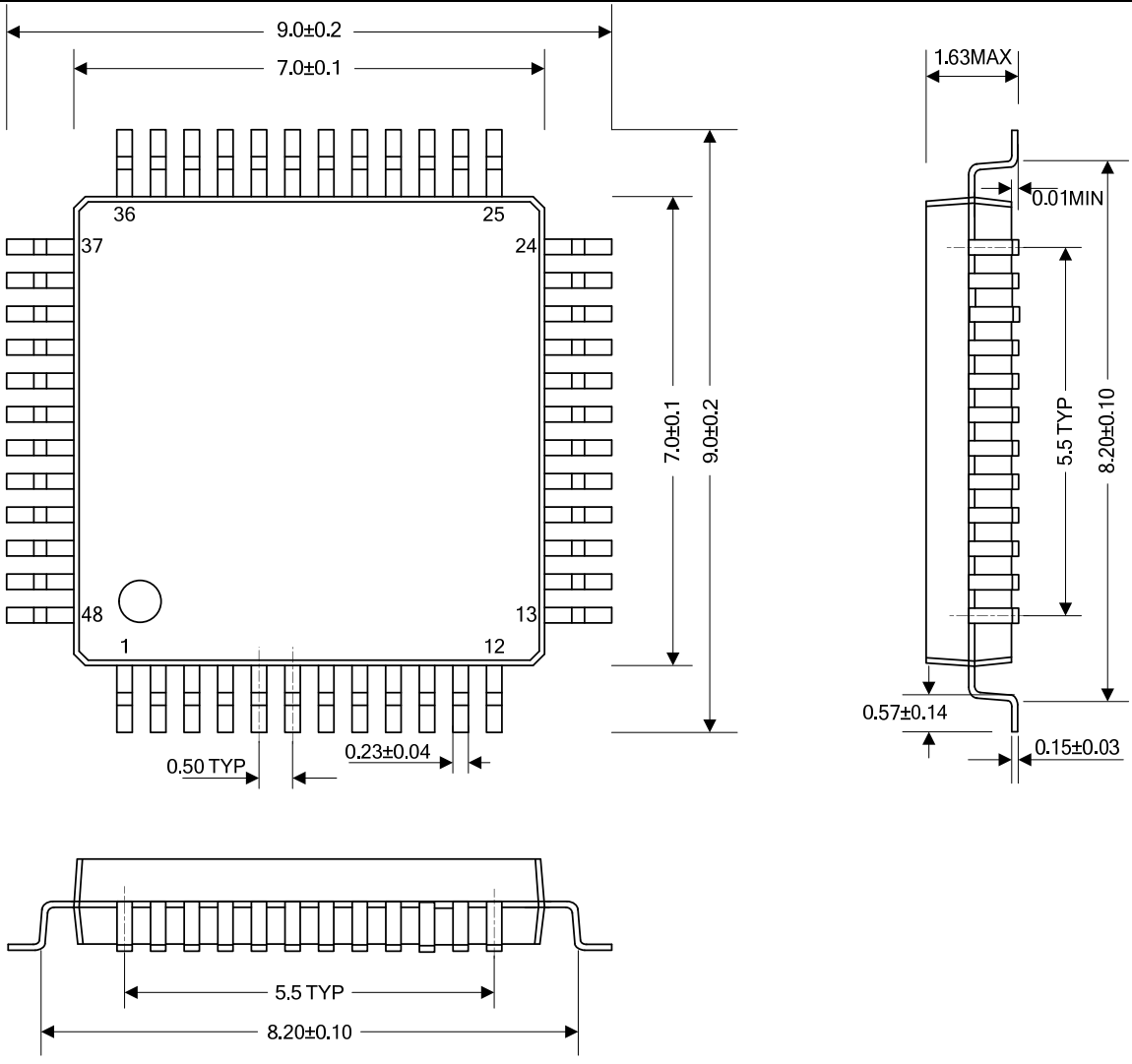
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.01	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D/E	4.90	5.00	5.10
D2/E2	3.50REF		
e	0.50BSC		
Nd/ Ne	3.50BSC		
L	0.35	0.40	0.45
h	0.30	0.35	0.40

QFN-48-6×6-0.40 **Unit: mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.85	1.00
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c		0.20REF	
D/E		6.00BSC	
D2/E2	4.05	4.4	4.65
e		0.4BSC	
Nd /Ne		4.4BSC	
L	0.30	0.40	0.50

LQFP-48-7×7-0.50 **Unit: mm**



单芯片 10/100M 以太网 PHY 收发器

概述

SR8201F-VB、 SR8201FL-VB和SR8201FN-VB都是单芯片/单端口的10/100Mbps以太网PHY收发器。芯片支持：

MII (介质独立接口)

RMII (简化介质独立接口)

SR8201F/FL/FN实现了所有10/100M以太网物理层，包括：物理编码子层 (PCS)，物理介质接入层 (PMA)，双绞线物理介质相关子层 (TP-PMD)，10Base-TX编码器/译码器和双绞线介质连接单元(TPMAU)。 同时芯片支持端口自动翻转（Auto-MDIX）。

SR8201F/FL/FN支持PECL接口的外部100Base-FX光纤收发器。

SR8201F/FL/FN采用了高级CMOS制程，可以满足低电压和低功耗的要求。片上DSP数字信号处理技术使得该芯片在所有工作条件下都表现了完美的性能。

应用范围

- MAU（介质连接单元）
- DTV（数字电视）
- CNR（网络通信扩展卡）
- 游戏控制台
- 网络打印及办公设备
- DVD播放和记录设备
- 以太网HUB（集线器）
- 以太网交换机

主要特点

- 支持IEEE 802.3az-2010（EEE）
- 兼容100Base-TX IEEE 802.3u
- 兼容10Base-T IEEE 802.3
- 支持MII模式
- 支持RMII模式
- 全/半双工工作
- 双绞线或者光纤模式输出
- 支持自协商
- 支持待机模式
- 支持断连省电模式
- 基线漂移 (BLW)补偿
- 支持Auto-MDIX
- 支持中断功能
- 支持局域网唤醒（WOL）
- 自适应均衡
- 自动极性矫正
- LED接口
  - SR8201F和SR8201FL提供两个网络状态的LED
  - SR8201FN提供三个网络状态的LED
- 支持25MHz晶振或外部振荡输入
- RMII模式支持50MHz外部时钟输入
- 支持50MHz时钟输出作为MAC的时钟源
- 1.1V和3.3V低功耗电压源；1.1V是由内部生成
- 小型化绿色封装：
  - QFN32‘绿色’封装（SR8201F）
  - LQFP48‘绿色’封装（SR8201FL）
  - QFN ‘绿色’封装（SR8201FN）

内部框图

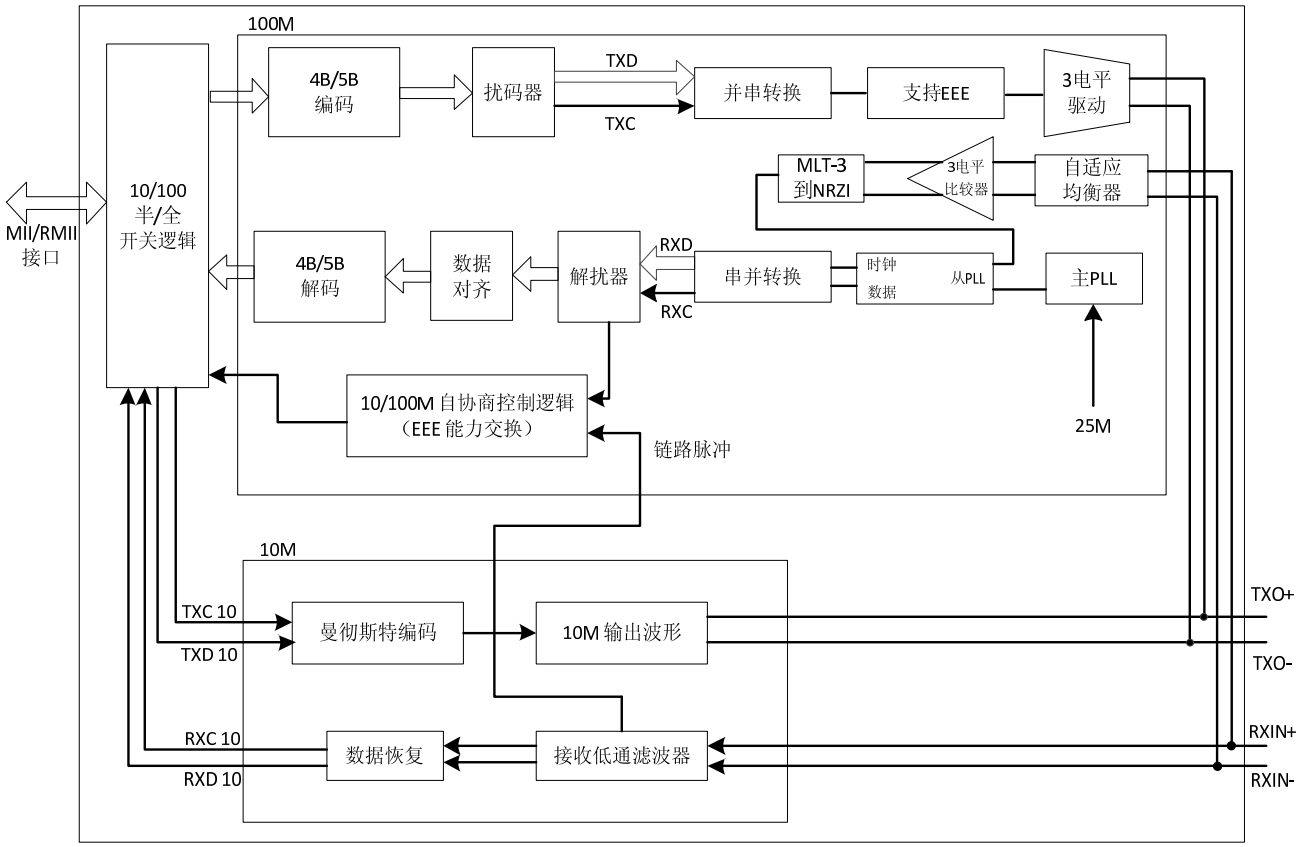

100M
4B/5B
编码
扰码器
TXD
TXC
并串转换
支持EEE
3电平
驱动
MLT-3
到NRZI
3电平
比较器
自适应
均衡器
10/100
半/全
开关逻辑
MII/RMII
接口
4B/5B
解码
数据
对齐
解扰器
RXD
RXC
串并转换
时钟
数据
从PLL
主PLL
25M
10/100M 自协商控制逻辑
（EEE 能力交换）
链路脉冲
10M
TXC 10
TXD 10
曼彻斯特编码
10M 输出波形
TXO+
TXO-
RXC 10
RXD 10
数据恢复
接收低通滤波器
RXIN+
RXIN-

图 1. 内部框图

应用框图

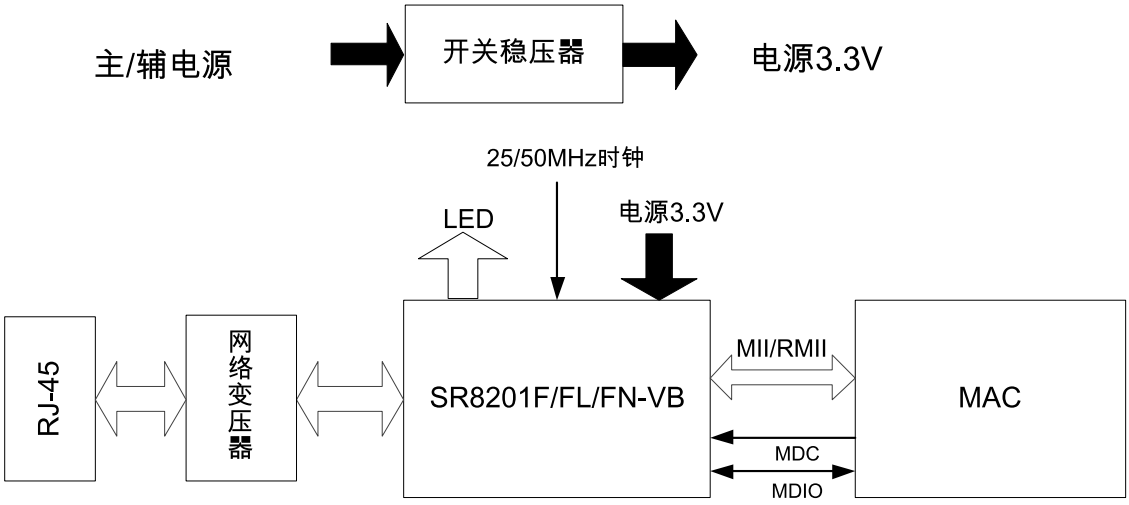

主/辅电源
开关稳压器
电源3.3V
25/50MHz时钟
LED
电源3.3V
RJ-45
网络变压器
SR8201F/FL/FN-VB
MII/RMII
MAC
MDC
MDIO

图 2. 应用框图

管脚排列图

SR8201F (32-Pin)

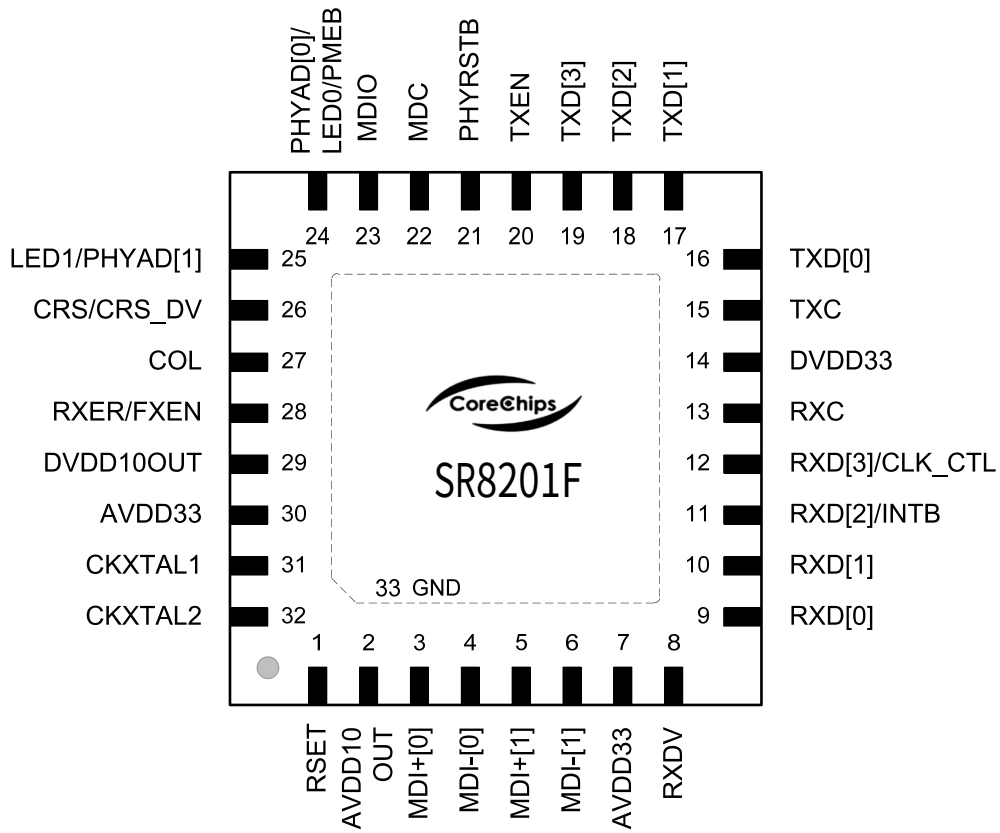


图 3. SR8201F QFN-32封装图

SR8201FN (48-Pin)

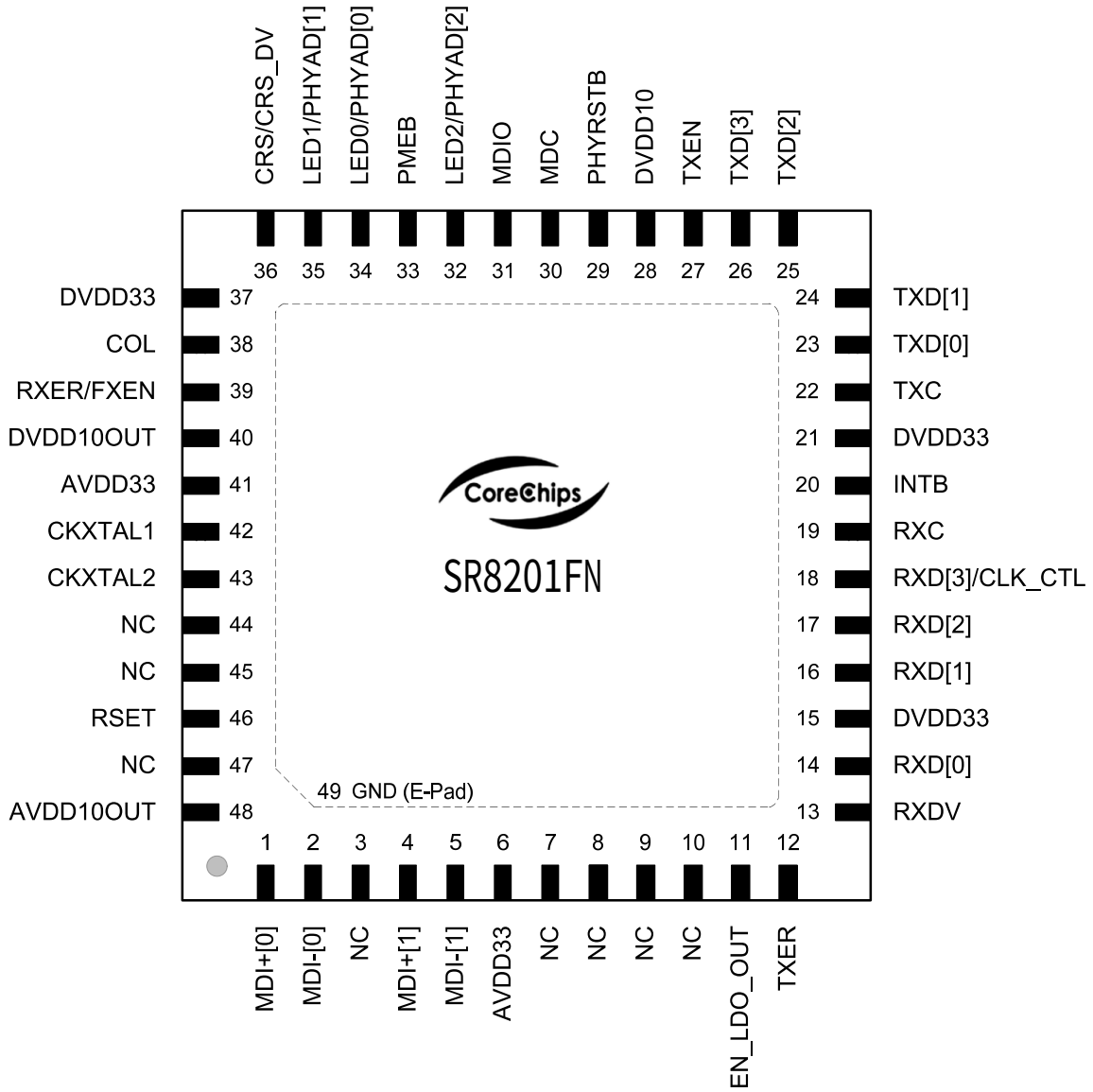


图4. SR8201FN QFN-48封装图

SR8201FL (48-Pin)

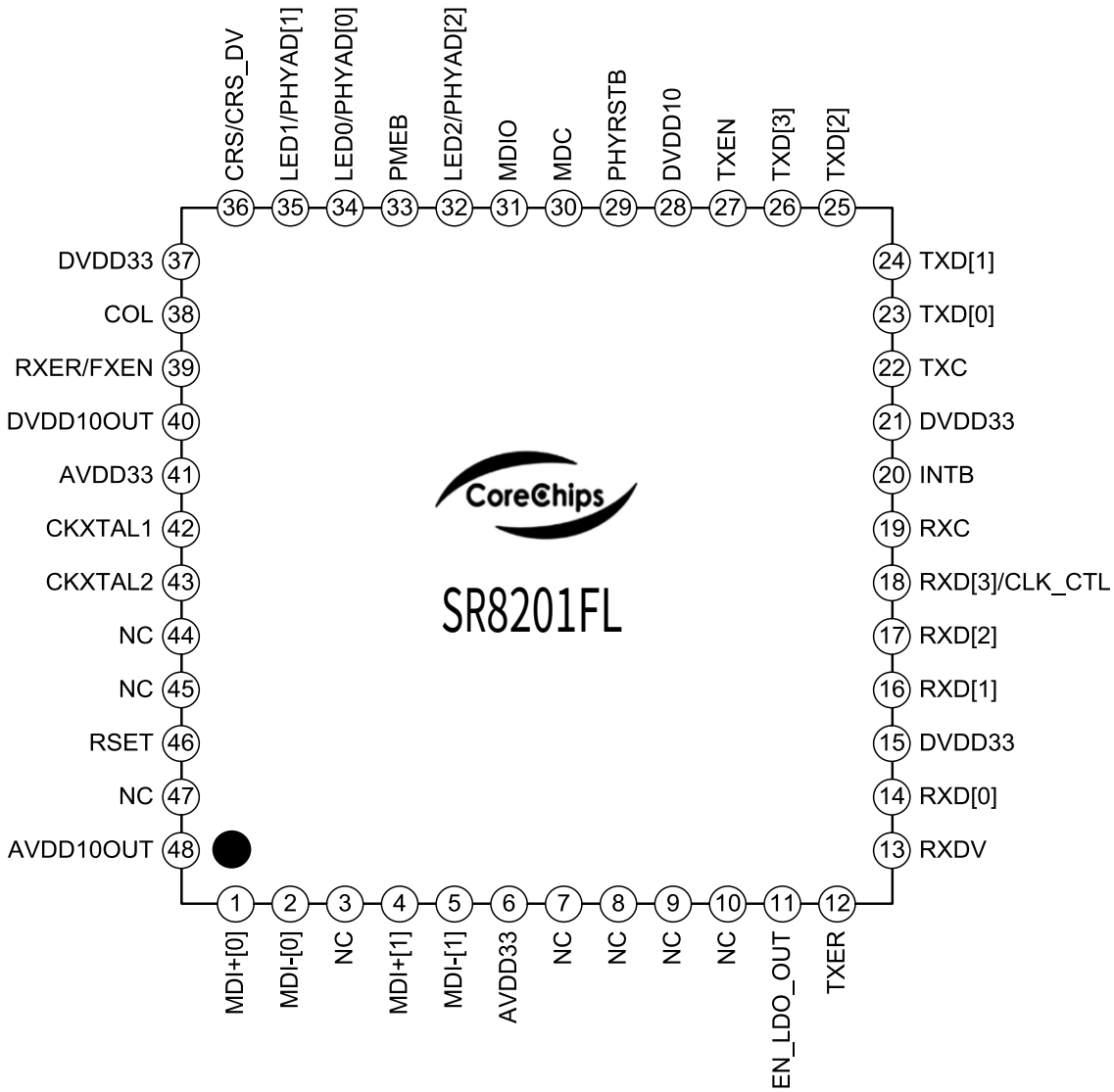


图 5. SR8201FL LQFP-48封装图

管脚定义

1. MII 接口

表 1. MII 接口

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	符号	类型	说明
15	22	22	TXC	O/PD	发送时钟。 此管脚提供一个连续的时钟作为TXD[3:0]和TXEN信号的工作时钟。 TXC在100Mbps模式下是25MHz，在10Mbps模式下是2.5MHz。
20	27	27	TXEN	I/PD	发送允许信号。
-	12	12	TXER	I/PD	发送错误。
16 17 18 19	23 24 25 26	23 24 25 26	TX[0] TXD[1] TXD[2] TXD[3]	I/PD I/PD I/PD I/PD	发送数据。
13	19	19	RXC	O/PD	接收时钟。 此管脚提供一个连续的时钟作为RXD[3:0]和RXDV信号的工作时钟。 RXC在100Mbps模式下是25MHz，10Mbps模式下是2.5MHz。
27	38	38	COL	O/PD	冲突检测。 当介质上检测一个冲突时，COL为高电平。
26	36	36	CRS/ CRS_DV	O/PD	载波检测。 如果介质不在空闲状态，此管脚信号有效。
8	13	13	RXDV	LI/O/PD	接收数据有效。 在RXC上升沿时有效。 一个内部的下拉电阻设置芯片工作于MII模式的默认值；外部的4.7KΩ的上拉电阻设置芯片工作于RMII模式。 电源上电加载成功后，该管脚作为接收数据有效的管脚来工作。

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	符号	类型	说明
9 10 - 11	14 16 17 -	14 16 17 -	RXD[0] RXD[1] RXD[2] RXD[2]/ INTB	O/PD LI/O/PD O/PD O/PD	接收数据。 在RXC上升沿时有效。 注1：RXD[1]内部的下拉电阻设置芯片工作于默认的LED功能；外部的4.7KΩ的上拉电阻使能SR8201F启用WOL功能。 注2：SR8201F的11管脚名为RXD[2]/INTB。当在RMII模式下，此管脚可用于中断功能。见表9的INTB描述。
12	18	18	RXD[3]/ CLK_CTL	LI/O/PD	接收数据。 同时RXD[3]/CLK_CTL也是RMII模式下的时钟设置脚：. 1：REF_CLK输入模式； 0：REF_CLK输出模式； 一个内部的下拉电阻设置REF_CLK为默认的输出模式。
28	39	39	RXER/ FXEN	LI/O/PD	接收数据错误。 如果一个5B的解码器错误产生，例如，无效的/J/K/，无效的/T/R/，甚至无效的符号，此管脚将会拉高。 同时此管脚用于介质的工作模式设置： 1：Fiber模式； 0：UTP模式； 一个内部的下拉电阻设置芯片工作于默认的UTP模式。外部的 4.7KΩ上拉电阻设置芯片工作于Fiber模式。 电源上电加载成功后，此管脚为接收错误管脚。

2. RMII 接口

表 2.RMII 接口

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	符号	类型	说明
15	22	22	TXC	IO/PD	接收和发送的50MHz参考时钟。输入输出方向由页7寄存器16设定。 默认值为参考时钟输出模式.
26	36	36	CRS/ CRS_DV	O/PD	载波/接收数据有效。
20	27	27	TXEN	I/PD	发送启用。
16，17	23，24	23，24	TXD[0:1]	I/PD	发送数据。

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	符号	类型	说明
9，10	14，16	14，16	RXD[0:1]	O/PD	接收数据。
28	39	39	RXER/FXEN	LI/O/PD	接收错误。

3. 串行管理接口

表 3.串行管理接口

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	符号	类型	说明
22	30	30	MDC	I/PU	管理数据时钟。 此管脚提供了一个到MDIO的同步时钟，它可以是与发送TXC和接受RXC的异步时钟。此时钟频率最高可达2.5MHz。内部的一个弱的上拉电阻防止总线浮空。
23	31	31	MDIO	IO/PU	管理数据输入/输出。 此管脚提供了双向信号用于传输管理信息

4. 时钟接口

表 4.时钟接口

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	符号	类型	说明
32	43	43	CKXTAL2	IO	25MHz 晶振输出。 此管脚提供了25MHz晶振输出。 如果使用外部的25MHz/50MHz振荡器或者时钟，振荡器或者时钟输出连接CKXTAL2管脚。
31	42	42	CKXTAL1	I	25MHz晶振输入。 此管脚提供了25MHz晶振输入。 当一个外部的振荡器或者时钟输出连接CKXTAL2管脚时，此管脚必须与地短路。

5. 10M/100M 网络接口

表 5.10M/100M 网络接口

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	符号	类型	说明
3 4	1 2	1 2	MDI+[0] MDI-[0]	IO	差分发送输出对。 100Base-TX，100Base-FX和10Base-T模式共用。当配置为100Base-TX，输出是MLT-3编码器波形；当配置为100Base-FX，输出是伪ECL级。
5 6	4 5	4 5	MDI+[1] MDI-[1]	IO	差分接收输入对。 100Base-TX，100Base-FX和10Base-T模式共用。

6. 发送偏置接口

表 6.发送偏置接口

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	符号	类型	说明
1	46	1	RSET	I	偏置电阻输入。 此管脚应该通过一个2.49KΩ (1%)电阻接地，以决定发送DAC的驱动电流。

7. 设备配置接口

表 7.设备配置接口

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	符号	类型	说明
8	13	13	RXDV	LI/O/PD	接收数据有效。 在RXC上升沿时有效。 一个内部的下拉电阻设置芯片工作于MII模式的默认值；外部的4.7KΩ的上拉电阻设置芯片工作于RMII模式。 电源上电加载成功后，该管脚作为接收数据有效的管脚来工作。
10	16	16	RXD[1]	LI/O/PD	一个内部的下拉电阻设置芯片工作于默认的LED功能；外部的4.7KΩ的上拉电阻使能SR8201F启用WOL功能。
12	18	18	RXD[3]/ CLK_CTL	LI/O/PD	接收数据。 同时RXD[3]/CLK_CTL也是RMII模式下的时钟输入输出设置脚：. 1：REF_CLK输入模式； 0：REF_CLK输出模式； 一个内部的下拉电阻设置REF_CLK为默认的输出模式。

<table>
<tr><th>Pin No (8201F)</th><th>Pin No (8201FL)</th><th>Pin No (8201FN)</th><th>符号</th><th>类型</th><th>说明</th></tr>
<tr><td>28</td><td>39</td><td>39</td><td>RXER/
FXEN</td><td>LI/O/PD</td><td>接收数据错误。
如果一个5B的解码器错误产生，例如，无效的/J/K/，无效的/T/R/，甚至无效的符号，此管脚将会拉高。
同时此管脚用于介质的工作模式设置：
1：Fiber模式；
0：UTP模式；
一个内部的下拉电阻设置芯片工作于默认的UTP模式。外部的 4.7KΩ上拉电阻设置芯片工作于Fiber模式。
电源上电加载成功后，此管脚为接收错误管脚。</td></tr>
<tr><td>-

24

25

-</td><td>34

-

35

-</td><td>34

-

35

32</td><td>LED0/
PHYAD[0]

LED0/
PHYAD[0]/
PMEB

LED1/
PHYAD[1]

LED2/
PHYAD[2]</td><td>LI/O/
PU

LI/O/
PU

LI/O/
PD

LI/O/
PD</td><td>网络状态LED指示和PHY地址设置。默认可用的PHY地址是：
SR8201F：00000~00011；
SR8201FL：
00100~00111 (当PMEB管脚被拉高)
00000~00011 (当PMEB管脚被拉低)
SR8201FN：00000~00111.
不同设置下LED功能：
<table>
<tr><td>LED_Sel</td><td>00</td><td>01</td><td>10</td><td>11</td></tr>
<tr><td>LED0</td><td>ACT_{ALL}</td><td>$Link_{ALL}$/ ACT_{ALL}</td><td>$Link_{10}$ / ACT_{ALL}</td><td>$LINK_{10}$ /ACT_{10}</td></tr>
<tr><td>LED1</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$/ ACT_{100}</td></tr>
<tr><td>LED2</td><td>保留</td><td>保留</td><td>保留</td><td>保留</td></tr>
</table>
注：LED_Sel默认值为11。
RXD[1]管脚内部弱的下拉电阻设置SR8201F 的LED0为默认值的LED功能；外部4.7KΩ的上拉电阻设置LED0管脚为启用WOL功能。
当WOL功能启用时，PHY地址必须是 00001或者00011。LED1功能为：
<table>
<tr><td>LED_Sel</td><td>00</td><td>01</td><td>10</td><td>11</td></tr>
<tr><td>LED1</td><td>LINK 100</td><td>LINK 100</td><td>LINK 100</td><td>LINK100/ ACT100</td></tr>
</table></td></tr>
</table>

8. 电源地管脚

表 8.电源地管脚

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	符号	类型	说明
7，30	6，41	21	AVDD33	P	3.3V模拟电源输入。 3.3V模拟电路电源。
14	15，21，37	-	DVDD33	P	3.3V数字电源输入。 3.3V数字电路电源。
-	28	11	DVDD10	P	1.1V数字电源。
2	48	24	AVDD10OUT	O	模拟电源输出。 需要连接一个0.1μF的陶瓷电容。 连接方式描述在第35页，3.3V电源和电压转换电路。
29	40	40	DVDD10OUT	O	数字电源输出。 需要连接一个0.1μF的陶瓷电容。 连接方式描述在第35页，3.3V电源和电压转换电路。
E-PAD	7, 20,33,47	E-PAD	GND	P	地 需要连接到一个较大的地平面。数字和模拟的地共用一个E-Pad。

9. 复位管脚

表 9.复位管脚

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	符号	类型	说明
7，30	6，41	21	PHYRSTB	I/HZ	低电平复位输入 为了保证一次完整的复位，此管脚必须保持低至少10ms。 注：WOL功能启用时，保持管脚为高电平（仅SR8201FN）。
14	15，21，37	-	INTB	O/OD	中断 如果链接状态改变、双工模式改变或者自协商失败，该管脚输出低电平表示有效的中断。 此管脚是一个漏极开路设计，并且默认值应通过4.7KΩ外部电阻拉高。如果没有使用，保持浮空。

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	符号	类型	说明
-	28	11	RXD[2]/INTB	O/PD	中断 如果链接状态改变、双工模式改变或者自协商失败，该管脚输出低电平表示有效的中断。 此管脚是一个漏极开路设计，并且默认值应通过4.7KΩ外部电阻拉高。如果没有使用，保持浮空。 备注：此管脚的中断功能仅在RMII模式可用。
2	48	24	PMEB	O/OD	电源管理启用。 如果接收到一个魔术封包或者唤醒帧，该管脚输出低电平表示有效的电源管理状态。

10. NC（未连接）管脚

表 10.NC（未连接）管脚

Pin No (8201F)	Pin No (8201FL)	Pin No (8201FN)	符号	类型	说明
-	3，8，9，11，44，45	3，7，8，9，10，44，45，47	NC	-	未连接

I=输入，**O**=输出，**I/O**=输入/输出，**I/PD**=输入带下拉，**I/PU**=输入带上拉，**HZ**=高阻，

LI=上电或复位后加载输入，**OD**=开漏输出，**P**=电源

寄存器描述

本章描述寄存器功能与使用。本章用到的简称说明如下：

RW ：可读可写
RO ：只读
RC ：读清除
EFUS ：从EFuse加载
RW/LI ：可读可写，复位加载
RW/SC ：可读可写，自清除
SC ：自清除

表 11.寄存器 0 基本模式控制寄存器

地址	名称	描述	模式	默认值
0:15	Reset	软件复位。此位带自清除功能，复位完成后恢复为 0。 1:软件复位 0:正常工作 软件复位（设置 bit15 为 1）会将寄存器 0 和寄存器 1 恢复为默认值，同时此行为将改变内部 PHY 的状态和与 PHY 物理连接设备的相关状态。	RW/ SC	0
0:14	Loopback	loopback 设置发送到接收数据路径。 1：启用 loopback 0：正常工作	RW	0
0:13	Speed Selection	网络速度 1:100Mbps 0:10Mbps 在完成自协商完成后，此位表示当前速度状态： 1：100Base-T 0：10Base-T 当 100Base-FX 模式启用，此位等于 1 且只读。	RW	1
0:12	Auto Negotiation Enable	自协商功能 1：启用自协商；bits13 和 8 将被忽略； 0：禁用自协商；bits13 和 8 将确定链接速度和数据传输模式。 当 100Base-FX 模式启用，此位等于 0 且只读。	RW	1
0:10	Isolate	隔离 1：从 MII/RMII 接口隔离 PHY。PHY 依旧能够响应 MDC/MDIO； 0：正常工作。	RW	0

地址	名称	描述	模式	默认值
0:11	Power Down	Power Down 此位关闭 PHY 芯片的内部电源，包括内部晶振电路。 MDC，MDIO 依旧允许 MAC 访问。 1：电源休眠 0：正常工作	RW	0
0:9	Restart Auto Negotiation	重启自协商 1：重启自协商 0：正常工作	RW/ SC	0
0:8	Duplex Mode	如果自协商被禁用(bit0:12=0)，此位设置双工模式： 1：全双工 0：半双工 自协商使能且在自协商完成之后，此位指示双工状态： 1：全双工 0：半双工	RW	1
0:7	Collision Test	碰撞测试 1：碰撞测试启用 0：正常运行 当设置的时候，此位将引起 COL 信号在 TXEN 中在 512-bit 时间内有效.COL 信号将会失效在 4-bit 时间内，回应给 RXEN 失效.	RW	0
0:6~0	Reserved	保留	-	-

表 12.寄存器 1 基本模式状态寄存器

地址	名称	描述	模式	默认值
1:15	100Base-T4	1：支持启用 100Base-T4 0：不支持 100Base-T4	RO	0
1:14	100Base_TX_FD	1：支持启用 100Base-TX 全双工 0：不支持 100Base-TX 全双工	RO	1
1:13	100Base_TX_HD	1：支持启用 100Base-TX 半双工 0：不支持 100Base-TX 半双工	RO	1
1:12	10Base_T_FD	1：支持启用 10Base-T 全双工 0：不支持 10Base-T 全双工	RO	1
1:11	10_Base_T_HD	1：支持启用 10Base-T 半双工 0：不支持 10Base-T 半双工	RO	1
1:10~7	Reserved	保留	-	-

地址	名称	描述	模式	默认值
1:6	MF Preamble Suppression	SR8201F/FL/FN 允许接收前导抑制的管理帧。	RO	1
1:5	Auto Negotiation Complete	1:自协商过程完成 0:自协商过程未完成	RO	0
1:4	Remote Fault	1:检测到远程错误情况（读取清除） 0:未检测到远程错误情况 当在 100Base-FX 模式下，此位意味着检测到信号的远端错误（见 8.10，第 37 页，远端错误指示）。	RC	0
1:3	Auto-Negotiation Ability	1：PHY 能执行自协商 0：PHY 不能执行自协商	RO	1
1:2	Link Status	1：已建立有效链接 0：未建立有效链接 此位指明从最后一次读取时，链接是否丢失。对现在的链接状态，读取寄存器两次.	RO	0
1:1	Jabber Detect	1：检测到 Jabber 条件 0：未检测到 jabber 条件	RO	0
1:0	Extended Capability	1：延伸寄存器能力 0：无延伸寄存器能力	RO	1

表 13.寄存器 2 PHY 标识寄存器 1

地址	名称	描述	模式	默认值
2:15~0	OUI	分别到 OUI 的第 6 到第 21 位组织唯一识别符 。	RO	001Ch

表 14.寄存器 3 PHY 标识寄存器 2

地址	名称	描述	模式	默认值
3:15~10	OUI_LSB	分配到 OUI 的第 0 到 5 位。	RO	110010
3:9~4	Model Number	型号	RO	000001
3:3~0	Revision Number	版本号	RO	0110

表 15.寄存器 4 自协商消息寄存器(ANAR)

此寄存器包括此设备要在自协商期间发送到链路伙伴的自协商能力

地址	名称	描述	模式	默认值
4:15	Next Page	下页字节 0：发送首要能力数据页 1：发送协议规则数据页	RW	0
4:14	Acknowledge	1：确认接收到链路伙伴能力数据字 0：未接收到确认信号	RO	0
4:13	Remote Fault	1：通知远程错误检测能力 0：不通知远程错误检测能力	RW	0
4:12	Reserved	保留	-	-
4:11	Asymmetric PAUSE	1：支持通知非对称暂停 0：不支持非对称暂停	RW	0
4:10	Pause	保留	RW	0
4:9	100Base-T4	1：本地节点支持 100Base-T4 0：本地节点不支持 100Base-T4	RO	0
4:8	100Base-TX-FD	1：本地节点支持 100Base-TX 全双工 0：本地节点不支持 100Base-TX 全双工	RW	1
4:7	100Base-TX	1：本地节点支持 100Base-TX 0：本地节点不支持 100Base-TX	RW	1
4:6	10Base-T-FD	1：本地节点支持 10Base-T 全双工 0：本地节点不支持 10Base-T 全双工	RW	1
4:5	10Base-T	1：本地节点支持 10Base-T 0：本地节点不支持 10Base-T	RW	1
4:4~0	Selector Field	此节点支持二进制编码选择器.目前只有 CSMA/CD 00001 是特殊.没有其他协议支持.	RO	00001

表 16.寄存器 5 自协商链路伙伴能力寄存器(ANLPAR)

此寄存器在自协商期间接收链路伙伴的消息能力。如果支持下一页功能，在一次成功的自协商之后内容改变.

地址	名称	描述	模式	默认值
5:15	Next Page	下页字节 0：发送首要能力数据页 1：发送协议规则数据页	RO	0
5:14	Acknowledge	1：链路伙伴确认接收到链路伙伴能力数据字 0：未接收到确认信号	RO	0
5:13	Remote Fault	1：链路伙伴指明一个远程错误 0：链路伙伴未指明一个远程错误	RO	0

地址	名称	描述	模式	默认值
5:12	Reserved	保留	-	-
5:11	Asymmetric Pause	1：链路伙伴支持非对称流量控制 0：当自协商启用，表示链路伙伴不支持非对称流量控制。此字节指示链路伙伴能力。	RO	0
5:10	Pause	1：链路伙伴支持流量控制 0：当自协商启用，表示链路伙伴不支持流量控制。此字节指示链路伙伴能力。	RO	0
5:9	100Base-T4	1：链路伙伴支持 100Base-T4 0：链路伙伴不支持 100Base-T4	RO	0
5:8	100Base-TX-FD	1：链路伙伴支持 100Base-TX 全双工 0：链路伙伴不支持 100Base-TX 全双工	RO	0
5:7	100Base-TX	1：链路伙伴支持 100Base-TX 0：链路伙伴不支持 100Base-TX	RO	0
5:6	10Base-T-FD	1:链路伙伴支持 10Base-T 全双工 0:链路伙伴不支持 10Base-T 全双工	RO	0
5:5	10Base-T	1:链路伙伴支持 10Base-T 0:链路伙伴不支持 10Base-T	RO	0
5:4~0	Selector Field	链路伙伴的二进制编码节点选择器.目前只有 CSMA/CD 00001 是特殊的	RO	00001

表 17.寄存器 6 自协商扩展寄存器(ANER)

此寄存器包含 Nway 自协商的额外状态.

地址	名称	描述	模式	默认值
6:15~5	Reserved	保留	-	-
6:4	Parallel Detection Fault	1：并行检测功能时检测到一个错误 0：并行检测功能时没有检测到错误	RC	0
6:3	Link Partner Next Page Ability	1：链路伙伴有下页能力 0：链路伙伴没有下页能力	RO	0
6:2	Local Next Page Ability	1：本地设备有下页能力 0：本地设备没有下页能力	RO	0
6:1	Page Received	1：收到一个新页 0：未收到一个新页	RC	0
6:0	Link Partner Auto-Negotiation Ability	如果本地设备自协商功能使能，此位意味着： 1：链路伙伴有自协商能力 0：链路伙伴没有自协商能力	RO	0

表 18.第 0 页 寄存器 13 MACR (MMD 访问控制寄存器；地址 0x0D)

位	名称	读写	默认值	描述
13:15~14	Function	WO	0	00:地址 01:数据; 无后期增加 10:数据; 后期读写增加 11:数据; 后期只写增加
13:13~5	Reserved	RO	000000000	保留
13:4~0	DEVAD	WO	0	设备地址

注 1:用于和 MAADR (寄存器 14) 连接来访问到MMD的地址空间

注 2:如果 MAADR访问的是地址 (Function=00)，那它直接指向MMD中的DEVAD指定的地址寄存器。

注 3:如果 MAADR访问的是数据 (Function!=00)，那它访问的是DEVAD区域和MMD地址寄存器 指向的MMD寄存器的数据。

表 19.第 0 页 寄存器 14 MAADR (MMD 访问地址数据寄存器；地址 0x0E)

位	名称	读写	默认值	描述
14:15~0	Address Data	RW	0x0000	13.15:14=00 à MMD和DEVAD的地址寄存器 13.15:14=01，10，or 11 à MMD和DEVAD的数据寄存器，由他的地址寄存器的内容指出

备注:用于和 MACR (寄存器 13)连接去提供访问到 MMD 的地址空间

表 20.寄存器 24 电源省电模式寄存器(PSMR)

地址	名称	描述	模式	默认值
15	Enpwrsave	开启电源省电模式 此位可以通过软件复位来返回到默认值	RW	1
14~0	Reserved	保留	-	-

备注:RMII 输出模式需要 REF_CLK 的输出时钟，LDPS (链接断开省电功能)必须禁用 (见 表 43，第 36 页).

表 21.寄存器 28 光纤模式和 Loopback 寄存器

地址	名称	描述	模式	默认值
28:15~6	Reserved	保留	-	-
28:5	Fxmode	光纤模式	RW	0
28:4~3	Reserved	保留.	-	-
28:2	En_autoMDIX	自动 DIX 功能	RW	1

地址	名称	描述	模式	默认值
28:1	Force_MDI	强制 MDI/MDIX 模式 如果自动 MDIX 功能为禁止： 1：强制 MDI 0：强制 MDIX	RW	1
28:0	Reserved	保留	-	-

表 22.寄存器 30 中断指示器和 SNR 显示寄存器

地址	名称	描述	模式	默认值
30:15	Anerr	自协商错误中断 1：启用 0：禁用	RC	0
30:14	Spdchg	速度模式改变中断 1：启用 0：禁用	RC	0
30:13	Duplexchg	双工模式改变中断 1：启用 0：禁用	RC	0
30:12	Reserved	保留	-	-
30:11	Linkstatusch g	链接状态改变中断 1：启用 0：禁用	RC	0
30:10~4	Reserved	保留	-	-
30:3~0	SNR_O	这4位显示信噪比的值	RO	0000

表 23.寄存器 31 页选择寄存器

地址	名称	描述	模式	默认值
31:15~8	Reserved	保留	-	-
31:7~0	PAGE SEL	选择页地址:00000000~11111111.	RW	00000000

表 24.第 4 页 寄存器 16 EEE 能力启用寄存器

地址	名称	描述	模式	默认值
16:15~14	Reserved	保留	-	-
16:13	EEE_10_cap	启用EEE 10M能力	RW	1
16:12	EEE_nway_en	启用自协商时的EEE 100M下页交换	RW/ EFUS	1
16:11~10	Reserved	保留	-	-
地址	名称	描述	模式	默认值

16:9	Tx_quiet_en	启用当TX在安静状态下关闭100M TX的能力。 当EEE启用时，此位建议设置为1。	RW/ EFUS	1
16:8	Rx_quiet_en	启用当RX在安静状态下关闭100M RX的能力。 当EEE启用时，此位建议设置为1。	RW/ EFUS	1
16:7:0	Reserved	保留	-	-

表 25.第 4 页 寄存器 21 EEE 能力寄存器

地址	名称	描述	模式	默认值
21:15~13	Reserved	保留	-	-
21:12	Rg_dis_ldvt	设置为1时，禁用模拟电路的线驱动。	RW	0
21:11~1	Reserved	保留	-	-
21:0	EEE_100_cap	自协商结果指示链路伙伴支持 EEE 100M.	RO	0

表 26.第 7 页 寄存器 16 RMII 模式设置寄存器(RMSR)

地址	名称	描述	模式	默认值
16:15~13	Reserved	保留	-	-
16:12	Rg_rmii_clkdir	此位设置RMII模式下TXC的输入输出： 0：输出 1：输入	RW/LI	0
16:11~8	Rg_rmii_tx_offset	调节RMII TX接口时序	RW/EFUS	1111
16:7~4	Rg_rmii_rx_offset	调节RMII RX接口时序	RW/EFUS	1111
16:3	Reserved	保留	RW/LI	0
16:2	Rg_rmii_rxdv_sel	0：CRS/CRS_DV管脚是CRS_DV信号 1：CRS/CRS_DV管脚是RXDV信号	RW/EFUS	0
16:1	Rg_rmii_rxdsel	0：仅RMII数据 1：有SSD错误的RMII数据	RW/EFUS	1
16:0	Reserved	保留	-	-

表 27.第 7 页 寄存器 17 自定义 LEDs 设置寄存器

此寄存器用于设置自定义 LED 功能。下表展示了自定义 LED 的矩阵表

表 27.1. 自定义 LED 矩阵表

链接状态 / LED	LINK		ACT
	10M	100M	
LED0	Bit0	Bit1	Bit3
LED1	Bit4	Bit5	Bit7
LED2	Bit8	Bit9	Bit11

LED Pin	ACT=0	ACT=1
LINK=0	悬空	All Speed ACT
LINK>0	Selected Speed LINK	Selected Speed LINK+ACT

备注:SR8201F/FL仅支持LED0和LED1.SR8201FN支持LED0，LED1和 LED2.

表 27.2. Page7 Register 17 Customized LEDs Setting Register

地址	名称	描述	模式	默认值
17:15~12	Reserved	保留.	-	-
17:11~8	LED_sel2	当设置第7页 寄存器19Bit3为1时，设定LED2自定义功能	RW/ EFUS	0000
17:7~4	LED_sel1	当设置第7页 寄存器19Bit3为1时，设定LED1自定义功能	RW/ EFUS	0000
17:3~0	LED_sel0	当设置第7页 寄存器19Bit3为1时，设定LED0自定义功能	RW/ EFUS	0000

表 28.第 7 页 寄存器 18 EEE LEDs 启用寄存器

地址	名称	描述	模式	默认值
18:15~3	Reserved	保留	-	-
18:2	EEE_LED_en2	启用 EEE/LPI 模式下 LED2 功能	RW	0
18:1	EEE_LED_en1	启用 EEE/LPI 模式下 LED1 功能	RW	0
18:0	EEE_LED_en0	启用 EEE/LPI 模式下 LED0 功能	RW	0

表 29.第 7 页 寄存器 19 中断、WOL 和 LED 功能寄存器

地址	名称	描述	模式	默认值
19:15~14	Reserved	保留	-	-
19:13	Int_linkchg	启用链接变化中断 1：允许链接变化产生中断 0：禁止链接变化产生中断 此位设置为0时仅在INTB管脚屏蔽链接变化中断事件； 寄存器30 Bit11总是反映链接变化中断行为。	RW	0
19:12	Int_dupchg	启用双工变化中断 1：允许链接变化产生中断 0：禁止链接变化产生中断 此位设置为0时仅在INTB管脚屏蔽双工变化中断事件； 寄存器30 Bit13总是反映双工变化中断行为。	RW	0

地址	名称	描述	模式	默认值
19:11	Int_anerr	启用自协商错误中断 1：允许自协商错误产生中断 0：禁止自协商错误产生中断 此位设置为0时仅在INTB管脚屏蔽自协商错误中断事件；寄存器30 Bit15总是反映自协商错误中断行为。	RW	0
19:10	Rg_led0_wol_sel	LED、Wake-On-LAN功能选择(仅SR8201F) 1：Wake-On-LAN功能启用 0：LED功能启用 RXD[1]的一个内部弱下拉电阻将其设置为默认的LED功能；用一个外部4.7KΩ上拉高电阻可以设置SR8201F启用WOL功能。	RW/LI	0
19:9~6	Reserved	保留	-	-
19:5~4	LED_sel[1:0]	传统LED功能选择 LED_sel / LED0 / LED1 / LED2 00 / ACT_{ALL} / $Link_{100}$ / Reserved 01 / $Link_{ALL}/ACT_{ALL}$ / $Link_{100}$ / Reserved 10 / $Link_{10}/ACT_{ALL}$ / $Link_{100}$ / Reserved 11 / $Link_{10}/ACT_{10}$ / $Link_{100}/ACT_{100}$ / Reserved	RW/ EFUS	11
19:3	Customized_LED	自定义LED启用 1:自定义LED功能启用 0:自定义LED功能禁用 见4.7节 自定义LED功能说明。	RW/ EFUS	0
19:2~1	Reserved	保留	-	-
19:0	En10mlpi	启用10M LPI LED功能	RW	0

表 30.第 7 页 寄存器 20 MII TX 隔离寄存器

地址	名称	描述	模式	默认值
20:15	Rg_tx_isolate_en	当TX空闲，隔离MII TX路径信号	RW	0
20:14~0	Reserved	保留	-	-

表 31.第 7 页 寄存器 24 扩展频谱时钟寄存器

地址	名称	描述	模式	默认值
24:15~1	Reserved	保留.	-	-
24:0	Rg_dis_ssc	0：SSC功能启用 1：SSC功能禁用	RW	0

表 32.MMD 映射寄存器与定义

注：MMD 寄存器地址位于第 0 页 寄存器 13 和寄存器 14

Device	Offset	Access	Name	Description
3	0	RW	EEEPC1R	EEE PCS控制1寄存器
3	1	RO/RO，LH	EEEPS1R	EEE PCS状态控制1寄存器
3	20	RO	EEECR	EEE能力寄存器
3	22	RC	EEEWER	EEE唤醒错误寄存器
7	60	RW	EEEAR	EEE通知寄存器
7	61	RO	EEELPAR	EEE链路伙伴能力寄存器

注:LH:加载为高

表 33.EEEPC1R（PCS 控制 1 寄存器，MMD 设备 3，地址 0x00）

地址	名称	描述	模式	默认值
3:0:15~11	Reserved	保留	RW	0
3:0:10	Clock Stop Enable	1：PHY在LPI时停止RXC时钟 0：RXC时钟不停止	RW	0
3:0:9~0	Reserved	保留	RW	0

表 34.EEEPS1R（PCS 状态 1 寄存器，MMD 设备 3，地址 0x01）

地址	名称	描述	模式	默认值
3:1:15~12	Reserved	保留	RO	0
3:1:11	TX LPI Received	1：TX PCS接收到LPI 0：未接收到LPI	RO，LH	0
3:1:10	RX LPI Received	1：RX PCS接收到LPI 0：未接收到LPI	RO，LH	0
3:1:9	TX LPI Indication	1：TX PCS正在接收LPI 0：TX PCS没有正在接收LPI	RO	0
3:1:8	RX LPI Indication	1：RX PCS正在接收LPI 0：RX PCS没有正在接收LPI	RO	0
3:1:7	Reserved	保留	RO	0
3:1:6	Clock Stop Capable	1：MAC在LPI中停止TXC 0：TXC不能停止	RO	1
3:1:5~0	Reserved	保留	RO	0

表 35.EEECR（EEE 能力寄存器，MMD 设备 3；地址 0x14）

地址	名称	描述	模式	默认值
3:20:15~2	Reserved	保留.	RO	0
3:20:1	100Base-TX EEE	1：支持100Base-TX下的EEE 0：不支持100Base-TX下的EEE	RO	1
3:20:0	Reserved	保留.	RO	1

表 36.EEECR（EEE 能力寄存器，MMD 设备 3；地址 0x14）

地址	名称	描述	模式	默认值
3:22:15~0	EEE Wake Error Counter	支持EEE功能的PHY唤醒错误计数。在指定PHY类型的要求时间内没有完成正常的唤醒序列的错误	RC	0

表 37.EEEAR（EEE 通知寄存器，MMD 设备 7；地址 0x3c）

地址	名称	描述	模式	默认值
7:60:15~3	Reserved	保留.	RW	0
7:60:1	100Base-TX EEE	通知100Base-TX EEE的能力 1：通知 0：不通知	RW	1
7:60:0	Reserved	保留	RW	0

表 38.EEELPAR（EEE 链路伙伴能力寄存器，MMD 设备 7；地址 0x3d）

地址	名称	描述	模式	默认值
7:61:15~3	Reserved	保留	RO	0
7:61:1	LP 100Base-TX EEE	1：链路伙伴有100Base-TX EEE的能力 0：链路伙伴没有100Base-TX EEE的能力	RO	0
7:61:0	Reserved	保留	RO	0

功能描述

SR8201F/FL/FN 是一款以太网物理层收发器芯片，它集成了 10Base-T、100Base-TX 和 100Base-FX 功能，以及额外的电源管理特性。具体功能如下：

- 有MDC/MDIO管理接口的MII接口与MAC通信
- IEEE 802.3u第28条款自协商能力
- 速度，双工，自协商能力通过线或者MDC/MDIO配置
- 支持省电模式
- 4B/5B转换
- 扰码、解扰
- NRZ到NRZI，NRZI到MLT-3
- 10Base-T下曼彻斯特码的编码和解码
- 时钟和数据恢复
- 自适应均衡器
- 自动极性矫正
- 光纤模式下的远端错误检测（FEFI）
- 网络状态指示LED等
- 网络唤醒（WOL）
- 节能以太网（EEE）
- RMII模式时钟输出扩展频谱（SSC）

1.MII 及管理接口

1.1.数据传输

MII（介质无关接口）是一个 IEEE802.3u 标准定义，介于 PHY 层和 MAC 层之间的信号接口。

此接口有两个工作频率： 25MHz 和 2.5MHz，分别支持 100Mbps/10Mbps 带宽下的收发功能。

发送

MAC 使能 TXEN 信号，然后产生 4-Bits 半字节数据通过 TXD[3:0]发往 PHY。PHY 提供同步时钟 TXC，在 TXEN 有效期间同步采样 TXD[3:0]。

接收

PHY 能 RXDV 信号，用 PHY 提供的同步时钟 RXC 把接收到的半字节数据发往 RXD[3:0]。CRS 和 COL 信号用于冲突检测及载波指示。

在 100Base-TX 模式下，当 5B 解码信号为非空闲时，CRS 信号将为有效。当 5B 被识别出为空闲时，它将为无效。在 10Base-T 模式下，当 10M 前导被确定，CRS 将为有效；当空闲向量被确定，它将为无效。

在 100Base-TX 模式下，当 5B 解码为/J/K/时，RXDV 信号将为有效；如果 5B 解码为/T/R/或者空闲时，它将为无效。在 10Mbps 模式下，RXDV 信号与 CRS 信号相同。

如果任意的 5B 解码错误产生，RXER(接收错误)将为有效，例如，一个无效的 J/K，无效的 T/R 或者无效的符号。此管脚将高电平一个或多个时钟周期来指出当前帧在某处的错误。

1.2.串行管理接口

MAC 层设备能用 MDC/MDIO 管理接口去控制一组最大为 4（SR8201F/FL）或 8（SR8201FN）个的设备，和不同的 PHY 地址配置（SR8201F/FL 为 00b 到 11b；SR8201FN 为 000b 到 111b）。框架传输 MDC/MDIO 管理接口应该有下表的帧结构。

表 39.管理帧格式

	管理帧域							
	Preamble	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
读	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
写	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

在硬件复位期间，PHYAD[0]和 PHYAD[1]管脚的逻辑电平作为串行管理访问的地址被锁存。管理接口的读写帧结构如下图所示：

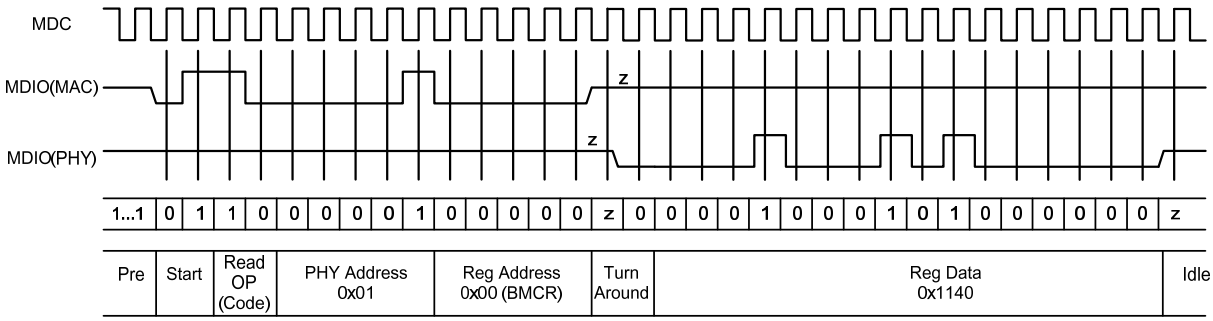


图6.读取周期

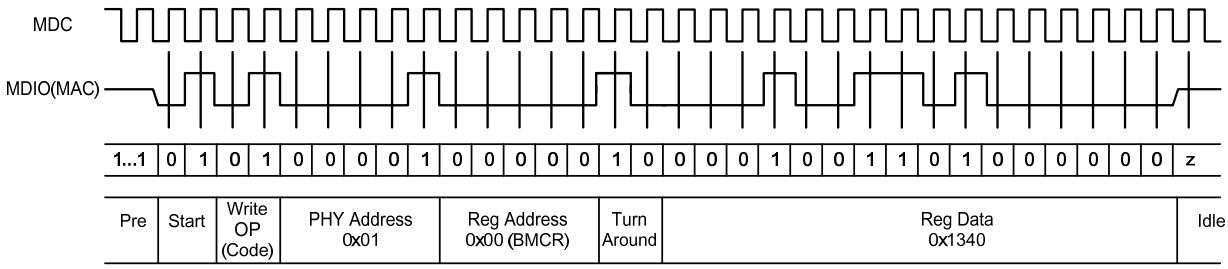


图7.写入周期

表 40.串行管理帧说明

名称	描述
Preamble	帧前导 MAC在MDIO接口上提供32个连续的1及32个MDC时钟。帧前导用来给PHY进行时钟同步。

名称	描述
ST	帧起始 由01向量表示。
OP	操作码 读：10 写：01
PHYAD	PHY地址，共5位 最多可以有4个（SR8201F/FL）或8个（SR8201FN）设备可以连到MAC，通过低2位（SR8201F/FL）或3位（SR8201FN）来选择不同的PHY，其余位必须保持0。
REGAD	寄存器地址 5位的地址可以选择PHY的32个寄存器。
TA	周转 在寄存器地址和数据序列之间的2位信号时间，避免在读传输时出现线控制权争夺。读传输帧时，第一个Bit时间，STA和PHY都保持高阻态，在第二个Bit时间由PHY驱动0电平完成信号周转。 在写传输时，由STA驱动10向量。
DATA	数据 16位的数据
IDLE	空闲 非真正管理帧的一部分，在此期间信号处于高阻状态。PHY的上拉电阻会将MDIO线拉高到逻辑1。

2.中断

无论何时，只要 SR8201F 检测到媒介端的状态改变，就会写入对应中断状态的寄存器（第 0 页 寄存器 14），并且在中断管脚（LED1/INTB 管脚 21）使能时，中断管脚会被置低表示发生一个中断事件。当 MAC 检测到中断事件时，可以通过 MDC/MDIO 端口访问到第 0 页寄存器 14 获取相应的中断状态。

一旦这些状态寄存器第 0 页寄存器 30 通过 MDC/MDIO 被 MAC 读取后，INTB 为无效状态。SR8201FN/FL 中断功能使得 MAC 无需通过 MDC/MDIO 管理接口连续轮询。

注1：当RMII模式下，SR8201F的RXD[2]/INTB管脚(Pin11)仅用作中断功能。

注2：中断功能默认被禁用。如需启用此功能，参见中断启用功能寄存器。

3.自协商及并行检测

SR8201F 支持 IEEE 802.3u 第 28 条款描述的自协商功能，它可与任何其它支持该功能的收发器进行协商。SR8201F 能自动检测链路伙伴的能力，并且决定两设备之间可能的最高速度/双工配置。如果链路伙伴不支持自协

商，那么 SR8201F 将启用半双工模式并且进入并行检测模式。SR8201F 将默认传输 FLP(快速链接脉冲)并等待链路伙伴响应。如果 SR8201F 接收到一个 FLP 那么自协商过程将继续；如果接收到一个 NLP(普通链接脉冲)，然后 SR8201F 将改为 10Mbps 半双工模。如果接收 100Mbps 空闲向量，SR8201F 将改为 100Mbps 半双工模式。

3.1 设置介质类型和接口模式

表 41.设置介质类型和接口模式

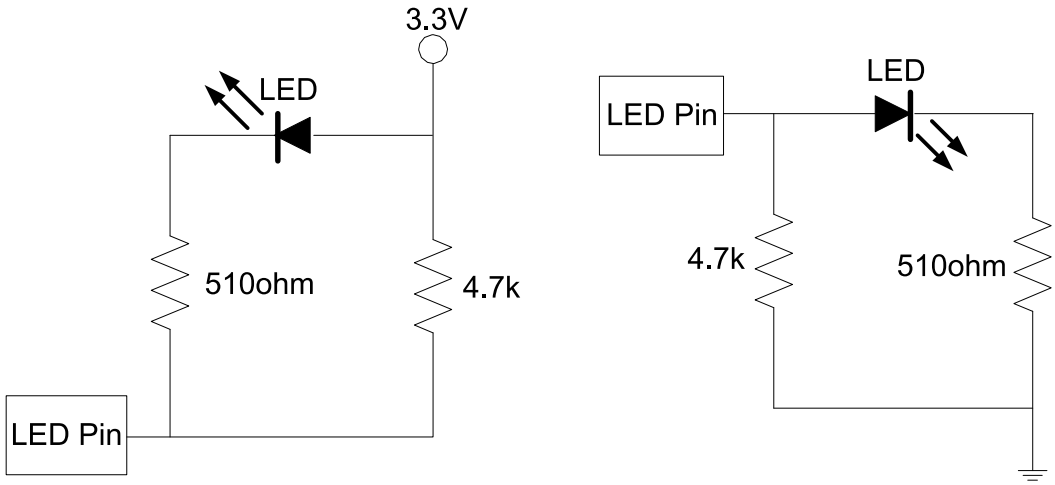
FXEN	RXDV	工作模式
H	L	光纤模式和MII模式
H	H	光纤模式和RMII模式
H	X	光纤模式和MII模式
L	L	UTP模式和MII模式
L	H	UTP模式和RMII模式
L	X	UTP模式和MII模式

4.LED 功能

SR8201FN 支持 3 LED 信号，SR8201F 和 SR8201FL 支持 2 LED 信号，4 种配置运行模式。以下描述 LED 的行为。

4.1.LED 和 PHY 地址

作为 PHYAD[0]和 LED 的输出管脚共用，约束了外部组件的要求，并且 LED 的使用必须仔细考虑以避免冲突。尤其是，当 LED 管脚被用作直接驱动 LED 灯，每一个输出驱动的有效状态是需要根据上电复位时 PHYAD 输入状态来决定。例如，如左图所示，如果一个已知的 PHYAD 输入是外部上拉的，那么同样的输出将会配置为低驱动为有效状态。对于右图而言，我们可以看到一个已知的 PHYAD 输入是外部下拉的，那么同样的输出将会配置为高驱动为有效状态。PHY 地址配置管脚不应该直接接地或 VCC，必须通过一个电阻来拉高/低（典型值 4.7KΩ）。如果不需要驱动 LED，LED 路径的组成（LED+510Ω）可以被移除。



PHY Address[x] = Logical 1
LED指示 = 低有效

PHY Address[x]= Logical 0
LED指示= 高有效

图 8. LED 和 PHY 地址配置

4.2.链接监视器

链接监视器检测链路完整，例如 LINK10，LINK100，LINK10/ACT 或者 LINK100/ACT。无论何时链接状态被建立，指定的链接 LED 管脚被驱动为低电平。一旦一个线缆断开链接，链接 LED 管脚被驱动为高电平，指明没有网络链接存在。

4.3.RX LED

在 10/100M 模式下，RX LED 的闪烁说明设备正在接收数据。

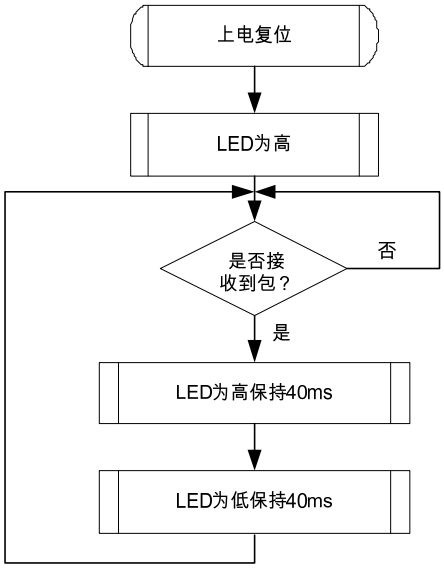


图 9. RX LED

4.4.TX LED

在10/100M模式下，TX LED灯的闪烁说明设备正在发送数据

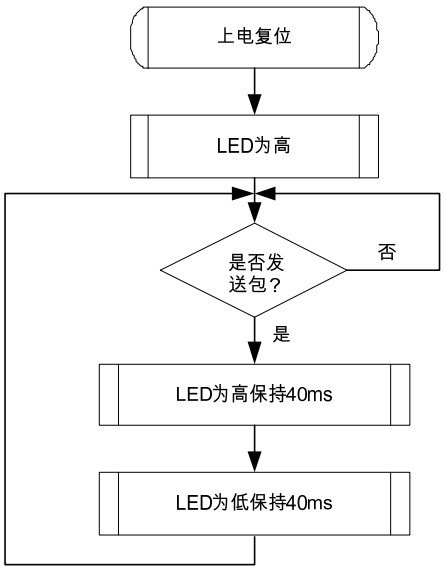


图 10. TX LED

4.5.TX/RX LED

在10/100M模式下，TX/RX LED灯的闪烁说明正在进行接收或发送数据.

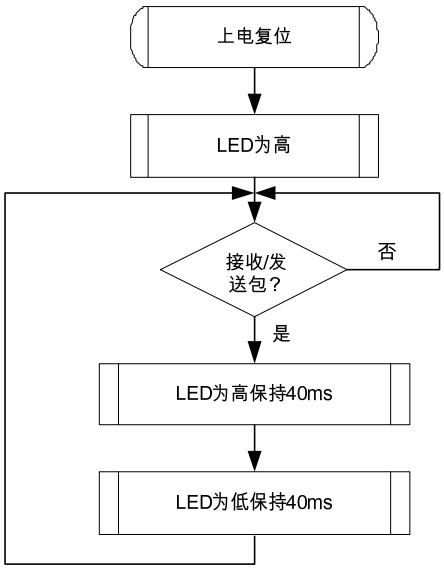


图 11. TX/RX LED

4.6.LINK/ACT LED

在 10/100M 模式下，LINK/ACT LED 灯亮表示链接成功；LED 灯闪烁，表明正在进行接收或发送数据；LED 灯长时间灭表明链接未成功.

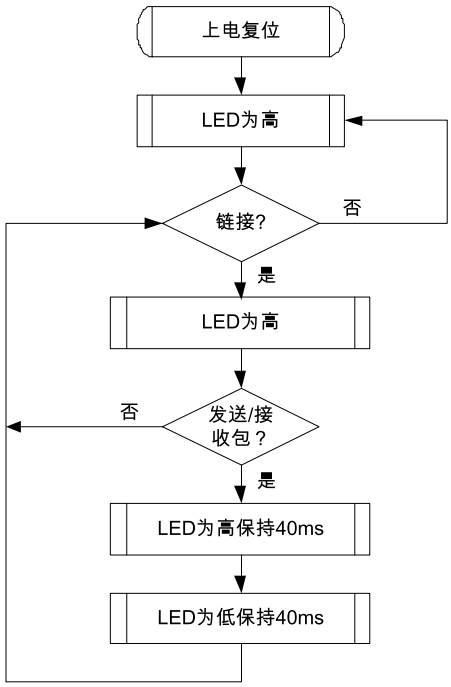


图 12. LINK/ACT LED

4.7 自定义 LED

SR8201F/FL/FN 支持在 10/100Mbps 模式下可编程的 LED。此功能可以通过第 7 页，寄存器 9 第 3 为启用/禁用(如图 13)。参见第 7 页 寄存器 17 的自定义 LED 寄存器设定

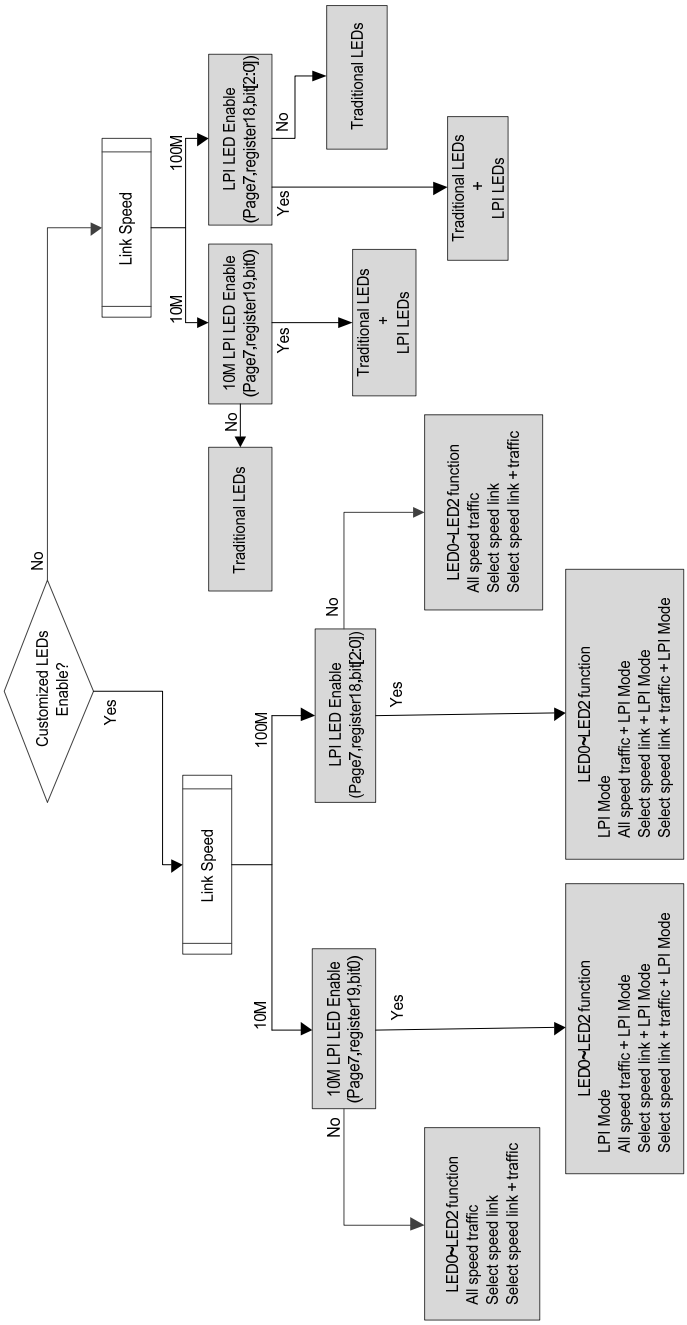


图 13.有/无 LPI LED 模式的自定义 LED

4.8 EEE LED 行为

EEE 空闲模式：LED 连续缓慢的闪烁

EEE 激活模式：LED 快速和缓慢的闪烁（在数据包传送和接收期间）。参见第 7 页 寄存器 18 的 EEE LED 启用设置.

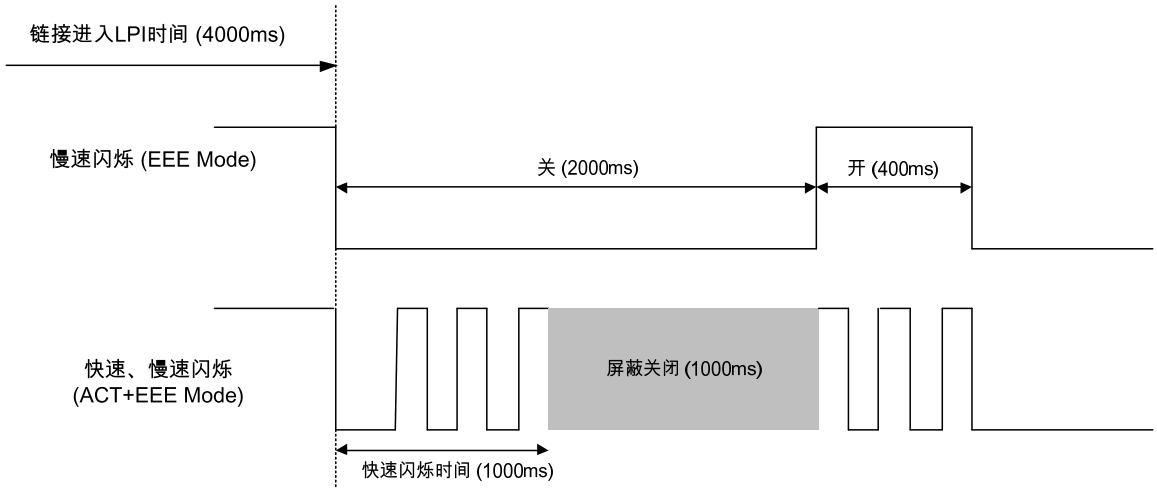


图 14.EEE LED 行为

5.断电和链接断开省电模式

SR8201F 支持两种省电模式。本章节描述如何通过软件实现每一种模式.

表 42.省电模式管脚设置

模式	描述
PWD	设置寄存器0的11位为1，将SR8201F/FL/FN处于断电模式(PWD)。这是最省电的模式，并且SR8201F/FL/FN仍是“活动”。在PWD模式下，SR8201F/FL/FN将关闭除了MDC/MDIO管理接口的所有模拟/数字功能。因此，如果SR8201F/FL/FN处于PWD模式，且MAC想要启用PHY，它必须通过它自己建立MDC/MDIO时序（这可以由软件完成）。
LDPS	设置寄存器24的15位为1，将SR8201F/FL/FN处于LDPS（断连省电）模式。在LDPS模式下，SR8201F/FL/FN将根据检测到的链接状态决定是否关闭传输功能。如果链接断开，FLP、100Mbps空闲向量或10Mbps的NLP将不会被传输。但是会传输一些与NLP相似的信号。一旦接收器检测到电平信号，它将停止信号并再次传输FLP、100Mbps空闲向量或10Mbps的NLP。当链接断开时，可以减少60%~80%的 能耗。

6.10M/100M 发送和接收

6.1.100Base-TX 发送和接收操作

100Base-TX发送

通过 TXD[3:0]接口在 25MHz（TXC）时钟下收到的 4-bit 半字节发送数据，由 4B/5B 编码器将转化为 5B 符号代码。在经过扰码器、串行转换器 转变为 125MHz 的信号，并从 NRZ 转变到 NRZI。在此过程之后，NRZI 信号传送到 MLT-3 编码器，然后发送给链接驱动。发送器首先使 TXEN 有效。在发送数据帧之前，将发送一个/J/K/符号（帧头分界符），然后发送数据符号，最终发送一个/T/R/符号作为帧尾结束符。对于更好的 EMI 性能，种子扰码是基于 PHY 地址的。在集线器和开关环境下，每一个 SR8201F 将有不同的扰码种子然后把 MLT-3 的信号输出延伸开。

100Base-TX 接收

接收信号首先通过自适应均衡器进行补偿，用来弥补由于线缆衰减和码间干扰（ISI）引起的信号失真。基线漂移修正监控过程并且动态修正信号均衡过程。锁相环然后从信号中恢复接收时钟和数据信息。接着，接收信号被采样成 NRZI（双向不归零）数据。下一步是将 NRZI 转换到 NRZ（不归零数据）。再经过数据解扰，串行转并行，5B 到 4B 转换，最后生成 4B 半字节送到 MII 接口。

6.2.100Base-FX 光纤发送和接收操作

SR8201F/FL/FN 能通过硬件配置工作于 100Base-FX 模式下。硬件 100Base-FX 设置优先级别高于 Nway 设置。100Base-FX 中不需要使用扰码器。

100Base-FX发送

TXD 之前的处理如 100Base-TX 一样，除了在 NRZI 阶段之前不含扰码器，NRZI 之后不用转换为如 100Base-TX 中的 MLT-3 信号， 而是将串行数据流驱动为 NRZI PECL 信号，以差分对形式进入光纤收发器。

100Base-FX接收

从 PECL 接口的光纤收发器传入的信号，直接进入时钟恢复电路来恢复数据/时钟。扰码器/解扰器在 100Base-FX 模式时被旁路。

6.3.10Base-T 发送和接收操作

10Base-T发送

通过 TXD[3:0]接口在 2.5MHz（TXC）时钟下收到的 4-bit 半字节发送数据，首先进入并行到串行转换，然后 10Mbps 的 NRZ 信号发送到曼彻斯特编码器。曼彻斯特编码器将 NRZ 数据转换为曼彻斯特编码数据流给 TP 发送器，并在数据的结尾添加一个由 IEEE802.3 协议中指定的起始空闲脉冲（SOI）。.最后，编码数据流经过内嵌的带限滤波器整形并发送出去。

10Base-T接收

在 10Base-T 接收模式下，SR8201F/FL/FN 中的曼彻斯特解码器将接收到的曼彻斯特编码数据流转换为 NRZ 数据，剥离 SOI 脉冲，并恢复出时钟。然后串行 NRZ 数据流转变为并行 4-bit 半字节信号并传送到 RXD[0:3]接口上。

7.复位和传输偏置

这里有两种 SR8201F/FL/FN 复位形式：

1. 硬件复位： PHY 的 RSTB 管脚拉低至少 10ms，然后拉高。PHY 的 RSTB 管脚拉高 150ms 后，才测访问 SR8201F/FL/FN 寄存器。在硬件复位之后，所有的寄存器都将恢复默认值。此时介质接口将断开链接并且重启自协商/并行检测过程。
2. 软件复位：设置寄存器 0 bit 15 为 1。至少等待 20ms 后再访问 SR8201F/FL/FN 寄存器。软件复位仅将部分寄存器复位，然后将芯片状态复位到“初始化”。

RSET 管脚必须通过 1%精度的 2.49KΩ 电阻拉低，以产生一个精准传输偏置。它将影响传输波形的信号质量。并保持它的电路远离其他时钟走线和传输/接收路径，以避免信号干扰。

8.3.3V 电源和电压转换电路

SR8201F/FL/FN 用 0.11μm 的工艺流程制造。核心电路需要 1.1V 的电压，但是，数字 IO 和 DAC 电路需要 3.3V 电源。SR8201F/FL/FN 内嵌的稳压器提供不 3.3V 到 1.1V 的转换。

注：内部线性稳压器输出电源为 1.1V.当使用外部作为内核电源时，必须使用一个 1.05V 的电源。

不建议用外部 1.05V 电源为 SR8201F/FL 供电，因为内部稳压器无法被禁用（SR8201F/FL 没有禁用 1.1V 电源的 EN_LDO_OUT 管脚），内部和外部电源可能发生冲突。

如同很多商业电压转换设备，此电路的 1.1V 输出管脚要求使用输出电容（0.1μF X5R 低 ESR 陶瓷电容）作为设备频率补偿的一部分。

模拟和数字接地平面应该尽可能的大且完整。如果接地平面足够大，模拟和数字接地可以分开，这是理想的配置。但是，如果总接地平面不够大，分割接地平面就不是一个好主意了。在这种情况下，所有的接地管脚能连在一起，成为一个单个大型和完整的接地平面。

备注：内嵌的 1.1V LDO 仅为 PHY 的内部应用而设计。不得提供电源给其他设备。

9.自动极性校正

在 10Base-T 模式下 SR8201F 自动校正接收对的极性错误 （极性在 100Base-TX 模式下是无关的）。在 10Base-T 模式下，极性错误被修正是基于有效间隔的链路脉冲的检测。检测开始在 MDI 交叉检测相位和当 10Base-T 链接上时锁定的期间。当链接断开时极性解锁。

10.远端错误指示

当 100FX 模式启用时，MII Reg.1.4 （远程错误） 是远端错误指示 （FEFI）位，当检测到 FEFI 时被设置。FEFI 是一个可供替代的带内信令的方法，它由 84 个连续的“1”后面跟一个“0”组成。当 SR8201F/FL/FN 检测到三次这样的信号，Reg.1.4 被设置，这意味着传输路径的远程端的接收路径有问题。另一方面，未能检测到 ‘Link OK’的信号，SR8201F/FL/FN 将开始发送 FEFI 信号，这将使得远端设备检测一个远端错误。这就意味着 SR8201F/FL/FN 的接收路径有问题。

11.Wake-On-LAN (WOL)

11.1 魔术包和唤醒帧格式

SR8201F/FL/FN 能监视网络唤醒帧或者魔术包，当这样一个事件发生，通过 PMEB （电源管理事件， ‘B’表示低电平有效）管脚通知系统。然后系统能被恢复到正常态去处理接下来的工作。PMEB 管脚必须和 4.7k 欧姆的

电阻连接，并且上拉至 3.3V。当一个唤醒帧或者魔术包发送到 PHY 时，PMEB 管脚将置低来通知系统去唤醒。详情参见 WOL 应用笔记。

魔术包唤醒仅发生在当满足以下条件时：

- 接收的魔术包的目的地址对于SR8201F/FL/FN是可接受的，例如，广播，多播，单播数据包地址匹配当前SR8201F/FL/FN的地址；
- 接收到的魔术包不包含CRC错误；
- 魔术包模版对比；例如，6 * FFh + MISC（可以没有） + 16 * DID（终点ID）在一个有效的以太网包的任意部分。

一个唤醒帧事件仅发生在当满足以下条件时：

- 接收到的唤醒帧的目的地址对SR8201F/FL/FN是可接受的，例如，广播，多播，单播数据包地址匹配当前SR8201F/FL/FN的地址；
- 接收到的唤醒帧不包含CRC错误
- 接收到的唤醒帧的16-bit CRC和由本地的设备操作系统给出的简单的16-bit CRC匹配。或者，SR8201F/FL/FN被配置成允许直接封包唤醒。例如，广播，多播，地址匹配当前SR8201F/FL/FN地址的单播数据包

注 1： 16-bit CRC：SR8201F/FL/FN 支持 8 个长唤醒帧 (从任意收到的网络封包的 0 to 127 字节由 128 个 屏蔽位来转换).CRC16 多项式 =x16+x12+x5+1。

注 2：详情参见 WOL 应用笔记 Wake-On-LAN 寄存器设定和波形时序。

11.2 低有效的网络唤醒

当 PHY 从链路伙伴那里接收到一个唤醒帧或者魔术封包，PMEB 管脚将拉低且 MAC 将在 T 周期后唤醒。PMEB 管脚将通过系统或者 MAC 被复位到高电平（见以下两图）。

详情参见 WOL 应用笔记。

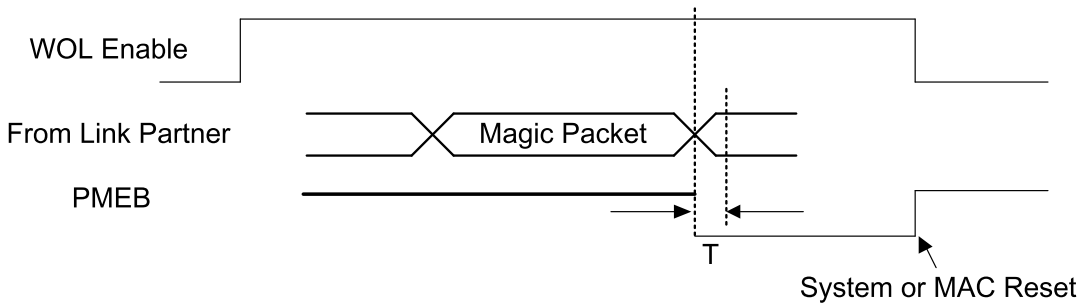


图 15.当接收魔术封包时为低有效

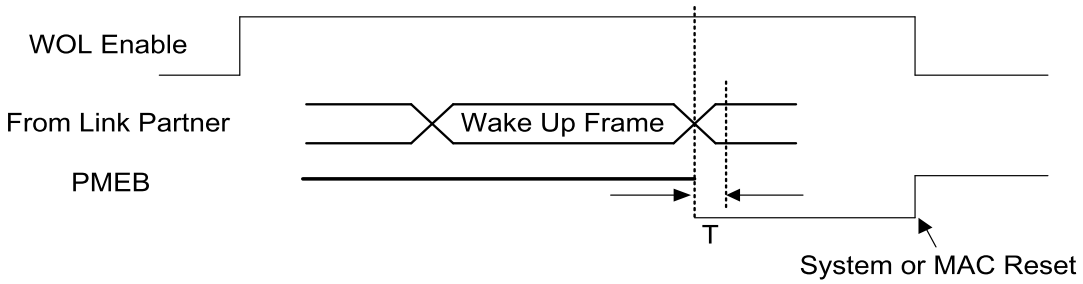


图 16.当接收唤醒帧时为低有效

11.3 低脉冲的 Wake-On-LAN

当 PHY 从链路伙伴那里接收到一个唤醒帧或者魔术封包，PMEB 管脚拉低一个周期（84ms，168ms（默认），336ms，或者 672ms； 通过 MDC/MDIO 设定），然后将在 T 周期后醒来（见以下两图）。

详情参见 WOL 应用笔记。

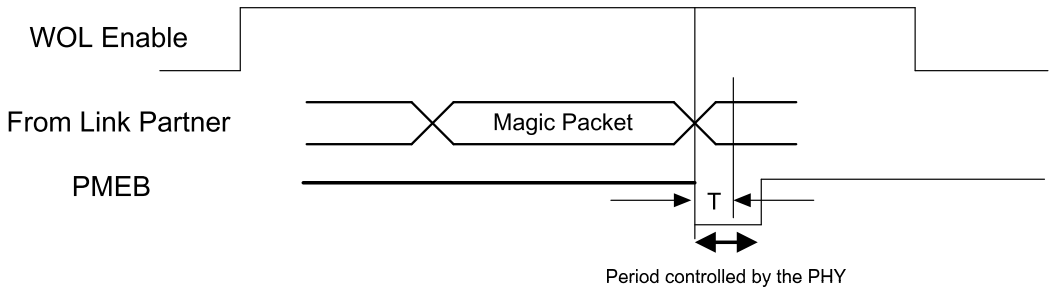


图 17.当接收魔术封包时为低脉冲

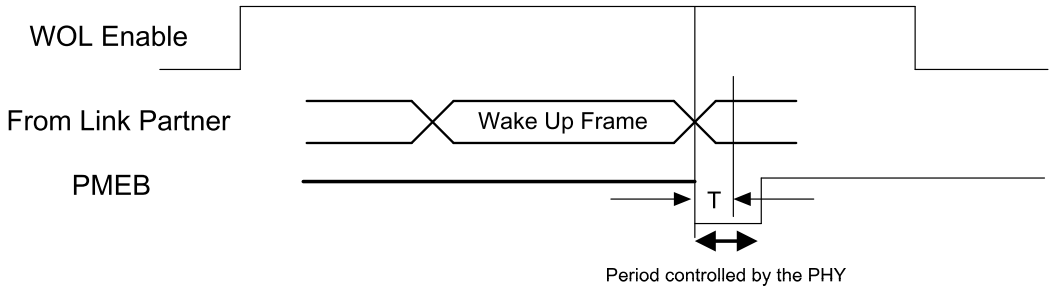


图 18.当接收唤醒帧时为低脉冲

11.4 Wake-On-LAN 管脚类型(MII 模式)

表 43.Wake-On-LAN 管脚类型(MII 模式)

Name	Type	Normal			WOL Enable
		100M	10M	Idle	
TXC	O/PD	25M CLK Output	2.5M CLK Output	2.5M CLK Output	O (2.5M/25M)/L/PD1
TXEN	I/PD	I	I	I	I/PD
TXD[0:3]	I/PD	I	I	I	I/PD
RXC	O/PD	25M CLK Output	2.5M CLK Output	2.5M CLK Output	O (2.5M/25M)/PD2
COL	LI/O/PD	O	O	O	O or PD2
CRS	LI/O/PD	O	O	O	O or PD2
RXDV	LI/O/PD	O	O	O	O or PD2
RXD[0:2]	O/PD	O	O	O	O or PD2
RXD[3]	LI/O/PD	O	O	O	O or PD2
RXER	LI/O/PD	O	O	O	O or PD2
MDC	I/PU	I	I	I	I/PU
MDIO	IO/PU	IO	IO	IO	IO/PU

备注 1：如果TX Isolate=1，停止TXC且管脚类型为 'L'.设置第0页，寄存器0，然后bit10=1把TXC管脚类型改为 'PD'。

备注2：如果RX Isolate=1，停止所有的MII RX接口且管脚类型为'PD'。

11.5 Wake-On-LAN 管脚类型(RMII 模式)

表 44.Wake-On-LAN 管脚类型(RMII 模式)

Name	Type	Normal			WOL Enable
		100M	10M	Idle	
TXC (REF_CLK)1	IO/PD	50M CLK Input/Output	50M CLK Input/Output	50M CLK Input/Output	I/O (50M)2
TXEN	I/PD	I	I	I	I/PD
TXD[0:1]	I/PD	I	I	I	I/PD
CRS_DV	LI/O/PD	O	O	O	O or PD3
RXD[0:1]	O/PD	O	O	O	O or PD3
RXER	LI/O/PD	O	O	O	O or PD3
MDC	I/PU	I	I	I	I/PU
MDIO	IO/PU	IO	IO	IO	IO/PU

备注 1：如果TXC (REF_CLK)在输入模式下(MAC到PHY)，REF_CLK不能停止在启用WOL。

备注2：当REF_CLK在输出模式下(PHY到MAC)，REF_CLK无法停止(切换到50MHz).设置TXC管脚类型为 'PD'，设置第0页，寄存器0，bit10=1。

备注3：如果RX Isolate=1，所有的RMII RX接口都停止且管脚类型为'PD'。

12.节能以太网（EEE）

SR8201F/FL/FN 支持 IEEE 802.3az-2010，也被称为节能以太网（EEE），包括 10Mbps 和 100Mbps 模式。它提供了一个基于网络利用率的在正常传输和低功耗等级（低能量空闲模式）间切换的协议。当没有数据包被传输，系统转为低能量空闲模式以节省能量。当数据包需要被传输，系统返回为正常模式，不需要改变链接状态也没有丢帧及引起错误帧。

对于省电，当系统处于低能量空闲模式时，大多数电路被禁用；但是从低能量空闲模式到正常模式的相互切换时间足够小使得可以满足高层协议和应用。

EEE 也指定一个协商模式去通知链路伙伴，以决定是否支持 EEE。

详情参见 http://www.ieee802.org/3/az/index.html

13.扩频时钟(SSC)

RMII 的 REF_CLK 路径可能成为 EMI 噪声源。扩频时钟（SSC）技术可以延伸 REF_CLK 信号到更宽的带宽，降低在某一频率辐射出的能量峰值，降低的 EMI 噪声。

当用 RMII REF_CLK 输出模式时，SSC 功能默认启用 （见第 7 页 寄存器 24 扩频时钟寄存器）。

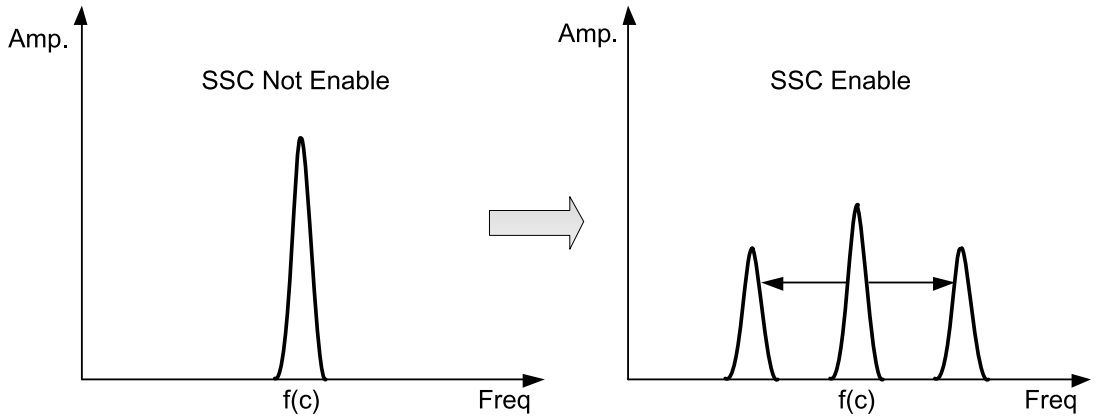


图 19.扩频时钟

电气特性

1.直流特性

1.1 极限参数

表 45. 极限参数

参数	符号	范围	单位
电源电压1	DVDD33，AVDD33	-0.4 ~ 3.7	V
电源电压2	DVDD10，DVDD10OUT，AVDD10OUT	-0.1 ~ 1.26	V
输入电压	Vi	-0.3 ~ 相应电源电压 +0.5V	V
输出电压	Vo	-0.3 ~ 相应电源电压 +0.5V	V
储存温度	Ts	-55 ~ 125	^{o}C

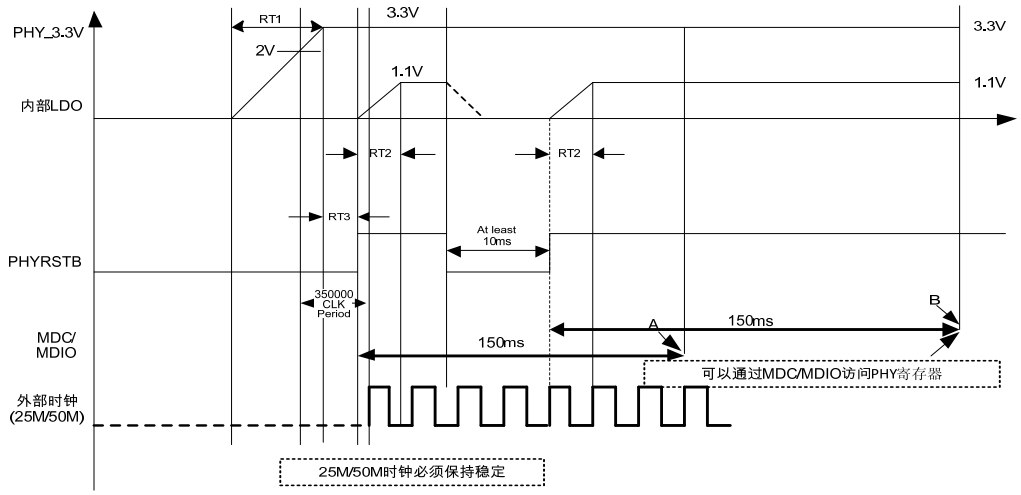
1.2 推荐工作条件

表 46. 推荐工作条件

参数	符号	范围	典型值	单位
电源电压	DVDD33，AVDD33	2.97 ~ 3.63	3.63	V
	DVDD10，DVDD10OUT，AVDD10OUT	1.00 ~ 1.16	1.16	V
工作环境温度	T_A	0 ~70	70	^{o}C
最高结点温度	Tj	- ~125	125	^{o}C

1.3 上电和 PHY 复位序列

SR8201F/FL/FN需要150ms的上电时间。150ms后允许从MDC/MDIO访问PHY寄存器。



注1：如果没有PHY的外部复位，MAC可以在A点访问PHY寄存器。
注2：如果有PHY的外部复位，MAC需要在B点访问PHY寄存器。

图20.上电和PHY复位序列

表 47.上电和 PHY 复位序列

符号	描述	最小值	最大值
Rt1	3.3V 上升时间@上电序列	100μs	-
Rt2	1.05V 上升时间@上电和PHY复位序列	100μs	-
Rt3	在PHY_3.3V稳定后，PHY RSTB无效	80μs	-

注：仅当使用外部1.05V电源供电时，Rt2需要100μs的上升时间.

1.4 RMII 输入模式功耗

整个系统的功耗（包括调节器损耗）见下表

表 48.RMII 输入模式功耗(全系统)

符号	条件	SR8201F	SR8201FN	SR8201FL	单位
P_{10IDLE}	10Base-T空闲，EEE未启用	36.3	36.3	36.3	mW
P_{10F}	10Base-T全双工	108.9	118.8	108.9	mW
$P_{100IDLE}$	100Base-T空闲，EEE未启用	148.5	151.8	155.1	mW
$P_{100IDLEEEE}$	100Base-T空闲，启用EEE	56.1	56.1	62.7	mW
P_{100F}	100Base-T全双工	174.9	178.2	178.2	mW
P_{LDPS}	断连省电	20.328	17.985	23.1	mW
P_{PHYRST}	PHY复位	3.3	3.3	3.3	mW

注：当系统在空闲模式时，设置第4页 寄存器21 bit12 到 '1' 将降低功耗.

1.5 输入输出电压

表 49.输入输出电压

符号	描述	条件	最小值	最大值
TTL V_{IH}	输入高电压	-	0.5*Vcc	Vcc+0.5V
TTL V_{IL}	输入低电压	-	-0.5V	0.7V
TTL V_{OH}	输出高电压	IOH=-8mA	0.65*Vcc	Vcc
TTL V_{OL}	输出低电压	IOL=8mA	-	0.7V
TTL I_{OZ}	三态漏电流	Vout=Vcc or GND	-110μA	10μA
I_{IN}	输入电流	Vin=Vcc or GND	-1μA	10μA
I_{PL}	带有弱的下拉电阻的输入电流	Vin=Vcc or GND	-1μA	100μA
I_{PH}	带有弱的上拉电阻的输入电流	Vin=Vcc or GND	-110μA	10μA
PECL V_{IH}	PECL输入高电压	-	Vdd-1.16V	Vdd-0.88V
PECL V_{IL}	PECL输入低电压	-	Vdd-1.81V	Vdd-1.47V
PECL V_{OH}	PECL输出高电压	-	Vdd-1.02V	-
PECL V_{OL}	PECL输出低电压	-	-	Vdd-1.62V

2.交流特性

所有的输出时序都假设等效荷载在10pF和25pF之间，包括PCB布局的走线和其他连接设备（例如，MAC）。

2.1 MII 传输周期时序

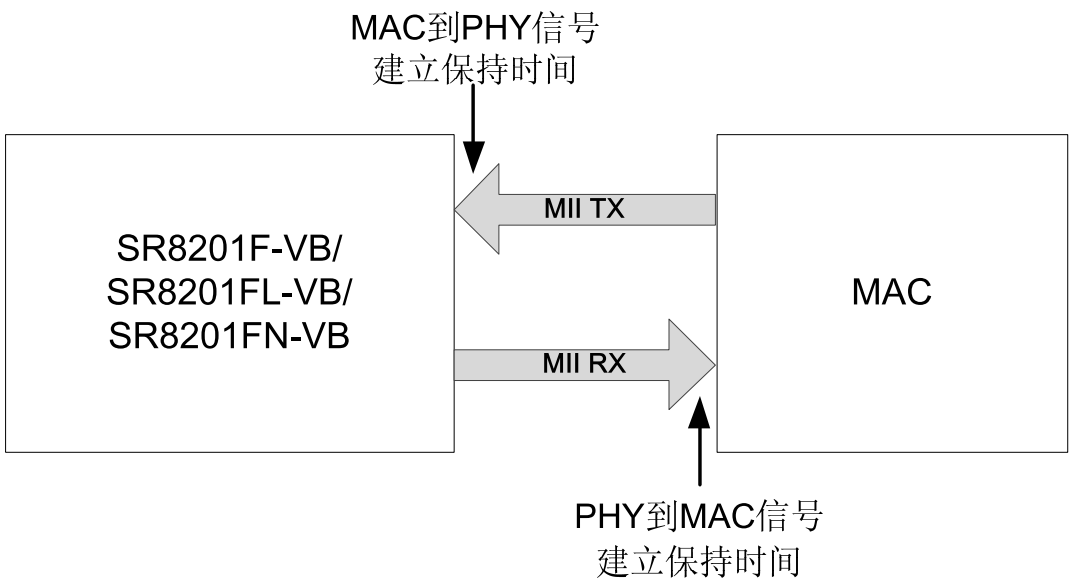


图21.MII接口设置/保持时间定义

下图显示了MII接口上从MAC到PHY传输一个数据包的例子。

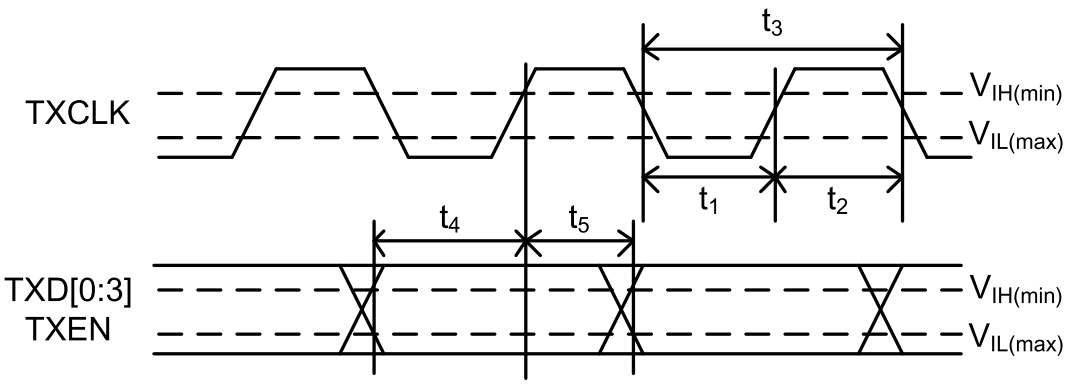


图22.MII传输周期时序-1

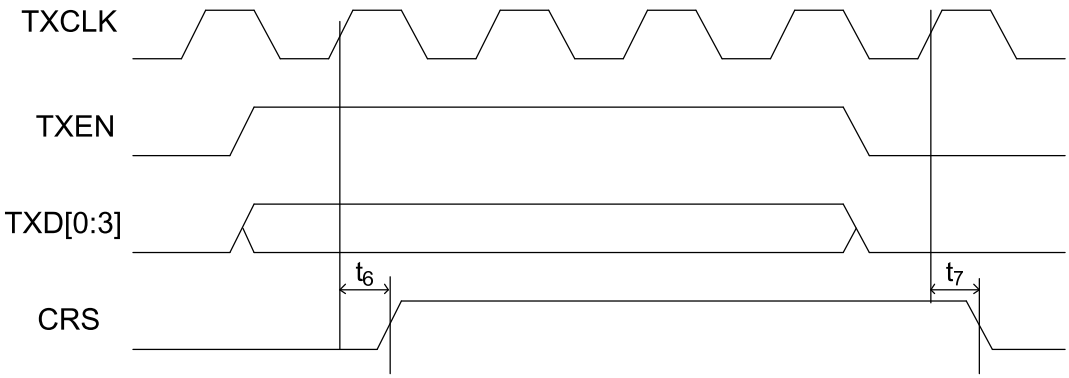


图23.MII传输周期时序-2

表 50.MII 传输周期时序

符号	描述		最小值	典型值	最大值	单位
t1	TXCLK高电平脉冲宽度	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t2	TXCLK低电平脉冲宽度	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t3	TXCLK周期	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t4	TXEN，TXD[0:3] 到TXCLK上升沿的建立时间	100Mbps	10	-	-	ns
		10Mbps	5	-	-	ns
t5	TXEN，TXD[0:3] 在TXCLK上升沿之后的保持时间	100Mbps	0	-	-	ns
		10Mbps	0	-	-	ns
t6	TXEN采样到CRS高	100Mbps	-	-	40	ns
		10Mbps	-	-	400	ns
t7	TXEN采样到CRS低	100Mbps	-	-	160	ns
		10Mbps	-	-	2000	ns

2.2 MII 接收周期时序

下图显示了 MII 接口上从 PHY 到 MAC 传输一个数据包的例子。

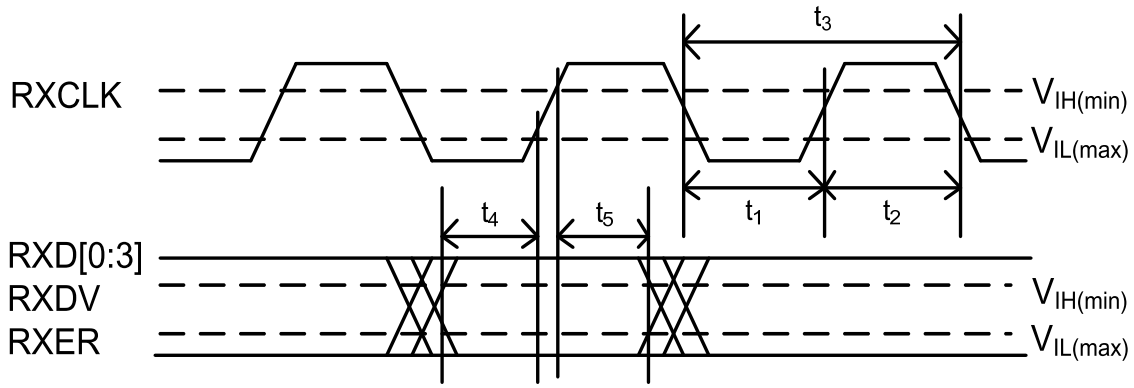


图 24.MII 接收周期时序-1

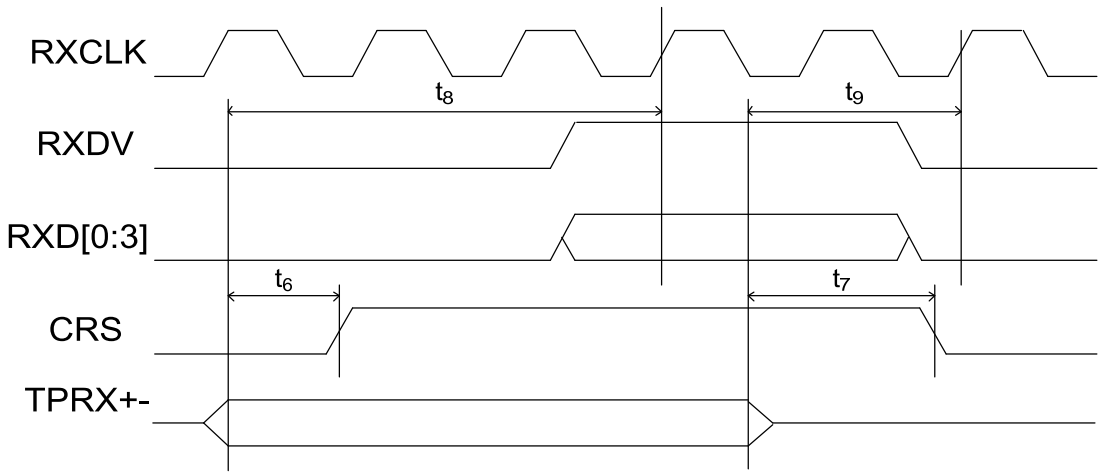


图 25.MII 接收周期时序-2

表 51.MII 接收周期时序

符号	描述		最小值	典型值	最大值	单位
t1	RXCLK高电平脉冲宽度	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t2	RXCLK低电平脉冲宽度	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t3	RXCLK周期	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns

符号	描述		最小值	典型值	最大值	单位
t4	RXER，RXDV， RXD[0:3]到RXCLK上升沿的建立时间	100Mbps	10	-	-	ns
		10Mbps	10	-	-	ns
t5	RXER，RXDV，RXD[0:3] 在RXCLK上升沿之后的保持时间	100Mbps	10	-	-	ns
		10Mbps	10	-	-	ns
t6	接收帧到CRS高	100Mbps	-	-	130	ns
		10Mbps	-	-	2000	ns
t7	接收帧的结束到CRS低	100Mbps	-	-	240	ns
		10Mbps	-	-	1000	ns
t8	接收帧采样到RXDV的边沿	100Mbps	-	-	150	ns
		10Mbps	-	-	3200	ns
t9	接收帧的结尾采样到RXDV的边沿	100Mbps	-	-	120	ns
		10Mbps	-	-	1000	ns

2.3 RMII 传输和接收周期时序

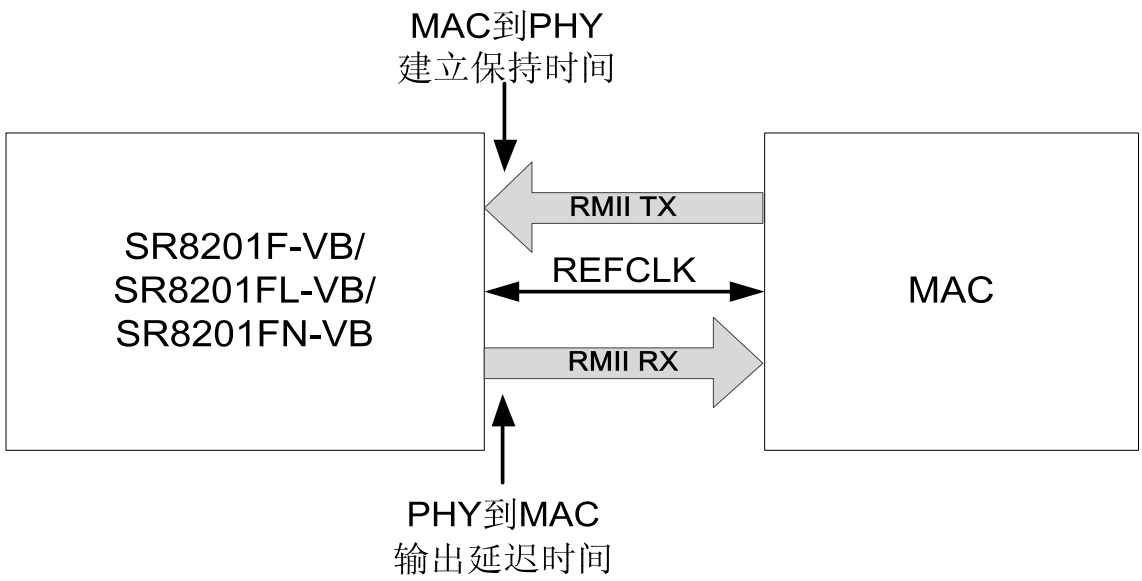


图 26.RMII 接口设置，保持时间和输出延时定义

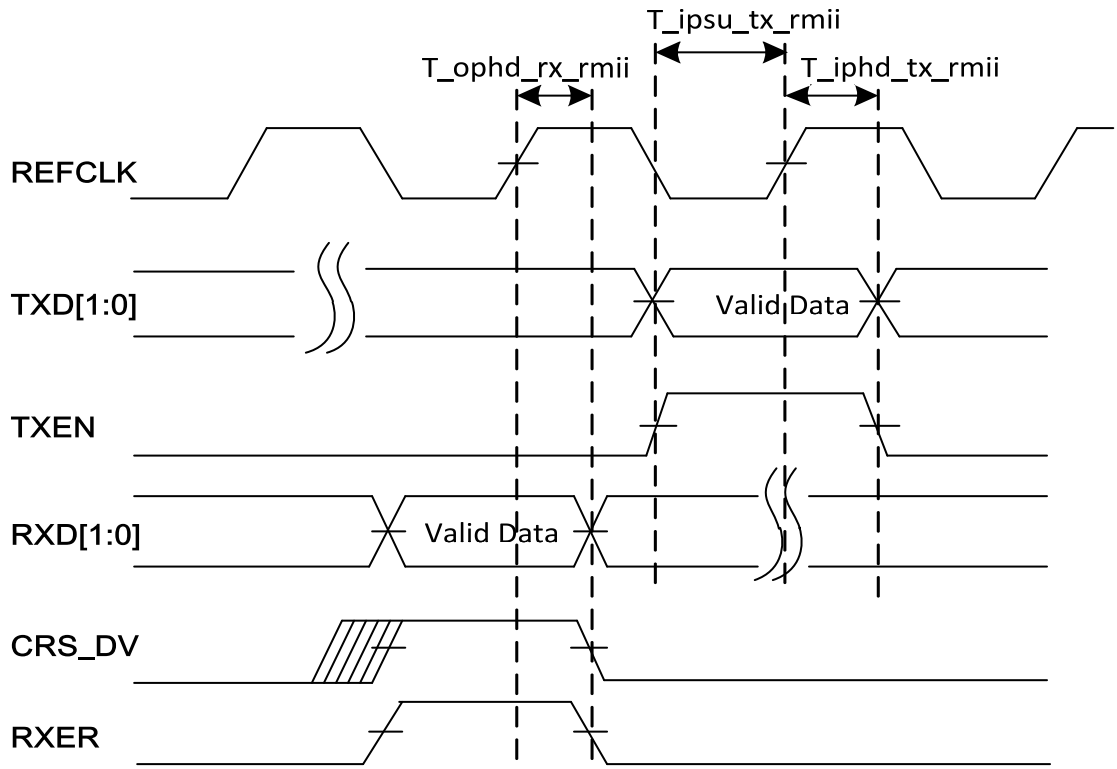


图 27.RMII 传输和接收周期时序

表 52.RMII 传输和接收周期时序

符号	描述	最小值	典型值	最大值	单位
Fref	REFCLK参考时钟频率	-	50	-	MHz
Dref	REFCLK参考时钟占空比	35	-	65	%
T_ipsu_tx_rmii	TXD[1:0]/TXEN设置时间到REFCLK	4	-	-	ns
T_iphd_tx_rmii	TXD[1:0]/TXEN保留时间从REFCLK	2	-	-	ns
T_ophd_rx_rmii	RXD[1:0]/CRS_DV/RXER输出延时从REFCLK	2	-	-	ns

注 1：RMII TX时序能通过第7页，寄存器16[11:8] 设置；最小的可调节分辨率为2ns。不建议对这些位的做任意改变，默认值是最优化的设置。

注 2：RMII RX时序能通过第7页，寄存器16[7:4] 设置；最小的可调节分辨率为2ns。不建议对这些位的做任意变，默认值是最优化的设置。

2.4 MDC/MDIO 时序

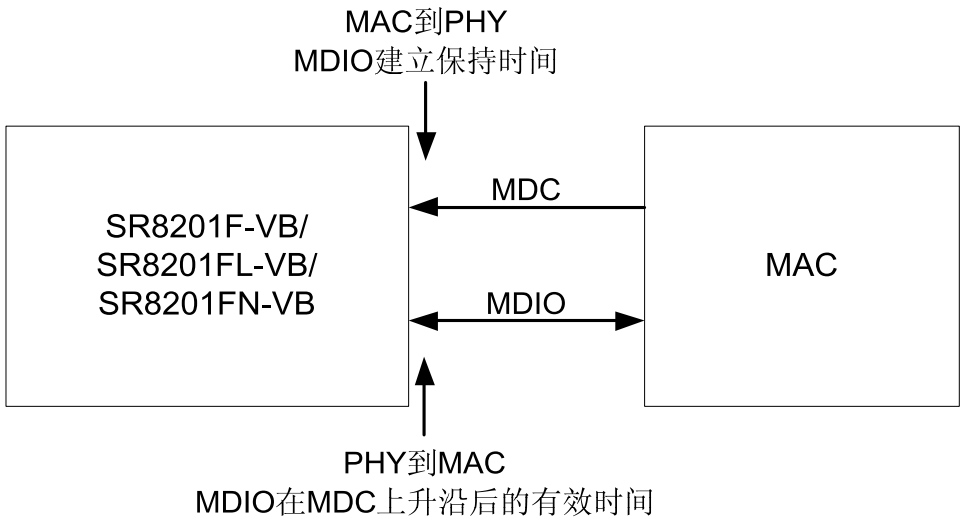


图 28.MDC/MDIO接口建立、保持时间和MDC上升有效时间定义

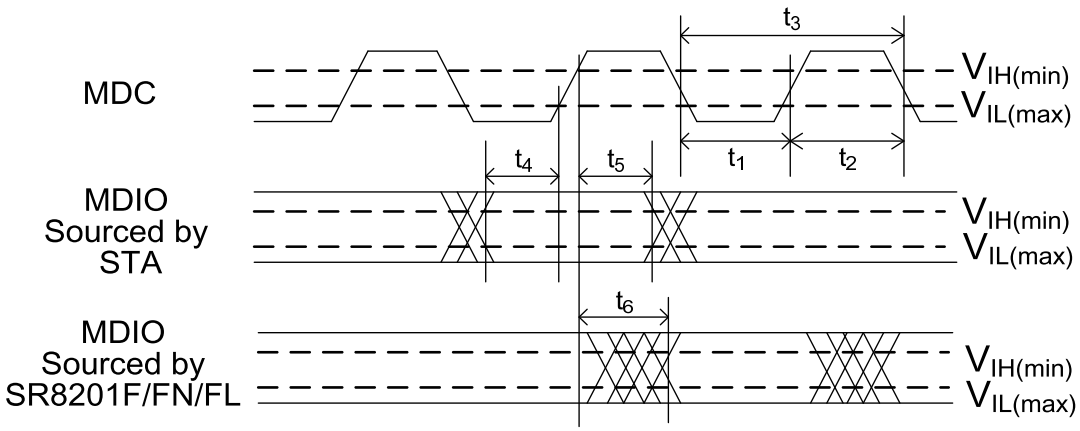


图 29.MDC/MDIO时序

表 53.MDC/MDIO 时序

符号	描述	最小值	最大值	单位
t_1	MDC高脉冲宽度	160	-	ns
t_2	MDC低脉冲宽度	160	-	ns
t_3	MDC周期	400	-	ns
t_4	MDIO设置到MDC上升沿	10	-	ns
t_5	MDIO保持时间到MDC上升沿	10	-	ns
t_6	MDIO有效从MDC上升沿	0	300	ns

2.5 无冲突的发送

下图列出从 MAC 到 PHY 的一个包传输。

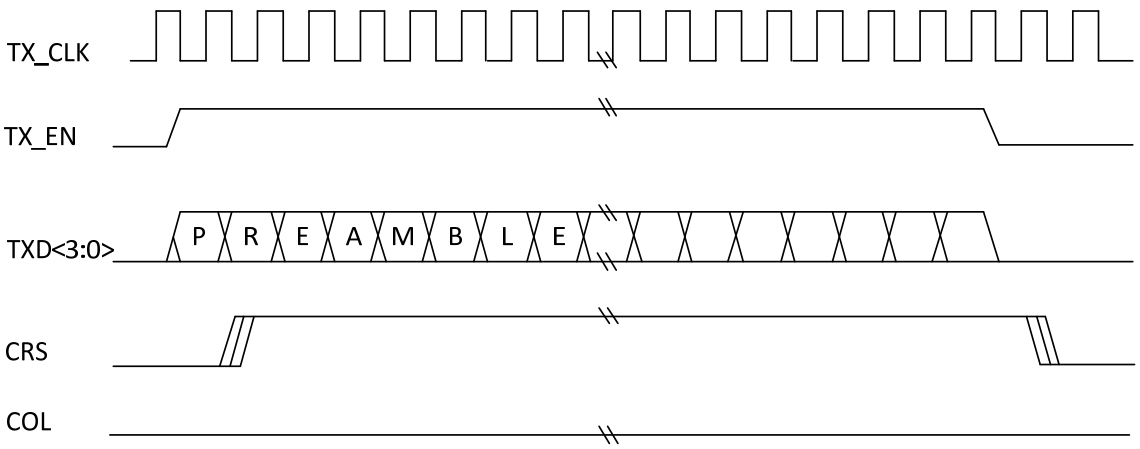


图 30.MAC 到 PHY 无冲突的发送

2.6 无错误的接收

下图列出了从 PHY 到 MAC 的一个包传输

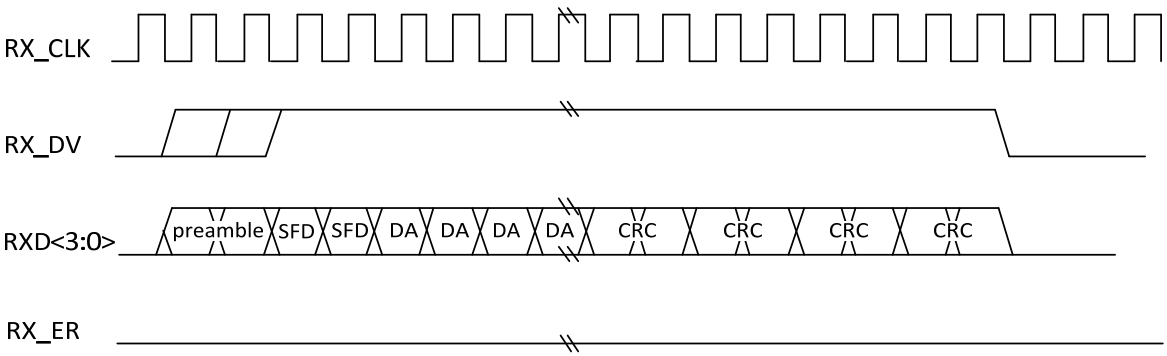


图31.PHY到MAC无错误的接收

3.晶体特性

表 54.晶体特性

符号	描述 / 条件	最小值	典型值	最大值	单位
Fref	并联共振晶体参考频率，基础模式，AT-Cut型	-	25	-	MHz
Fref Stability	并联共振晶体频率的稳定性，基础模式，AT-Cut型.T_a=0°C~70°C.	-30	-	+30	ppm
Fref Tolerance	并联共振晶体频率的限度，基础模式，AT-Cut型.T_a=25°C.	-50	-	+50	ppm
Fref Duty Cycle	参考时钟输入占空比	40	-	60	%
ESR	等效串联电阻	-	-	30	Ω
DL	驱动等级	-	-	0.3	mW
Jitter	带宽抖动峰峰值[1，2]	-	-	500	ps

注 1：25KHz 到 25MHz RMS < 3ps.

注 2：带宽RMS < 9ps.

4.振荡器要求

表 55.振荡器要求

参数	条件	最小值	典型值	最大值	单位
频率	-	-	25/50	-	MHz
频率稳定性	Ta = 0°C~+70°C	-30	-	30	ppm
频率限度	Ta = 25°C	-50	-	50	ppm
占空比	-	40	-	60	%
带宽抖动峰峰值[1，2]	-	-	-	500	ps
V峰峰值	-	3.15	3.3	3.45	V
上升时间(10%~90%)	-	-	-	10	ns
下降时间(10%~90%)	-	-	-	10	ns
工作温度范围	-	0	-	70	°C

注 1：25KHz 到 25MHz RMS < 3ps.

注 2：宽带 RMS < 9ps.

5.时钟要求

表 56.时钟要求

参数	最小值	典型值	最大值	单位
频率	-	25/50	-	MHz
频率稳定性	-30	-	30	ppm
频率限度	-50	-	50	ppm
占空比	40	-	60	%
带宽抖动峰峰值[1，2]	-	-	500	ps
Vpeak-to-peak	3.15	3.3	3.45	V
上升时间(10%~90%)	-	-	10	ns
下降时间(10%~90%)	-	-	10	ns

注 1：25KHz 到 25MHz RMS < 3ps.

注 2：宽带 RMS < 9ps.

6.变压器特性

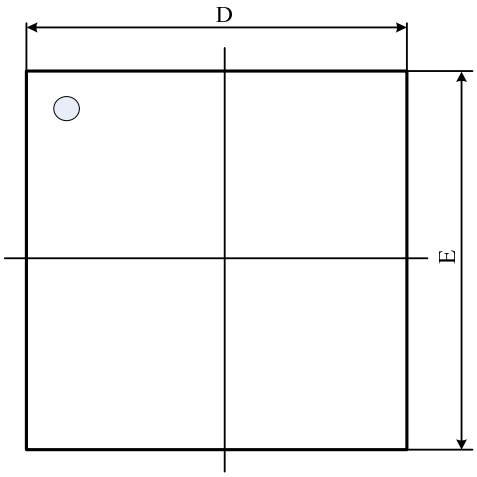
表 57.变压器特性

参数	发送端	接收端
匝比	1:1 CT	1:1 CT
电感(min.)	350μH @ 8mA	350μH @ 8mA

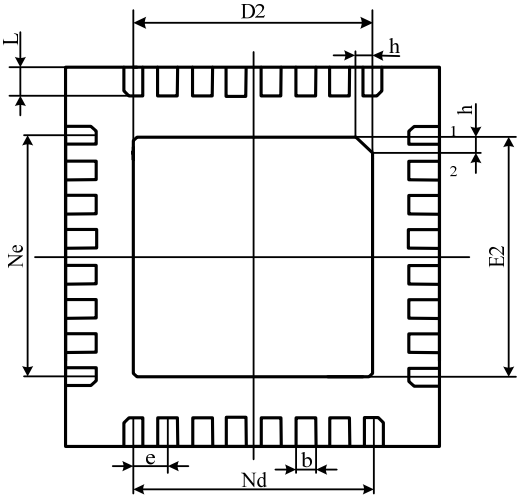
封装外形图

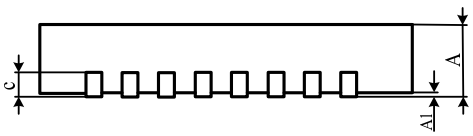
QFN-32-5×5-0.50 单位：**mm**

TOP VIEW



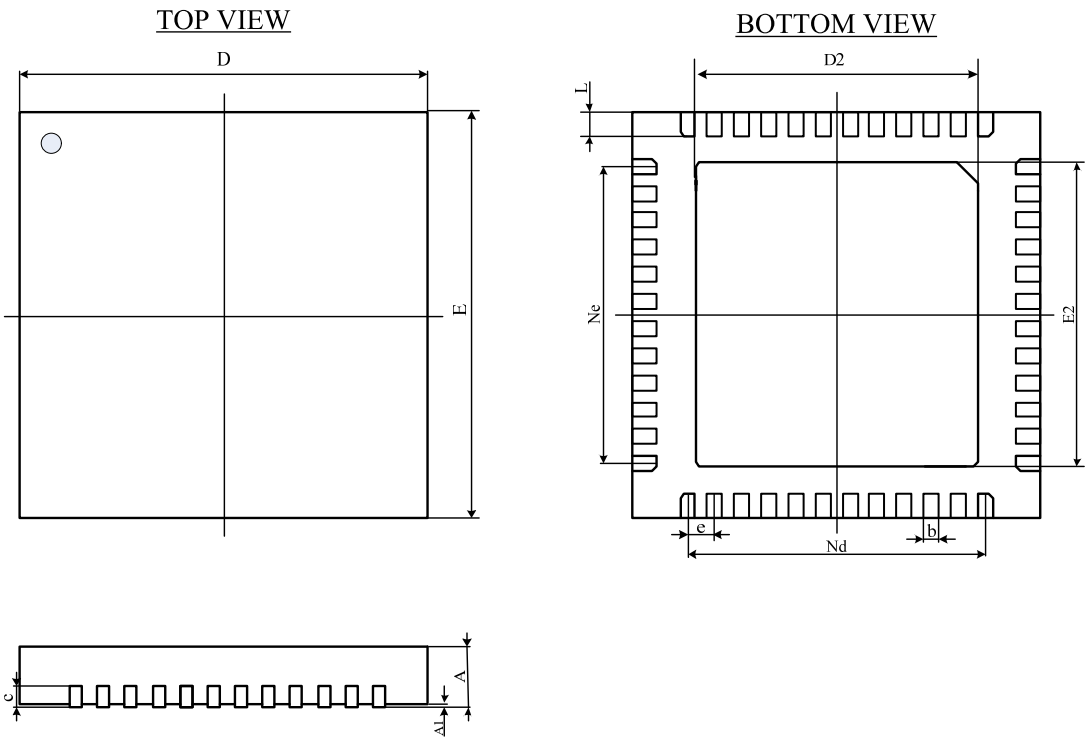
BOTTOM VIEW





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.01	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D/E	4.90	5.00	5.10
D2/E2	3.50REF		
e	0.50BSC		
Nd/ Ne	3.50BSC		
L	0.35	0.40	0.45
h	0.30	0.35	0.40

QFN-48-6×6-0.40 单位：**mm**



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.85	1.00
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c		0.20REF	
D/E		6.00BSC	
D2/E2	4.05	4.4	4.65
e		0.4BSC	
Nd /Ne		4.4BSC	
L	0.30	0.40	0.50

LQFP-48-7×7-0.50 单位：**mm**