250 V to 600 V, 1.5 A to 2.5 A
High Voltage 3-phase Motor Driver ICs
SLA/SMA6820MH Series

Data Sheet

Description

SLA/SMA6820MH series are high voltage 3-phase motor driver ICs in which transistors, pre-driver ICs (MICs), and bootstrap circuits (diodes and resistors) are highly integrated.

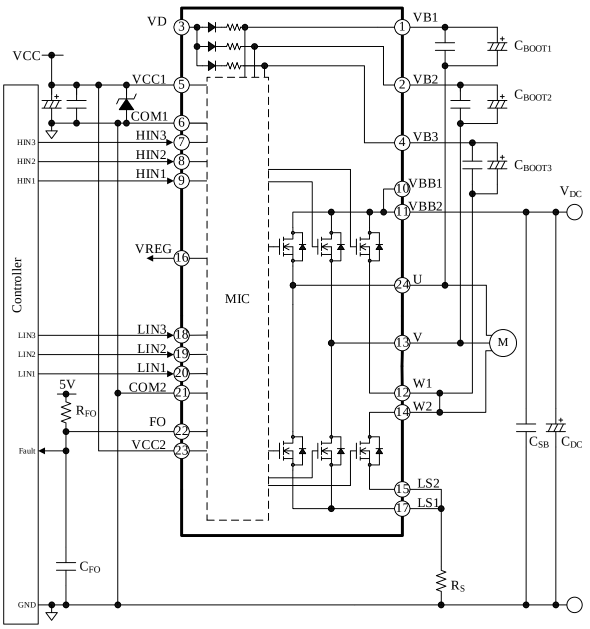
You can select from the fully-molded type or the heatsink-type ZIP24 package according to your mounting condition.

SLA/SMA6820MH series are optimal for the inverting control of small to middle power motors.

Features

- Built-in Bootstrap Diodes with Current Limmiting Resistors (22 Ω)
- CMOS-compatible Input (3.3 or 5 V)
- Fault Signal Output (FO pin)
- 7.5 V Regurator Output
- Bare lead frame: Pb-free (RoHS compliant)
- Protections
  Undervoltage Lockout for Power Supply
    High-side (UVLO_VB): Auto-restart
    Low-side (UVLO_VCC): Auto-restart
  Thermal Detection (TD): Fault Signal Output

Typical Application



Packages

ZIP24

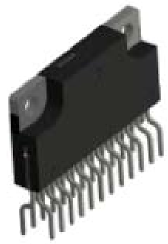
Fully Molded Type (SMA682xMH)

Heatsink Type (SLA6826MH)

LF No. 2451

LF No. 2175

LF No. 2452



LF No. 2171

Not to scale

Selection Guide

- **Packages**

Package	Part Number
Fully Molded Type	SMA682xMH
Heatsink Type	SLA6826MH

- **Output Charactaristic**

V_{DSS}	I_O	Part Number
250 V	2.0 A	SLA6826MH
		SMA6821MH
500 V	1.5 A	SMA6822MH
	2.5 A	SMA6823MH
600 V	1.5 A	SMA6824MH

Applications

- Washing Machine Fan Motor and Pump Motor
- Air Conditioner Fan Motor
- Air Cleaner Fan Motor
- Fan Motor for Electric Stand Fan

Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: a current flow going into the IC (sinking) is positive current (+); and a current flow coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25°C, COM1 = COM2 that is called COM.

Characteristic	Symbol	Conditions	Rating	Unit	Remarks
MOSFET Breakdown Voltage	V_{DSS}	I_D = 100 μA V_{INx} = 0 V	250	V	SLA6826MH SMA6821MH
			500		SMA6822MH SMA6823MH
			600		SMA6824MH
Logic Supply Voltage	V_{CC}	VCC1–COM VCC2–COM	20	V	
Bootstrap Supply Voltage	V_{BS}	VB1–U VB2–V VB3–W1	20	V	
Output Current (DC)	I_O	T_C = 25 °C	1.5	A	SMA6822MH SMA6824MH
			2.0		SLA6826MH SMA6821MH
			2.5		SMA6823MH
Output Current (Pulse)	I_{OP}	T_C = 25 °C, $P_W \leq$ 100 μs, Duty = 1%	2.25	A	SMA6822MH SMA6824MH
			3.0		SLA6826MH SMA6821MH
			3.75		SMA6823MH
Regulator Output Current	I_{REG}		35	mA	
Input Voltage	V_{IN}	HIN1–COM HIN2–COM HIN3–COM LIN1–COM LIN2–COM LIN3–COM	−0.5 to 7	V	
Power Dissipation	P_D	T_C = 25 °C	28	W	SMA682xMH
			32		SLA6826MH
Operating Case Temperature	$T_{C(OP)}$		−30 to 100	°C	
Junction Temperature	T_j		150	°C	
Storage Temperature	T_{stg}		−40 to 150	°C	

2. Recommended Operating Conditions

Unless specifically noted, T_A = 25°C, COM1 = COM2 that is called COM.

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Main Supply Voltage	V_{DC}	VBB–LS1 VBB–LS2	—	150	200	V	SLA6826MH SMA6821MH
			—	300	400	V	SMA6822MH SMA6823MH
			—	300	450	V	SMA6824MH
Logic Supply Voltage	V_{CC}	VCC1–COM VCC2–COM	13.5	—	16.5	V	
Dead Time of Input Signal	t_{DEAD}	T_J = −25 to 150 °C	1.5	—	—	Ms	
Minimum Input Pulse Width	$t_{IN\_MIN(ON)}$	T_J = −25 to 150 °C	0.5	—	—	μs	
	$t_{IN\_MIN(OFF)}$	T_J = −25 to 150 °C	0.5	—	—	μs	

3. Electrical Characteristics

Current polarities are defined as follows: a current flow going into the IC (sinking) is positive current (+); and a current flow coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, V_{CC} = 15 V, T_A = 25°C, COM1 = COM2 that is called COM.

3.1. Characteristics of Control Parts

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Logic Supply Current	I_{CC}	I_{REG} = 0 A	—	4	6	mA	
Input Voltage	V_{IH}		—	2.0	2.5	V	All transistors on state.
	V_{IL}		1.0	1.5	—	V	All transistors off state.
	V_{HYS}		—	0.5	—	V	
Input Current	I_{IH}	INx = 5 V	—	50	100	μA	
	I_{IL}	INx = 0 V	—	—	2	μA	
Undervoltage Lockout for Power Supply (High side)	V_{UVHL}	VB1–U VB2–V VB3–W1	9.0	10.0	11.0	V	
	V_{UVHH}		9.5	10.5	11.5	V	
	V_{UV_HYS}		—	0.5	—	V	
Undervoltage Lockout for Power Supply (Low side)	V_{UVLL}	VCC1–COM VCC2–COM	10.0	11.0	12.0	V	
	V_{UVLH}		10.5	11.5	12.5	V	
	V_{UV_HYS}		—	0.5	—	V	
FO Pin Output Voltage	V_{FOL}		0	—	1.0	V	
	V_{FOH}		4.0	—	5.5	V	
Thermal Detection Threshold Temperature	T_{DH}	I_{REG} = 0 mA, No heatsink	135	150	165	°C	
	T_{DL}		105	120	135	°C	
	T_{D_HYS}		—	30	—	°C	
Regulator Output Voltage	V_{REG}	I_{REG} = 0 to 35 mA	6.75	7.5	8.25	V	

3.2. Bootstrap Diode Characteristics

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Bootstrap Diode Forward Voltage	V_{FB}	I_{FB} = 0.15 A	—	1.1	1.3	V	
Bootstrap Diode Leakage Current	I_{LBD}	V_R = 250 V	—	—	10	μA	SLA6826MH SMA6821MH
		V_R = 500 V	—	—	10		SMA6822MH SMA6823MH
		V_R = 600 V	—	—	10		SMA6824MH
Bootstrap Diode Series Resistor	R_B		17.6	22.0	26.4	Ω	

3.3. Thermal Resistance Characteristics

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Junction-to-Case Thermal Resistance	R_{J-C}	All transistors operation	—	—	4.46	°C/W	SMA682xMH
			—	—	3.8		SLA6826MH
Junction-to-Ambient Thermal Resistance	R_{J-A}	All transistors operation	—	—	31.25	°C/W	SMA682xMH

3.4. Transistor Characteristics

Figure 3-1 shows the definition of switching characteristics.

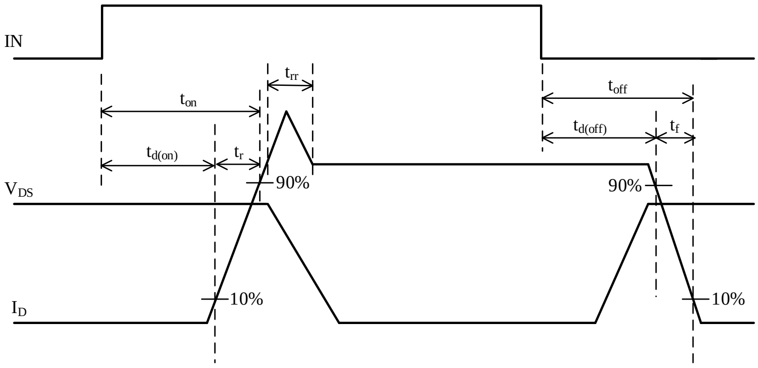


Figure 3-1. Switching Characteristics Definitions

3.4.1. SLA6826MH

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 250 V, V_{IN} = 0 V	—	—	100	µA
Drain-to-Source Saturation Voltage	$R_{DS(ON)}$	I_D = 1.0 A, V_{IN} = 5 V	—	1.25	1.5	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} = 1.0 A, V_{IN} = 0 V	—	1.1	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 150 V, I_D = 2.0 A, V_{IN} = 0 ~ 5 V, T_J = 25 °C, inductive load	—	65	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	430	—	ns
Rise Time	t_r		—	55	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	355	—	ns
Fall Time	t_f		—	20	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 150 V, I_D = 2.0 A, V_{IN} = 0 ~ 5 V, T_J = 25 °C, inductive load	—	65	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	505	—	ns
Rise Time	t_r		—	60	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	495	—	ns
Fall Time	t_f		—	20	—	ns

3.4.2. SMA6821MH

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 250 V, V_{IN} = 0 V	—	—	100	μA
Drain-to-Source Saturation Voltage	$R_{DS(ON)}$	I_D = 1.0 A, V_{IN} = 5 V	—	1.25	1.5	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} = 1.0 A, V_{IN} = 0 V	—	1.1	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 150 V, I_D = 2.0 A, V_{IN} = 0 ~ 5 V, T_J = 25 °C, inductive load	—	65	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	430	—	ns
Rise Time	t_r		—	55	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	355	—	ns
Fall Time	t_f		—	20	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 150 V, I_D = 2.0 A, V_{IN} = 0 ~ 5 V, T_J = 25 °C, inductive load	—	65	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	505	—	ns
Rise Time	t_r		—	60	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	495	—	ns
Fall Time	t_f		—	20	—	ns

3.4.3. SMA6822MH

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 500 V, V_{IN} = 0 V	—	—	100	μA
Drain-to-Source Saturation Voltage	$R_{DS(ON)}$	I_D = 0.75 A, V_{IN} = 5 V	—	3.2	4.0	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} = 0.75 A, V_{IN} = 0 V	—	1.1	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_D = 1.5 A, V_{IN} = 0 ~ 5 V, T_J = 25 °C, inductive load	—	120	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	485	—	ns
Rise Time	t_r		—	85	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	420	—	ns
Fall Time	t_f		—	30	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_D = 1.5 A, V_{IN} = 0 ~ 5 V, T_J = 25 °C, inductive load	—	130	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	620	—	ns
Rise Time	t_r		—	100	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	585	—	ns
Fall Time	t_f		—	25	—	ns

3.4.4. SMA6823MH

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 500 V, V_{IN} = 0 V	—	—	100	μA
Drain-to-Source Saturation Voltage	$R_{DS(ON)}$	I_D = 1.25 A, V_{IN} = 5 V	—	2.0	2.4	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} = 1.25 A, V_{IN} = 0 V	—	1.1	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_D = 2.5 A, V_{IN} = 0 ~ 5 V, T_J = 25 °C, inductive load	—	170	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	700	—	ns
Rise Time	t_r		—	165	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	580	—	ns
Fall Time	t_f		—	40	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_D = 2.5 A, V_{IN} = 0 ~ 5 V, T_J = 25 °C, inductive load	—	170	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	800	—	ns
Rise Time	t_r		—	180	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	690	—	ns
Fall Time	t_f		—	35	—	ns

3.4.5. SMA6824MH

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 600 V, V_{IN} = 0 V	—	—	100	μA
Drain-to-Source Saturation Voltage	$R_{DS(ON)}$	I_D = 0.75 A, V_{IN} = 5 V	—	2.9	3.5	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} = 0.75 A, V_{IN} = 0 V	—	1.0	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_D = 1.5 A, V_{IN} = 0 ~ 5 V, T_J = 25 °C, inductive load	—	155	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	685	—	ns
Rise Time	t_r		—	115	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	555	—	ns
Fall Time	t_f		—	55	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, I_D = 1.5 A, V_{IN} = 0 ~ 5 V, T_J = 25 °C, inductive load	—	155	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	740	—	ns
Rise Time	t_r		—	130	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	670	—	ns
Fall Time	t_f		—	35	—	ns

4. Truth Table

Table 4-1 is a truth table that provides the logic level definitions of operation modes.

In the case where HINx and LINx signals in each phase are high at the same time, both the high-side and low-side transistors are set on (simultaneous on-state). You must set the input signals so that the simultaneous on-state is not occuerd.

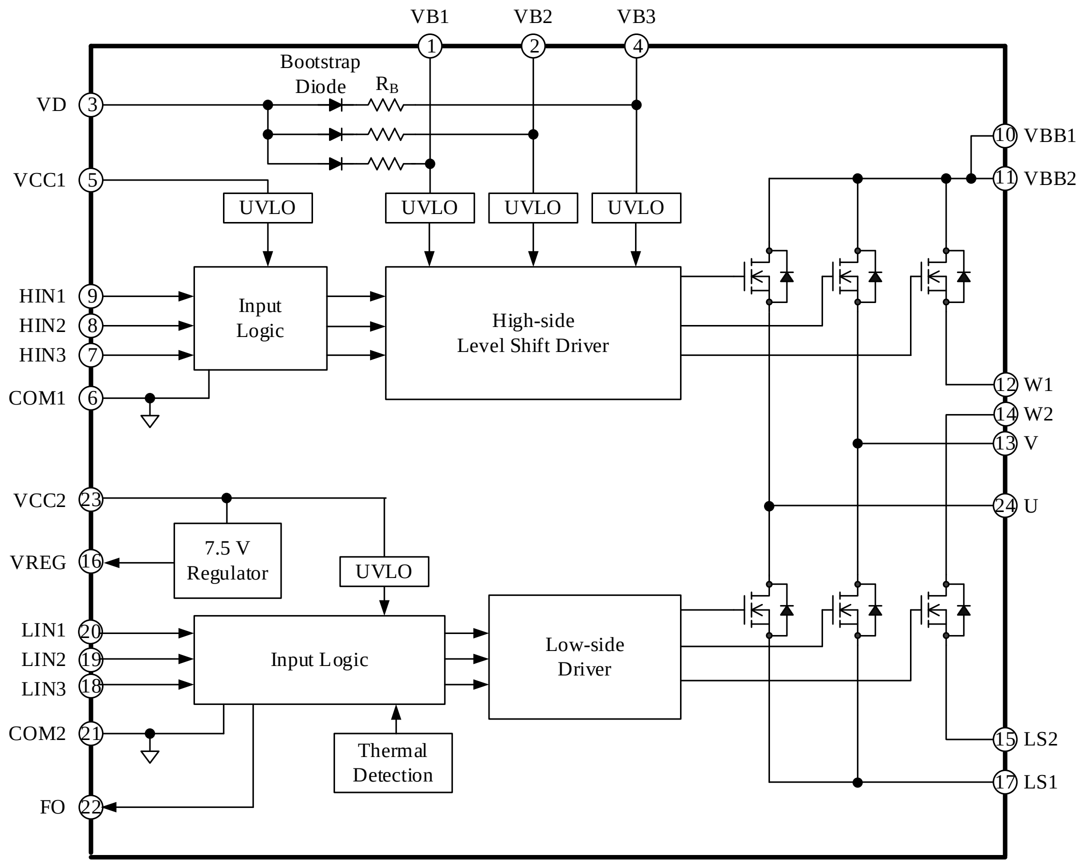
After recovering from a UVLO_VCC condition, the high-side and low-side transistors resume switching according to the input logic levels of the next HINx and LINx signals (level-triggered).

After recovering from a UVLO_VB condition, the high-side transistors resume switching at the next rising edge of an HIN signal (edge-triggered).

Table 4-1. Truth Table for Operation Modes

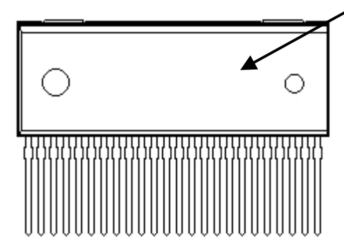
Mode	HINx	LINx	High-side Transistors	Low-side Transistors
Normal Operation	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	ON
	H	H	ON	ON
High-side Undervoltage Lockout for Power Supply (UVLO_VB)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	ON
Low-side Undervoltage Lockout for Power Supply (UVLO_VCC)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF
Thermal Detection (TD)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	ON
	H	H	ON	ON

5. Block Diagram

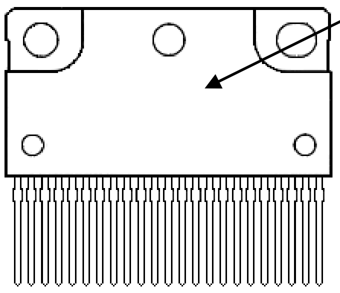


6. Pin Configuration Definitions

SMA682xMH



SLA6826MH



Pin Number	Pin Name	Functions
1	VB1	U-phase high-side floating supply voltage input
2	VB2	V-phase high-side floating supply voltage input
3	VD	Anode of bootstrap diodes
4	VB3	W-phase high-side floating supply voltage input
5	VCC1	High side logic supply voltage input
6	COM1	High side logic ground
7	HIN3	Logic input for W-phase high-side gate driver
8	HIN2	Logic input for V-phase high-side gate driver
9	HIN1	Logic input for U-phase high-side gate driver
10	VBB1	Positive DC bus supply voltage (be connected toVBB2 by PCB trace)
11	VBB2	Positive DC bus supply voltage (be connected toVBB2 by PCB trace)
12	W1	W-phase output (be connected toW2 by PCB trace)
13	V	V-phase output
14	W2	W-phase output (be connected toW1 by PCB trace)
15	LS2	U and V-phase power MOSFET Source (be connected toLS1 by PCB trace)
16	VREG	Regulator output
17	LS1	W-phase power MOSFET Source (be connected toLS2 by PCB trace)
18	LIN3	Logic input for W-phase low-side gate driver
19	LIN2	Logic input for V-phase low-side gate driver
20	LIN1	Logic input for U-phase low-side gate driver
21	COM2	Low side logic ground
22	FO	Fault signal output for thermal detection and UVLO, active high
23	VCC2	Low side logic supply voltage input
24	U	U-phase output

7. Typical Application

Capacitors should be place near the IC. If the circuit noise is large, connect the noise reduction ceramic capacitor to the electrolytic capacitor in parallel.

Pull down resistance (about 100 kΩ) is built-in the HINx pin and the LINx pin. If the unstable signal or noisy signal may be input, connect the resistor in external to the HINx pin and the LINx pin.

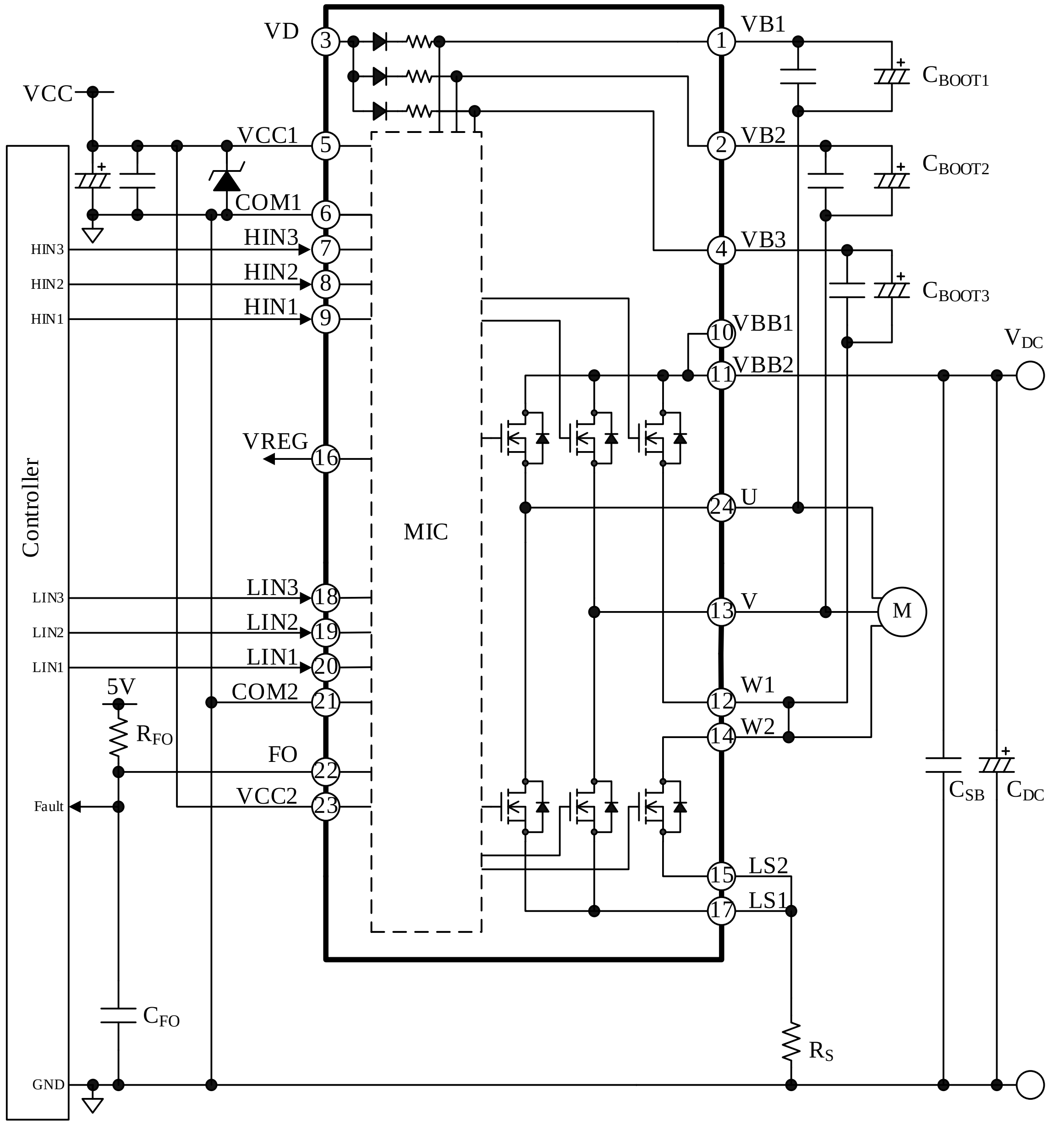


Figure 7-1. Typical Application

8. Timing Chart in Protection Operation

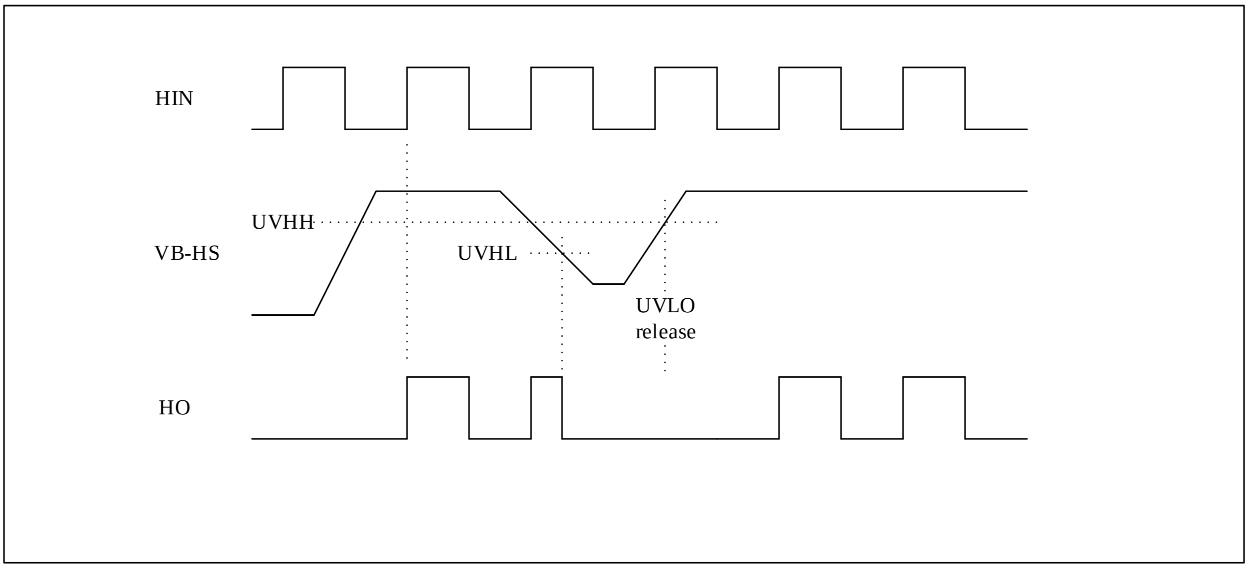


Figure 8-1. High-side Undervoltage Lockout for Power Supply (UVLO_VB)

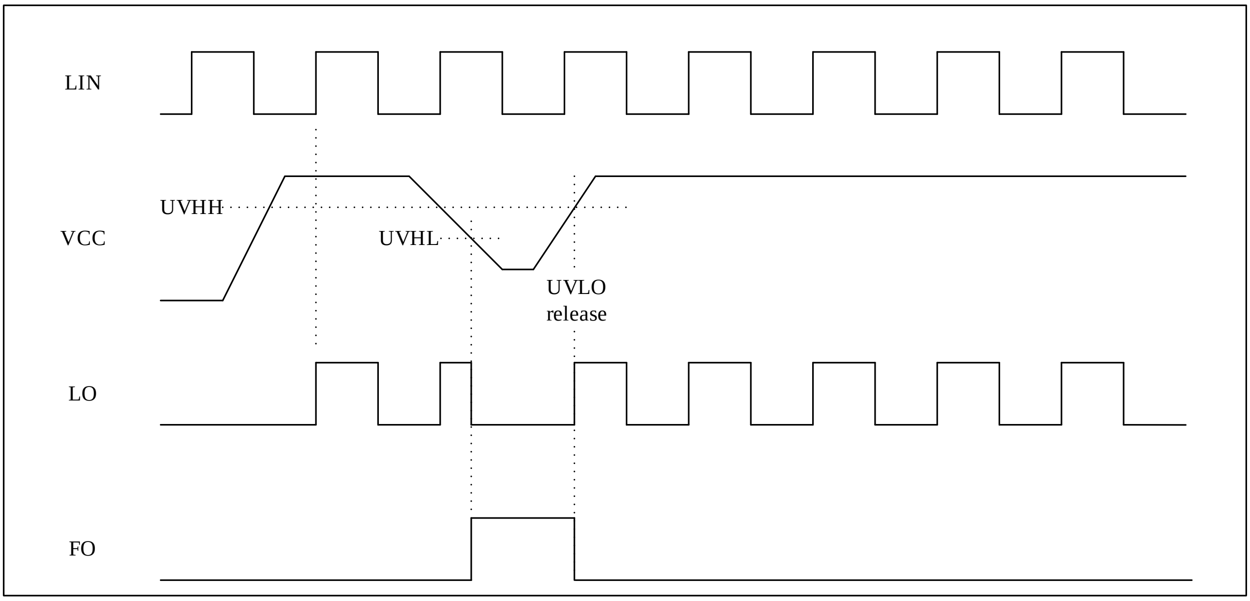


Figure 8-2. Low-side Undervoltage Lockout for Power Supply (UVLO_VCC)

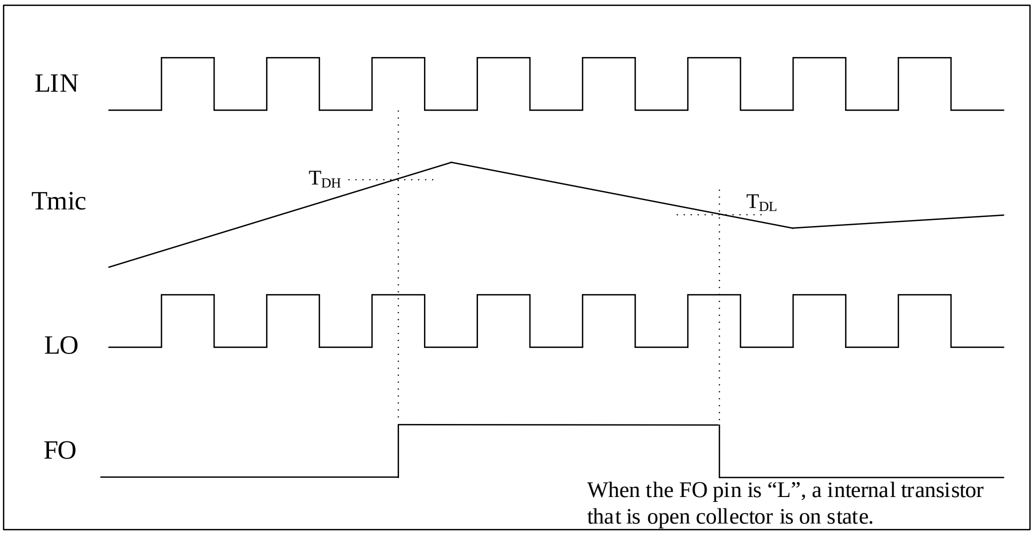
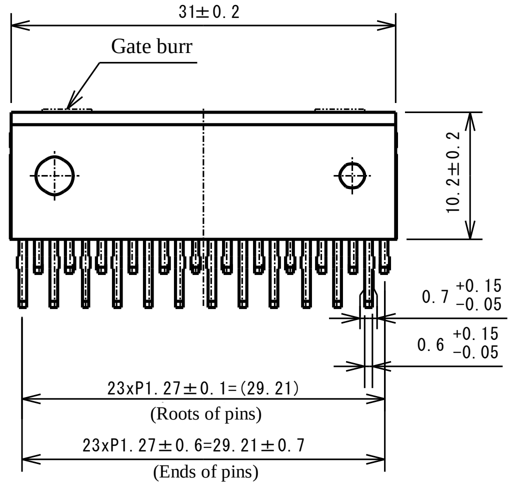


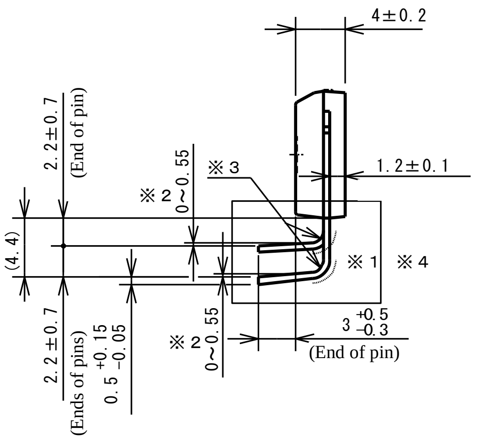
Figure 8-3. Thermal Detection (TD)

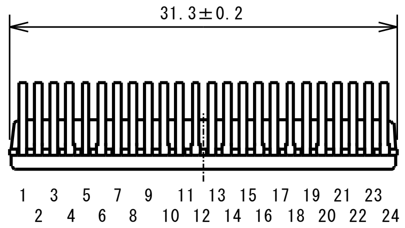
9. Physical Dimensions

9.1. ZIP24 (Fully Molded Type)

● **LF No. 2451**



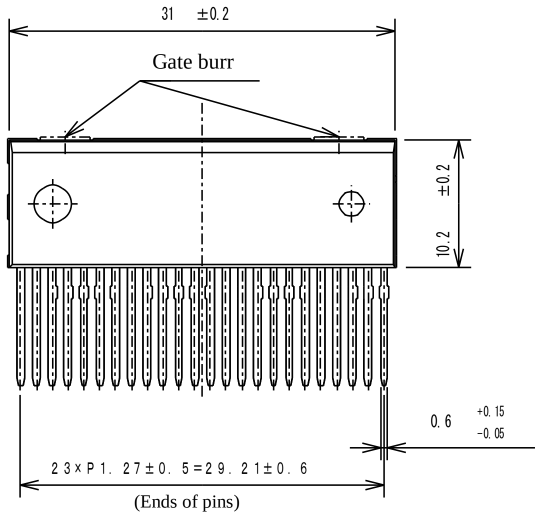


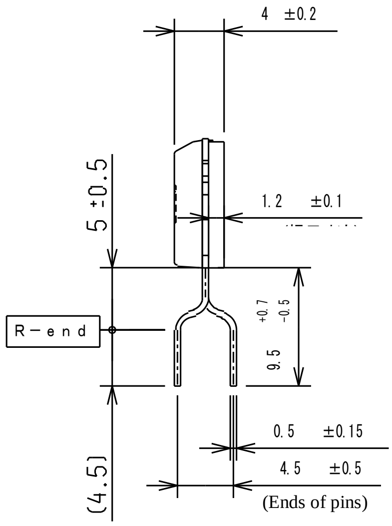


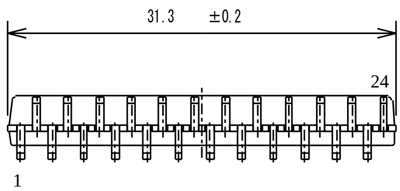
NOTES:

- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)
- Maximum "Gate burr" height: 3 mm

● **LF No. 2452**





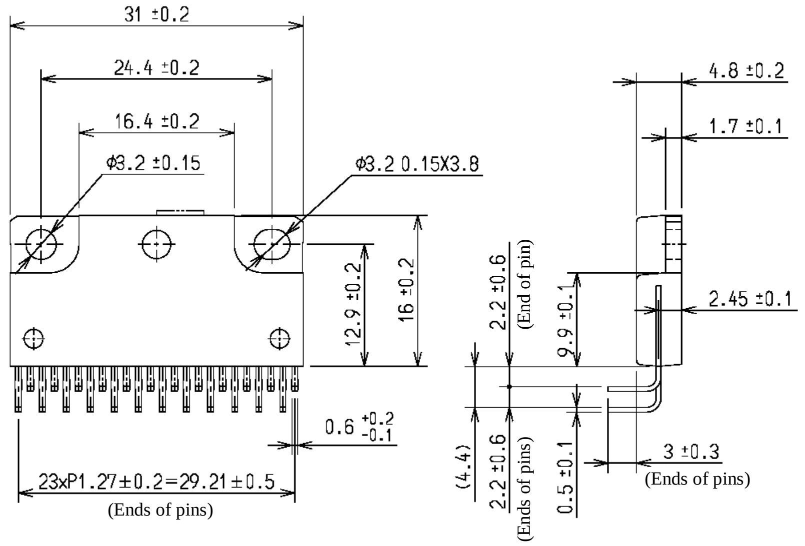


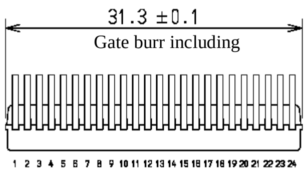
NOTES:

- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)
- Maximum "Gate burr" height: 3 mm

9.2. ZIP24 (Heatsink Type)

- **LF No. 2175**

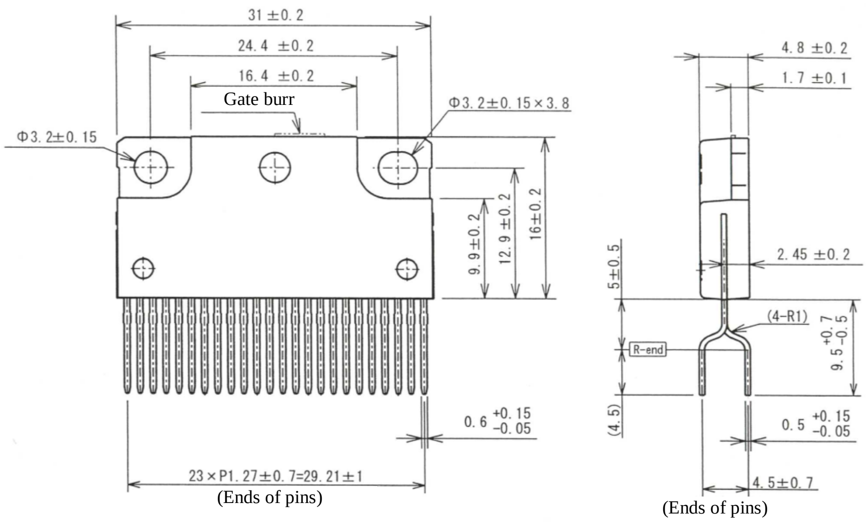


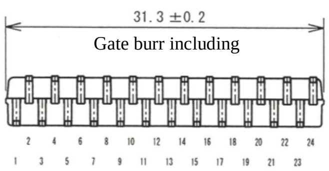


NOTES:

- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)
- The recommended screw torque: 58.8~78.4N·cm (6.0 ~ 8.0 kgf·cm)

- **LF No. 2171**





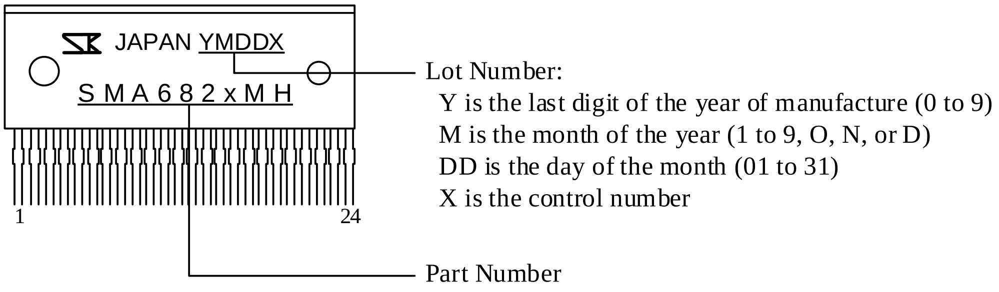
NOTES:

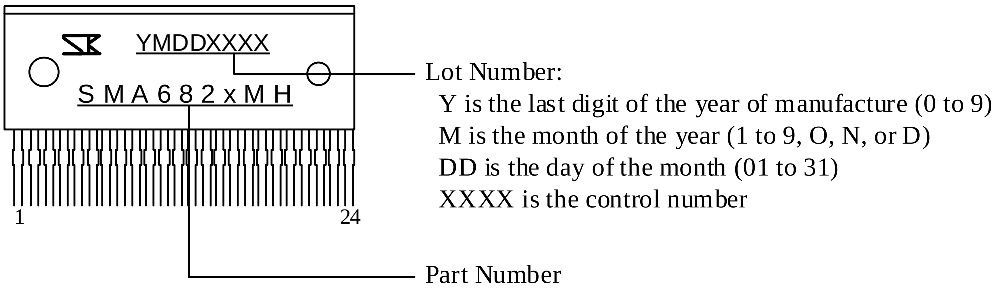
- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)
- The recommended screw torque: 58.8~78.4N·cm (6.0 ~ 8.0 kgf·cm)

10. Marking Diagrams

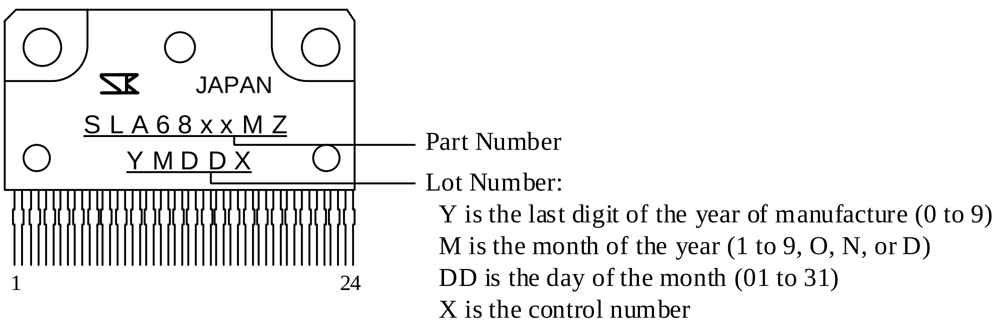
10.1. ZIP24 (Full Molded Type)

The marking diagrams of ZIP24 package is either in follows:





10.2. ZIP24 (Heatsink Type)



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