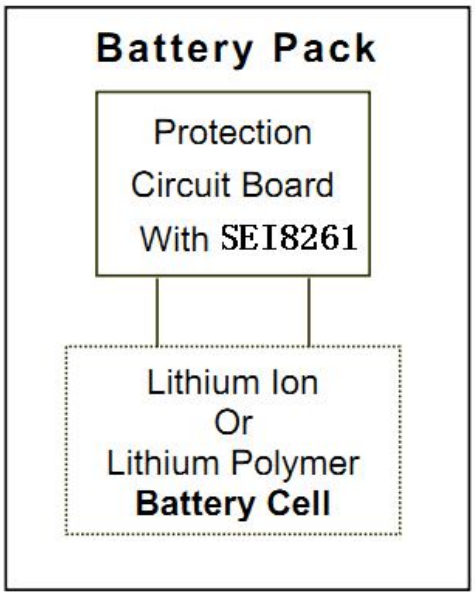
SEI8261
One-Cell Li Battery Protectors

General Description

The SEI8261 Series are protectors for lithium-ion and lithium polymer rechargeable battery with high accuracy voltage detection. They can be used for protecting single cell lithium-ion or/and lithium polymer battery packs from overcharge, over-discharge, excess current and short circuit. These ICs have suitable protection delay functions and low power consumption property.

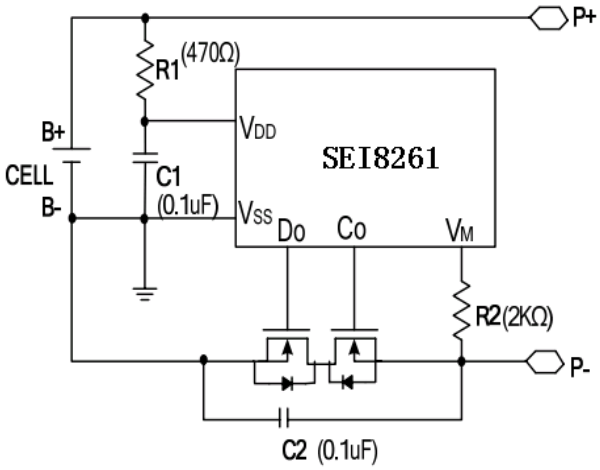
Applications



Features

- Overcharge Threshold
  - 4.200~ 4.400V
  - Accuracy ±25mV(25℃)
    ±50mV (-30℃~80℃)
- Over-discharge Threshold
  - 2.30V~3.00V
  - Accuracy ±75mV
- Excess Current Protection Threshold
  - 0.05V~0.150V @ V_{DD} = 3.30V
  - Accuracy ±0.015V
- Short Circuit Protection Threshold
  - Typ. 0.80V @ V_{DD} = 3.30V
  - Accuracy ±0.15V
- Low Supply Current
  - Typ. 4.0uA @ V_{DD} = 3.9V (Standard working)
  - Typ. 0.1uA @ V_{DD} = 2.0V (Without auto wake up)
  - Typ. 1.8uA @ V_{DD} = 2.0V (With auto wake up)
- Small Package
  - SOT-23-6L
  - DFNWB2*2-6L

Typical Application Circuits



Notes

R1 and C1 are to stabilize the supply voltage of the SEI8261 series. R1C1 is hence regarded as the time constant for V_{DD} pin. C2 is to stabilize the voltage of V_M pin. R1 and R2 can also be a part of current limit circuit for the SEI8261 series.Recommended values of these elements are as follows:

- R1 ＜1kΩ. A larger value of R1 results in higher detection voltage, introducing errors.
- R2＜2.5kΩ. A larger value of R2 possibly prevents resetting from over-discharge even with a charger.
- R1+R2 ＞ 1kΩ. Smaller values may lead to power consumption over the maximum dissipation rating of the SEI8261 series.
- The above diagram and parameters can't insure the circuit work well, please choose the suitable parameters through test.

Product list

Table 1. (@25℃)

Type Number	Over charge threshold (Vdet1)	Over charge release hysteresis voltage (Vhc)	Over discharge threshold(Vdet2)	Over discharge release hysteresis voltage (Vhd)	Discharge over current threshold (Vdet3)	Abnormal Charge Current threshold (Vcha)	Auto wake up function	Delay time combination	Mark (ST/DF)
SEI8261-KA	4.225V	0.1V	2.85V	0.30V	0.100V	-0.120V	No	(2)	61KAS/D
SEI8261-KB	4.225V	0.2V	2.85V	0V	0.150V	-0.120V	No	(3)	61KBS/D
SEI8261-LA	4.275V	0.1V	2.29V	0.10V	0.100V	-0.100V	Yes	(2)	61LAS/D
SEI8261-LB	4.275V	0.1V	2.29V	0.10V	0.150V	-0.120V	No	(1)	61LBS/D
SEI8261-LC	4.275V	0.1V	2.29V	0.10V	0.150V	-0.120V	Yes	(1)	61LCS/D
SEI8261-LD	4.275V	0.1V	2.88V	0.13V	0.050V	-0.075V	No	(2)	61LDS/D
SEI8261-LE	4.275V	0.1V	2.88V	0.30V	0.100V	-0.120V	No	(2)	61LES/D
SEI8261-LF	4.275V	0.2V	2.88V	0V	0.150V	-0.120V	No	(3)	61LFS/D
SEI8261-HA	4.325V	0.1V	2.31V	0.10V	0.150V	-0.120V	No	(1)	61HAS/D
SEI8261-HB	4.325V	0.1V	2.58V	0.12V	0.150V	-0.145V	Yes	(2)	61HBS/D
SEI8261-SA	4.350V	0.1V	2.33V	0.10V	0.150V	-0.120V	No	(1)	61SAS/D
SEI8261-TA	4.375V	0.1V	2.34V	0.10V	0.150V	-0.120V	No	(1)	61TAS/D

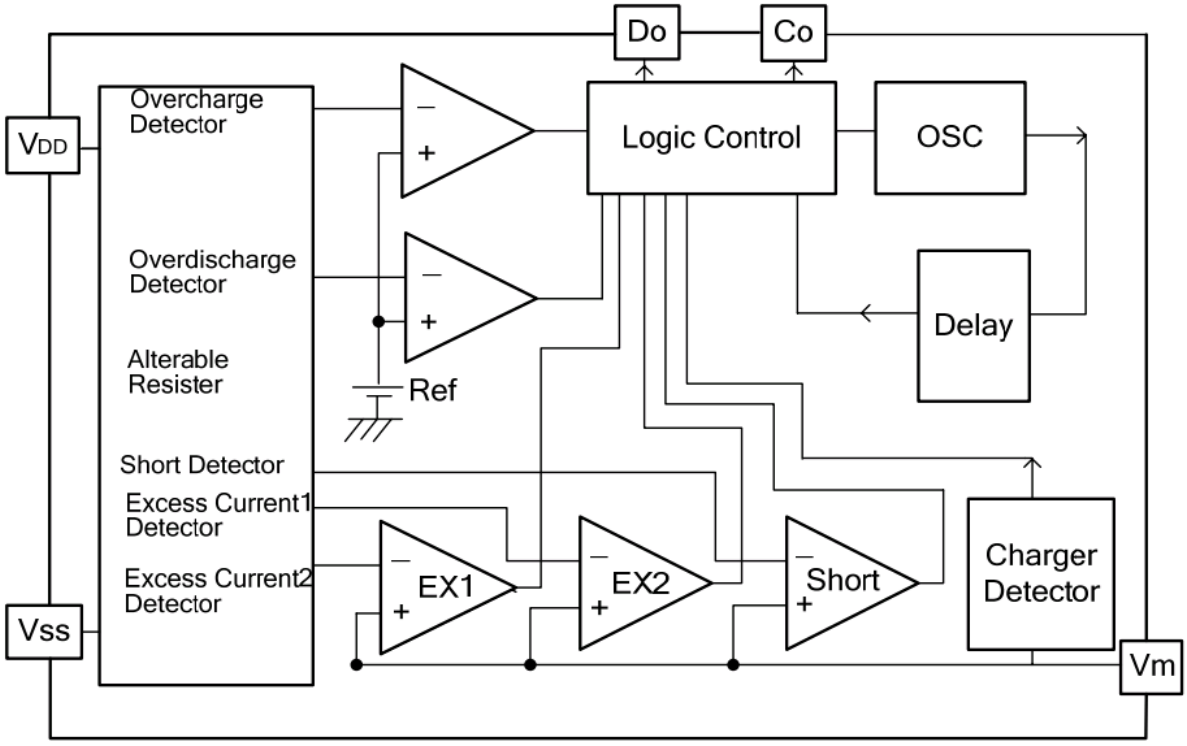
Table 2 The detail of delay time combination (1)to(3) (@ 25℃)

Delay time combination	Output Delay Of Overcharge Tvdet1	Abnormal Charge Delay Time Tab	Output Delay Of Over-discharge Tvdet2	Output Delay Of Excess Current 1 Tvdet3
(1)	300~900ms Typ:600ms	9~27ms Typ:18ms	36~108ms Typ:72ms	5~15ms Typ:10ms
(2)	300~900ms Typ:600ms	5~15ms Typ:10ms	36~108ms Typ:72ms	5~15ms Typ:10ms
(3)	0.55~1.65s Typ:1.1s	5~15ms Typ:10ms	36~108ms Typ:72ms	5~15ms Typ:10ms

Table 3 The detail of delay time combination (1)' to (3)' (@ -30℃~80 ℃)

Delay time combination	Output Delay Of Overcharge Tvdet1	Abnormal Charge Delay Time Tab	Output Delay Of Over-discharge Tvdet2	Output Delay Of Excess Current 1 Tvdet3
(1)'	250~1000ms Typ:600ms	7.5~30ms Typ:18ms	30~120ms Typ:72ms	4~16ms Typ:10ms
(2)'	250~1000ms Typ:600ms	3~18ms Typ:10ms	30~120ms Typ:72ms	3~18ms Typ:10ms
(3)'	0.55~1.65s Typ:1.1s	3~18ms Typ:10ms	30~120ms Typ:72ms	3~18ms Typ:10ms

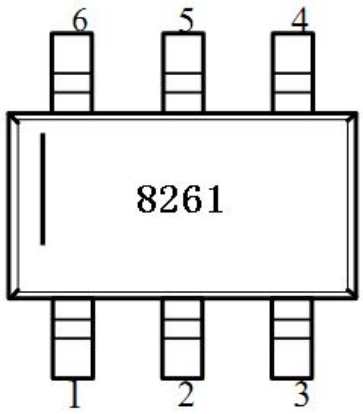
Block Diagram



Pin Description

Table 1 SOT-23-6L

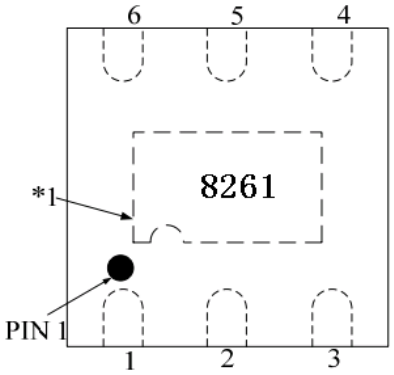
Pin	Symbol	Function Description
1	D_O	Over-discharge detection, CMOS output
2	V_M	Connected to charger's negative pin
3	C_O	Overcharge detection, CMOS output
4	NC	No connection
5	V_{DD}	Power supply
6	V_{SS}	Ground



SOT-23-6
(Top Side)

Table 2 DFNWB2*2-6L

Pin	Symbol	Function Description
1	C_O	Overcharge detection, CMOS output
2	V_M	Connected to charger's negative pin
3	D_O	Over-discharge detection, CMOS output
4	V_{SS}	Ground
5	V_{DD}	Power supply
6	NC	No connection
*1	NC	No connection



DFNWB2*2-6L
(Top Side)

Notes: Overcharge delay, excess-current delay and over-discharge delay will all be shorten with the DP connected to V_{DD}. In normal condition, DP should be connected to Vss or floating. In the package of DFNWB2*2-6L, Pin1 to pin6 are the lead connection.

Function Description

Normal Condition:

V_{DD} is between the Over-discharge Detection Threshold(Vdet2) and Overcharge Detection Threshold (Vdet1) and the VM pad voltage is between Charger Detection Voltage (Vcha) and the Excess Current 1 Threshold Voltage (Vdet3),therefore the outputs of D_O pad and C_O pad are high and the MOSFETs of charge and discharge are all on. Charging and discharging can be carried out freely.

Overcharge Condition:

When V_{DD} increases and passes Vdet1 during charging under the normal condition, the output of Co pad will change from high to low after Overcharge Detection Delay Time (Tvdet1),turning off the charging control FET.

If, within Tvdet1, V_{DD} becomes lower than Vdet1 and stays for duration shorter than Overcharge Reset Delay Time (Treset) before rising up over Vdet1 again, this type of instantaneous falling of V_{DD} is ignored. Otherwise, if the time V_{DD} stays lower than Vdet1 is longer than Treset, the timing related to Tvdet1 shall be reset.

Abnormal Charge Current Condition:

If the V_M pin voltage falls below the Charger Detection Voltage (Vcha) during charging under normal condition and it continues for the Abnormal Charge Current Delay Time (Tab) or longer, the charging control FET turns off and charging stops. This action is called the abnormal charge current detection.

Abnormal charge current detection works when the D_O pin voltage is “H” and the V_M pin voltage falls below the Charger Detection Voltage (Vcha). To an over-discharged battery,only when charging makes the battery voltage higher than the Over-discharge Detection Threshold (VDT), the Abnormal Charge Current Detection can act. Abnormal charge current state is released, once the voltage difference between V_M pin and V_{SS} pin becomes less than the Abnormal Charge Current Detection Threshold Voltage(VAB) value.

Overcharge Protection Release Condition:

The charging state can be reset and the output of Co becomes high when V_{DD} becomes lower than the Overcharge Release Voltage (Vrel1) and stays longer than Overcharge Release Delay Time (Tvrel1).

When a load is connected to V_{DD} after a charger is disconnected from the battery pack, while the V_{DD} level is lower than Vdet1, the output of Co becomes high.

Over-discharge Condition:

While discharging, after V_{DD} lowers below Over-discharge Detection Threshold (Vdet2), Do pad goes low after Over-discharge Detection Delay Time (Tvdet2). The Do pad would switch off the discharging control FET and stop discharging.

Over-discharge Protection Release Condition:

When IC is in over-discharge condition, if a charger is connected to the battery pack, and the battery supply voltage becomes higher than Vdet2, and VM is lower than Charger Detection Voltage (Vcha), Do pad becomes high, allowing discharging action.

IC without Auto wake up function:The discharging state also can be reset and the output of Do becomes high when V_{DD} becomes higher than the Over-discharge Release Voltage(Vrel2), VM is between Vdet3 and Vcha, and stays longer than Release Delay Time (Tvrel2).

IC with Auto wake up function: The discharging state also can be reset and the output of Do becomes high when V_{DD} becomes higher than the Over-discharge Release Voltage(Vrel2), VM is between Vcha and Vdd, and stays longer than Release Delay Time (Tvrel2).

When a charger is connected from the battery pack, while

the V_{DD} level is lower than Vdet2, the battery pack makes charger current allowable through the external diode.

Charger Detect Condition:

When a battery in the over-discharge condition is connected to a charger and provided that the V_M pin voltage is lower than the Charger Detection Voltage (Vcha), IC releases the over-discharge condition and turns on the discharging control FET as the battery voltage becomes higher than the Over-discharge Detection Voltage (Vdet2) since the charger detection function works. This action is called charger detection.

When a battery in the over-discharge condition is connected to a charger and provided that the V_M pin voltage is between the Charger Detection Voltage (Vcha) and Excess Current 1 Threshold Voltage (Vdet3), IC releases the over-discharge condition when the battery voltage reaches the Over-discharge Release Voltage (Vrel2) or higher.

Excess Current 1 Protection:

During discharging, the current varies with load, and V_M increases with the rise of the discharging current. Once V_M rises up to the Excess Current 1 Threshold Voltage (Vdet3) or higher and stays longer than the Excess Current 1 Delay Time(Tvdet3), Do pad switches to low, turning off the discharging control FET. After that excess current state is removed, i.e.V_M＜Vdet3, and the circuit recovers to normal condition.

Excess Current 2 Protection:

During discharging, the current varies with load, and V_M increases with the rise of the discharging current. Once V_M rises up to Excess Current 2 Threshold Voltage (Vdet4) or higher, and stays longer than Excess Current 2 Delay Time(Tvdet4), Do pad switches to low, turning off the discharging control FET. After that excess current state is removed, i.e.V_M ＜ Vdet3, and the circuit recovers to normal condition.

Short Circuit Protection:

This function has the same principle as the excess current protection. But, the delay time Tshort is far shorter than Tvdet3 and Tvdet4, and the threshold Vshort is far higher than Vdet3 and Vdet4. When the circuit is shorted, VM increases rapidly. Once V_M≥Vshort, Do pad switches to low, turning off the discharging control FET. After the short circuit state is removed, i.e. V_M ＜ Vdet3, the circuit recovers to the normal condition. The short circuit peak current is related to Vshort and the ON resistance of the two FETs in series. Output types of Co and Do are CMOS level.

0V battery charge function

This function is used to recharge the connected battery whose voltage is 0V due to the self-discharge. When the 0 V battery charge starting charger voltage (V0cha) or higher is applied between P+ and P− pins (see the Typical Application Circuits of Page1) by connecting a charger, the charging control FET gate is fixed to V_{DD} pin voltage. When the voltage between the gate and source of the charging control FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging control FET turns on to start charging. At this time, the discharging control FET is off and the charging current flows through the internal parasitic diode in the discharging control FET. When the battery voltage becomes equal to or higher than the Over-discharge Detection Threshold (Vdet2), the IC enters the normal condition.

Electrical Characteristics [1*]

(TOPT=25℃ unless otherwise specified)

Symbol	Item	Conditions	Min.	TYP.	Max.	Unit
DETECTION VOLTAGE AND DELAY TIME						
Vdet1[2*]	Overcharge Threshold 4.200~4.400V, Step 5mV	25℃	Vdet1–0.025	Vdet1	Vdet1 + 0.025	V
Vrel1[3*]	Release Voltage For Overcharge Detection		VDET1–1.3Vhc	VDET1–Vhc	VDET1 –0.7Vhc	V
Vdet2 [2*]	Over-discharge Threshold 2.2~2.4V	Detect falling edge of supply voltage	Vdet2 – 0.075	Vdet2	Vdet2 + 0.075	V
Vrel2[3*]	Release Voltage For Over-discharge Detection		VDET2+0.7Vhd	VDET2+Vhd	VDET2+1.3Vhd	V
Vdet3	Excess Current 1 Threshold	V_{DD} = 3.30V	Vdet3-0.015	Vdet3	Vdet3+0.015	V
Vdet4	Excess Current 2 Threshold	V_{DD} = 3.30V	0.35	0.40	0.45	V
Vshort	Short Protection Voltage	V_{DD} = 3.30V	0.65	0.80	0.95	V
Vcha	Charger Detection(Abnormal Charge)		Vcha -0.030	Vcha	Vcha +0.030	V
V0cha	0V Battery Charge Starting Charger Voltage	Applied for 0V battery charge function	1.2			V
Tvrel1	Overcharge ReleaseDelay Time	V_{DD}= 4.4V→4.0V	8	25	40	ms
Treset	Overcharge Reset Delay Time	V_{DD}= 4.4V→4.0V→4.4V	5	23	38	ms
Tvrel2	Over-discharge Release Delay Time	V_{DD}= 2.0V→3.0V, VM= 0V	1.1	2.2	3.3	ms
Tvdet4	Output Delay Of Excess Current 2	V_{DD}=3.30V	0.6	1.1	1.6	ms
Tshort	Output Delay Of Short Protection	V_{DD}=3.30V	70	140	210	us
OUTPUT VOLTAGE AND VM INTERNAL RESISTANCE						
V_{cOL}	CO Pin L Voltage	I_{OL}=50uA, V_{DD} =4.4V	0.15	0.20	0.25	V
V_{cOH}	CO Pin H Voltage	I_{OH}=-50uA, V_{DD}=3.9V	3.75	3.70	3.65	V
V_{DOL}	DO Pin L Voltage	I_{OL}=50uA, V_{DD}=2.0V	0.05	0.07	0.09	V
V_{DOH}	DO Pin H Voltage	I_{OH}=-50uA,V_{DD} =3.9V	3.85	3.83	3.81	V
R_{VMD}	Resistance between VM and VDD	V_{DD}=2.0V, V_M =0V	100	300	900	kΩ
R_{VMS}	Resistance between VM and VSS	V_{DD}=3.3V, V_M =1V	60	130	300	kΩ
OPERRATION VOLTAGE AND CURRENT CONSUMPTION						
V_{DD}	Operating Input Voltage	V_{DD}-Vss	1.6	VDD	8	V
VM	Operating Input Voltage	V_{DD}-V_M	1.5	--	28	V
I_{DD}	Supply Current	V_{DD} = 3.9V, V_M = 0V	--	4.0	7.0	uA
$I_{STANDBY}$	Standby Current (for products without Auto wake up)	V_{DD} = 2.0V, V_M = 0V→2.0V	--	0.1	0.7	uA
$I_{STANDBY}$4*	Standby Current (for products with Auto wake up)	V_{DD} = 2.0V	--	1.8	3.5	uA

1* The Electrical parameters for this temperature range is guaranteed by design, not tested in production.

2* See “Selection Guide” section.

3* VDET1 and VDET2 are the Overcharge and Over-discharge threshold voltage of actual testing.

4* Vhc and Vhd are the Overcharge and Over-discharge hysteresis voltage.

Electrical Characteristics [1*]

(TOPT= -30℃~80℃ unless otherwise specified)

Symbol	Item	Conditions	Min.	TYP.	Max.	Unit
DETECTION VOLTAGE AND DELAY TIME						
Vdet1[2*]	Overcharge Threshold 4.200~4.400V, Step 5mV	25℃	Vdet1–0.050	Vdet1	Vdet1 + 0.050	V
Vrel1[3*]	Release Voltage For Overcharge Detection Vhc=0.1V~0.3V		VDET1–1.4Vhc	VDET1–Vhc	VDET1 –0.6Vhc	V
Vdet2 [2*]	Over-discharge Threshold 2.2~2.4V	Detect falling edge of supply voltage	Vdet2 – 0.1	Vdet2	Vdet2 + 0.1	V
Vrel2[3*]	Release Voltage For Over-discharge Detection Vhc=0.1V~0.3V		VDET2+0.6Vhd	VDET2+Vhd	VDET2+1.4Vhd	V
Vdet3	Excess Current 1 Threshold	V_{DD} = 3.30V	Vdet3-0.020	Vdet3	Vdet3+0.020	V
Vdet4	Excess Current 2 Threshold	V_{DD} = 3.30V	0.27	0.40	0.53	V
Vshort	Short Protection Voltage	V_{DD} = 3.30V	0.50	0.80	1.30	V
Vcha	Charger Detection(Abnormal Charge)		Vcha -0.040	Vcha	Vcha +0.040	V
V0cha	0V Battery Charge Starting Charger Voltage	Applied for 0V battery charge function	1.2			V
Tvrel1	Overcharge ReleaseDelay Time	V_{DD}= 4.4V→4.0V	5	25	42	ms
Treset	Overcharge Reset Delay Time	V_{DD}= 4.4V→4.0V→4.4V	3	23	40	ms
Tvrel2	Over-discharge Release Delay Time	V_{DD}= 2.0V→3.0V, V_M= 0V	0.9	2.2	3.6	ms
Tvdet4	Output Delay Of Excess Current 2	V_{DD}=3.30V	0.45	1.1	1.8	ms
Tshort	Output Delay Of Short Protection	V_{DD}=3.30V	55	140	230	us
OUTPUT VOLTAGE AND VM INTERNAL RESISTANCE						
V_{cOL}	CO Pin L Voltage	I_{OL}=50uA, V_{DD} =4.4V	0.10	0.20	0.30	V
V_{cOH}	CO Pin H Voltage	I_{OH}=-50uA, V_{DD}=3.9V	3.80	3.70	3.60	V
V_{DOL}	DO Pin L Voltage	I_{OL}=50uA, V_{DD}=2.0V	0.03	0.07	0.11	V
V_{DOH}	DO Pin H Voltage	I_{OH}=-50uA,V_{DD} =3.9V	3.87	3.83	3.79	V
R_{VMD}	Resistance between VM and VDD	V_{DD}=2.0V, V_M =0V	78	300	1310	kΩ
R_{VMS}	Resistance between VM and VSS	V_{DD}=3.3V, V_M =1V	40	130	400	kΩ
OPERRATION VOLTAGE AND CURRENT CONSUMPTION						
V_{DD}	Operating Input Voltage	V_{DD}-Vss	1.6	VDD	8	V
V_M	Operating Input Voltage	V_{DD}-V_M	1.5	--	28	V
I_{DD}	Supply Current	V_{DD} = 3.9V, V_M = 0V	--	4.0	8.0	uA
$I_{STANDBY}$	Standby Current (for products without Auto wake up)	V_{DD}=2.0V,V_M= 0V→2.0V	--	0.1	1	uA
$I_{STANDBY}$4*	Standby Current (for products with Auto wake up)	V_{DD} = 2.0V	--	1.8	4.0	uA

1* The Electrical parameters for this temperature range is guaranteed by design, not tested in production.

2* See “Selection Guide” section.

3* VDET1 and VDET2 are the Overcharge and Over-discharge threshold voltage of actual testing.

4* Vhc and Vhd are the Overcharge and Over-discharge hysteresis voltage.

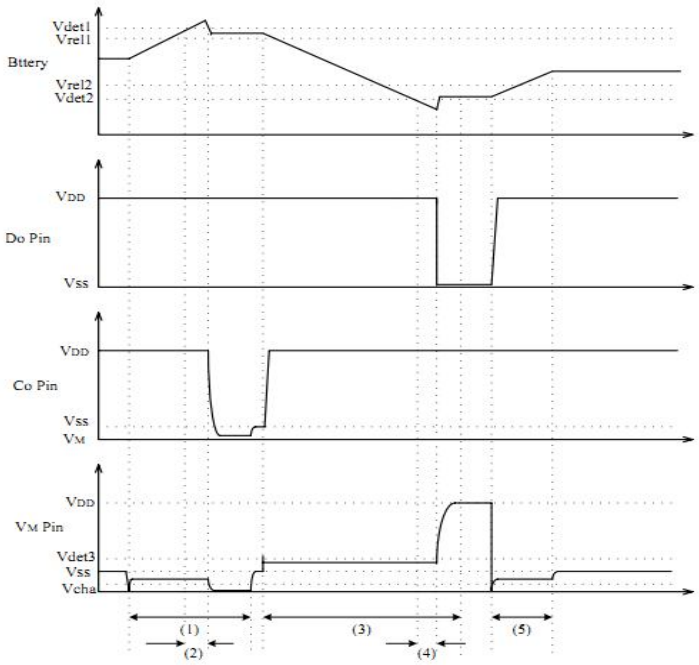
Absolute Maximum Ratings（Ta= 25 ºC　Vss=0 V）

Symbol	Item	Ratings	Unit
V_{DD}	Supply Voltage	-0.3 to 8	V
V_M	V_M Pin Input Voltage	V_{DD} -28 to V_{DD} +0.3	V
V_{CO}	Co Pin Output Voltage	V_{DD} -28 to V_{DD} +0.3	V
V_{DO}	Do Pin Output Voltage	Vss-0.3 to V_{DD} +0.3	V
Pd	Power Dissipation	150	mW
Topt	Operating Temperature Range	-30 to 80	℃
Tstg	Storage Temperature Range	-55 to 125	℃

Caution: These values must not be exceeded under any conditions.

Operation Timing Chart (1)

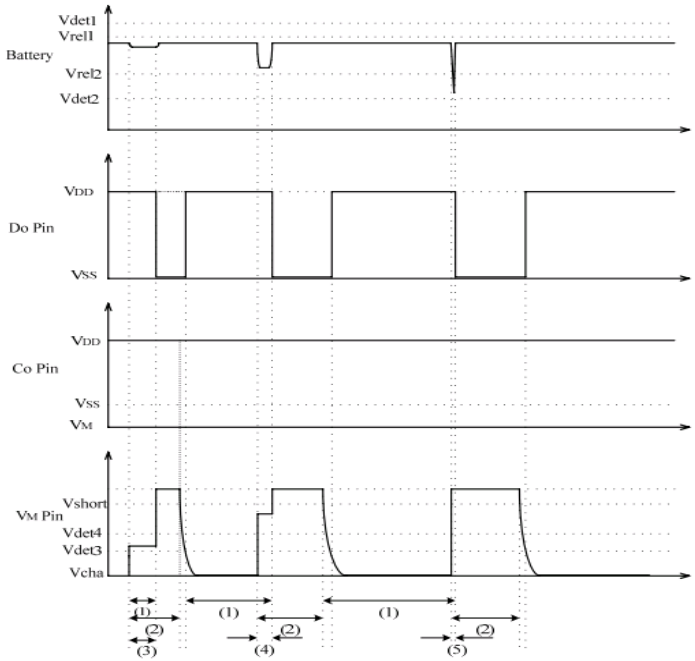
Overcharge/Over-discharge Detection



(1) Charger connected
(2) Overcharge Detection Delay Time (Tvdet1)
(3) Load connected
(4) Over-discharge Detection Delay Time (Tvdet2)
(5) Normal charging

Operation Timing Chart (2)

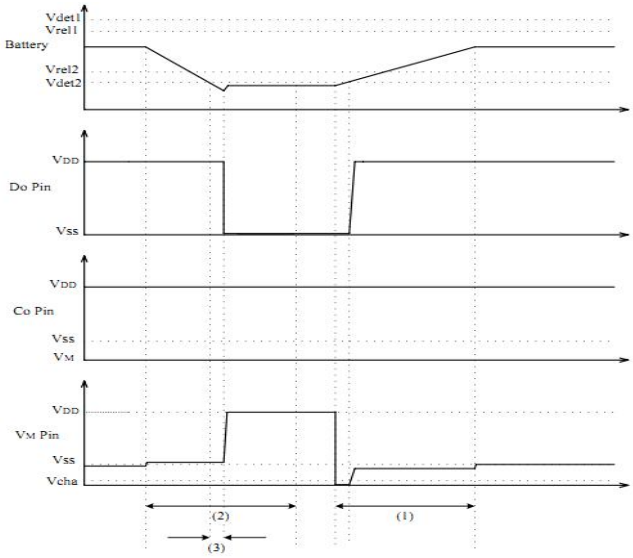
Excess Current and Short Protection



(1) Normal condition
(2) Load connection
(3) Excess Current 1 Delay Time (Tvdet3)
(4) Excess Current 2 Delay Time (Tvdet4)
(5) Short Circuit Delay Time (Tshort)

Operation Timing Chart (3)

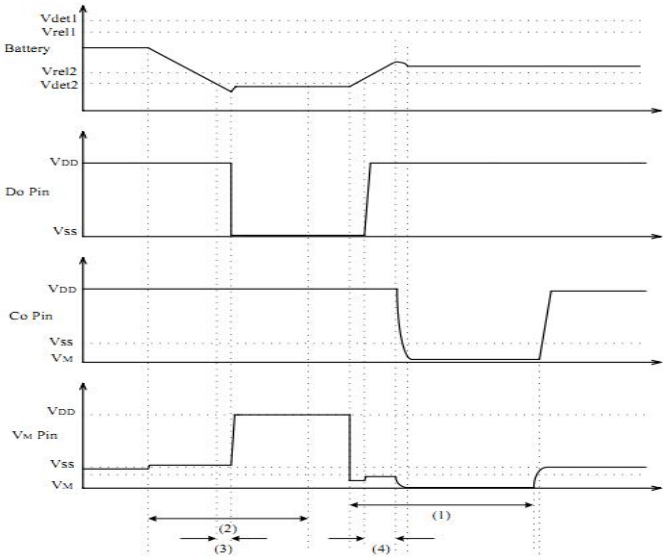
Charger Connection Detection



(1) Charger connection
(2) Load connection
(3) Over-discharge Detection Delay (Tvdet2)

Operation Timing Chart (4)

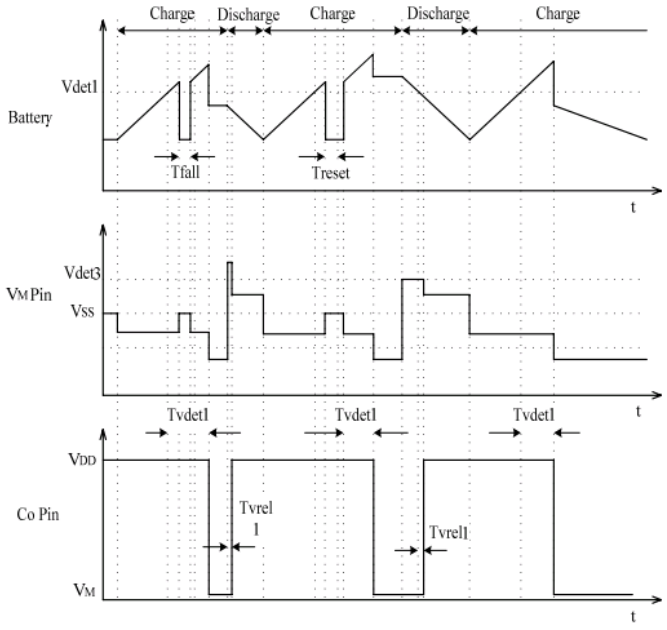
Abnormal Charge Current Detection



(1) Charger connection
(2) Load connection
(3) Over-discharge Detection Delay Time (Tvdet2)
(4) Abnormal Charging Current Detection Delay Time

Operation Timing Chart (5)

Overcharge, Timer Reset for Overcharge



Test Circuits

(1) Overcharge detection voltage and overcharge release voltage

Test circuit 1

The Overcharge Detection Voltage (Vdet1) is the voltage between V_{DD} and V_{SS} to which when V1 increases and keeps the condition for overcharge delay time, Vco changes from “H” to “L”. The Overcharge Release Voltage (Vrel1) is the voltage between V_{DD} and V_{SS} to which when V1 decreases, Vco changes from “L” to “H”.

(2) Over-discharge detection voltage and over-discharge release voltage

Test circuit 1

The Over-discharge Detection Voltage (Vdet2) is the voltage between V_{DD} and V_{SS} to which when V1 decreases and keep the condition for over-discharge delay time, V_{DO} changes from “H” to “L”. The over-discharge Release Voltage (Vrel2) is the voltage between V_{DD} and V_{SS} to which when V1 increases, V_{DO} changes from “L” to “H”.

(3) Over current detection voltage and short circuit detection voltage

Test circuit 2

The Excess Current 1 Detection Voltage (Vdet3) is the voltage between V_M and V_{SS} to which when VM increases within 10 us and keep the condition for Excess Current 1 Delay Time (Tvdet3), V_{DO} changes from “H” to “L”.

The Excess Current 2 Detection Voltage (Vdet4) is the voltage between V_M and V_{SS} to which when V_M increases within 10 us and keep the condition for Excess Current 2 Delay Time (Tvdet4), V_{DO} changes from “H” to “L”.

The Short Circuit Detection Voltage (Vshort) is the voltage between V_M and V_{SS} to which when VM increases within 10us and keep the condition for Short Circuit Delay Time(Tshort), V_{DO} changes from “H” to “L”.

(4) Charger detection voltage and abnormal charge current detection voltage

Test circuit 2

In the over-discharge condition, increase V1 gradually until it is between Vdet2 and Vrel2. The voltage between V_M and V_{SS} to which when V2 decreases, V_{DO} changes from “L” to“H”, is the Charger Detection Voltage (Vcha).

In the normal charging condition, the voltage between V_M and V_{SS} to which when V2 decreases, Vco changes from “H” to “L” is the abnormal charge current detection voltage.It has the same value as the Charger Detection Voltage(Vcha).

(5) 0V battery charge starting charger voltage

Test circuit 2

Set V1=V2=0V and decrease V2 gradually. The voltage between V_{DD} and V_M when Vco goes “H”(VVM+0.1V or higher) is the 0V battery charge starting charger voltage.

(6) Normal operation current consumption and power down current consumption

Test circuit 2

Set V1=3.5V and V2=0V under normal condition, the current I_{DD} flowing through V_{DD} pin is the normal operation consumption current (I_{DD}).

Set V1=3.5V and V2=0V，let IC work in normal condition,set V1 from 3.5V to 2.0V, then set V2=2.0V under over-discharge condition, the current I_{DD} flowing through V_{DD} pin is the power down current consumption ($I_{STANDBY}$).

(7) Overcharge detection (release) delay time and over-discharge detection (release) delay time

Test circuit 3

If V1 increases to be Vdet1 or over Vdet1 and keeps the condition for some time, Vco will change from “H” to “L”. The time is called overcharge detection delay time. It is used to judge whether overcharge happens indeed. If V1 decreases from Vdet1 or over Vdet1 to below Vrel1, Vco will change from “L” to “H”. The difference between this time and Treset is called overcharge release delay time.

If V1 decreases to be Vdet2 or below Vdet2 and keeps the condition for some time, V_{DO} will change from “H” to “L”. The time is called over-discharge detection delay time. It is used to judge whether over-discharge happens indeed. If V1 increases from Vdet2 or below Vdet2 to over Vrel2 and keeps the condition for some time, V_{DO} will change from “L” to “H”. The time is called over-discharge release delay time.

(8) Over current detection delay time and short circuit detection delay time

Test circuit 3

If V2 increases to be Vdet3 or over Vdet3 and keeps the condition for some time, V_{DO} will change from “H” to “L”. The time is called over current 1 delay time. It is used to judge whether over current 1 happens indeed.

If V2 increases to be Vdet4 or over Vdet4 and keeps the condition for some time, V_{DO} will change from “H” to “L”. The time is called over current 2 delay time. It is used to judge whether over current 2 happens indeed.

If V2 increases to be Vshort or over Vshort and keeps the condition for some time, V_{DO} will change from “H” to “L”. The time is called short circuit delay time. It is used to judge whether short circuit happens indeed.

(9) Co pin H resistance, Co pin L resistance

Test circuit 4

Set V1=3.9V, V2=0 V, I_{Co}=50uA (from Co to V3), K1 on and K2 off. (V1-V3)/I_{Co} is the Co pin H resistance.

Set V1=4.4 V, V2=0 V, I_{Co}=-50uA (from V3 to Co), K1 on and K2 off. V3/ICo is the Co pin L resistance.

(10) Do pin H resistance, Do pin L resistance

Test circuit 4

Set V1=3.9 V, V2=0 V, I_{Do}=50uA (from Do to V4), K1 off and K2 on. (V1-V4)/I_{Do} is the Do pin H resistance.

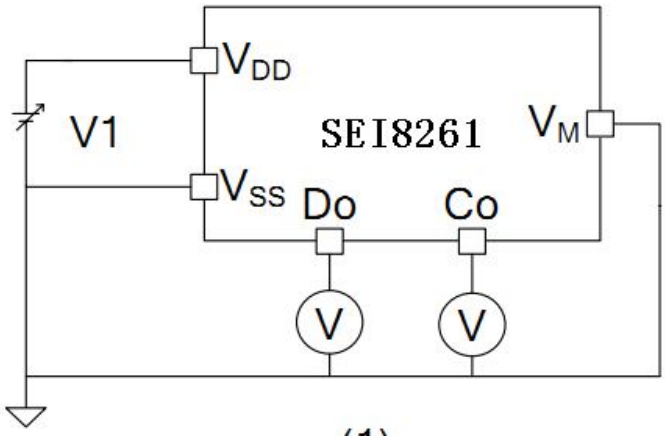
Set V1=2.0 V, V2=0 V and I_{Do}=50uA (from V4 toDo), K1 off and K2 on. V4/I_{Do} is the Do pin L resistance.

(11) Internal resistance V_M -V_{DD} and V_M -V_{SS}

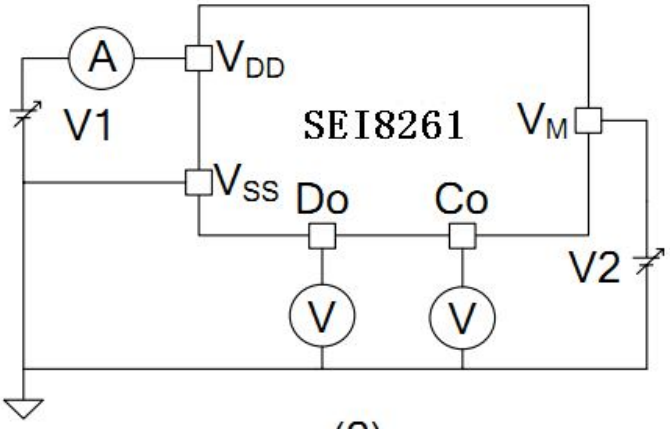
Test circuit 4

Set V1=2.0 V, V2=0 V, K1 off and K2 off, V1/I_{VM} is the internal resistance R_{VMD}.

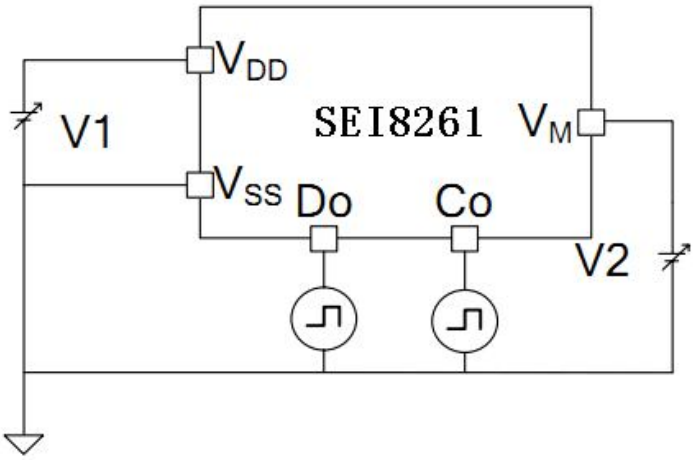
Set V1=3.3 V, V2=1 V, K1 off and K2 off, V2/I_{VM} is the internal resistance R_{VMS}.


V1
VDD
VSS
SEI8261
VM
Do
Co
V
V

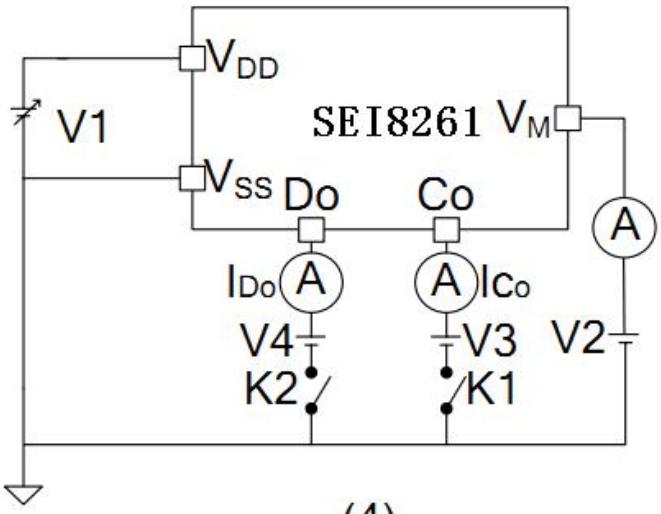
(1)


A
V1
VDD
VSS
SEI8261
VM
Do
Co
V2
V
V

(2)


V1
VDD
VSS
SEI8261
VM
Do
Co
V2

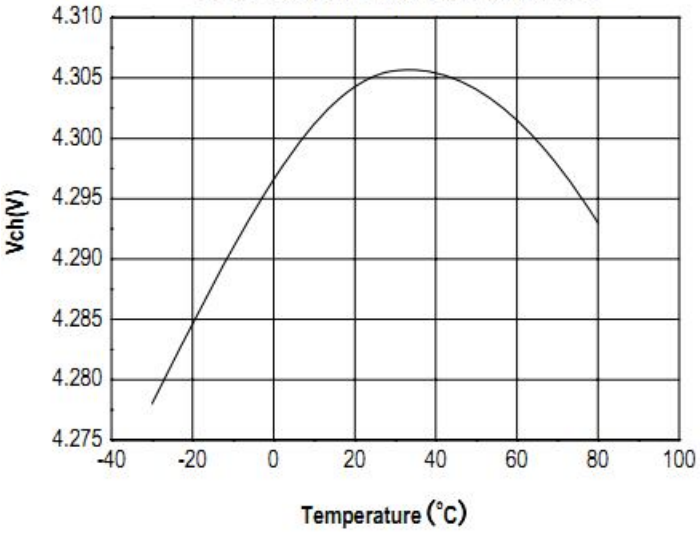
(3)


V1
VDD
VSS
SEI8261
VM
Do
Co
A
IDo
A
A
ICo
V4
V3
V2
K2
K1

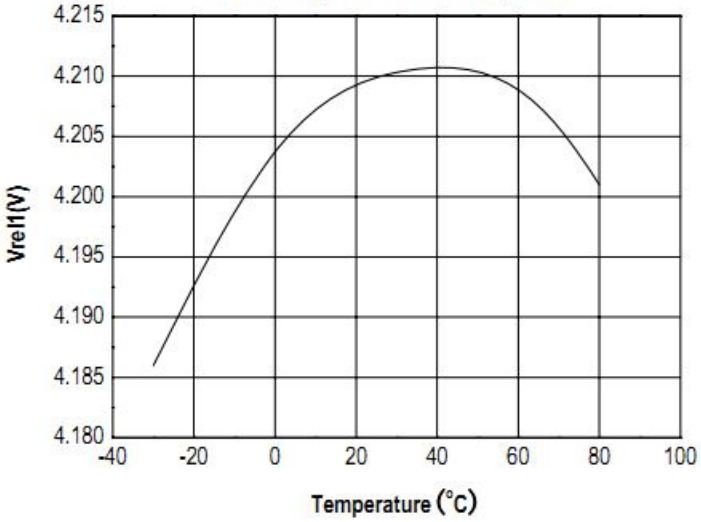
(4)

Typical Characteristic Charts

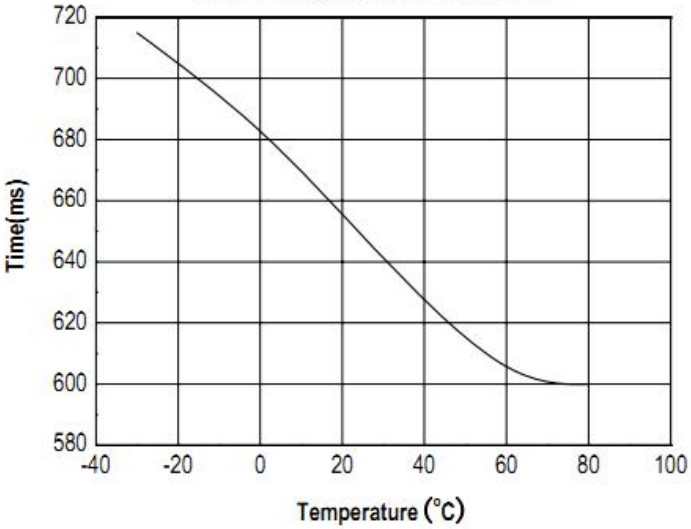
1.Over-charge Threshold VS. Temperature



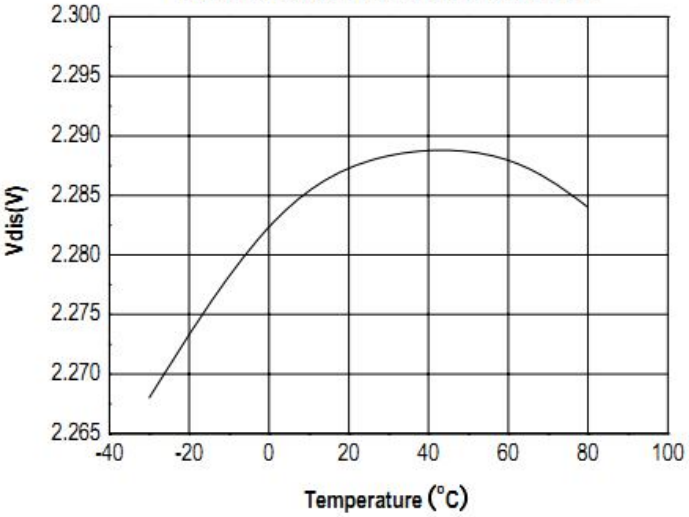
2.Over-charge Release VS. Temperature



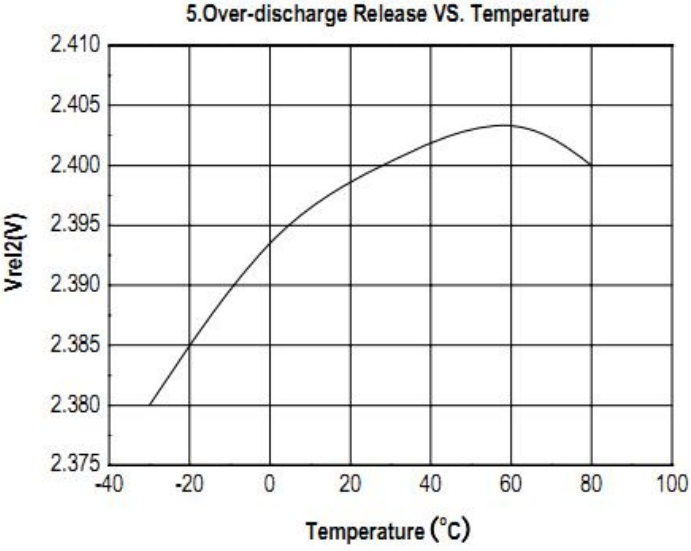
3.Over-charge Delay VS. Temperature



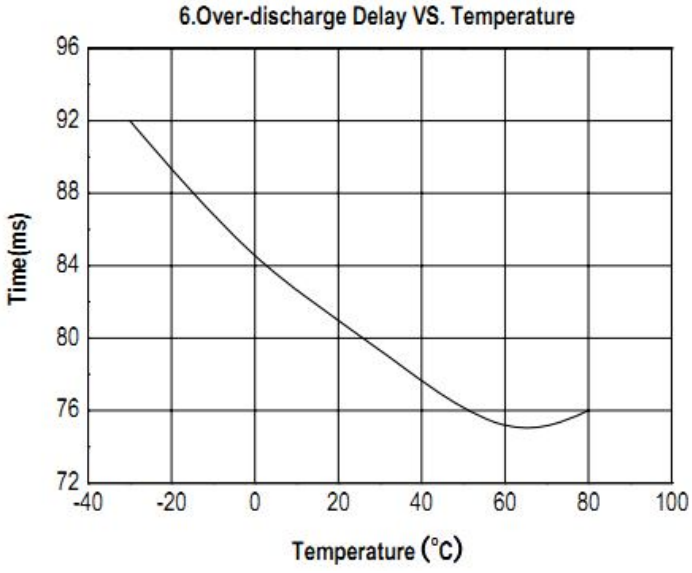
4.Over-discharge Threshold VS. Temperature

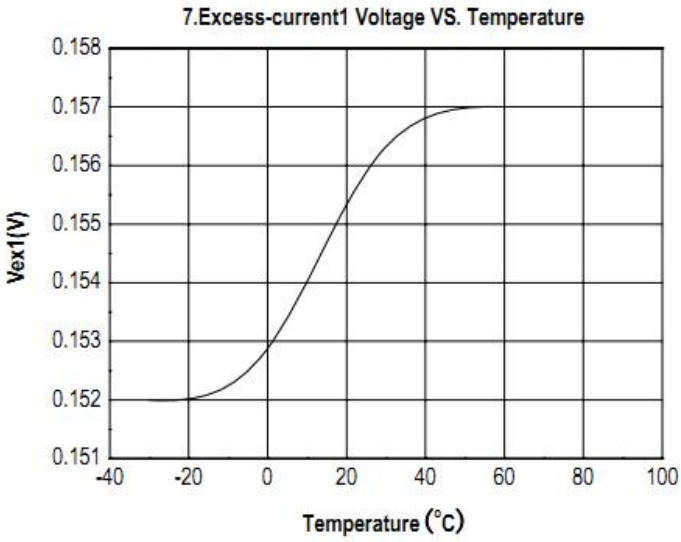


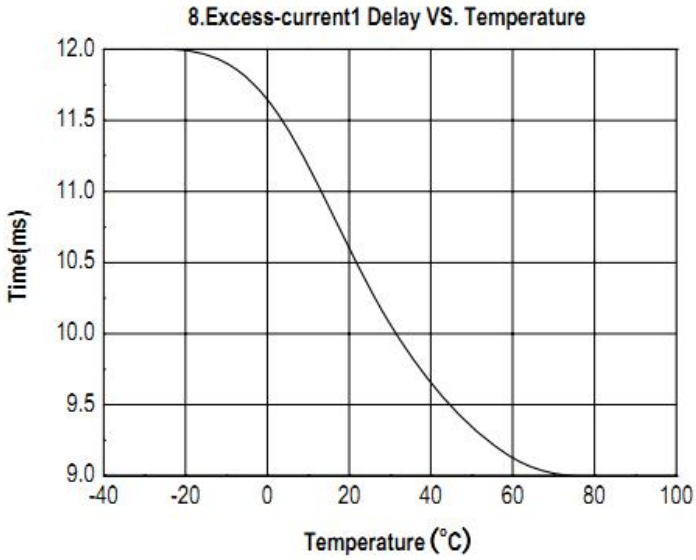
5.Over-discharge Release VS. Temperature



6.Over-discharge Delay VS. Temperature

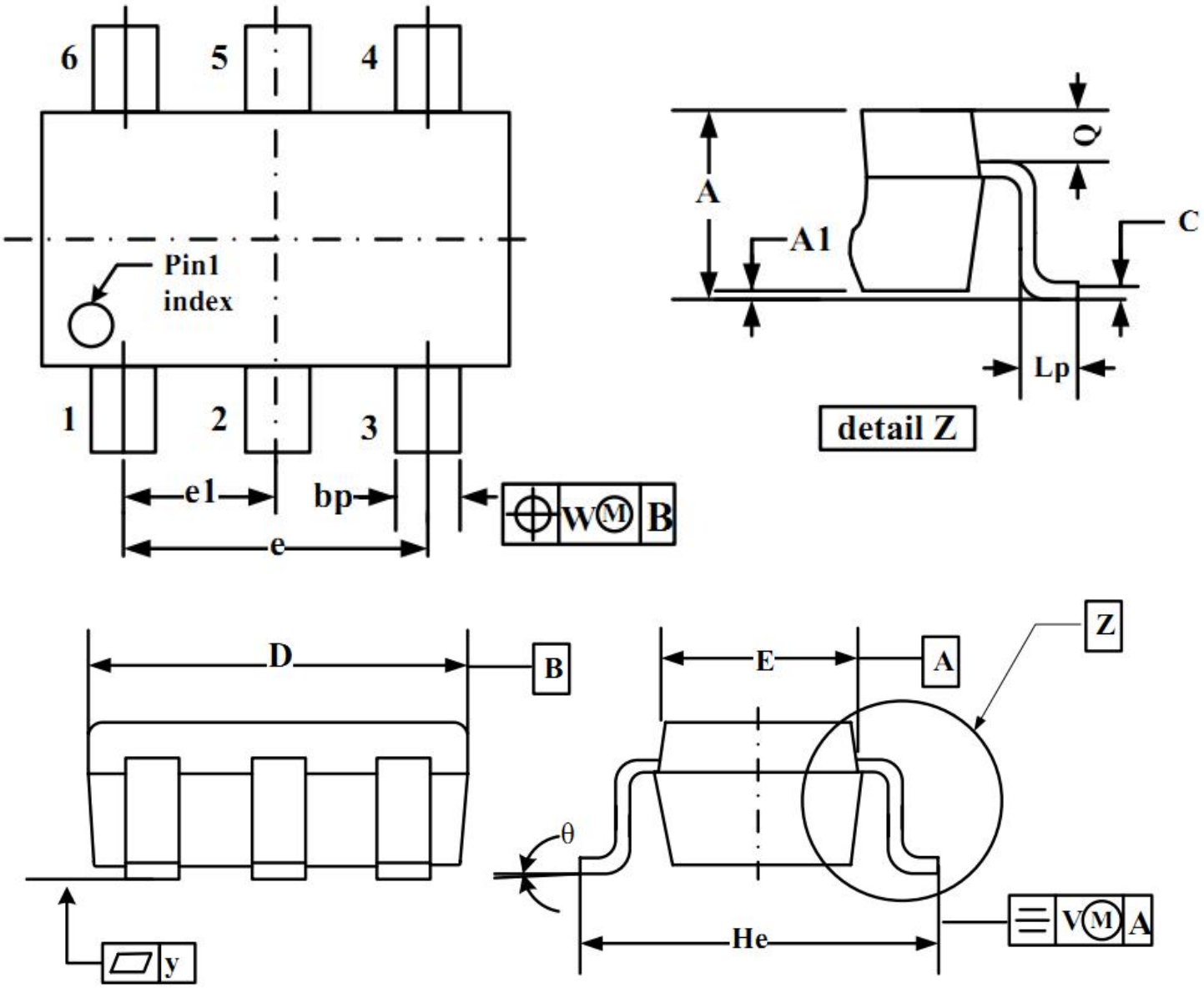



7.Excess-current1 Voltage VS. Temperature
Vex1(V)
0.158
0.157
0.156
0.155
0.154
0.153
0.152
0.151
-40
-20
0
20
40
60
80
100
Temperature (°C)


8.Excess-current1 Delay VS. Temperature
Time(ms)
12.0
11.5
11.0
10.5
10.0
9.5
9.0
-40
-20
0
20
40
60
80
100
Temperature (°C)

Package Outline

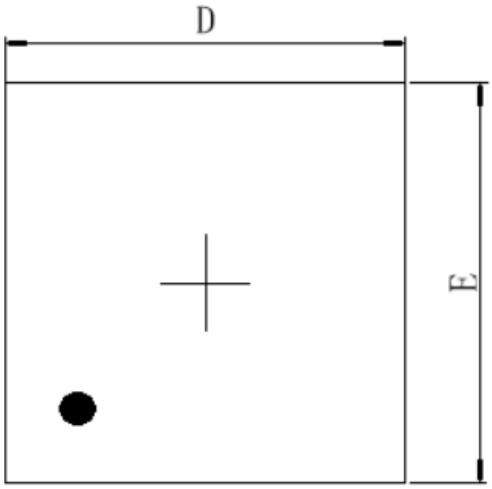
SOT-23-6L



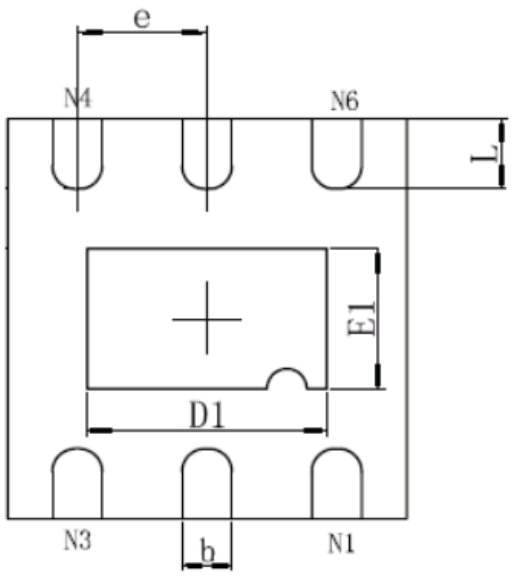
Dimensions (mm)

A	A1	bp	c	D	E	e	e1	He	Lp	Q	v	w	y	θ
1.3	0.15	0.50	0.20	3.1	1.7	1.9	0.95	3.0	0.6	0.33	0.2	0.2	0.1	0°
1.0	0.03	0.35	0.10	2.7	1.3			2.5	0.2	0.23				10°

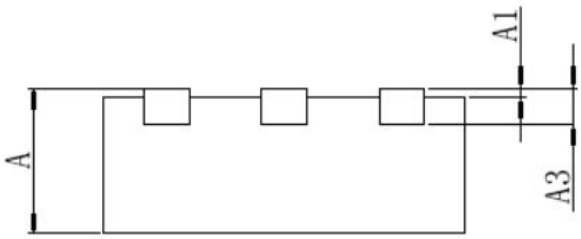
DFNWB2*2-6L



Top View



Bottom View



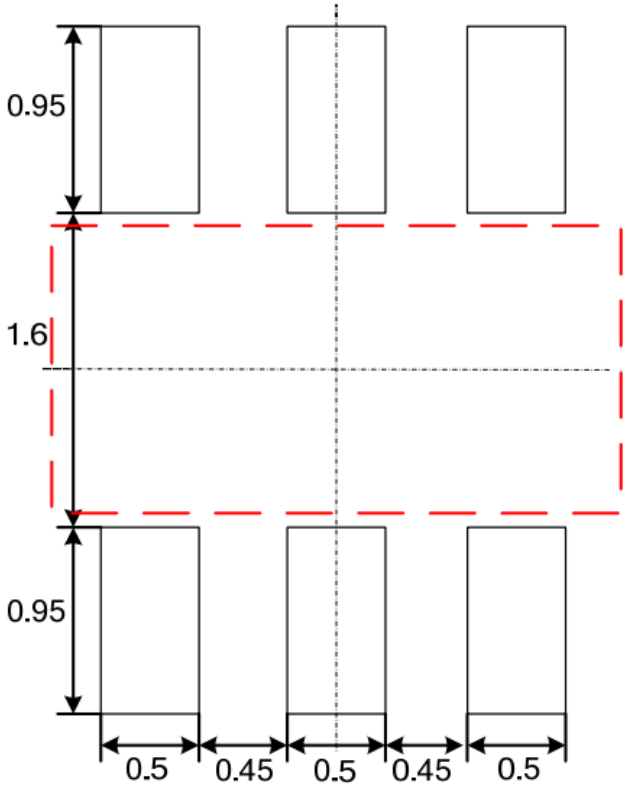
Side View

Dimensions (mm)

A	A1	A3	D	E	D1	E1	b	e	L
0.8	0	0.228	2.05	2.05	1.3	0.8	0.3	0.7	0.4
0.7	0.5	0.178	1.95	1.95	1.1	0.6	0.2	0.6	0.3

PCB Layout

SOT-23-6L



DFNWB2*2-6L