

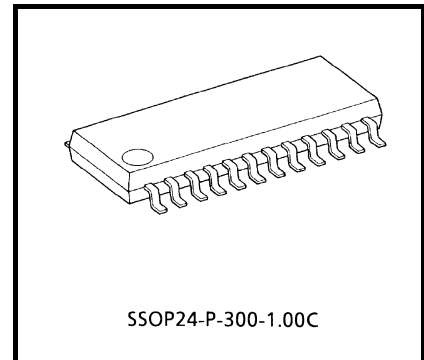
# TPD2005F

## High-Side Power Switch Array (8 Channels) for Motors, Solenoids, and Lamp Drivers

The TPD2005F is an 8-channel high-side switch array for vertical power MOSFET output. A monolithic power IC, it can directly drive a power load from a CMOS or TTL logic circuit (such as an MPU). It offers overcurrent and overtemperature protection functions.

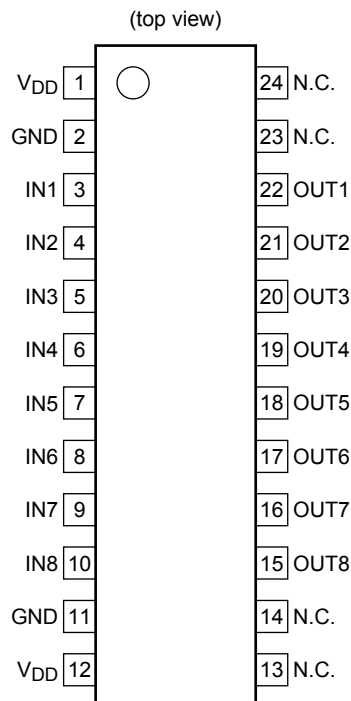
### Features

- A high-side switch array incorporating an N-channel power MOSFET (1.2 Ωmax.) and an 8-channel charge pump
- Can directly drive a power load from a microprocessor.
- Built-in protection against overtemperature protection and overcurrent protection
- 8-channel access enables space-saving design
- High operating supply voltage : 40 V
- Low on resistance : 1.2 Ω max. (@V<sub>DD</sub> = 12 V, I<sub>O</sub> = 0.5 A (per channel))
- Supports parallel operation.
- Low supply current : 5 mA max. (@V<sub>DD</sub> = 40 V, V<sub>IN</sub> = 0 V)
- Supplied in an SSOP-24 package (300 mil) in embossed taping.

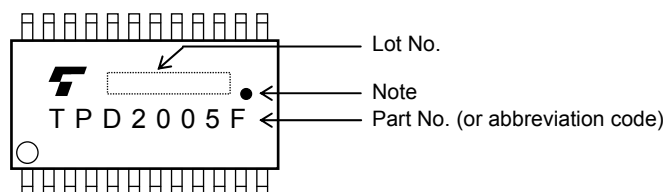


Weight: 0.29g (typ.)

### Pin Assignment



### Marking



Note : A dot marking for identifies the indication of product Labels.

Without a dot: [[Pb]]/INCLUDES > MCV

With a dot: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

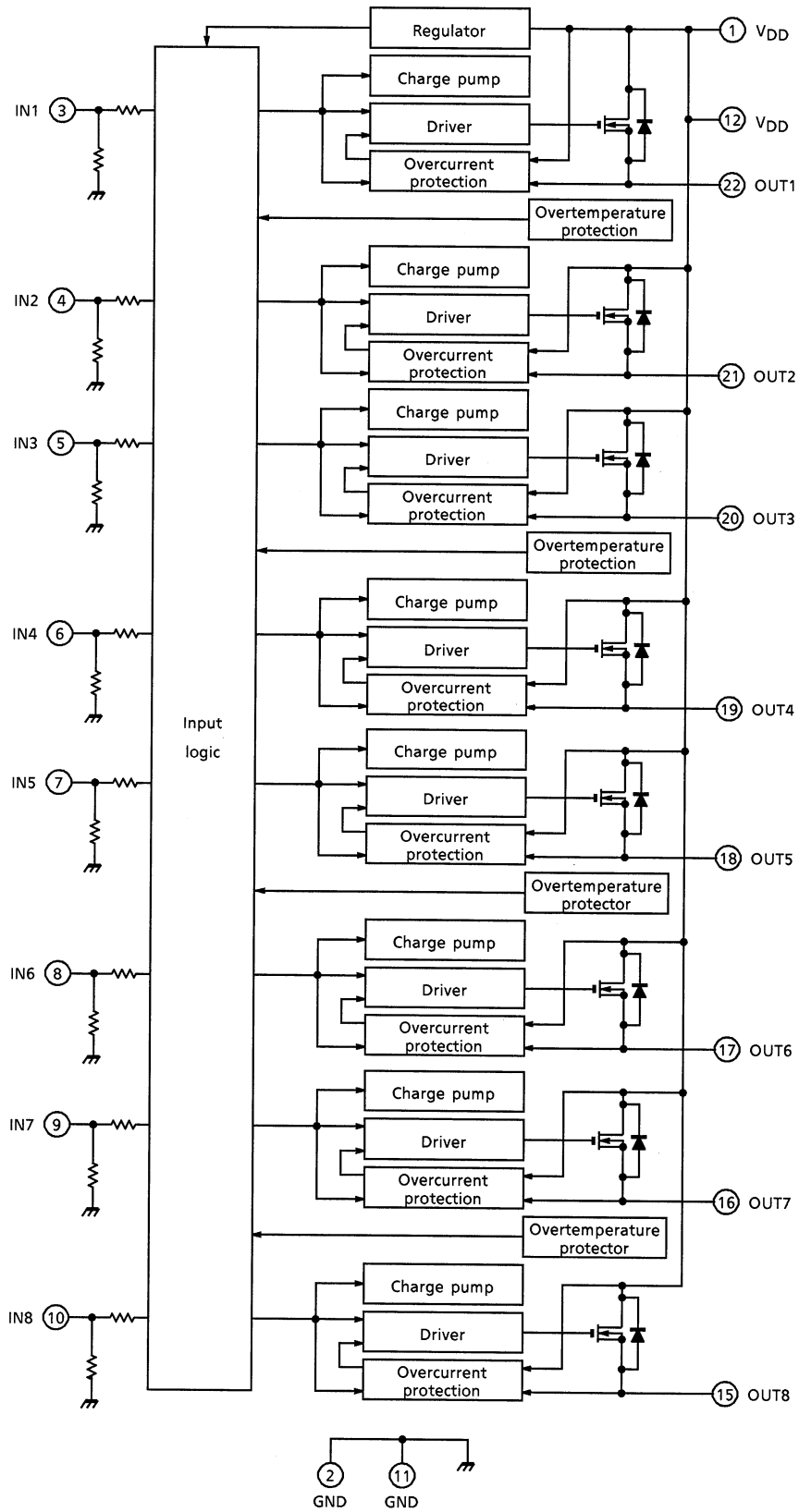
Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.

The RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Note: Due to its MOS structure, this product is sensitive to static electricity.

Start of commercial production  
1999-05

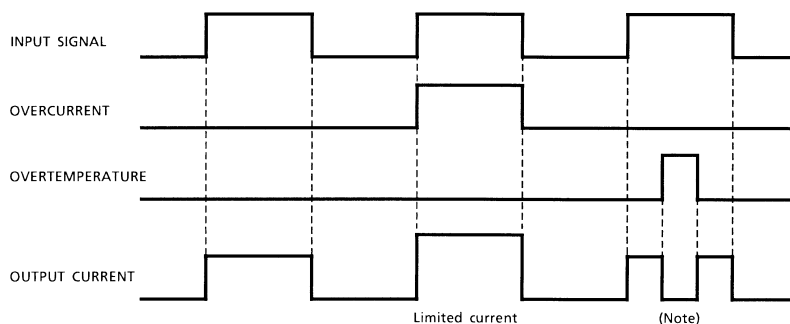
## Block Diagram



## Pin Description

| Pin No. | Symbol          | Description   |
|---------|-----------------|---|
| 1       | V <sub>DD</sub> | Power supply pin; in common with the pin No.12 internally.                    |
| 2       | GND             | GND pin; in common with the pin No.11 internally.                             |
| 3       | IN1             | Control input pin for channel 1 and built-in pull-down resistor (100 kΩ typ.) |
| 4       | IN2             | Control input pin for channel 2 and built-in pull-down resistor (100 kΩ typ.) |
| 5       | IN3             | Control input pin for channel 3 and built-in pull-down resistor (100 kΩ typ.) |
| 6       | IN4             | Control input pin for channel 4 and built-in pull-down resistor (100 kΩ typ.) |
| 7       | IN5             | Control input pin for channel 5 and built-in pull-down resistor (100 kΩ typ.) |
| 8       | IN6             | Control input pin for channel 6 and built-in pull-down resistor (100 kΩ typ.) |
| 9       | IN7             | Control input pin for channel 7 and built-in pull-down resistor (100 kΩ typ.) |
| 10      | IN8             | Control input pin for channel 8 and built-in pull-down resistor (100 kΩ typ.) |
| 11      | GND             | GND pin; in common with the pin No.2 internally.                              |
| 12      | V <sub>DD</sub> | Power supply pin; in common with the pin No.1 internally.                     |
| 13      | N.C.            | —   |
| 14      | N.C.            | —   |
| 15      | OUT8            | Output pin for channel 8  |
| 16      | OUT7            | Output pin for channel 7  |
| 17      | OUT6            | Output pin for channel 6  |
| 18      | OUT5            | Output pin for channel 5  |
| 19      | OUT4            | Output pin for channel 4  |
| 20      | OUT3            | Output pin for channel 3  |
| 21      | OUT2            | Output pin for channel 2  |
| 22      | OUT1            | Output pin for channel 1  |
| 23      | N.C.            | —   |
| 24      | N.C.            | —   |

## Timing Chart



Note: The overtemperature detector circuits feature hysteresis. After overtemperature is detected, normal operation is restored only when the junction temperature falls by the hysteresis amount (10°C typ.) in relation to the overtemperature detection temperature.

## Truth Table

| Input Signal | Output Signal      | State           |
|--------------|--------------------|-----------------|
| L            | L                  | Normal          |
| H            | H                  |                 |
| L            | L                  | Overcurrent     |
| H            | Internally limited |                 |
| L            | L                  | Overtemperature |
| H            | L                  |                 |

## Absolute Maximum Ratings (Ta = 25°C)

| Characteristic   | Symbol           | Rating             | Unit |
|--|------------------|--------------------|------|
| Supply voltage   | V <sub>DD</sub>  | 45                 | V    |
| Input voltage  | V <sub>IN</sub>  | - 0.5 to 7         | V    |
| Drain-source voltage                                     | V <sub>DS</sub>  | 60                 | V    |
| Output current   | I <sub>O</sub>   | Internally limited | A    |
| Power dissipation<br>(operating all channels, Ta = 25°C) | P <sub>T</sub>   | 0.8                | W    |
|  |                  | 1.2 (Note 1)       |      |
| Single pulse avalanche energy                            | E <sub>AS</sub>  | 10                 | mJ   |
| Operating temperature                                    | T <sub>opr</sub> | - 40 to 85         | °C   |
| Junction temperature                                     | T <sub>j</sub>   | 150                | °C   |
| Storage temperature                                      | T <sub>stg</sub> | - 55 to 150        | °C   |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Thermal Characteristics

| Characteristic  | Symbol                | Rating         | Unit   |
|---|-----------------------|----------------|--------|
| Thermal resistance junction to ambient<br>(Operating all channels, Ta = 25°C) | ΣR <sub>th(j-a)</sub> | 156.3          | °C / W |
|   |                       | 104.2 (Note 1) |        |

Note 1: 60 mm × 60 mm × 1.6 mm when a device is mounted on a glass epoxy PCB (DC).

## Electrical Characteristics

(Unless otherwise specified,  $V_{DD} = 8$  to  $40V$ ,  $T_j = 25^\circ C$ )

| Characteristic            | Symbol        | Test Circuit    | Test Condition                   | Min | Typ. | Max | Unit       |
|---------------------------|---------------|-----------------|----------------------------------|-----|------|-----|------------|
| Operating supply voltage  | $V_{DD(opr)}$ | —               | —                                | 8   | —    | 40  | V          |
| Supply current            | $I_{DD}$      | —               | $V_{DD} = 40 V, V_{IN} = 0 V$    | —   | —    | 5   | mA         |
| Input voltage             | "L" level     | $V_{IL}$        | —                                | —   | —    | 1.5 | V          |
|                           | "H" level     | $V_{IH}$        | —                                | 3.5 | —    | —   |            |
| Input current             | $I_{IL}$      | —               | $V_{DD} = 24 V, V_{IN} = 0 V$    | -10 | —    | 10  | $\mu A$    |
|                           | $I_{IH}$      | —               | $V_{DD} = 24 V, V_{IN} = 5 V$    | —   | 50   | 200 |            |
| On resistance             | $R_{DS(ON)}$  | —               | $V_{DD} = 12 V, I_O = 0.5 A$     | —   | 0.9  | 1.2 | $\Omega$   |
| Output leakage current    | $I_{OL}$      | —               | $V_{DD} = 40 V, V_{IN} = 0 V$    | —   | —    | 100 | $\mu A$    |
| Overcurrent protection    | $I_S$         | —               | —                                | 1   | —    | 3   | A          |
| Overtemperature detection | Temperature   | $T_{SD}$        | —                                | —   | 160  | —   | $^\circ C$ |
|                           | Hysteresis    | $\Delta T_{SD}$ | —                                | —   | 10   | —   |            |
| Switching time            | $t_{ON}$      | 1               | $V_{DD} = 12 V, R_L = 24 \Omega$ | —   | 11   | 200 | $\mu s$    |
|                           | $t_{OFF}$     |                 |                                  | —   | 4    | 50  |            |

## Description of Protector Circuit

### (1) Overtemperature Protection

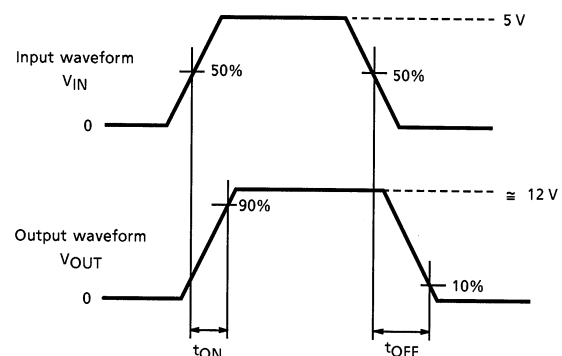
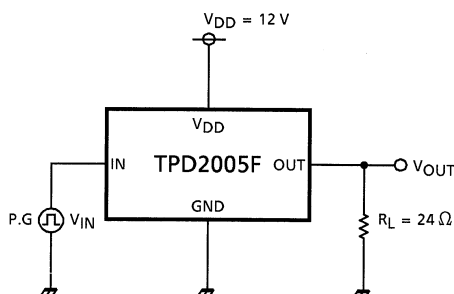
- There are four built-in overtemperature detector circuits, one each for channels 1 and 2; channels 3 and 4; channels 5 and 6; and channels 7 and 8, respectively. The circuit logic is such that, when any of the four detectors detects overtemperature, the circuit turns off the output of both its channels (for example, both channels 1 and 2).
- The overtemperature detector circuits feature hysteresis. After overtemperature is detected, normal operation is restored only when the junction temperature falls by the hysteresis amount ( $10^\circ C$  typ.) in relation to the overtemperature detection temperature.

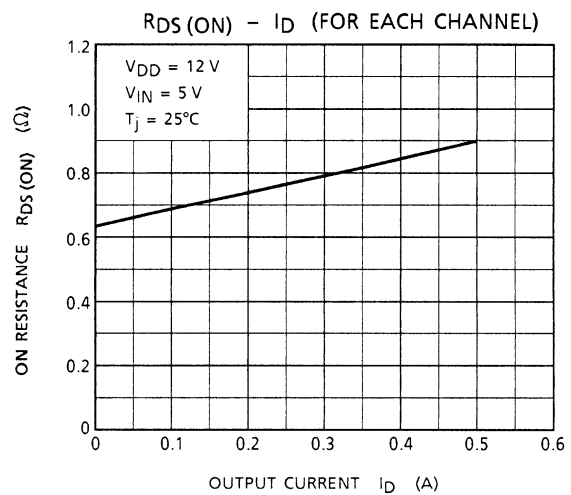
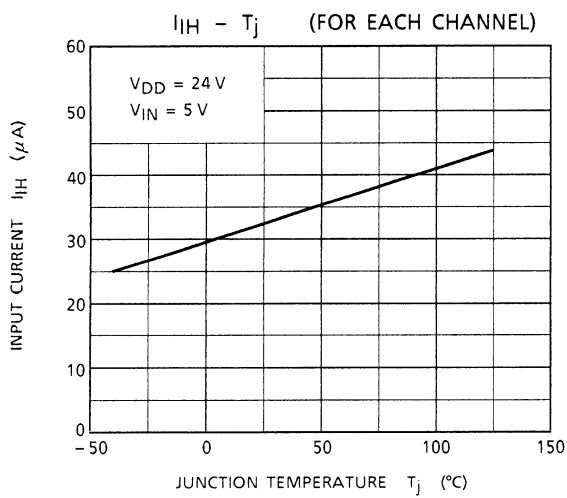
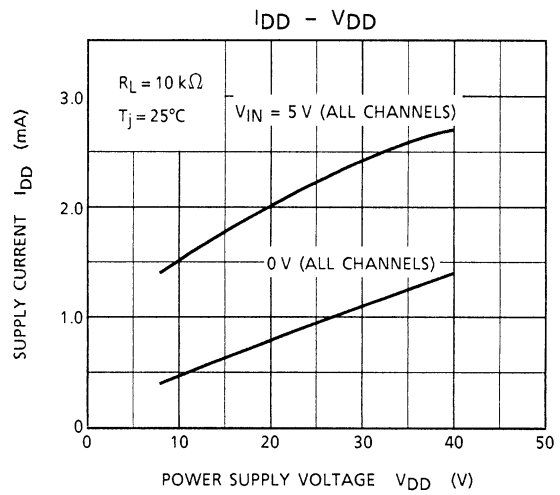
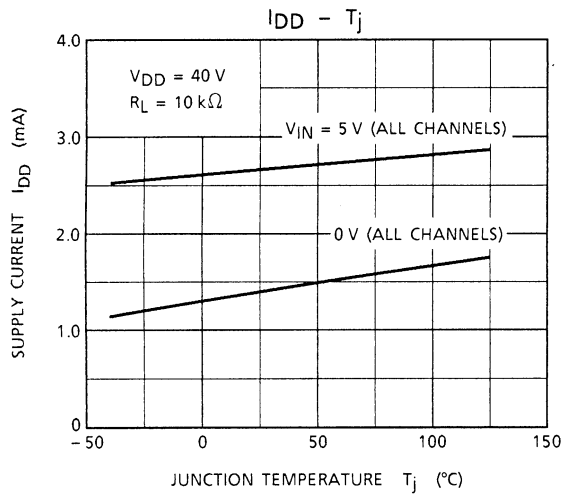
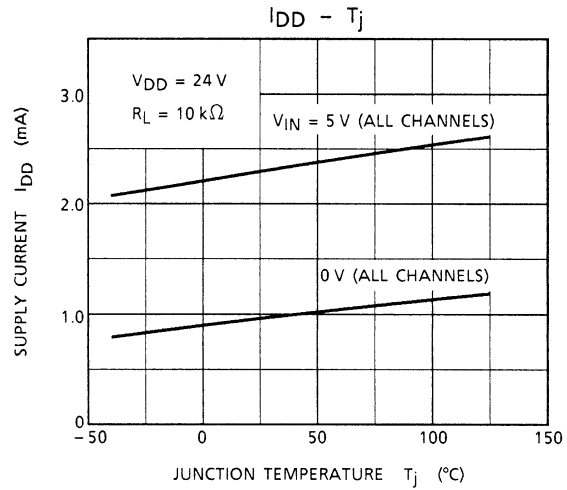
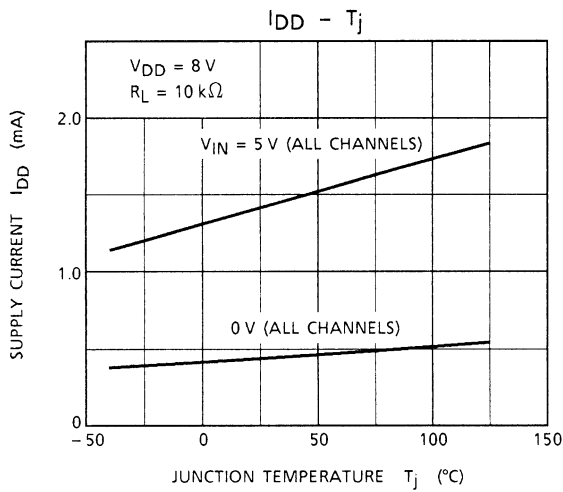
### (2) Overcurrent Protection

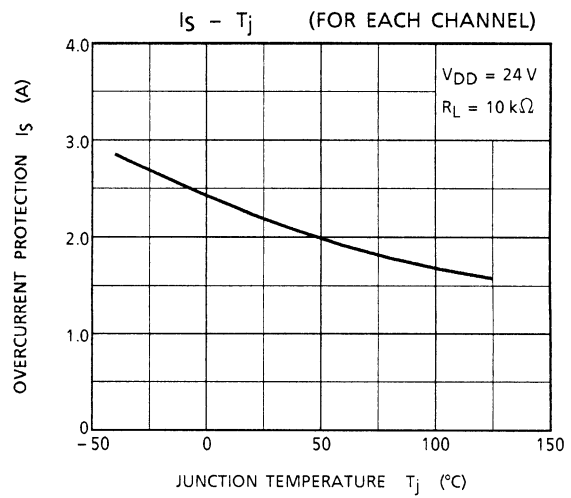
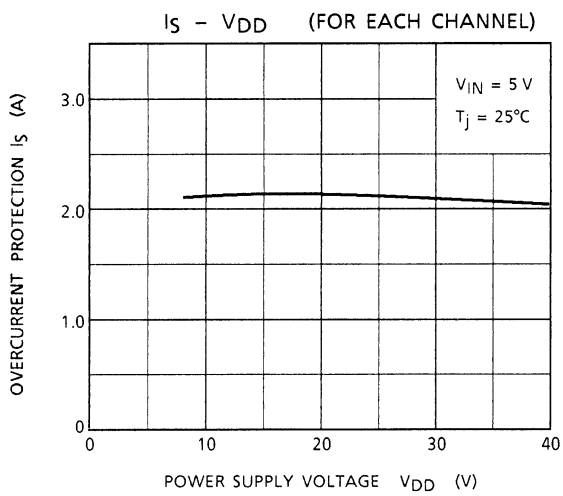
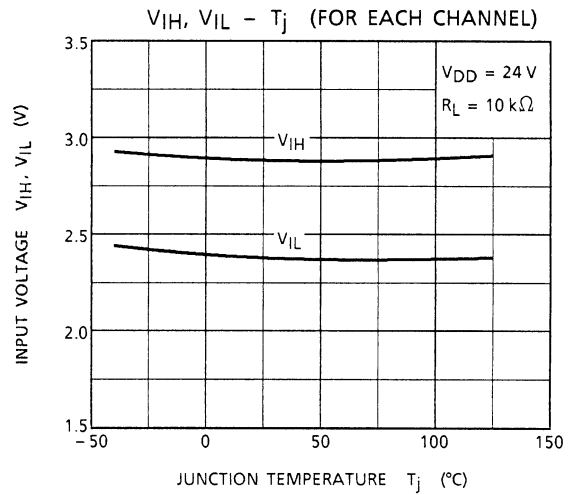
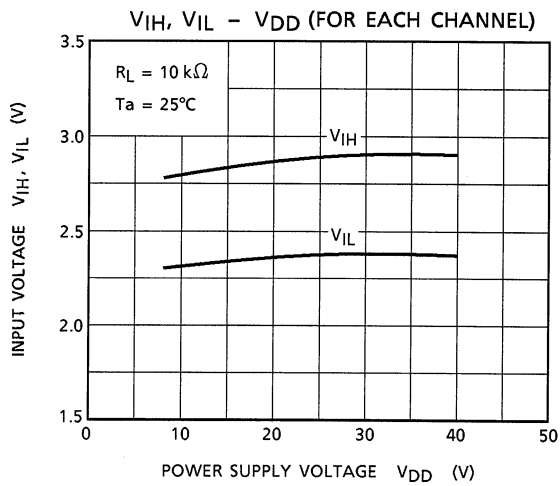
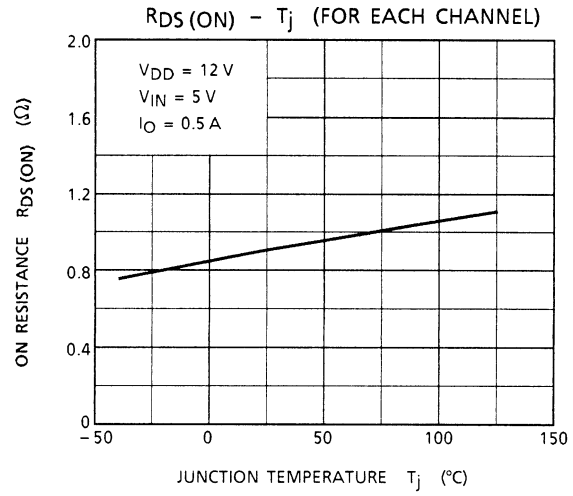
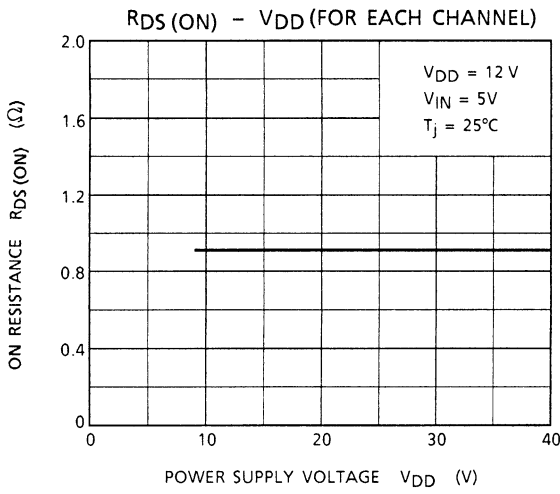
- When overcurrent is detected, the overcurrent limiter function limits the output current. Normal operation is restored when the load current drops below the overcurrent detection value.

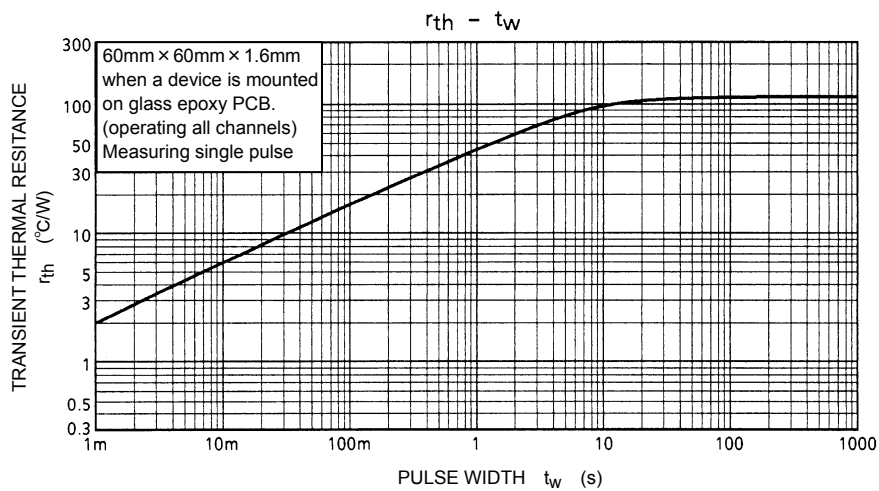
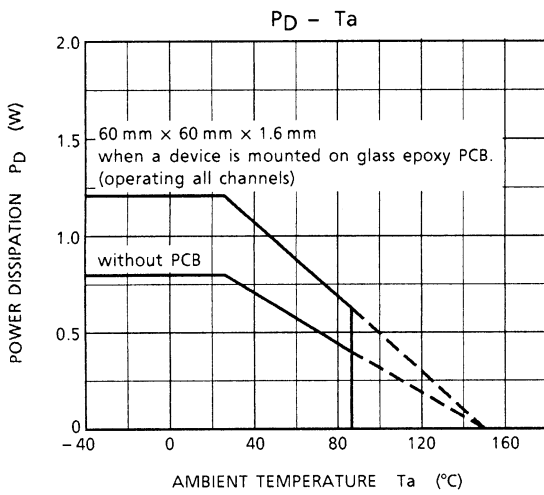
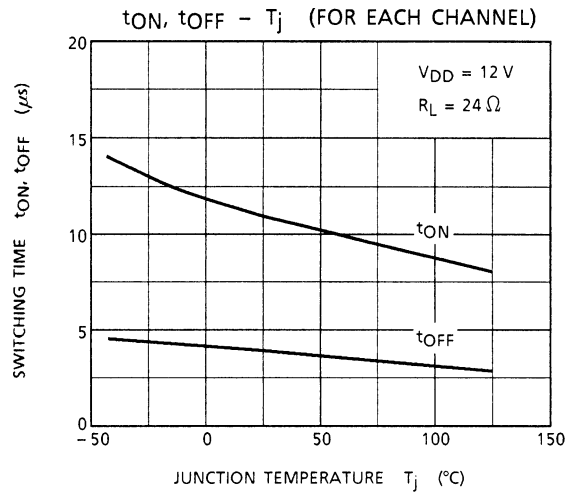
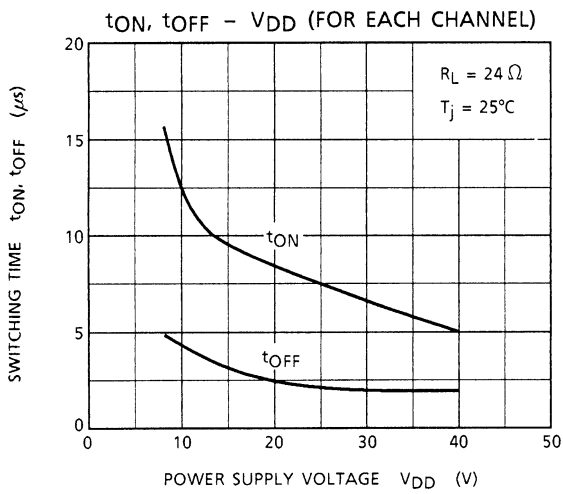
## Test Circuit

### Switching Time











**Caution on Usage**

1. As protection against reverse connection of batteries is not provided, take protective measures using external circuits.
2. As a negative bias protector circuit is not built into the output pins, if negative bias is applied to the output pins, be sure to connect a freewheel diode between OUT and GND.

**Moisture-Proof Packing**

After the pack is opened, use the devices in a 30°C, 60% RH environment, and within 48 hours.

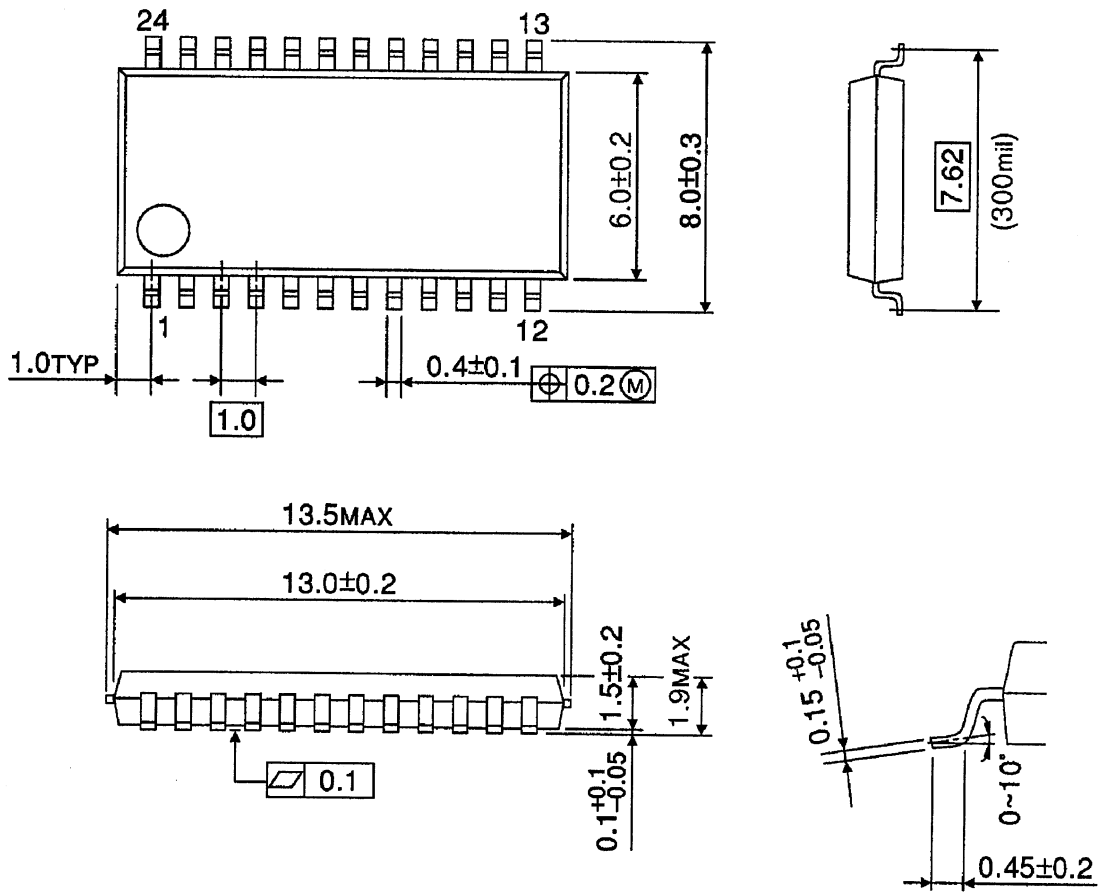
Embossed-tape packing cannot be baked. Devices so packed must be within their allowable time limits after unpacking, as specified on the packing.

Standard tape packing quantity: 2000 devices / reel (EL1)

**Package Dimensions**

SSOP24-P-300-1.00C

Unit: mm



Weight: 0.29g (typ.)

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