# High Efficiency 2.7A Synchronous Boost Convertor

General Description

The LP6252 is a Synchronous current mode boost DC-DC converter. Its PWM circuitry with built-in 2.7A Current power MOSFET makes this converter highly power efficiently. Selectable high switching frequency allows faster loop response and easy filtering with a low noise output. The non-inverting input its error amplifier is connected to an internal 800mV precision reference voltage. Current mode control and compensation network make it easy and flexible to stabilize the system.

Features

◆ Up to 95% efficiency

◆ Output to Input Disconnect at Shutdown Mode

◆ Shut-down current:<1uA

◆ Output voltage Up to 5.5V

◆ Over Output Voltage Protection

◆ Over Current Protection

◆ Over Temperature Protection

◆ Internal Compensation of Soft-start

◆ 1MHz fixed frequency switching

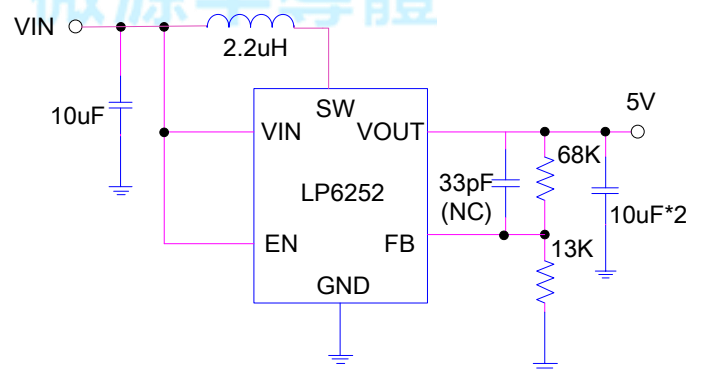◆ High switch on current:2.7A

◆ Available in SOT23-6 and TDFN-6 Package

Order Information

LP6252 ☐ ☐ ☐

└─ F: Halogen Free and Pb Free

└─ Package Type
B6: SOT23-6
QV:TDFN-6
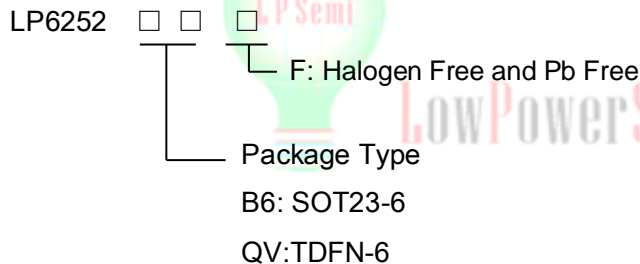
Applications

✧ Battery products

✧ Host Products

✧ Panel

Typical Application Circuit

Marking Information

| Device	Marking	Package	Shipping
LP6252B6F	LPS 5VYWX	SOT23-6	3K/REEL
LP6252QVF	LPS 5TYW	TDFN-6	4K/REEL
Marking indication: Y:Production year W:Production period X:Production batch			

Functional Pin Description

Package Type	Pin Configurations
TDFN-6 / SOT23-6	TDFN-6 SOT23-6

Pin		Name	Description
TDFN-6	SOT23-6		
1	6	FB	Regulation Feedback Input. Connect to an external resistive voltage divider from the output to FB to set the output voltage. The pin is 0.8V.
2	5	GND	Ground Pin.
3	4	SW	Pin for switching.
4	3	VIN	Voltage supply input pin.
5	2	OUT	Voltage output Pin.
6	1	EN	Chip enable pin. LP6252 will turn on when V_{EN}=high, and turn off when V_{EN}=0.

Function Diagram
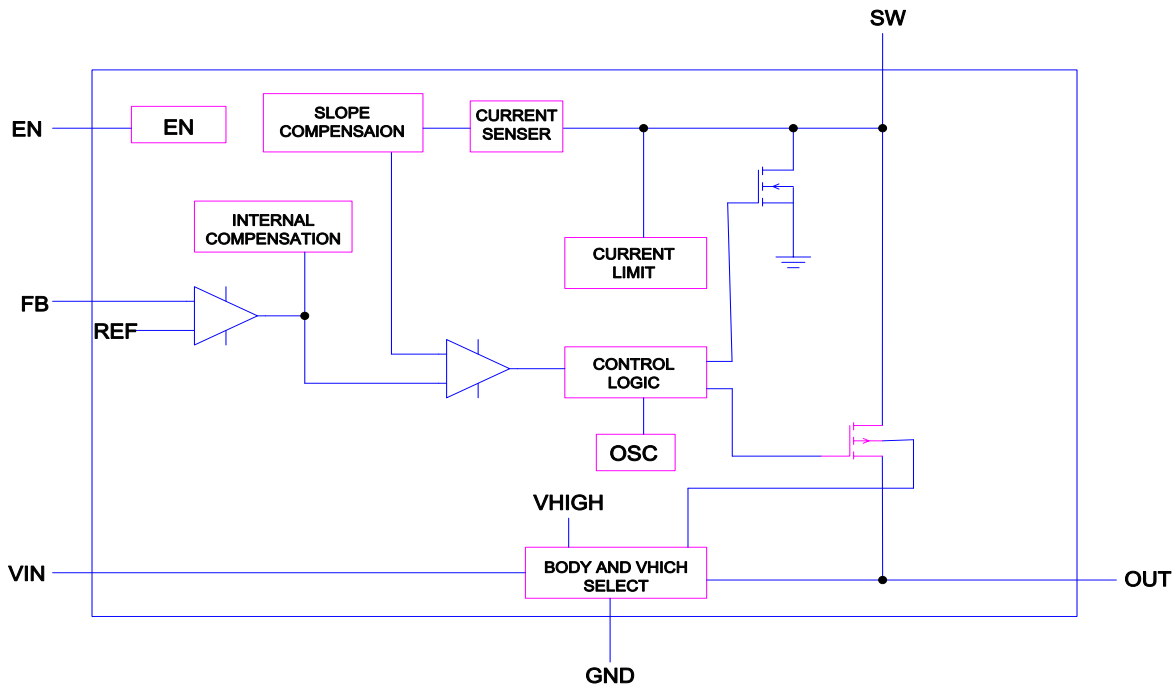
Absolute Maximum Ratings [Note 1]

✧ Input and VOUT to GND --- 6V
✧ Other Pin to GND (FB,EN,SW) -- 6V
✧ Maximum Junction Temperature -- 150°C
✧ Operating Ambient Temperature Range (T_A) --- -40°C to 85°C
✧ Maximum Soldering Temperature (at leads, 10 sec) -- 260°C

Note 1.   Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

✧ Maximum Power Dissipation (SOT23-6, PD,T_A=25°C) -- 0.45W
✧ Thermal Resistance (SOT23-6, J_A) --- 250°C/W
✧ Maximum Power Dissipation (TDFN-6, PD,T_A=25°C) -- 1.2W
✧ Thermal Resistance (TDFN-6, J_A) -- 95°C/W

ESD Susceptibility

✧ HBM(Human Body Mode) -- 2KV
✧ MM(Machine Mode) --- 200V

Electrical Characteristics

(V_{IN}=3.5V, V_{OUT}=5V, C_{IN}=10uF, C_{OUT}=22uF, L=2.2uH, R_1=68K, R_2=13K)

| Parameter	Condition	Min	Typ	Max	Units
Supply Voltage		2.5		5.5	V
Output Voltage Range		2.5		5.4	V
UVLO		1.8		2.4	V
Supply Current(Shutdown)	V_{EN}=0V,V_{IN}=5V		0.05	1	uA
Feedback Voltage		784	800	816	mV
Feedback Input Current	V_{FB}=0.82V		50		nA
Switching Frequency			1000		KHz
Maximum Duty Cycle		80	90	95	%
EN Input Low Voltage				0.4	V
EN Input High Voltage		1.4			V
Low-side Current Limit		2.7	3		A
High-side On Resistance	V_{OUT}=3.3V		200		mΩ
Low-side On Resistance			150		mΩ

Typical Operating Characteristics
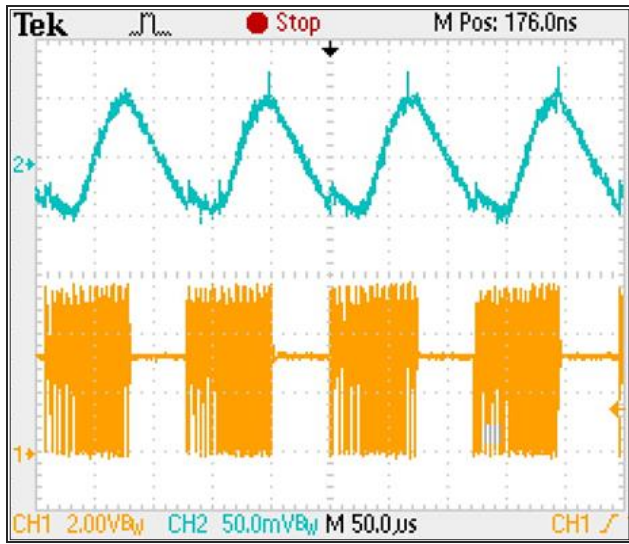
V_{OUT}=5V, V_{IN}=3V, I_{OUT}=2mA, CH$_1$=V$_{SW}$,CH$_2$=△V$_{OUT}$
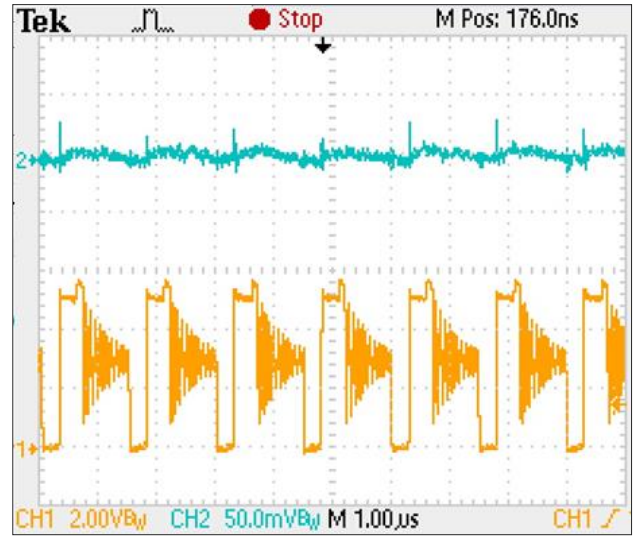
V_{OUT}=5V, V_{IN}=3V, I_{OUT}=100mA, CH$_1$=V$_{SW}$,CH$_2$=△V$_{OUT}$
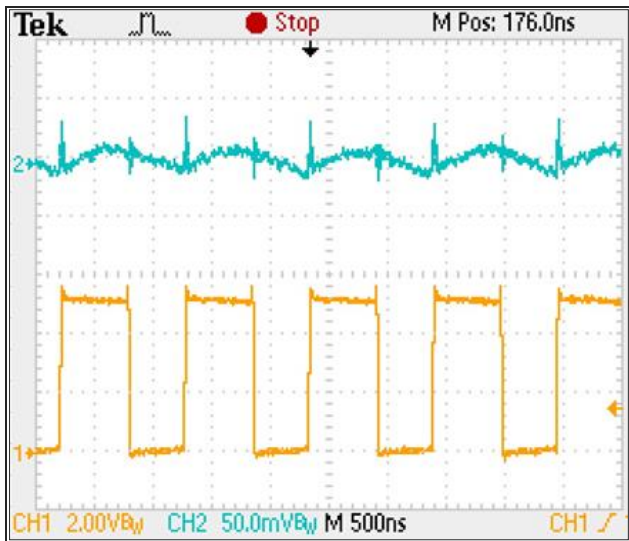
V_{OUT}=5V, V_{IN}=3V, I_{OUT}=500mA, CH$_1$=V$_{SW}$,CH$_2$=△V$_{OUT}$
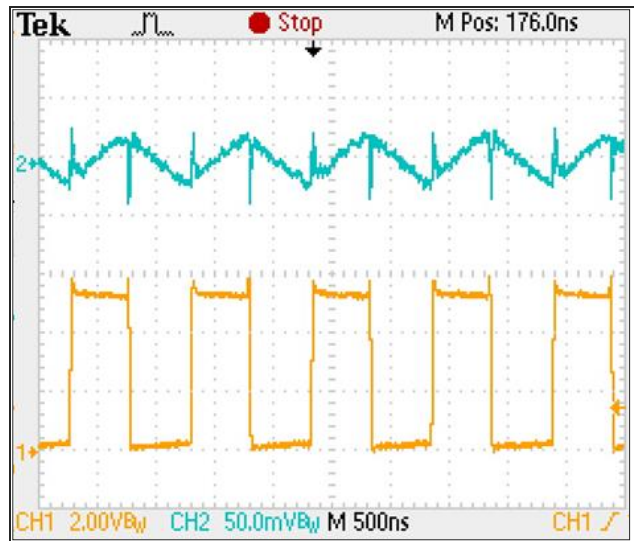
V_{OUT}=5V, V_{IN}=3V, I_{OUT}=1A, CH$_1$=V$_{SW}$,CH$_2$=△V$_{OUT}$

Efficiency VS. Iout
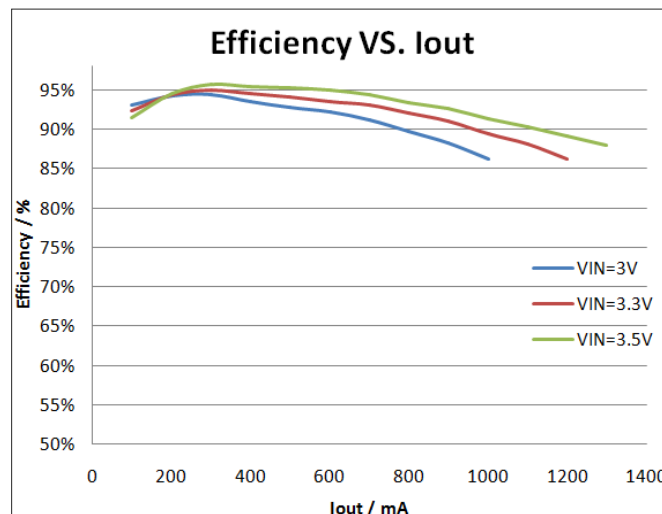
Operation Information

The LP6252 uses a synchronous 1MHz fixed frequency, current-mode regulation architecture to regulate the output voltage. The LP6252 measures the output voltage through an external resistive voltage divider and compares that to the internal 0.8V reference to generate the error voltage to the inductor current to regulate the output voltage. The use of current-mode regulation improves transient response and control loop stability.

When the LP6252 is disable (EN=Low), both power switches are off. There is no current path from SW to OUT. Therefore, the output voltage discharges to ground. When the LP6252 is enabled(EN=High),a limited start-current charges the output voltage rising to SW, then the part operates in force PWM mode for regulating the output voltage to the target value. At the beginning of each cycle, the N-channel MOSFET switch is turned on, forcing the inductor current to rise, The current at the source of the switch is internally measured and converted to a voltage by the current sense amplifier. That voltage is compared to the error voltage. When the inductor current rises sufficiently, the PWM comparator turns off the switch, forcing the inductor current to the output capacitor through the internal P-Channel MOSFET rectifier, which forces the inductor current to decrease. The peak inductor current is controlled by the error voltage. Thus the output voltage controls the inductor current to satisfy the lode.

Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the 0.8V feedback voltage. Use a 100K resistor for R_2 of the voltage divider. Determine the high-side resistor R_1 by the equation:

$$V_{OUT} = (R_1 / R_2 + 1) \times V_{FB}$$

Pre-Boost Current and Short Circuit Protect

Initially output voltage is lower than battery voltage, and the LP6252 enters pre-boost phase. During pre-boost phase, the internal NMOSFET/PMOSFET is turned off/on and a constant current is provided from battery to output until the output voltage close to the battery voltage. The constant current is limited by internal controller. If the output short to ground, the LP6252 also limits the output current to avoid damage condition

Output Capacitor Selection

For lower output voltage ripple, low-ESR ceramic capacitors are recommended. The tantalum capacitors can be used as well, but the ESR is bigger than ceramic capacitor. The output voltage ripple consists of two components: one is the pulsating output ripple current flows through the ESR, and the other is the capacitive ripple caused by charging and discharging.

$$V_{RIPPLE} = V_{RIPPLE\_ESR} + V_{RIPPLE\_C}$$
$$\cong I_{PEAK} \times R_{ESR} + \frac{I_{PEAK}}{C_{OUT}} \left(\frac{V_{OUT} - V_{IN}}{V_{OUT} \times f_{OSC}} \right)$$

Inductor Selection

For a better efficiency in high switching frequency converter, the inductor selection has to use a proper core material such as ferrite core to reduce the core loss and choose low ESR wire to reduce copper loss. The most important point is to prevent the core saturated when handling the maximum peak current. Using a shielded inductor can minimize radiated noise in sensitive applications. The maximum peak inductor current is the maximum input current plus the half of inductor ripple current. The calculated peak current has to be smaller than the current limitation in the electrical characteristics. A typical setting of the inductor ripple current is 20% to 40% of the maximum input current. If the selection is 40%, the maximum peak inductor current is

$$I_{PEAK} = I_{IN(MAX)} + \frac{1}{2}I_{RIPPLE} = 1.2 \times I_{IN(MAX)}$$
$$= 1.2 \times \left[\frac{I_{OUT(MAX)} \times V_{OUT}}{\eta \times V_{IN(MIN)}}\right]$$

The minimum inductance value is derived from the following equation :

$$L = \frac{\eta \times V_{IN(MIN)}^2 \times \left[V_{OUT} - V_{IN(MIN)}\right]}{0.4 \times I_{OUT(MAX)} \times V_{OUT}^2 \times f_{OSC}}$$

Depending on the application, the recommended inductor value is between 1μH to 4.7μH.

Input Capacitor Selection

For better input bypassing, low-ESR ceramic capacitors are recommended for performance. A 10μF input capacitor is sufficient for most applications. For a lower output power requirement application, this value can be decreased.

Layout Guide

For high frequency switching power supplies, the PCB layout is important step in system application design. In order to let IC achieve good regulation, high efficiency and stability, it is strongly recommended the power components(Inductor, input and output capacitor) should be placed as close as possible to chip. The set races should be wide and short. The feedback pin and then works of feedback and compensation should keep away from the power loops, and be shielded with a ground trace or plane to prevent noise coupling.
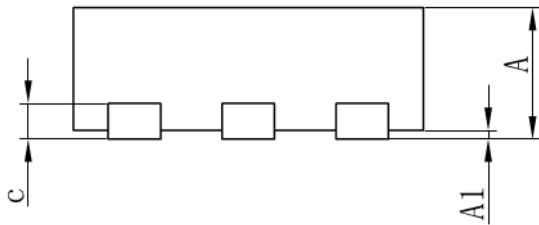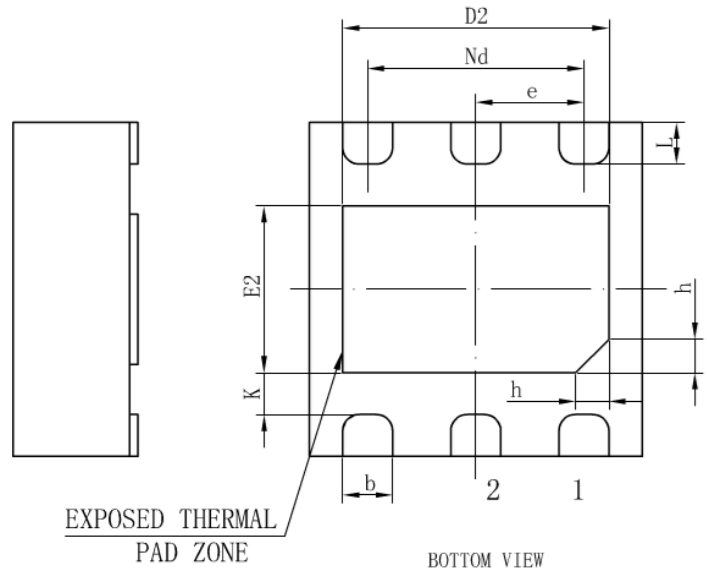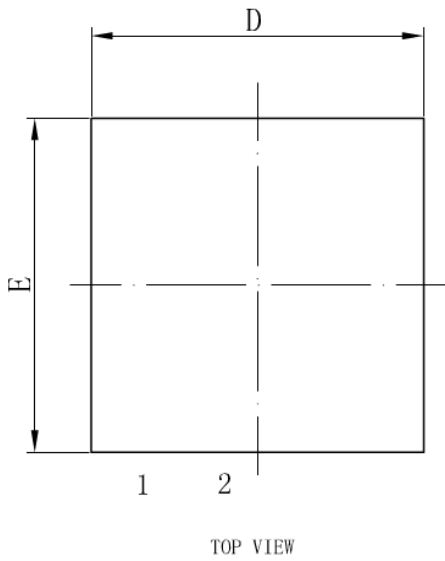
Packaging Information

SOT23-6
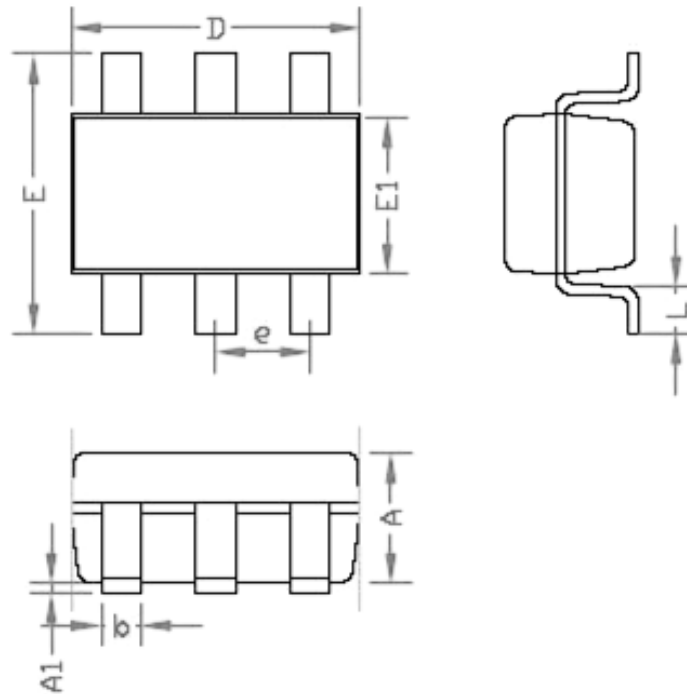
SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.45	-	0.057
A1	0.00	0.15	0.000	0.006
b	0.30	0.50	0.012	0.020
D	2.90		0.114	
E1	1.60		0.063	
e	0.95		0.037	
E	2.60	3.00	0.102	0.118
L	0.3	0.60	0.012	0.024

TDFN-6

TOP VIEW

BOTTOM VIEW

EXPOSED THERMAL PAD ZONE

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.25	0.30	0.35
c	0.18	0.20	0.25
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
e	0.65BSC		
Nd	1.30BSC		
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
K	0.20	–	–
L	0.20	0.25	0.30
h	0.15	0.20	0.25
L/F载体尺寸 (MIL)	69X47		