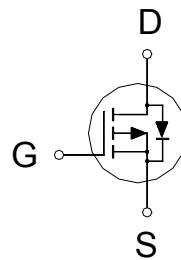


NIKO-SEM**P-Channel Logic Level Enhancement Mode
Field Effect Transistor****PK501BA
PDFN 5x6P
Halogen-Free & Lead-Free****PRODUCT SUMMARY**

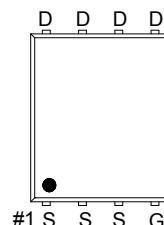
$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	7mΩ	-43A

**Features**

- Pb-Free, Halogen Free and RoHS compliant.
- Low $R_{DS(on)}$ to Minimize Conduction Losses.
- Ohmic Region Good $R_{DS(on)}$ Ratio.
- Optimized Gate Charge to Minimize Switching Losses.
- ESD Protected up to 2KV.

Applications

- Protection Circuits Applications.
- Logic/Load Switch Circuits Applications.



G : GATE
D : DRAIN
S : SOURCE

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current	I_D	-43	A
		-27	
		-13	
		-10	
Pulsed Drain Current ¹	I_{DM}	-110	
Avalanche Current	I_{AS}	-38	
Avalanche Energy	E_{AS}	72	mJ
Power Dissipation	P_D	25	W
		10	
		2.2	
		1.4	
Operating Junction & Storage Temperature Range	T_j, T_{stg}	-55 to 150	°C

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THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$R_{\theta JA}$		56	
Junction-to-Case	$R_{\theta JC}$		5	°C / W

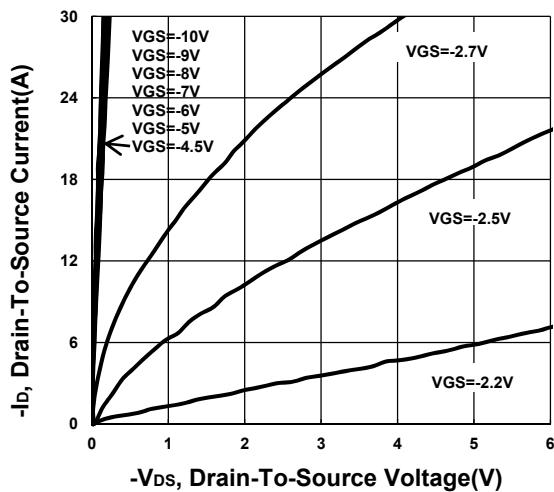
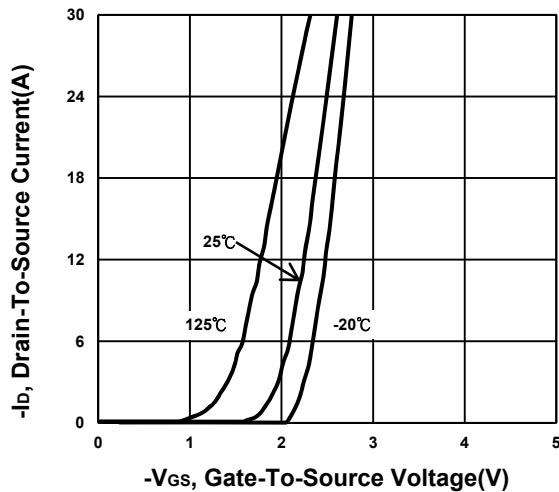
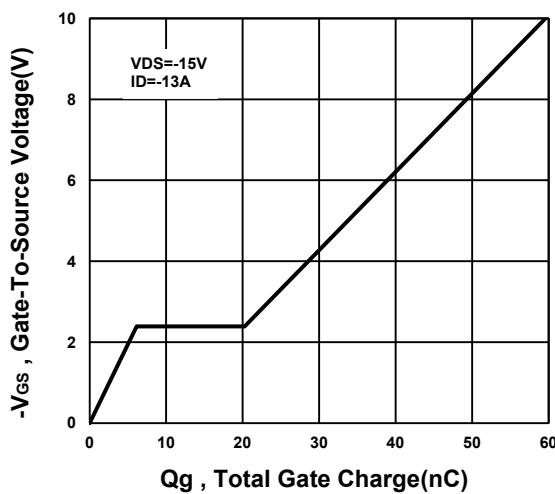
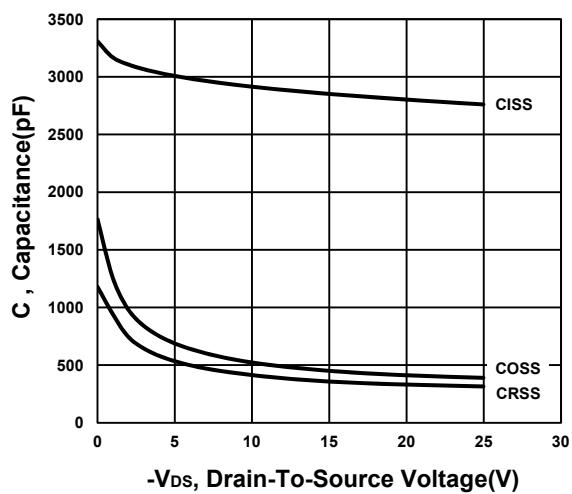
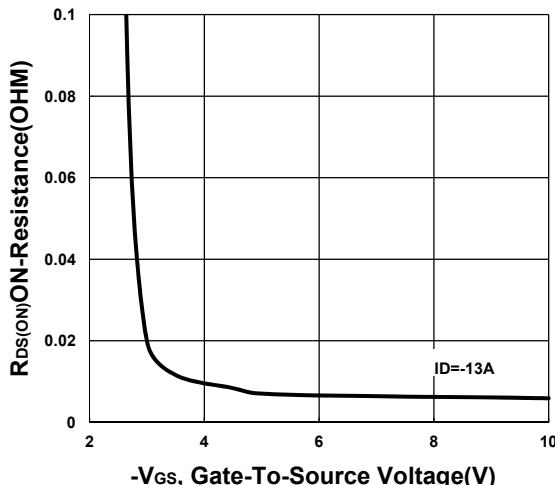
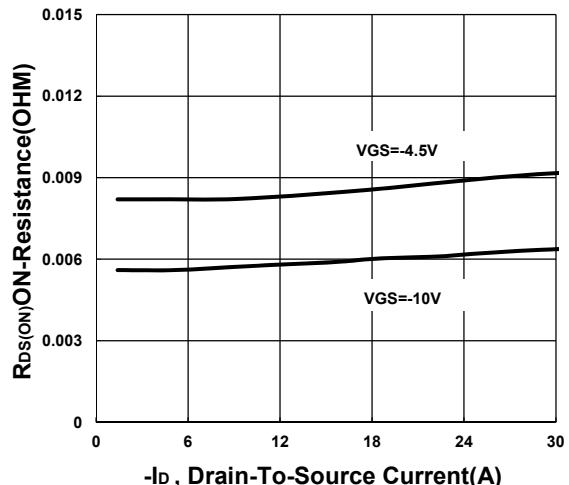
¹Pulse width limited by maximum junction temperature.²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$. The value in any given application depends on the user's specific board design.**ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ C$, Unless Otherwise Noted)**

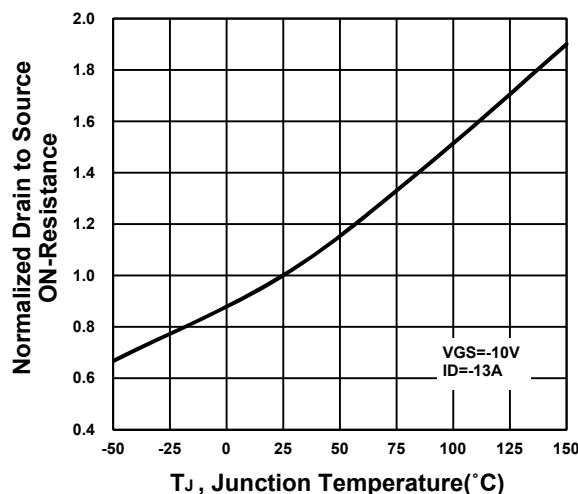
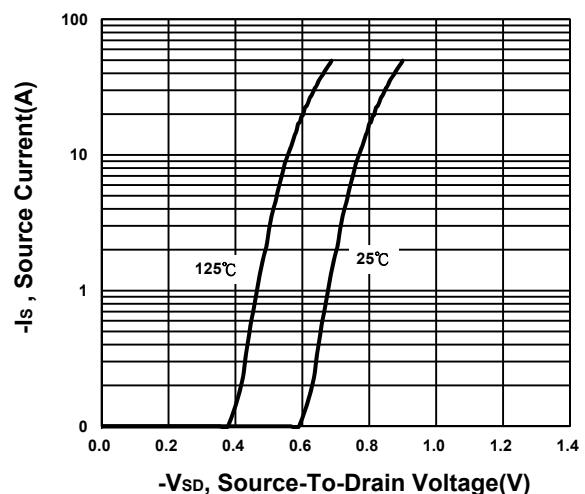
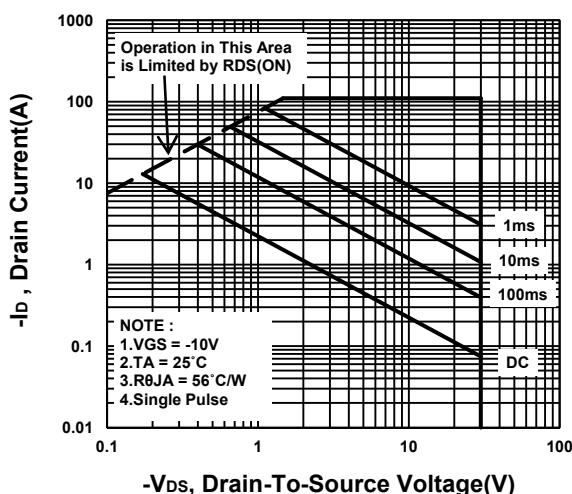
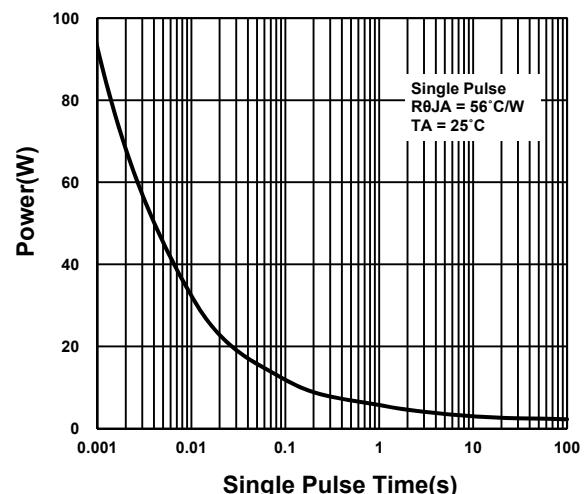
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.5	-3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 25V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			-1	
		$V_{DS} = -20V, V_{GS} = 0V, T_J = 125^\circ C$			-10	uA
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -4.5V, I_D = -13A$		8.4	12	
		$V_{GS} = -10V, I_D = -13A$		5.7	7	mΩ
Forward Transconductance ¹	g_f	$V_{DS} = -5V, I_D = -13A$		40		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$		2822		pF
Output Capacitance	C_{oss}			452		
Reverse Transfer Capacitance	C_{rss}			364		
Gate Resistance	R_g	$V_{GS} = 0V, V_{DS} = 0V, f = 1MHz$		4		Ω
Total Gate Charge ²	$Q_{g(VGS=-10V)}$	$V_{DS} = -15V, I_D = -13A$		60		nC
	$Q_{g(VGS=-4.5V)}$			30		
Gate-Source Charge ²	Q_{gs}			6.1		
Gate-Drain Charge ²	Q_{gd}			14		
Turn-On Delay Time ²	$t_{d(on)}$			39		
Rise Time ²	t_r			26		
Turn-Off Delay Time ²	$t_{d(off)}$	$I_D \approx -13A, V_{GS} = -10V, R_{GS} = 6\Omega$		161		nS
Fall Time ²	t_f			100		

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SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ\text{C}$)						
Continuous Current	I_S				-19	A
Forward Voltage ¹	V_{SD}	$I_F = -13\text{A}$, $V_{GS} = 0\text{V}$			-1.3	V
Reverse Recovery Time	t_{rr}	$I_F = -13\text{A}$, $dI_F/dt = 100 \text{ A} / \mu\text{s}$		23		nS
Reverse Recovery Charge	Q_{rr}			6		nC

¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.

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PDFN 5x6P
Halogen-Free & Lead-Free****Output Characteristics****Transfer Characteristics****Gate charge Characteristics****Capacitance Characteristic****On-Resistance VS Gate-To-Source****On-Resistance VS Drain Current**

NIKO-SEM**P-Channel Logic Level Enhancement Mode
Field Effect Transistor****PK501BA
PDFN 5x6P
Halogen-Free & Lead-Free****On-Resistance VS Temperature****Source-Drain Diode Forward Voltage****Safe Operating Area****Single Pulse Maximum Power Dissipation****Transient Thermal Response Curve**