General Description

The WSD2018DN22 is the highest performance trench N-Ch MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the small power switching and load switch applications.

The WSD2018DN22 meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

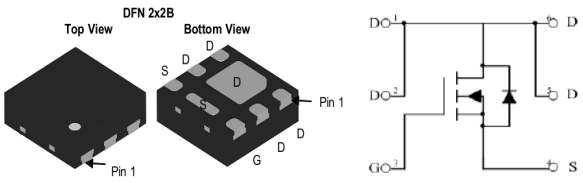
Product Summery

BVDSS	RDSON	ID
20V	15mΩ(MAX)	12A

Applications

- High Frequency Point-of-Load Synchronous s
  Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

DFNWB2×2-6L-J Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	±10	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 4.5V[1]	12	A
I_D@T_C=70℃	Continuous Drain Current, V_{GS} @ 4.5V[1]	10	A
I_{DM}	Pulsed Drain Current[2]	40	A
P_D@T_A=25℃	Total Power Dissipation[3]	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient [1]	---	167	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	65	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	20	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.027	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=4.5V , I_D=5A	---	10	15	mΩ
		V_{GS}=2.5V , I_D=5A	---	13	18	
		V_{GS}=1.8V , I_D=5A		18	30	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	0.4	0.7	1.0	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	2.56	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=16V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=16V , V_{GS}=0V , T_J=55℃	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±12V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=4V , I_D=9.7A	20	---	---	S
R_g	Gate Resistance	f=1MHz	---	2.5	---	Ω
Q_g	Total Gate Charge (4.5V)	V_{DS}=4V , V_{GS}=5V , I_D=10A	---	---	32	nC
Q_{gs}	Gate-Source Charge		---	2.5	---	
Q_{gd}	Gate-Drain Charge		---	6.5	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=4V , V_{GS}=4.5V , R_G=1Ω I_D=10A ,RL=0.4Ω	---	12	20	ns
T_r	Rise Time		---	10	25	
$T_{d(off)}$	Turn-Off Delay Time		---	65	70	
T_f	Fall Time		---	20	60	
C_{iss}	Input Capacitance	V_{DS}=4V , V_{GS}=0V , f=1MHz	---	1800	---	pF
C_{oss}	Output Capacitance		---	650	---	
C_{rss}	Reverse Transfer Capacitance		---	450	---	

Notes :

1.Surface mounted on FR4 board using 1 square inch pad size,1oz copper.

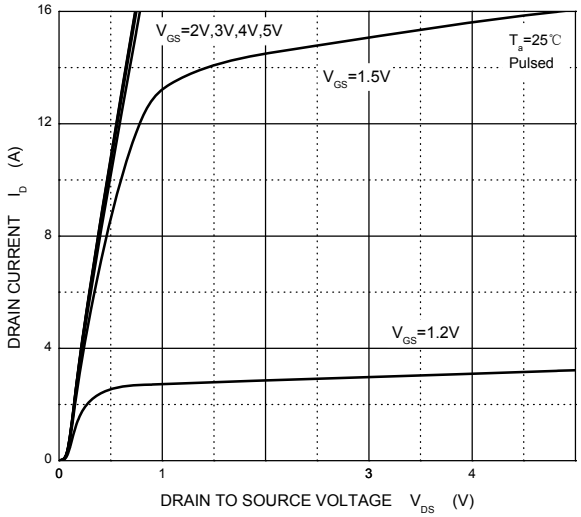
2.Surface mounted on FR4 board using the minimum pad size,1oz copper.

3. Pulse test : Pulse width=300μs, duty cycle≤2%.

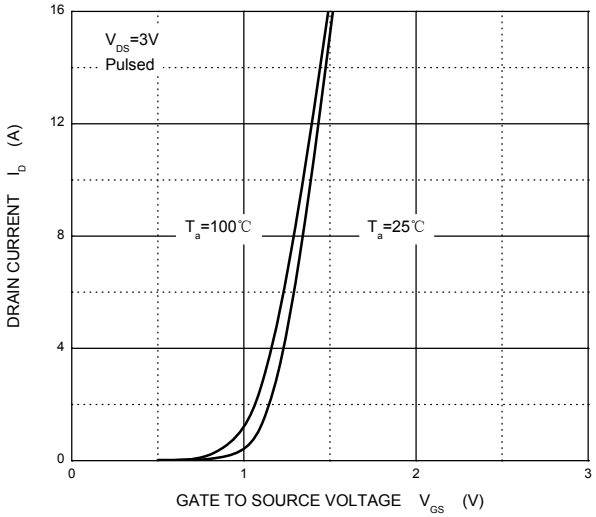
4. These parameters have no way to verify.

Typical Characteristics

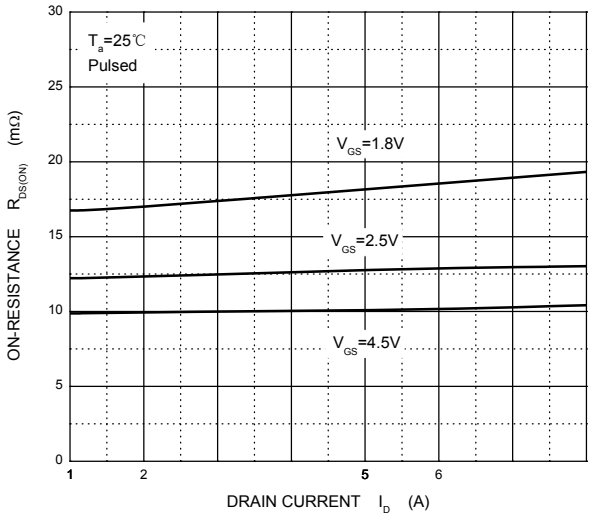
Output Characteristics



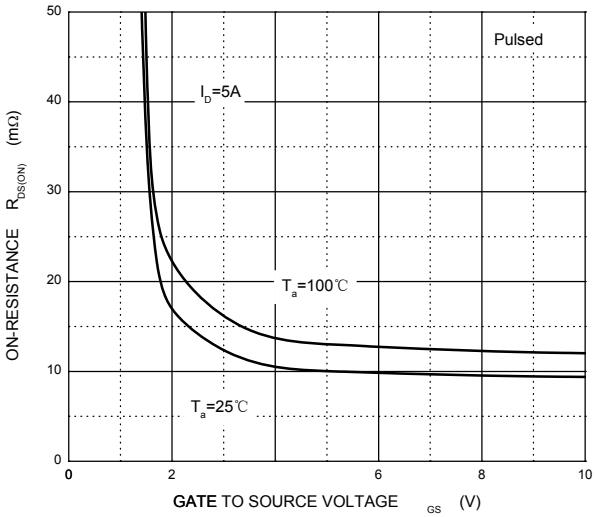
Transfer Characteristics



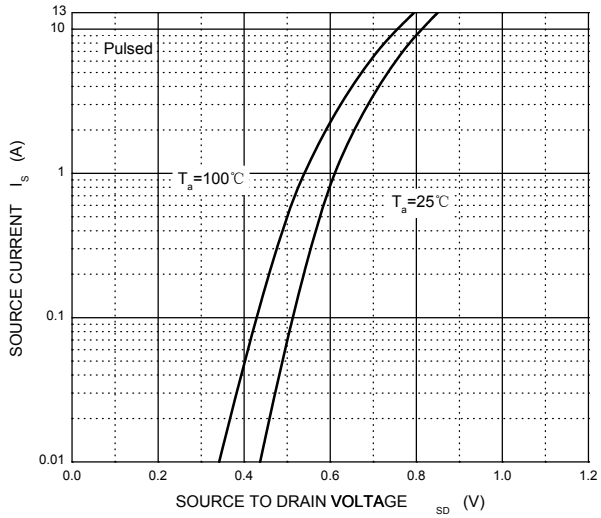
$R_{DS(ON)}$ —— I_D



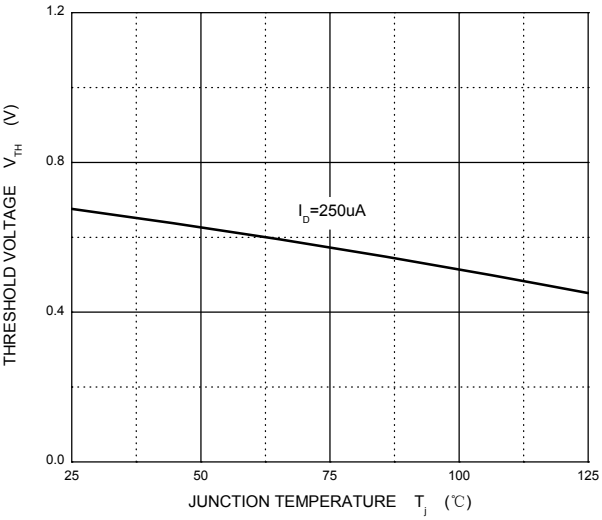
$R_{DS(ON)}$ —— V_{GS}



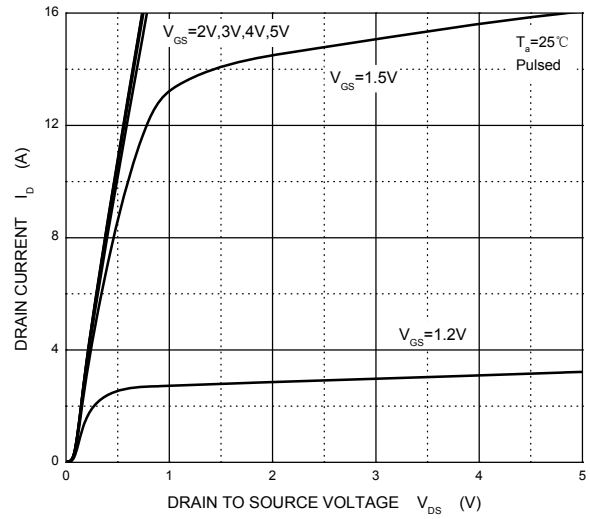
I_S —— V_{SD}



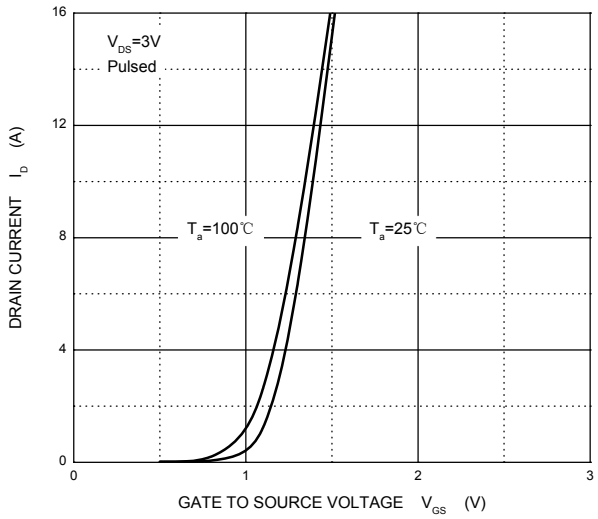
Threshold Voltage



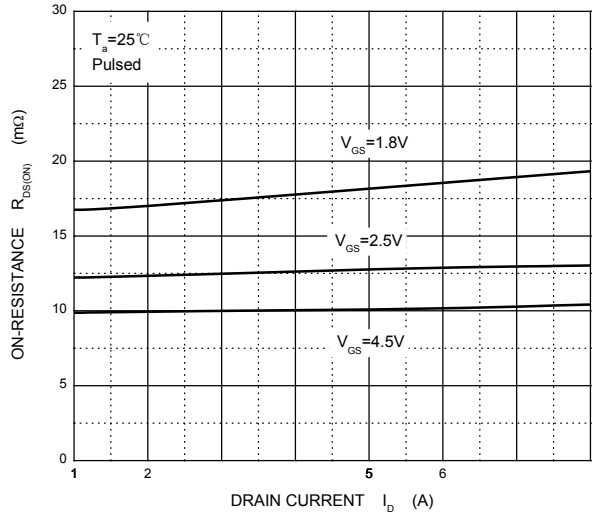
Output Characteristics



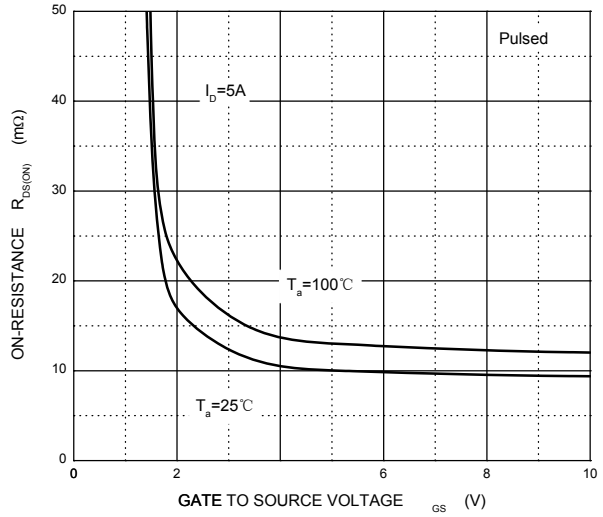
Transfer Characteristics



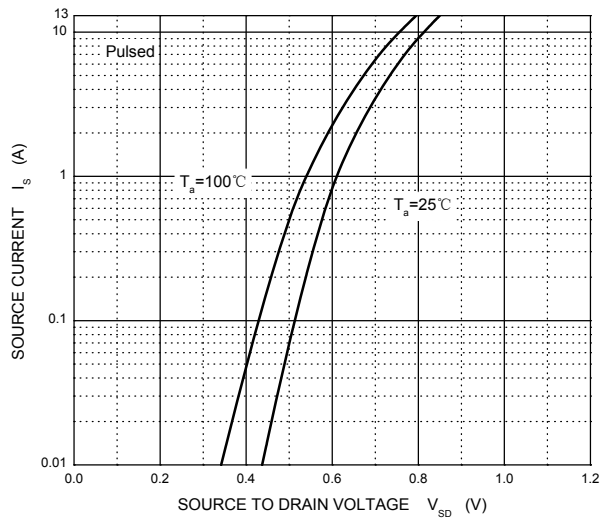
$R_{DS(ON)}$ —— I_D



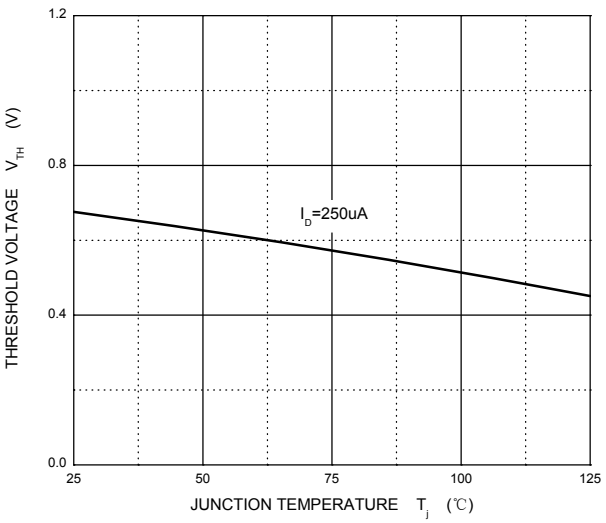
$R_{DS(ON)}$ —— V_{GS}



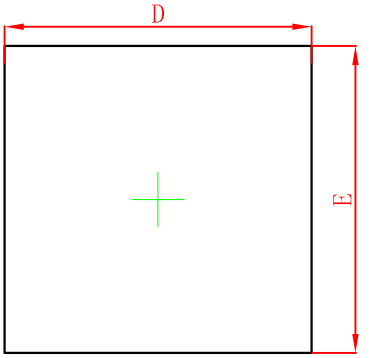
I_S —— V_{SD}

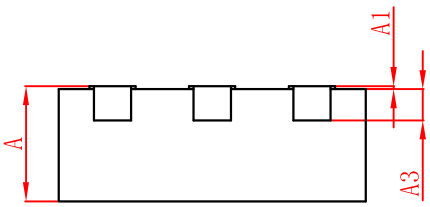


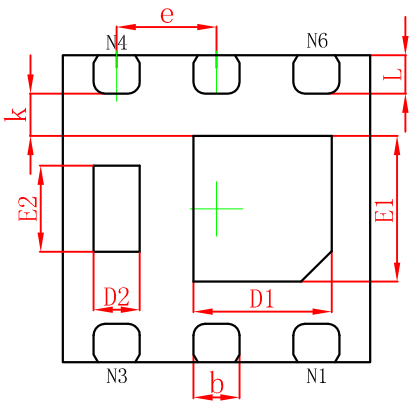
Threshold Voltage



DFNWB2X2-6L-J Package Outline Dimensions

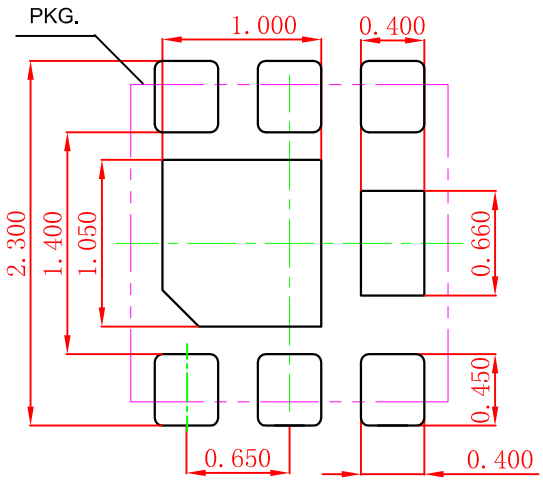






Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800		0.032
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	1.924	2.076	0.076	0.082
D1	0.800	1.000	0.031	0.039
E1	0.850	1.050	0.033	0.041
D2	0.200	0.400	0.008	0.016
E2	0.460	0.660	0.018	0.026
k	0.200MIN.		0.008MIN.	
b	0.250	0.350	0.010	0.014
e	0.650TYP.		0.026TYP.	
L	0.174	0.326	0.007	0.013

DFNWB2X2-6L-J Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.

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