Genesys Logic, Inc.

GL838T

USB 2.0 Single-LUN SD/MMC/MS Card Reader Controller

Datasheet

Revision 1.02
Jun. 24, 2016

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Revision History

Revision	Date	Description
1.00	09/05/2012	First formal release
1.01	07/09/2015	Update Table 4.3 DC Characteristics, p.10
1.02	06/24/2016	Update CH2 Features

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CHAPTER 1 GENERAL DESCRIPTION

The GL838T is a high performance USB 2.0 Interface Flash Card Reader controller and targets for the application which require operating temperature -40°C to 85°C. GL838T supports USB 2.0 high-speed transmission to Secure Digital™ (SD), miniSD™, micro SD™ (T-Flash) , SDXC, MultiMediaCard™ (MMC), RS MultiMediaCard™ (RS-MMC), MMC Plus, MMC Micro, MMC Mobile , Memory Stick™ (MS), Memory Stick Duo™ (MS Duo), High Speed Memory Stick™ (HS MS), Memory Stick PRO™ (MS PRO), Memory Stick PRO™ Duo (MS PRO Duo), Memory Stick ROM and MS PRO Micro on one chip. As a single chip solution for USB 2.0 flash card reader, the GL838T complies with Universal Serial Bus specification rev. 2.0, USB Storage Class specification ver.1.0, and flash card interface specification each.

The GL838T can support different kinds of interfaces in single LUN and integrates a high speed 8051 microprocessor and a high efficiency hardware engine for the best data transfer performance between USB and flash card interfaces. Besides, the GL838T integrates 5V to 3.3V, 3.3V to 1.8V regulators and MOSFET switches. It also enables the function of on-chip clock source (OCCS) which means no external 12MHz XTAL is needed and that effectively reduces the total BOM cost.

The GL838T pin assignment design fits to card sockets to provide easier PCB layout. 28 Pin QFN (5x5 mm) package is the available package type.

CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with 480Mbps Universal Serial Bus specification rev. 2.0.
  - Comply with USB Storage Class specification rev. 1.0.
  - Support 1 device address and up to 4 endpoints: Control (0)/ Bulk Read (1)/ Bulk Write (2)/Interrupt (3).
- Integrated USB building blocks
  - USB2.0 transceiver macro (UTM), Serial Interface Engine (SIE), Build-in power-on reset (POR).
- Embedded 1T 8051 micro-controller
  - Embedded 48K Byte mask ROM and 40K+8K Byte SRAM
- Secure Digital™ and MultiMediaCard™
  - Supports SD specification v1.0 / v1.1 / v2.0
  - Compliant with Secure Digital™ v5.0
  - Compatible with SDXC (Up to 2TB)
  - Supports MMC specification v3.X / v4.0 / v4.1 / v4.2 / v4.3.
  - x1 / x4 data transmission.
- Memory Stick™ / Memory Stick PRO / Memory Stick PRO Duo / Memory Stick Micro / Memory Stick XC
  - Comply with Memory Stick specification: MS 1.43, MS PRO 1.03, MS Micro 1.04
- Support external serial Flash interface (8bit format) for the flexibility to load vender information and system option; it can be ISP by USB.
- On chip clock source (OCCS) and no need of 12MHz Crystal Clock input.
- On-Chip 5V to 3.3V and 3.3V to 1.8V regulator. No external regulator required.
- On-Chip power MOSFETs for supplying flash media card power with programmable over current protection mechanism
- Provide the thermal detection and protection mechanism
- Available in 28 Pin QFN(5x5 mm) package

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinout

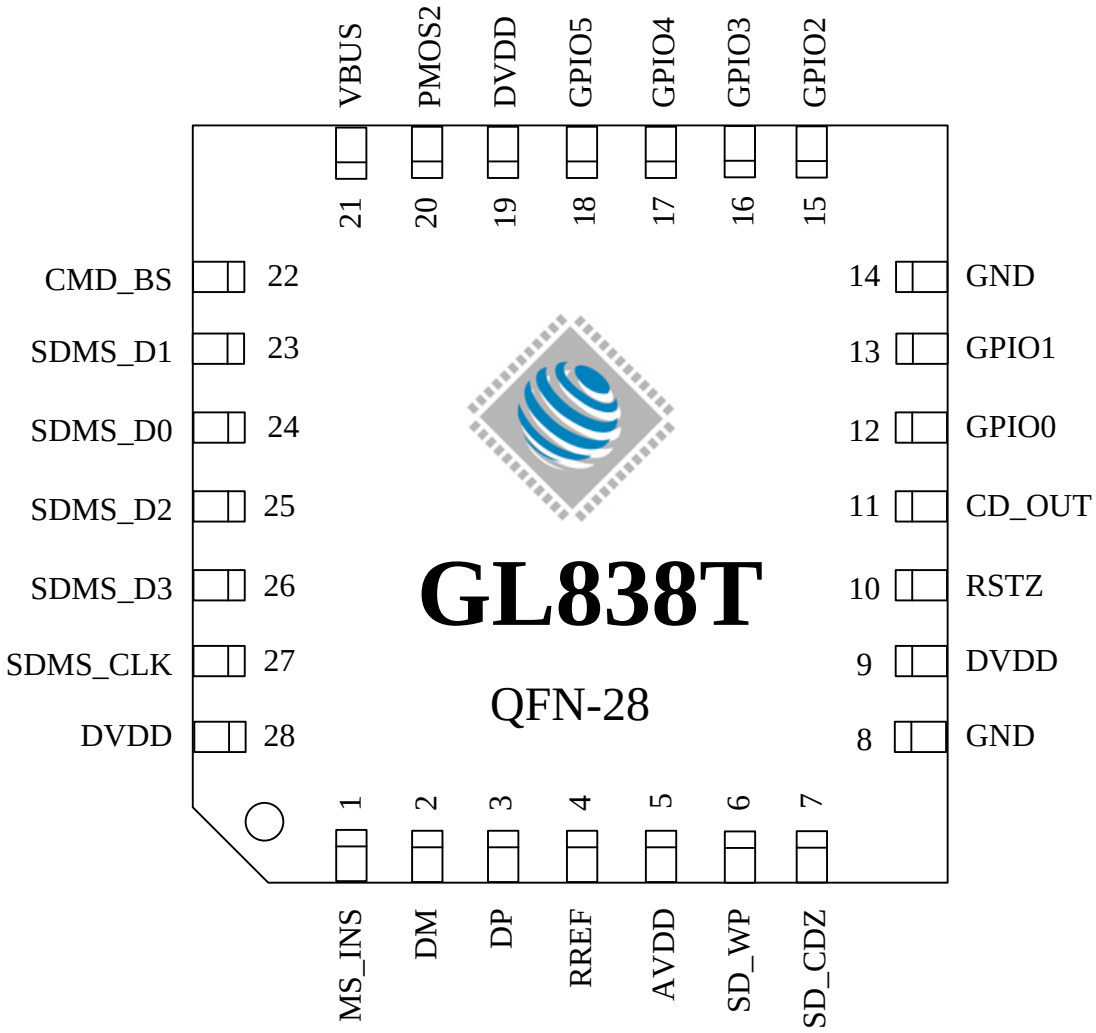


Figure 3.1 - 28 Pin QFN Pin out Diagram

3.2 Pin List/Descriptions

Table 3.1 - Pin Descriptions

Pin name	QFN28 Pin	Type	Description
Power/ Ground			
VBUS	21	P	USB power
AVDD	5	P	Analog power , connect DVDD through Bead
DVDD	9,19,28	P	Digital power 3.3V
PMOS2	20	P	SD/MMC/MS card power, card power 250mA
GND	8,14	P	Ground
USB PHY			
DM	2	A	USB D-
DP	3	A	USB D+
RREF	4	A	USB Reference resistor, external resistor value is 715 +/- 1% ohm
Card Interface			
SDMS_CLK	27	B	Memory Stick CLK SD/MMC CLK
CMD_BS	22	B	Memory Stick BS SD/MMC CMD
SDMS_D[3:0]	26,25,23,24	B	MS/SD/MMC data pins D0~D3
SD_CDZ	7	B	SD card detect 0: Card insert 1: No card
SD_WP	6	B	SD Write Protect signal 0: Write enable 1: Write protect
MS_INS	1	B	MS insertion detect 0: Card insert 1: No card
Others			
CD_OUT	11	O	Card Detect Output
GPIO0	12	B	GPIO0: LED
GPIO1	13	B	General purpose I/O
GPIO[5:2]	18,17,16,15	B	GPIO2: SPI Flash Clock GPIO3: SPI Flash Chip Select GPIO4: Data Output from GL838T to SPI Flash GPIO5: Data Input from SPI Flash to GL838T
RSTZ	10	I, pu	System reset, active low

Notation:

Type **I, pu** The pin is in input mode with internal Pull Up

B Bi-directional in Pad

P Power / Ground Pad

A Analog Pad

O The pin is in output mode, drive “H” or “L”

CHAPTER 4 ELECTRICAL AND AC CHARACTERISTICS

4.1 Temperature Conditions

Table 4.1 - Temperature Conditions

Parameter	Value
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C

4.2 Operating Conditions

Table 4.2 - Operating Conditions

Parameter	Value
Supply Voltage	+4.75V to +5.25V
Ground Voltage	0V

4.3 DC Characteristics

Table 4.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	USB Power Voltage		4.75	5.0	5.25	V
V_{D33}	Digital Power Voltage		3.0	3.3	3.6	V
V_{AVDD}	Analog Power Voltage		3.0	3.3	3.6	V
V_{PMOS2}	PMOS2 Power Voltage		2.7	3.3	3.6	V
V_{IH}	Input High Voltage		2.0	-	-	V
V_{IL}	Input Low Voltage		-	-	0.4	V
I_I	Input Leakage current	$0 < V_{IN} < V_{CC}$	-10	-	10	μA
V_{OH}	Output High Voltage		2.8	-	-	V
V_{OL}	Output Low Voltage		-	-	0.4	V
I_{OH}	Output Current High		8		-	mA
I_{OL}	Output Current Low		8		-	mA
C_{IN}	Input Pin Capacitance		-	5	-	pF
I_{SUSP}	Suspend current	1.5K external pull-up included	-	-	450	μA
I_{CC}	Operating current	Connect to USB with 8051 operating	-	-	70	mA
R_{Pu-RST}	Pull-up resistor of RSTZ		7	-	14	KΩ
R_{P-GP}	Pull-up/down resistor of GPIO and SD CMD		14	-	48	KΩ
R_{Pu-IO}	Pull-up resistor of SD data and control pins		38	-	117	KΩ

R_{Pd-IO}	Pull-down resistor of SD data and control pins		30	-	106	KΩ

4.4 AC Characteristics of Reset Timing

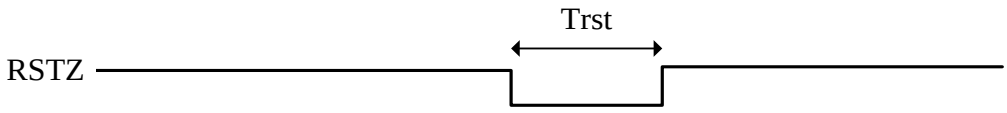


Figure 4.1 - Timing Diagram of Reset Width

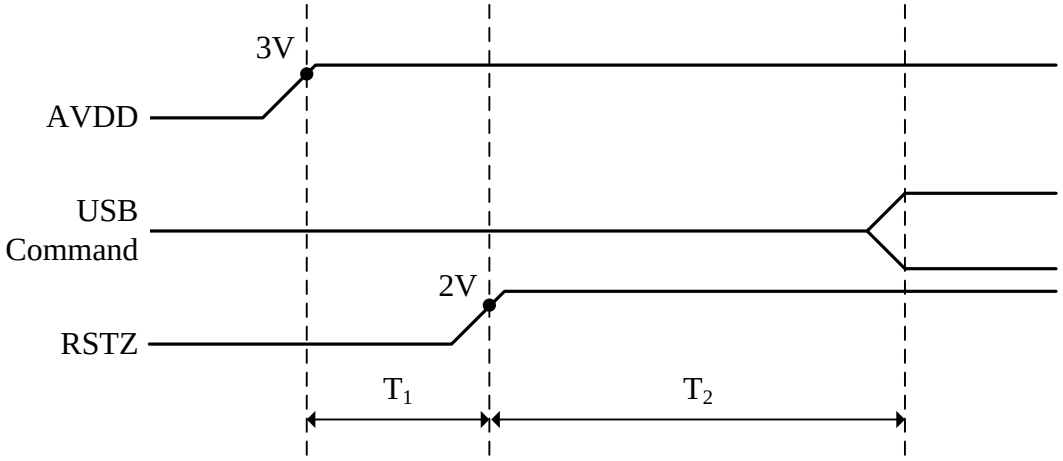


Figure 4.2 - Timing Diagram of Power Good to USB Command Receive Ready

Table 4.4 - Reset Timing

Parameter	Description	Min.	Unit
Trst	Chip reset sense timing width	1	ms
T1	AVDD power up to reset de-assert	4	ms
T2	Reset de-assert to respond USB command ready	72	ms

4.5 Memory Card Clock Frequency

Table 4.5 – SD/MMC Card Clock Frequency

Parameter	Description	Max.	Unit
F_{ID}	Clock frequency Identification Mode	375	KHz
F_{DS}	Clock frequency Default Speed Mode	15	MHz
$F_{DS(Note\ 1)}$	Clock frequency Default Speed Mode	24	MHz
$F_{HS(Note\ 1)}$	Clock frequency High Speed Mode	48	MHz

* Note 1: 24MHz and 48MHz are supported by external Firmware

CHAPTER 5 BLOCK DIAGRAM

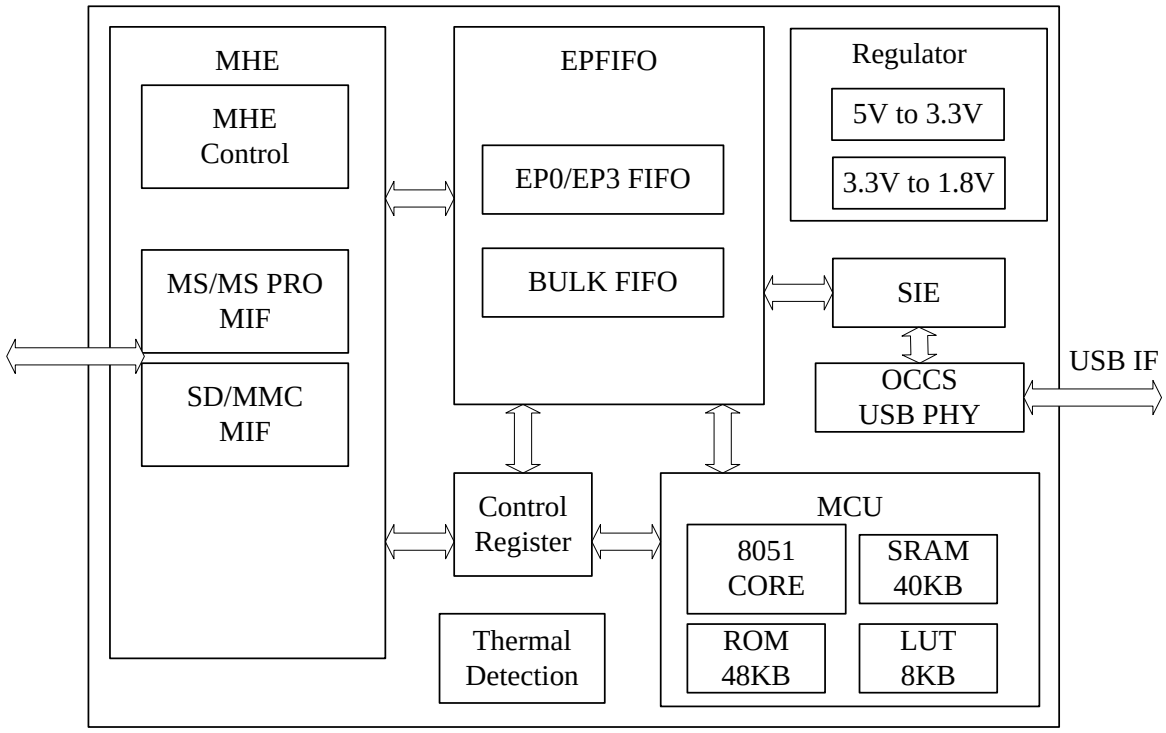


Figure 5.1 - Block Diagram

CHAPTER 6 FUNCTION BLOCK DESCRIPTION

6.1 OCCS USB PHY

The USB 2.0 Transceiver Macrocell is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic. On chip clock source and no need of 12MHz Crystal Clock input.

6.2 SIE

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

6.3 EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0), interrupt FIFO (FIFO3), Bulk In/Out FIFO (BULKFIFO)

- **Control FIFO** FIFO of control endpoint 0.
  It is 64-byte FIFO, and it is used for endpoint 0 data transfer.
- **Interrupt FIFO** 64-byte depth FIFO of endpoint 3 for status interrupt
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It contains ping-pong FIFO (512 bytes each bank) for transmit/receive data continuously.
  2. It can be directly accessed by uC

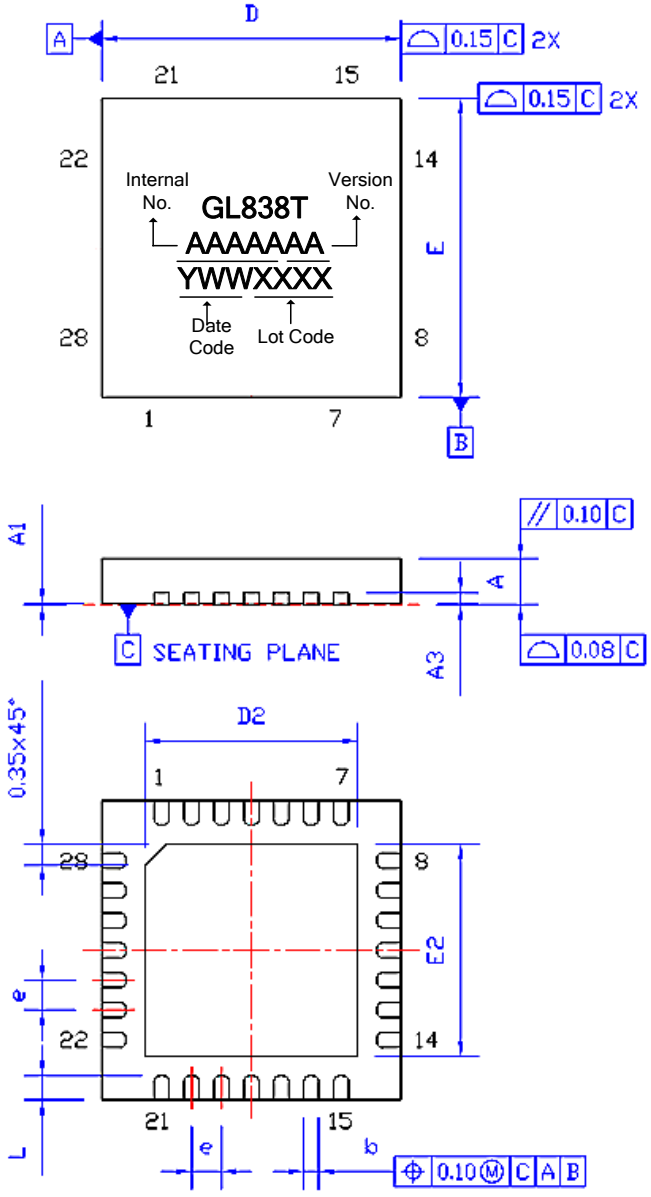
6.4 MHE

It contains 4 MIFs (Media Interface)

- **MIFs**
  1. SD / MMC
  2. Memory Stick/ Memory Stick PRO

- **External Reset Circuit**
  Non-inverting, Schmitt input with weak pull-up using DVDD power.

CHAPTER 7 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.18 (7.1)	0.25 (9.8)	0.30 (11.8)
D	5.00 (196.9) BSC		
D2	3.40 (133.9)	3.55 (139.8)	3.70 (145.7)
E	5.00 (196.9) BSC		
E2	3.40 (133.9)	3.55 (139.8)	3.70 (145.7)
e	0.50 (19.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

Figure 7.1 - GL838T 28 Pin QFN Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Green/Wire Material	Version	Status
GL838T-OHG*XX	QFN 28	Green Package + Au Wire	XX	Available

*The marking of "OHG" will not be shown on the IC due to QFN 28 package size limitation.