

### Product Overview

The NSi814x devices are high reliability quad-channel digital isolators. The NSi814x device is safety certified by UL1577 support several insulation withstand voltages (3.75kVrms, 5kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi814x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 150kV/us. The NSi814x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi814x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use. AEC-Q100 (Grade 1) option is provided for all devices.

### Key Features

- Up to 5000V<sub>RMS</sub> Insulation voltage
- Data rate: DC to 150Mbps
- Power supply voltage: 2.5V to 5.5V
- AEC-Q100 Grade 1 available for All devices
- High CMTI: 150kV/us
- Chip level ESD: HBM: ±6kV
- High system level EMC performance: Enhanced system level ESD, EFT, Surge immunity
- Default output high level or low level option
- Isolation Barrier Life: >60 years
- Low power consumption: 1.5mA/ch (1 Mbps)
- Low propagation delay: <15ns
- Operation temperature: -40°C~125°C
- RoHS-compliant packages:

SOIC-16 narrow body

SOIC-16 wide body

### Safety Regulatory Approvals (pending)

- UL recognition: up to 5000V<sub>RMS</sub> for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A approval IEC60950-1 standard
- DIN VDE V 0884-10 (VDE V 0884-10): 2006-12

### Applications

- Industrial automation system
- Isolated SPI, RS232, RS485
- General-purpose multichannel isolation
- Motor control

### Functional Block Diagrams

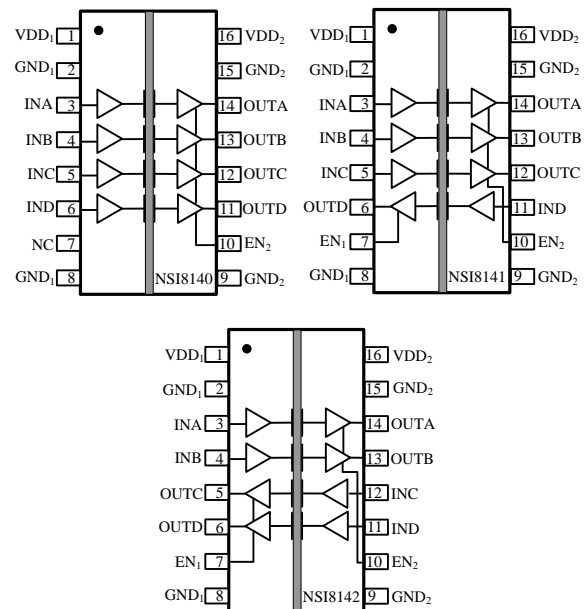


Figure 1. NSi814x Block Diagram

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# NSi8140/NSi8141/NSi8142

## 1.0 ABSOLUTE MAXIMUM RATINGS

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD1, VDD2	-0.5		6.5	V	
Maximum Input Voltage	VINA, VINB, VINC, VIND	-0.4		VDD+0.4	V	
Maximum Output Voltage	VOUTA, VOUTB, VOUTC	-0.4		VDD+0.4	V	
Maximum Input/Output Pulse Voltage	VINA, VINB, VINC, VOUTA, VOUTB, VOUTC	-0.8		VDD+0.8	V	Pulse width should be less than 100ns, and the duty cycle should be less than 10%
Common-Mode Transients	CMTI			±150	kV/us	
Output current	I <sub>o</sub>	-15		15	mA	
Maximum Surge Isolation Voltage	V <sub>IOSM</sub>			5.3	kV	
Operating Temperature	T <sub>opr</sub>	-40		125	°C	
Storage Temperature	T <sub>stg</sub>	-40		150	°C	
Electrostatic discharge	HBM			±6000	V	
	CDM			±2000	V	

## 2.0 SPECIFICATIONS

### 2.1 ELECTRICAL CHARACTERISTICS

(VDD1=2.5V~5.5V, VDD2=2.5V~5.5V, T<sub>a</sub>=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, T<sub>a</sub> = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power on Reset	VDD <sub>POR</sub>		2.2		V	POR threshold as during power-up
	VDD <sub>HYS</sub>		0.1		V	POR threshold Hysteresis
Input Threshold	V <sub>IT</sub>		1.6		V	Input Threshold at rising edge
	V <sub>IT_HYS</sub>		0.4		V	Input Threshold Hysteresis
High Level Input Voltage	V <sub>IH</sub>	2			V	
Low Level Input Voltage	V <sub>IL</sub>			0.8	V	
High Level Output Voltage	V <sub>OH</sub>	VDD-0.3			V	I <sub>OH</sub> = -4mA
Low Level Output Voltage	V <sub>OL</sub>			0.3	V	I <sub>OL</sub> = 4mA
Output Impedance	R <sub>out</sub>		50		ohm	

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Input Pull high or low Current	$I_{pull}$		8	15	$\mu$ A	
Start Up Time after POR	trbs		40		usec	
Common Mode Transient Immunity	CMTI	100		150	kV/us	

(VDD1=5V $\pm$  10%, VDD2=5V $\pm$  10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 5V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	<b>NSi8140</b>					
	$I_{DD1}(Q0)$		0.894	1.34	mA	All Input 0V for NSi8140x0 Or All Input at supply for NSi8140x1
	$I_{DD2}(Q0)$		2.326	3.5	mA	
	$I_{DD1}(Q1)$		5.316	7.8	mA	All Input at supply for NSi8140x0 Or All Input 0V for NSi8140x1
	$I_{DD2}(Q1)$		2.432	3.65	mA	
	$I_{DD1}(1M)$		3.087	4.63	mA	All Input with 1Mbps, $C_L=15pF$
	$I_{DD2}(1M)$		2.728	4.09	mA	
	$I_{DD1}(10M)$		3.182	4.77	mA	All Input with 10Mbps, $C_L=15pF$
	$I_{DD2}(10M)$		5.834	8.75	mA	
	$I_{DD1}(100M)$		3.918	5.88	mA	All Input with 100Mbps, $C_L=15pF$
	$I_{DD2}(100M)$		37.06	55.6	mA	
	<b>NSi8141</b>					
	$I_{DD1}(Q0)$		1.244	1.87	mA	All Input 0V for NSi8141x0 Or All Input at supply for NSi8141x1
	$I_{DD2}(Q0)$		2.164	3.25	mA	
	$I_{DD1}(Q1)$		4.658	7	mA	All Input at supply for NSi8141x0 Or All Input 0V for NSi8141x1
	$I_{DD2}(Q1)$		3.416	5	mA	
	$I_{DD1}(1M)$		3.07	4.6	mA	All Input with 1Mbps, $C_L=15pF$
	$I_{DD2}(1M)$		3.064	4.6	mA	
	$I_{DD1}(10M)$		3.82	5.7	mA	All Input with 10Mbps, $C_L=15pF$
	$I_{DD2}(10M)$		5.496	8.2	mA	
	$I_{DD1}(100M)$		10.708	16.06	mA	All Input with 100Mbps, $C_L=15pF$
	$I_{DD2}(100M)$		29.336	44	mA	
	<b>NSi8142</b>					
$I_{DD1}(Q0)$		1.688	2.5	mA	All Input 0V for NSi8142x0 Or All Input at supply for NSi8142x1	
$I_{DD2}(Q0)$		1.704	2.56	mA		

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	I <sub>DD1</sub> (Q1)		4.038	6.06	mA	All Input at supply for NSi8142x0 Or All Input 0V for NSi8142x1
	I <sub>DD2</sub> (Q1)		4.1	6.15	mA	
	I <sub>DD1</sub> (1M)		3.06	4.6	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		3.108	4.7	mA	
	I <sub>DD1</sub> (10M)		4.578	6.9	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.694	7	mA	
	I <sub>DD1</sub> (100M)		19	28.5	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		20.868	31	mA	
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t <sub>PLH</sub>	5	8.20	15	ns	See <a href="#">Figure 2.9</a> , C <sub>L</sub> = 15pF
	t <sub>PHL</sub>	5	10.56	15	ns	See <a href="#">Figure 2.9</a> , C <sub>L</sub> = 15pF
Pulse Width Distortion  t <sub>PHL</sub> - t <sub>PLH</sub>	PWD			5.0	ns	See <a href="#">Figure 2.9</a> , C <sub>L</sub> = 15pF
Rising Time	t <sub>r</sub>			5.0	ns	See <a href="#">Figure 2.9</a> , C <sub>L</sub> = 15pF
Falling Time	t <sub>f</sub>			5.0	ns	See <a href="#">Figure 2.9</a> , C <sub>L</sub> = 15pF
Peak Eye Diagram Jitter	t <sub>JIT</sub> (PK)		350		ps	
Channel-to-Channel Delay Skew	t <sub>SK</sub> (c2c)			2.5	ns	
Part-to-Part Delay Skew	t <sub>SK</sub> (p2p)			5.0	ns	
Disable high to Tri-State	t <sub>PHZ</sub>		14.88		ns	See <a href="#">Figure 2.10</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k
Enable to Data high Valid	t <sub>PZH</sub>		10.00		ns	See <a href="#">Figure 2.10</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k
Disable low to Tri-State	t <sub>PLZ</sub>		17.25		ns	See <a href="#">Figure 2.10</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k
Enable to Data high Valid	t <sub>PZL</sub>		10.85		ns	See <a href="#">Figure 2.10</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k

(VDD1=3.3V± 10%, VDD2=3.3V± 10%, Ta=-40°C to 125°C. Unless otherwise noted, Typical values are at VDD1 = 3.3V, VDD2 = 3.3V, Ta = 25°C)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	<b>NSi8140</b>					
	I <sub>DD1</sub> (Q0)		0.832	1.25	mA	All Input 0V for NSi8140x0 Or All Input at supply for NSi8140x1
	I <sub>DD2</sub> (Q0)		2.214	3.3	mA	
	I <sub>DD1</sub> (Q1)		5.23	7.9	mA	All Input at supply for NSi8140x0 Or All Input 0V for NSi8140x1
	I <sub>DD2</sub> (Q1)		2.32	3.48	mA	
	I <sub>DD1</sub> (1M)		3.01	4.5	mA	All Input with 1Mbps,

# NSi8140/NSi8141/NSi8142

	I <sub>DD2</sub> (1M)		2.486	3.73	mA	C <sub>L</sub> =15pF
	I <sub>DD1</sub> (10M)		3.106	4.66	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.476	6.7	mA	
	I <sub>DD1</sub> (100M)		3.826	5.74	mA	All Input with 100Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (100M)		25.5	38	mA	
<b>NSi8141</b>						
	I <sub>DD1</sub> (Q0)		1.165	1.75	mA	All Input 0V for NSi8141x0 Or All Input at supply for NSi8141x1
	I <sub>DD2</sub> (Q0)		2.062	3.1	mA	
	I <sub>DD1</sub> (Q1)		4.566	6.85	mA	All Input at supply for NSi8141x0 Or All Input 0V for NSi8141x1
	I <sub>DD2</sub> (Q1)		3.306	5	mA	
	I <sub>DD1</sub> (1M)		2.954	4.4	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		2.862	4.3	mA	
	I <sub>DD1</sub> (10M)		3.452	5.2	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		4.368	6.5	mA	
	I <sub>DD1</sub> (100M)		8.084	12	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		19.96	30	mA	
<b>NSi8142</b>						
	I <sub>DD1</sub> (Q0)		1.598	2.4	mA	All Input 0V for NSi8142x0 Or All Input at supply for NSi8142x1
	I <sub>DD2</sub> (Q0)		1.618	2.43	mA	
	I <sub>DD1</sub> (Q1)		3.942	5.9	mA	All Input at supply for NSi8142x0 Or All Input 0V for NSi8142x1
	I <sub>DD2</sub> (Q1)		4.004	6	mA	
	I <sub>DD1</sub> (1M)		2.901	4.3	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		2.9452	4.4	mA	
	I <sub>DD1</sub> (10M)		3.898	5.85	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		3.976	6	mA	
	I <sub>DD1</sub> (100M)		12.9	19	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		14.868	22	mA	
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t <sub>PLH</sub>	5	9.20	15	ns	See <a href="#">Figure 2.9</a> , C <sub>L</sub> = 15pF
	t <sub>PHL</sub>	5	10.40	15	ns	See <a href="#">Figure 2.9</a> , C <sub>L</sub> = 15pF
Pulse Width Distortion  t <sub>PHL</sub> - t <sub>PLH</sub>	PWD			5.0	ns	See <a href="#">Figure 2.9</a> , C <sub>L</sub> = 15pF

# NSi8140/NSi8141/NSi8142

Rising Time	$t_r$			5.0	ns	See <a href="#">Figure 2.9</a> , $C_L = 15\text{pF}$
Falling Time	$t_f$			5.0	ns	See <a href="#">Figure 2.9</a> , $C_L = 15\text{pF}$
Peak Eye Diagram Jitter	$t_{JIT(PK)}$		350		ps	
Channel-to-Channel Delay Skew	$t_{SK(c2c)}$			2.5	ns	
Part-to-Part Delay Skew	$t_{SK(p2p)}$			5.0	ns	
Disable high to Tri-State	$t_{PHZ}$		17.85		ns	See <a href="#">Figure 2.10</a> , $C_L = 15\text{pF}$ , $R_L=1\text{k}$
Enable to Data high Valid	$t_{PZH}$		13.37		ns	See <a href="#">Figure 2.10</a> , $C_L = 15\text{pF}$ , $R_L=1\text{k}$
Disable low to Tri-State	$t_{PLZ}$		20.6		ns	See <a href="#">Figure 2.10</a> , $C_L = 15\text{pF}$ , $R_L=1\text{k}$
Enable to Data high Valid	$t_{PZL}$		13.67		ns	See <a href="#">Figure 2.10</a> , $C_L = 15\text{pF}$ , $R_L=1\text{k}$

( $V_{DD1}=2.5\text{V}\pm 10\%$ ,  $V_{DD2}=2.5\text{V}\pm 10\%$ ,  $T_a=-40^\circ\text{C}$  to  $125^\circ\text{C}$ . Unless otherwise noted, Typical values are at  $V_{DD1} = 2.5\text{V}$ ,  $V_{DD2} = 2.5\text{V}$ ,  $T_a = 25^\circ\text{C}$ )

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply current	<b>NSi8140</b>					
	$I_{DD1}(Q0)$		0.802	1.2	mA	All Input 0V for NSi8140x0 Or All Input at supply for NSi8140x1
	$I_{DD2}(Q0)$		2.161	3.24	mA	
	$I_{DD1}(Q1)$		5.17	7.8	mA	All Input at supply for NSi8140x0 Or All Input 0V for NSi8140x1
	$I_{DD2}(Q1)$		2.282	3.4	mA	
	$I_{DD1}(1M)$		2.968	4.45	mA	All Input with 1Mbps, $C_L=15\text{pF}$
	$I_{DD2}(1M)$		2.384	3.58	mA	
	$I_{DD1}(10M)$		3.056	4.58	mA	All Input with 10Mbps, $C_L=15\text{pF}$
	$I_{DD2}(10M)$		3.862	5.8	mA	
	$I_{DD1}(100M)$		3.772	5.67	mA	All Input with 100Mbps, $C_L=15\text{pF}$
	$I_{DD2}(100M)$		19.54	29.3	mA	
	<b>NSi8141</b>					
	$I_{DD1}(Q0)$		1.128	1.7	mA	All Input 0V for NSi8141x0 Or All Input at supply for NSi8141x1
	$I_{DD2}(Q0)$		2.012	3	mA	
	$I_{DD1}(Q1)$		4.51	6.8	mA	All Input at supply for NSi8141x0 Or All Input 0V for NSi8141x1
	$I_{DD2}(Q1)$		3.248	4.9	mA	
$I_{DD1}(1M)$		2.894	4.3	mA	All Input with 1Mbps, $C_L=15\text{pF}$	
$I_{DD2}(1M)$		2.766	4.15	mA		
$I_{DD1}(10M)$		3.272	4.9	mA	All Input with 10Mbps, $C_L=15\text{pF}$	
$I_{DD2}(10M)$		3.892	5.8	mA		

# NSi8140/NSi8141/NSi8142

	I <sub>DD1</sub> (100M)		6.95	10.4	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		15.706	23.56	mA	
<b>NSi8142</b>						
	I <sub>DD1</sub> (Q0)		1.556	2.3	mA	All Input 0V for NSi8142x0 Or All Input at supply for NSi8142x1
	I <sub>DD2</sub> (Q0)		1.574	2.4	mA	
	I <sub>DD1</sub> (Q1)		3.884	5.8	mA	All Input at supply for NSi8142x0 Or All Input 0V for NSi8142x1
	I <sub>DD2</sub> (Q1)		3.942	5.9	mA	
	I <sub>DD1</sub> (1M)		2.824	4.3	mA	All Input with 1Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (1M)		2.866	4.3	mA	
	I <sub>DD1</sub> (10M)		3.574	5.36	mA	All Input with 10Mbps, C <sub>L</sub> =15pF
	I <sub>DD2</sub> (10M)		3.642	5.46	mA	
	I <sub>DD1</sub> (100M)		10.678	16	mA	All Input with 100Mbps, C <sub>L</sub> = 15pF
	I <sub>DD2</sub> (100M)		11.618	17	mA	
Data Rate	DR	0		150	Mbps	
Minimum Pulse Width	PW			5.0	ns	
Propagation Delay	t <sub>PLH</sub>	5	10.0	15	ns	See <a href="#">Figure 2.9</a> , C <sub>L</sub> = 15pF
	t <sub>PHL</sub>	5	10.0	15	ns	See <a href="#">Figure 2.9</a> , C <sub>L</sub> = 15pF
Pulse Width Distortion  t <sub>PHL</sub> - t <sub>PLH</sub>	PWD			5.0	ns	See <a href="#">Figure 2.9</a> , C <sub>L</sub> = 15pF
Rising Time	t <sub>r</sub>			5.0	ns	See <a href="#">Figure 2.9</a> , C <sub>L</sub> = 15pF
Falling Time	t <sub>f</sub>			5.0	ns	See <a href="#">Figure 2.9</a> , C <sub>L</sub> = 15pF
Peak Eye Diagram Jitter	t <sub>JIT</sub> (PK)		350		ps	
Channel-to-Channel Delay Skew	t <sub>SK</sub> (c2c)			2.5	ns	
Part-to-Part Delay Skew	t <sub>SK</sub> (p2p)			5.0	ns	
Disable high to Tri-State	t <sub>PHZ</sub>		20.6		ns	See <a href="#">Figure 2.10</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k
Enable to Data high Valid	t <sub>PZH</sub>		18.12		ns	See <a href="#">Figure 2.10</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k
Disable low to Tri-State	t <sub>PLZ</sub>		21.85		ns	See <a href="#">Figure 2.10</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k
Enable to Data high Valid	t <sub>PZL</sub>		20.02		ns	See <a href="#">Figure 2.10</a> , C <sub>L</sub> = 15pF, R <sub>L</sub> =1k



# NSi8140/NSi8141/NSi8142

## 2.2. TYPICAL PERFORMANCE CHARACTERISTICS

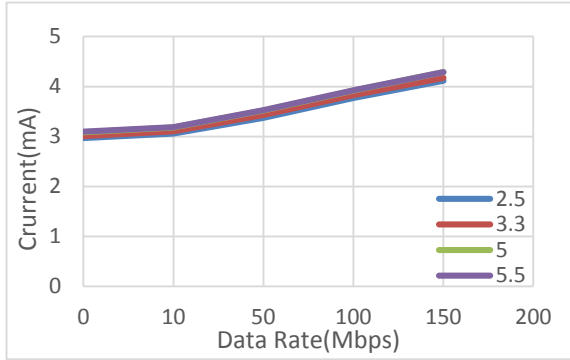


Figure 2.1 NSi8140 VDD1 Supply Current vs Data Rate

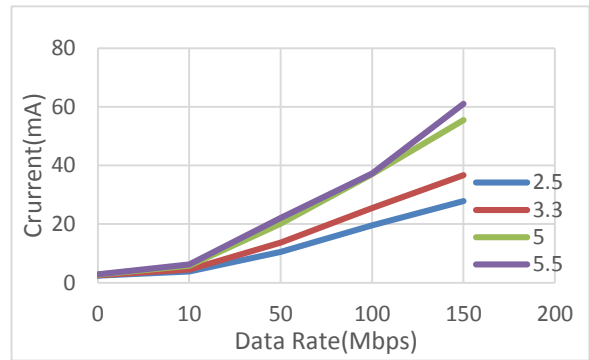


Figure 2.2 NSi8140 VDD2 Supply Current vs Data Rate

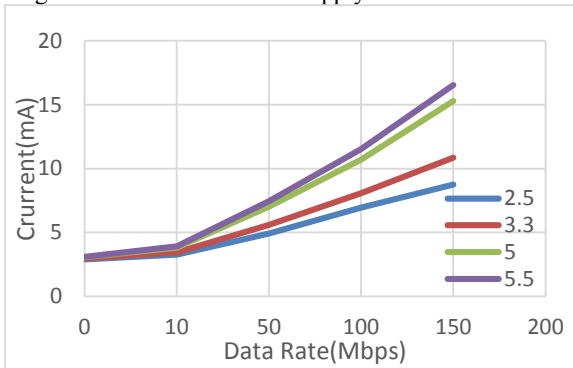


Figure 2.3 NSi8141 VDD1 Supply Current vs Data Rate

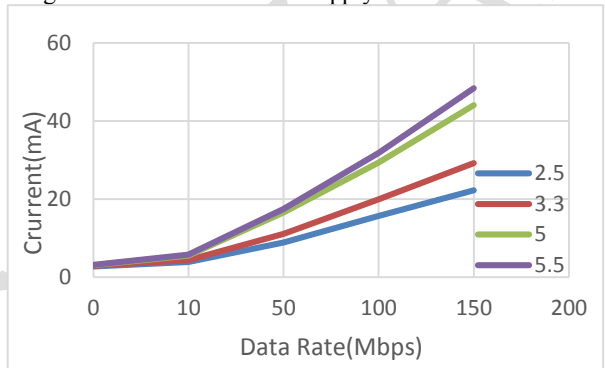


Figure 2.4 NSi8141 VDD2 Supply Current vs Data Rate

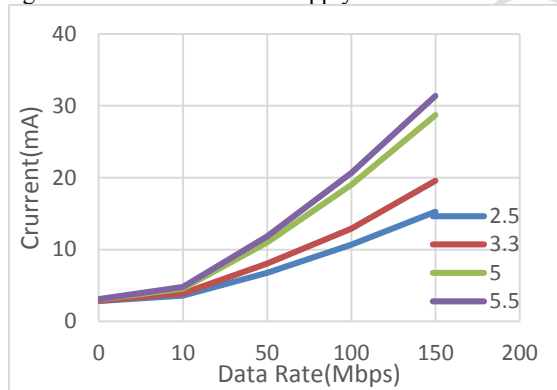


Figure 2.5 NSi8142 VDD1 Supply Current vs Data Rate

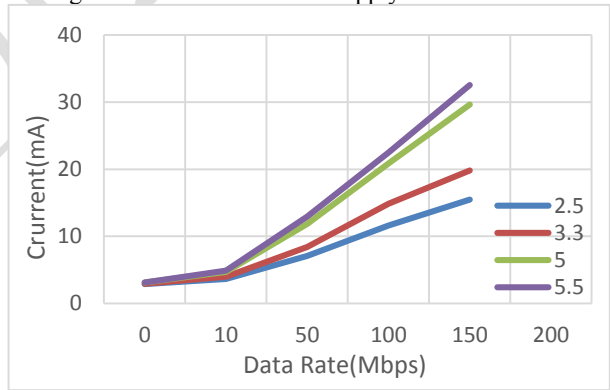
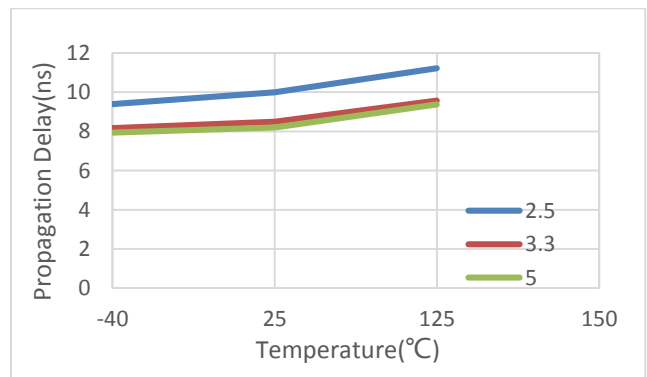
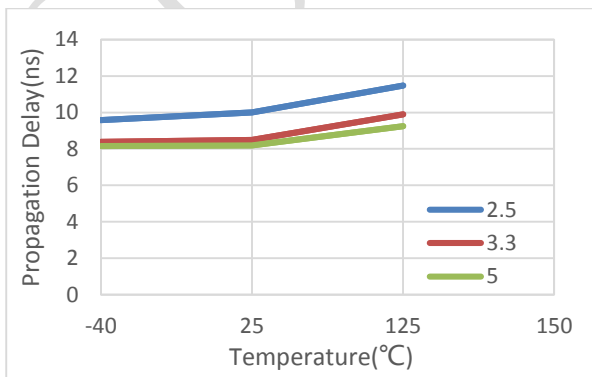


Figure 2.6 NSi8142 VDD2 Supply Current vs Data Rate



# NSi8140/NSi8141/NSi8142

Figure 2.7 Rising Edge Propagation Delay Vs Temp

Figure 2.8 Falling Edge Propagation Delay Vs Temp

## 2.3. PARAMETER MEASUREMENT INFORMATION

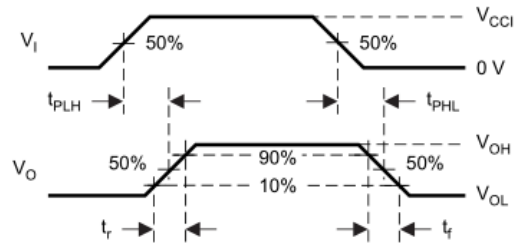
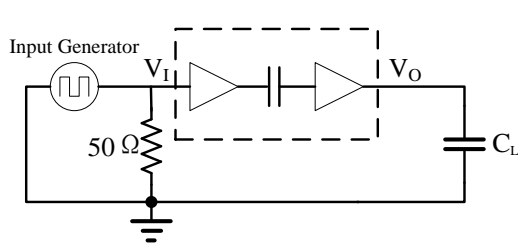


Figure 2.9 Switching Characteristics Test Circuit and Waveform

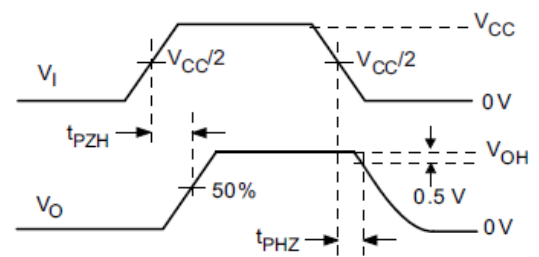
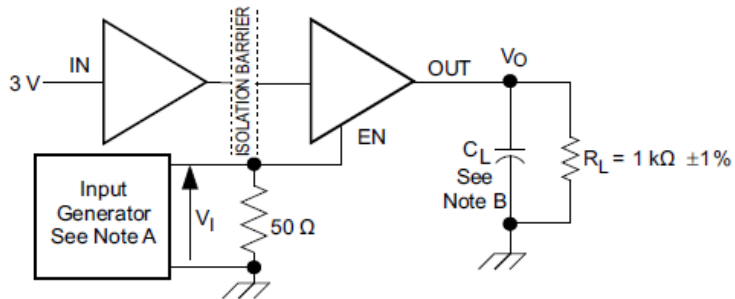
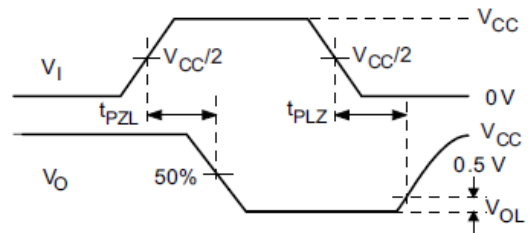
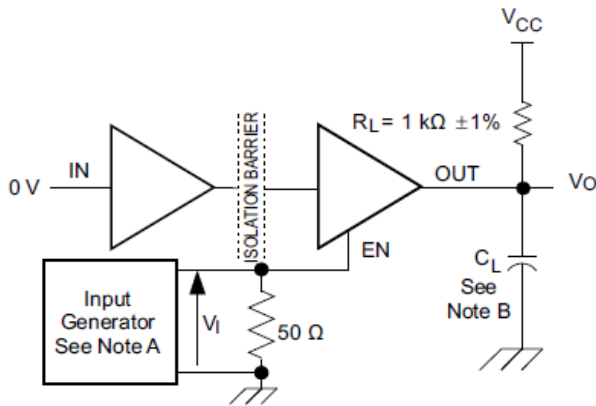


Figure 2.10 Enable/Disable Propagation Delay Time Test Circuit and Waveform

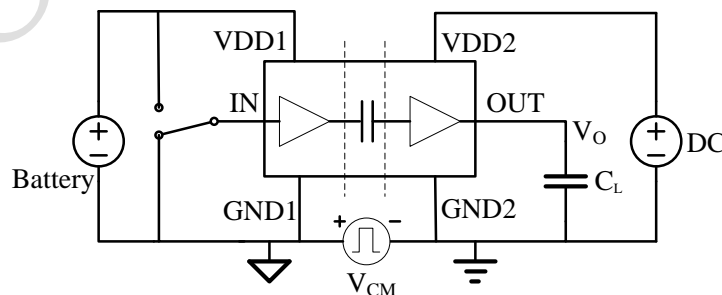


Figure 2.11 Common-Mode Transient Immunity Test Circuit

### 3.0 HIGH VOLTAGE FEATURE DESCRIPTION

#### 3.1. INSULATION AND SAFETY RELATED SPECIFICATIONS

Parameters	Symbol	Value		Unit	Comments
		NB-SOIC-16	WB-SOIC-16		
Minimum External Air Gap (Clearance)	L(I01)	4.0	7.8	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	L(I02)	4.0	7.8	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	20		um	Distance through insulation
Tracking Resistance(Comparative Tracking Index)	CTI	>600		V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I			

#### 3.2. DIN VDE V 0884-10 (VDE V 0884-10) INSULATION CHARATERISTICS

Description	Test Condition	Symbol	Value		Unit
			NB-SOIC-16	WB-SOIC-16	
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage $\leq 150V_{rms}$			I to IV	I to IV	
For Rated Mains Voltage $\leq 300V_{rms}$			I to III	I to IV	
For Rated Mains Voltage $\leq 400V_{rms}$			I to III	I to IV	
Climatic Classification			10/105/21	10/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum repetitive isolation voltage		VIORM	565	800	Vpeak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$ , 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge $< 5$ pC	$V_{pd(m)}$	847	1200	Vpeak
Input to Output Test Voltage, Method A					
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge $< 5$ pC	$V_{pd(m)}$	678	960	Vpeak

# NSi8140/NSi8141/NSi8142

After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge $< 5$ pC	$V_{pd(m)}$	678	960	Vpeak
Maximum transient isolation voltage	$t = 60$ sec	VIOTM	5300	7000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065, 1.2/50us waveform, VTEST=VIOSM	VIOSM	5384	5384	Vpeak
Isolation resistance	VIO =500V	RIO	$>10^9$	$>10^9$	$\Omega$
Isolation capacitance	$f = 1$ MHz	CIO	0.6	0.6	pF
Input capacitance		CI	2	2	pF
Total Power Dissipation at 25°C		Ps		1499	W
Safety input, output, or supply current	$\theta_{JA} = 140$ °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C	Is	160		mA
	$\theta_{JA} = 84$ °C/W, V I = 5.5 V, T J = 150 °C, T A = 25 °C			237	mA
Case Temperature		Ts	150	150	°C

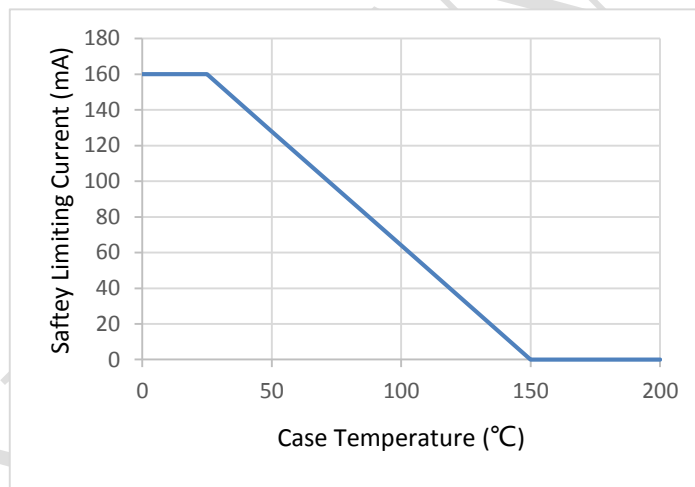
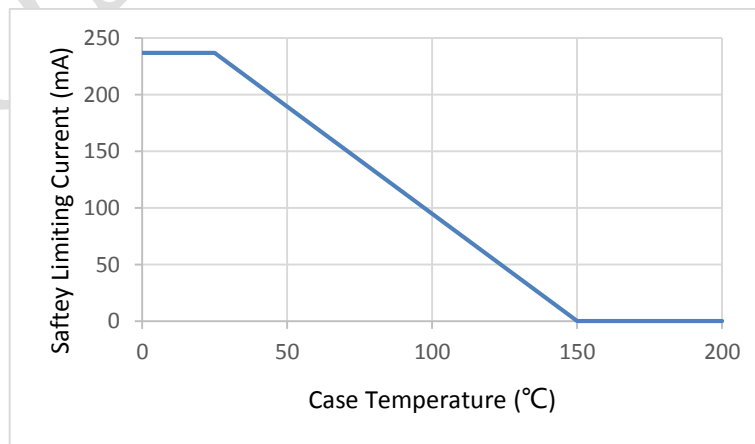


Figure 3.1 NSi8140N/NSi8141N/NSi8142N Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10



# NSi8140/NSi8141/NSi8142

Figure 3.2 NSi8140W/NSi8141W/NSi8142W Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

### 3.3. REGULATORY INFORMATION

The NSi8140N/NSi8141N/NSi8142N are approved or pending approval by the organizations listed in table.

<i>UL</i>	<i>CSA</i>	<i>VDE</i>	<i>CQC</i>
UL 1577 Component Recognition Program <sup>1</sup>	Approved under CSA Component Acceptance Notice 5A IEC60950-1	DIN V VDE V0884-10 (VDE V 0884-10):2006-12 <sup>2</sup>	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3750Vrms Isolation voltage	400V <sub>RMS</sub> basic insulation working voltage	Basic Insulation 565V <sub>peak</sub> , V <sub>IOSM</sub> =7000V <sub>peak</sub>	Basic insulation at 400V <sub>RMS</sub> (565V <sub>peak</sub> )
File (pending)	File (pending)	File (pending)	File (pending)

<sup>1</sup> In accordance with UL 1577, each NSi8140N/NSi8141N/NSi8142N is proof tested by applying an insulation test voltage  $\geq 4500$  V rms for 1 sec.

<sup>2</sup> In accordance with DIN V VDE V 0884-10, each NSi8140N/NSi8141N/NSi8142N is proof tested by applying an insulation test voltage  $\geq 1059$  V peak for 1 sec (partial discharge detection limit = 5 pC). The \* marking branded on the component designates DIN V VDE V 0884-10 approval.

The NSi8140W/NSi8141W/NSi8142W are approved or pending approval by the organizations listed in table.

<i>UL</i>	<i>CSA</i>	<i>VDE</i>	<i>CQC</i>
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A IEC60950-1	DIN V VDE V0884-10 (VDE V 0884-10):2006-12	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000Vrms Isolation voltage	800V <sub>RMS</sub> basic insulation working voltage 400V <sub>RMS</sub> Reinforced insulation working voltage	Basic Insulation 1131V <sub>peak</sub> , V <sub>IOSM</sub> =5384V <sub>peak</sub>	Basic insulation at 800V <sub>RMS</sub> (1131V <sub>peak</sub> ) Reinforced insulation at 400V <sub>RMS</sub> (565V <sub>peak</sub> )
File (pending)	File (pending)	File (pending)	File (pending)

<sup>1</sup> In accordance with UL 1577, each NSi8140W/NSi8141W/NSi8142W is proof tested by applying an insulation test voltage  $\geq 6000$  V rms for 1 sec.

<sup>2</sup> In accordance with DIN V VDE V 0884-10, each NSi8140W/NSi8141W/NSi8142W is proof tested by applying an insulation test voltage  $\geq 1592$  V peak for 1 sec (partial discharge detection limit = 5 pC). The \* marking branded on the component designates DIN V VDE V 0884-10 approval.

## 4.0 FUNCTION DESCRIPTION

The NSi814x is a Quad-channel digital isolator based on a capacitive isolation barrier technique. The digital signal is modulated with RF carrier generated by the internal oscillator at the Transmitter side. Then it is transferred through the capacitive isolation barrier and demodulated at the Receiver side.

The NSi814x devices are high reliability quad-channel digital isolator with AEC-Q100 qualified. The NSi814x device is safety certified by UL1577 support several insulation withstand voltages (3.75kVrms, 5kVrms), while providing high electromagnetic immunity and low emissions at low power consumption. The data rate of the NSi814x is up to 150Mbps, and the common-mode transient immunity (CMTI) is up to 150kV/us. The NSi814x device provides digital channel direction configuration and the default output level configuration when the input power is lost. Wide supply voltage of the NSi814x device support to connect with most digital interface directly, easy to do the level shift. High system level EMC performance enhance reliability and stability of use.

The NSi814x has a default output status when VDDIN is unready and VDDOUT is ready as shown in Table 4.1, which helps for diagnosis when power is missing at the transmitter side. The output B follows the same status with the input A within 1us after powering up.

# NSi8140/NSi8141/NSi8142

Table 4.1 Output status vs. power status

Input	EN <sub>x</sub>	VDD1 status	VDD2 status	Output	Comment
H	H or NC	Ready	Ready	H	Normal operation.
L	H or NC	Ready	Ready	L	
X	L	Ready	Ready	Z	Output Disabled, the output is high impedance
X	H or NC	Unready	Ready	L H	The output follows the same status with the input within 60us after input side VDD1 is powered on.
X	L	Unready	Ready	Z	Output Disabled, the output is high impedance
X	X	Ready	Unready	X	The output follows the same status with the input within 60us after output side VDD2 is powered on.

## 5.0 APPLICATION NOTE

### 5.1. PCB LAYOUT

The NSi814x requires a 0.1 μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the package. Figure 5.1 to Figure 5.2 show the recommended PCB layout, make sure the space under the chip should keep free from planes, traces, pads and via. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω, ±40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

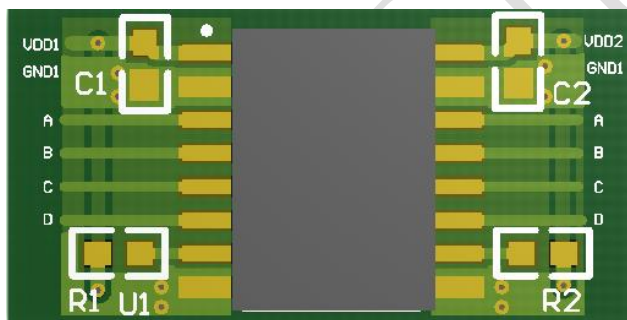


Figure 5.1 Recommended PCB Layout — Top Layer



Figure 5.2 Recommended PCB Layout — Bottom Layer

### 5.2. HIGH SPEED PERFORMANCE

Figure 5.5 shows the eye diagram of NSi814x at 200Mbps data rate output. The result shows a typical measurement on the NSi814x with 350ps p-p jitter.

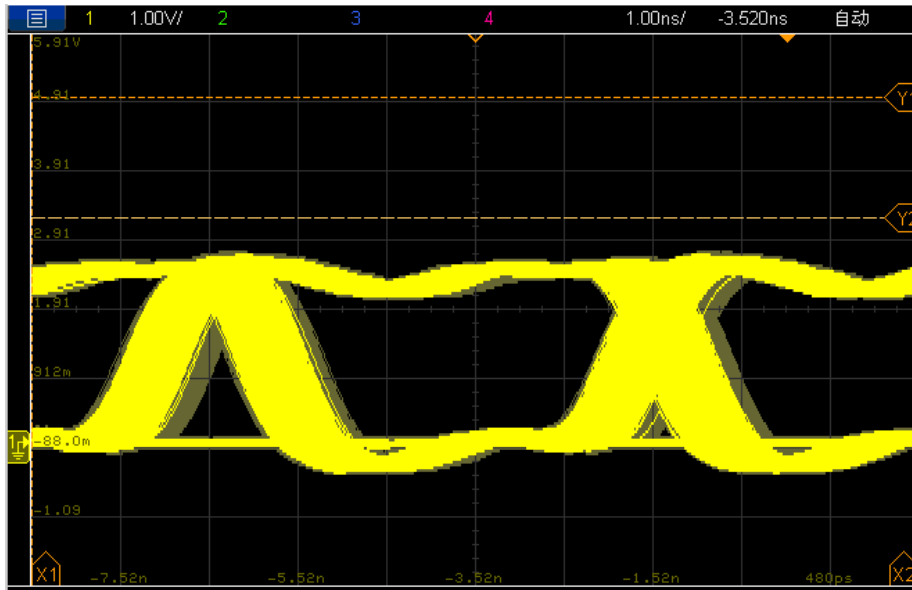


Figure5.3 NSi814x Eye Diagram

### 5.3. TYPICAL SUPPLY CURRENT EQUATIONS

The typical supply current of NSi814x can be calculated using below equations.  $I_{DD1}$  and  $I_{DD2}$  are typical supply currents measured in mA,  $f$  is data rate measured in Mbps,  $C_L$  is the capacitive load measured in pF

#### NSi8140:

$$I_{DD1} = 0.19 * a1 + 1.45 * b1 + 0.82 * c1.$$

$$I_{DD2} = 1.36 + VDD1 * f * C_L * c1 * 10^{-9}$$

When  $a1$  is the channel number of low input at side 1,  $b1$  is the channel number of high input at side 1,  $c1$  is the channel number of switch signal input at side 1.

#### NSi8141:

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD1 * f * C_L * c1 * 10^{-9}$$

When  $b1$  is the channel number of high input at side 1,  $c1$  is the channel number of switch signal input at side 1,  $b2$  is the channel number of high input at side 2,  $c2$  is the channel number of switch signal input at side 2.

#### NSi8142:

$$I_{DD1} = 0.87 + 1.26 * b1 + 0.63 * c1 + VDD1 * f * C_L * c2 * 10^{-9}$$

$$I_{DD2} = 0.87 + 1.26 * b2 + 0.63 * c2 + VDD1 * f * C_L * c1 * 10^{-9}$$

When  $b1$  is the channel number of high input at side 1,  $c1$  is the channel number of switch signal input at side 1,  $b2$  is the channel number of high input at side 2,  $c2$  is the channel number of switch signal input at side 2.

## 6.0 PACKAGE INFORMATION

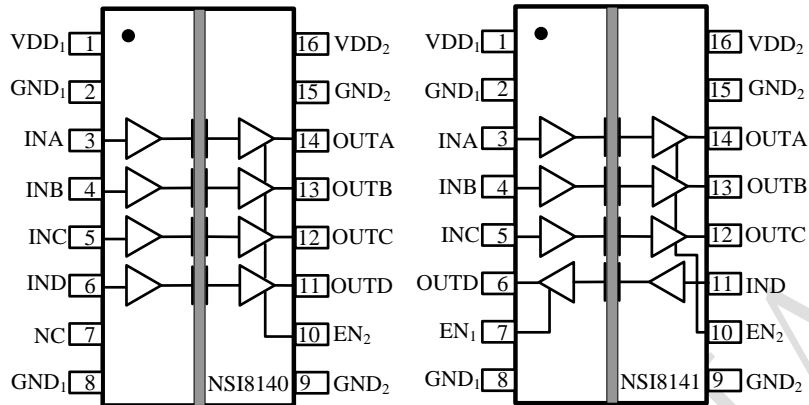


Figure 6.1 NSi8140N Package

Figure 6.2 NSi8141N Package

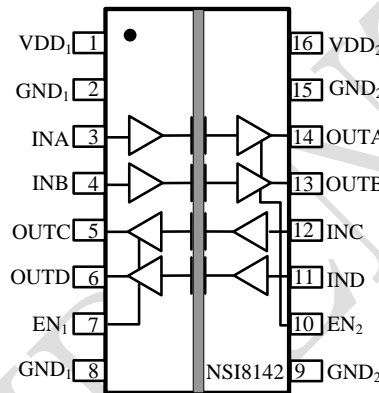


Figure 6.3 NSi8142N Package

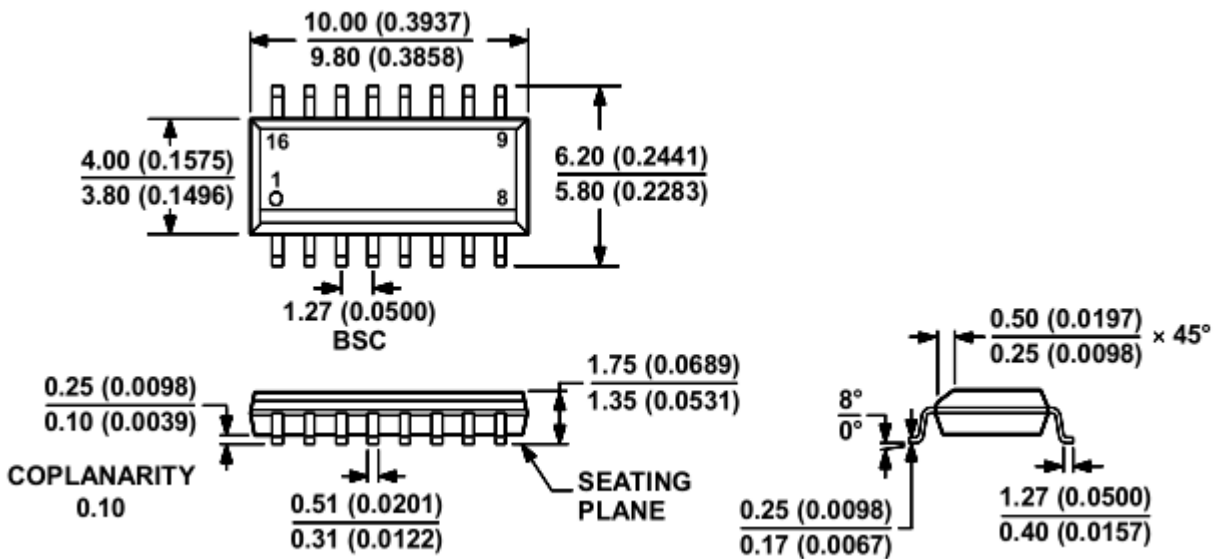


Figure 6.4 NB SOIC16 Package Shape and Dimension in millimeters (inches)

Table 6.1 NSi8140N/ NSi8141N/ NSi8142N Pin Configuration and Description



# NSi8140/NSi8141/NSi8142

<i>NSi8140N</i> PIN NO.	<i>NSi8141N</i> PIN NO.	<i>NSi8142N</i> PIN NO.	<i>SYMBOL</i>	<i>FUNCTION</i>
1	1	1	VDD <sub>1</sub>	Power Supply for Isolator Side 1
2	2	2	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
3	3	3	INA	Logic Input A
4	4	4	INB	Logic Input B
5	5	12	INC	Logic Input C
6	11	11	IND	Logic Input D
7	7	7	NC/ EN <sub>1</sub>	No Connection. or Output Enable 1. Active high logic input. When EN <sub>1</sub> is high or NC, the output of Side 1 are enabled. When EN <sub>1</sub> is low, the output of Side 1 are disabled to high impedance state.
8	8	8	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
9	9	9	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2
10	10	10	EN <sub>2</sub>	Output Enable 2. Active high logic input. When EN <sub>2</sub> is high or NC, the output of Side 2 are enabled. When EN <sub>2</sub> is low, the output of Side 2 are disabled to high impedance state.
11	6	6	OUTD	Logic Output D
12	12	5	OUTC	Logic Output C
13	13	13	OUTB	Logic Output B
14	14	14	OUTA	Logic Output A
15	15	15	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2
16	16	16	VDD <sub>2</sub>	Power Supply for Isolator Side 2

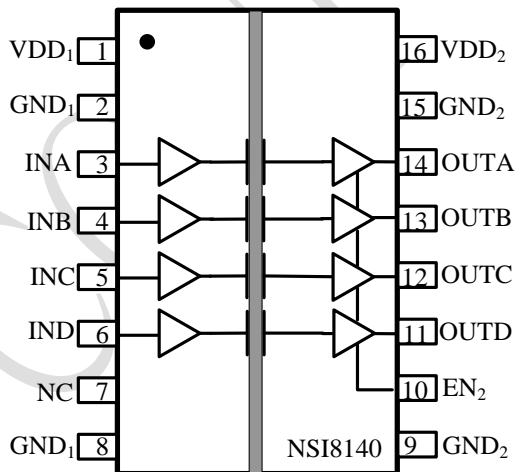


Figure 6.5 NSi8140W Package

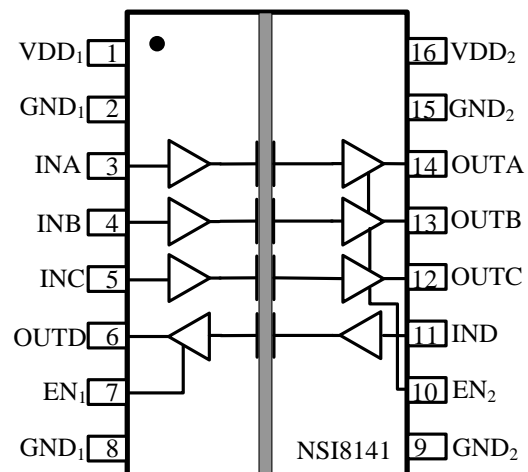


Figure 6.6 NSi8141W Package

# NSi8140/NSi8141/NSi8142

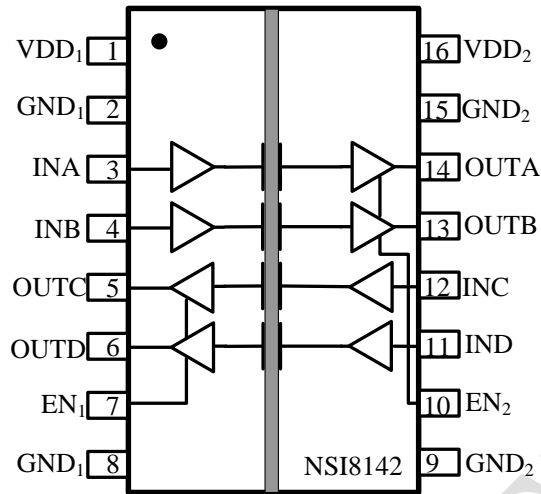


Figure 6.7 NSi8142W Package

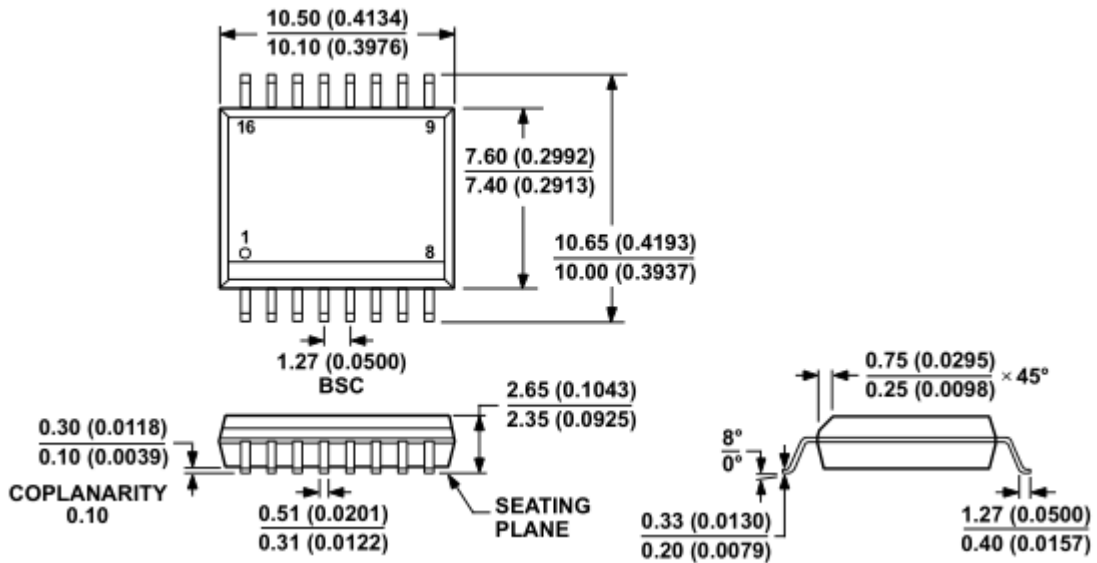


Figure 6.8 WB SOIC16 Package Shape and Dimension in millimeters and (inches)

Table 6.2 NSi8140W/ NSi8141W/ NSi8142W Pin Configuration and Description

NSi8140W PIN NO.	NSi8141W PIN NO.	NSi8142W PIN NO.	SYMBOL	FUNCTION
1	1	1	VDD <sub>1</sub>	Power Supply for Isolator Side 1
2	2	2	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
3	3	3	INA	Logic Input A
4	4	4	INB	Logic Input B
5	5	12	INC	Logic Input C
6	11	11	IND	Logic Input D
7	7	7	NC/ EN <sub>1</sub>	No Connection. or

# NSi8140/NSi8141/NSi8142

				Output Enable 1. Active high logic input. When EN <sub>1</sub> is high or NC, the output of Side 1 are enabled. When EN <sub>1</sub> is low, the output of Side 1 are disabled to high impedance state.
8	8	8	GND <sub>1</sub>	Ground 1, the ground reference for Isolator Side 1
9	9	9	GND <sub>2</sub>	Ground 2, the ground reference for Isolator Side 2
10	10	10	EN <sub>2</sub>	Output Enable 2. Active high logic input. When EN <sub>2</sub> is high or NC, the output of Side 2 are enabled. When EN <sub>2</sub> is low, the output of Side 2 are disabled to high impedance state.
11	6	6	OUTD	Logic Output D
12	12	5	OUTC	Logic Output C
13	13	13	OUTB	Logic Output B
14	14	14	OUTA	Logic Output A
15	15	15	GND2	Ground 2, the ground reference for Isolator Side 2
16	16	16	VDD2	Power Supply for Isolator Side 2

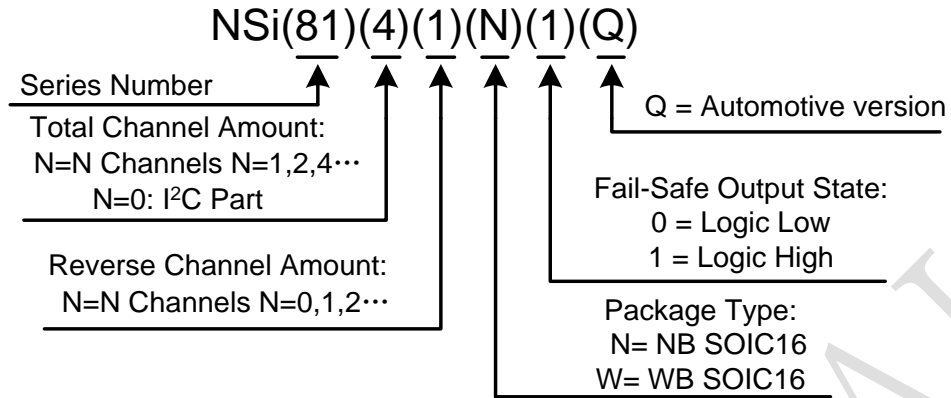
## 7.0 ORDER INFORMATION

Part No.	Isolation Rating(kV)	Number of side 1 inputs	Number of side 2 inputs	Max Data Rate (Mbps)	Default Output State	Temperature	Automotive	Package
NSi8140N0	3.75	4	0	150	Low	-40 to 125°C	NO	NB SOIC16
NSi8140N1	3.75	4	0	150	High	-40 to 125°C	NO	NB SOIC16
NSi8141N0	3.75	3	1	150	Low	-40 to 125°C	NO	NB SOIC16
NSi8141N1	3.75	3	1	150	High	-40 to 125°C	NO	NB SOIC16
NSi8142N0	3.75	2	2	150	Low	-40 to 125°C	NO	NB SOIC16
NSi8142N1	3.75	2	2	150	High	-40 to 125°C	NO	NB SOIC16
NSi8140W0	5	4	0	150	Low	-40 to 125°C	NO	WB SOIC16
NSi8140W1	5	4	0	150	High	-40 to 125°C	NO	WB SOIC16
NSi8141W0	5	3	1	150	Low	-40 to 125°C	NO	WB SOIC16
NSi8141W1	5	3	1	150	High	-40 to 125°C	NO	WB SOIC16
NSi8142W0	5	2	2	150	Low	-40 to 125°C	NO	WB SOIC16
NSi8142W1	5	2	2	150	High	-40 to 125°C	NO	WB SOIC16
NSi8140W0Q	5	4	0	150	Low	-40 to 125°C	YES	WB SOIC16
NSi8140W1Q	5	4	0	150	High	-40 to 125°C	YES	WB SOIC16
NSi8141W0Q	5	3	1	150	Low	-40 to 125°C	YES	WB SOIC16
NSi8141W1Q	5	3	1	150	High	-40 to 125°C	YES	WB SOIC16
NSi8142W0Q	5	2	2	150	Low	-40 to 125°C	YES	WB SOIC16
NSi8142W1Q	5	2	2	150	High	-40 to 125°C	YES	WB SOIC16

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 ° C according to the JEDEC industry standard classifications and peak solder temperatures.  
All devices are AEC-Q100 qualified.

Part Number Rule:

# NSi8140/NSi8141/NSi8142



## 8.0 REVISION HISTORY

Revision	Description	Date
1.0		2017/11/15
1.1	Add maximum operation current spec.	2018/10/12
1.2	Change to ordering information	2018/12/20