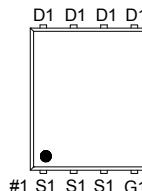
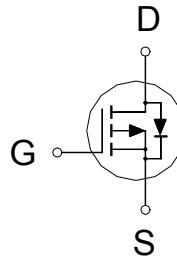


NIKO-SEM**P-Channel Logic Level Enhancement Mode
Field Effect Transistor****PK537BA
PDFN 5x6P
Halogen-Free & Lead-Free****PRODUCT SUMMARY**

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	8mΩ	-38A



G : GATE
D : DRAIN
S : SOURCE

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current	I_D	-38	A
		-24	
		-12	
		-10	
Pulsed Drain Current ¹	I_{DM}	-100	
Avalanche Current	I_{AS}	-37	
Avalanche Energy	E_{AS}	68.4	mJ
Power Dissipation	P_D	20	W
		8.3	
		2.3	
		1.4	
Operating Junction & Storage Temperature Range	T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$R_{\theta JA}$		54	°C / W
Junction-to-Case	$R_{\theta JC}$		6	

¹Pulse width limited by maximum junction temperature.

²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

NIKO-SEM
**P-Channel Logic Level Enhancement Mode
Field Effect Transistor**
PK537BA
PDFN 5x6P
Halogen-Free & Lead-Free
ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1	-1.6	-3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±25V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24V, V _{GS} = 0V			-1	
		V _{DS} = -20V, V _{GS} = 0V, T _J = 125 °C			-10	uA
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -4.5V, I _D = -12A		8.9	14	mΩ
		V _{GS} = -10V, I _D = -12A		5.9	8	
Forward Transconductance ¹	g _f	V _{DS} = -5V, I _D = -12A		40		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		2464		
Output Capacitance	C _{oss}			374		
Reverse Transfer Capacitance	C _{rss}			271		pF
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz		3.9		Ω
Total Gate Charge ²	Q _{g(VGS=-10V)}	V _{DS} = -15V, I _D = -12A		60		
	Q _{g(VGS=-4.5V)}			27.6		
Gate-Source Charge ²	Q _{gs}			8		nC
Gate-Drain Charge ²	Q _{gd}			13.6		
Turn-On Delay Time ²	t _{d(on)}	V _{DS} = -15V, I _D ≈ -12A, V _{GS} = -10V, R _{GS} = 6Ω		22		
Rise Time ²	t _r			25		
Turn-Off Delay Time ²	t _{d(off)}			100		nS
Fall Time ²	t _f			75		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)						
Continuous Current	I _S				-15	A
Forward Voltage ¹	V _{SD}	I _F = -12A, V _{GS} = 0V			-1.3.	V
Reverse Recovery Time	t _{rr}	I _F = -12A, dI _F /dt = 100 A / μS		26		nS
Reverse Recovery Charge	Q _{rr}			13		nC

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

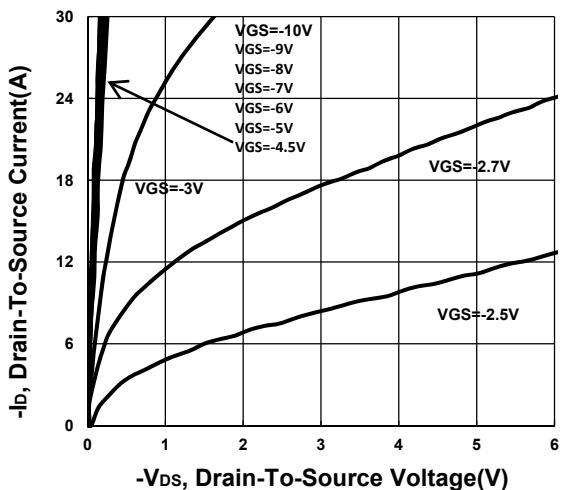
²Independent of operating temperature.

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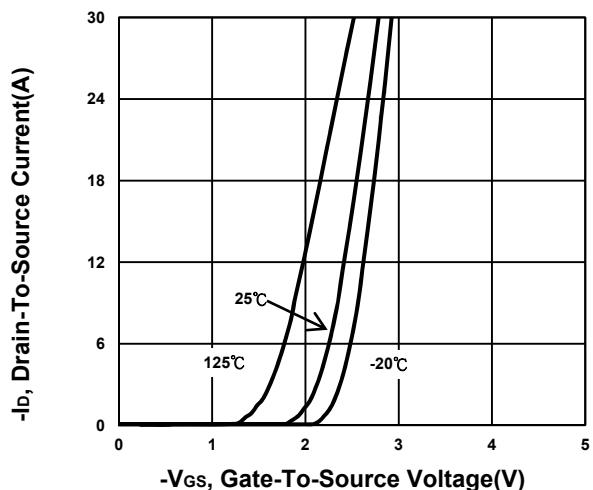
**P-Channel Logic Level Enhancement Mode
Field Effect Transistor**

PK537BA
PDFN 5x6P
Halogen-Free & Lead-Free

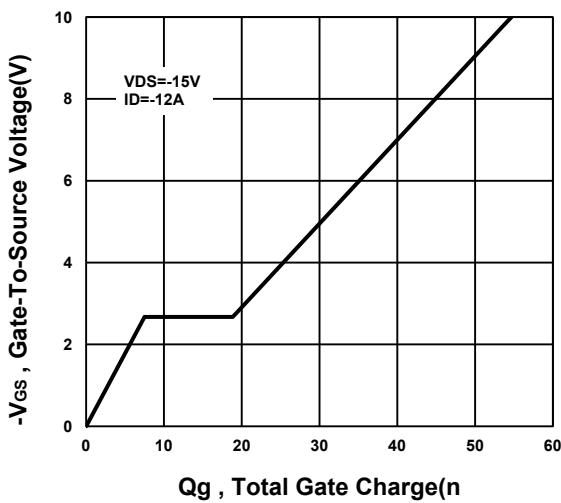
Output Characteristics



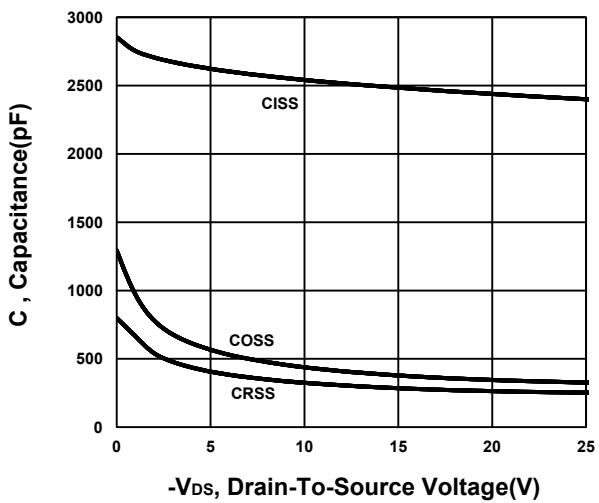
Transfer Characteristics



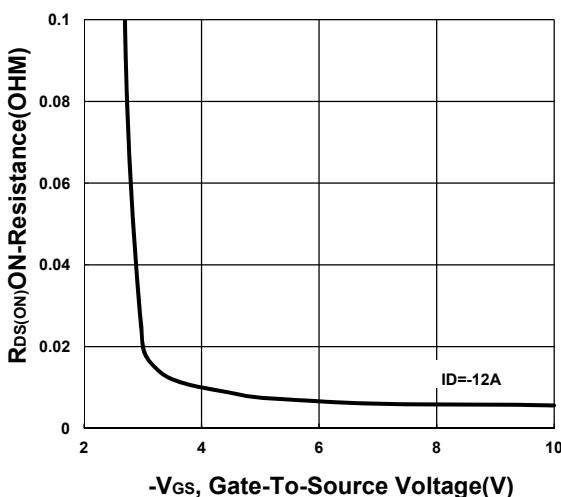
Gate charge Characteristics



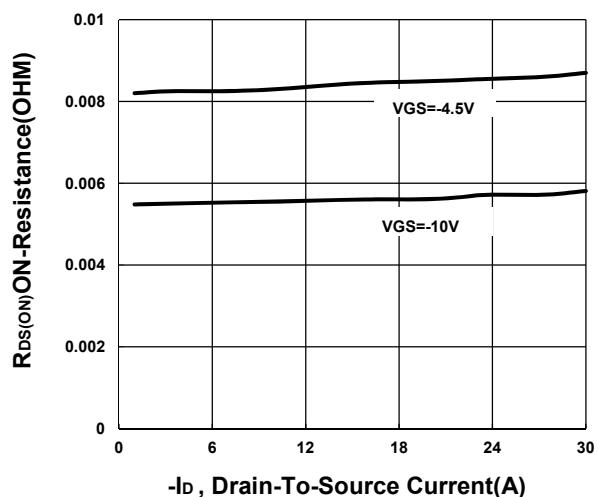
Capacitance Characteristic

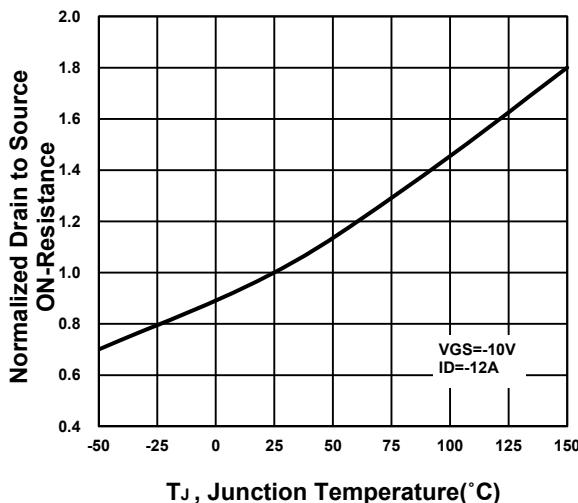
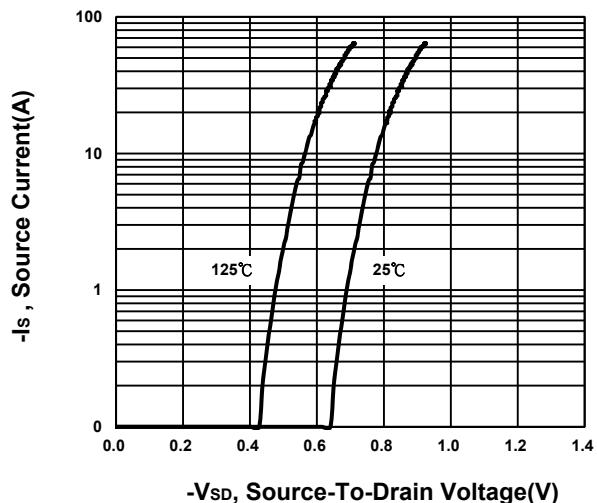
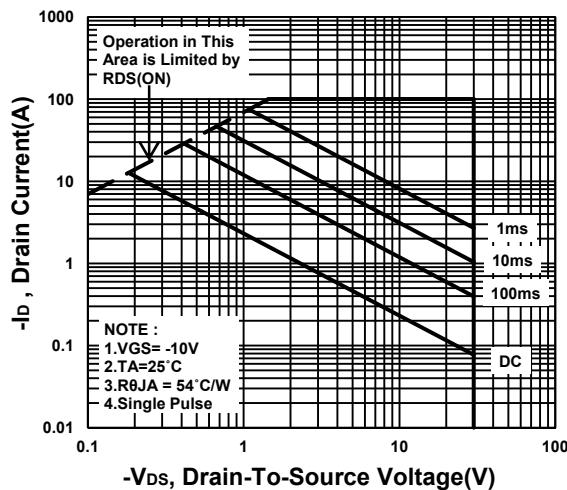
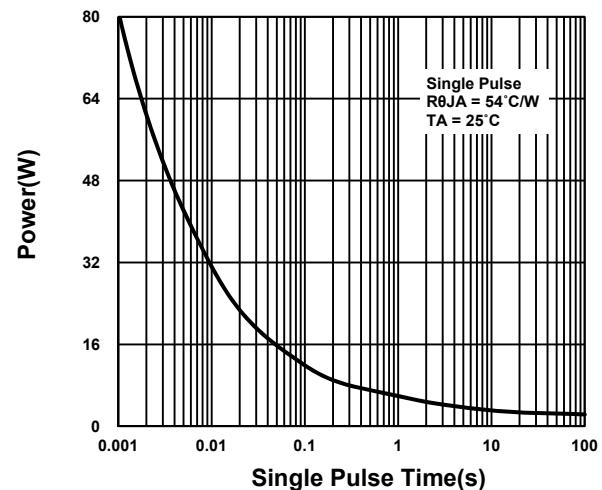
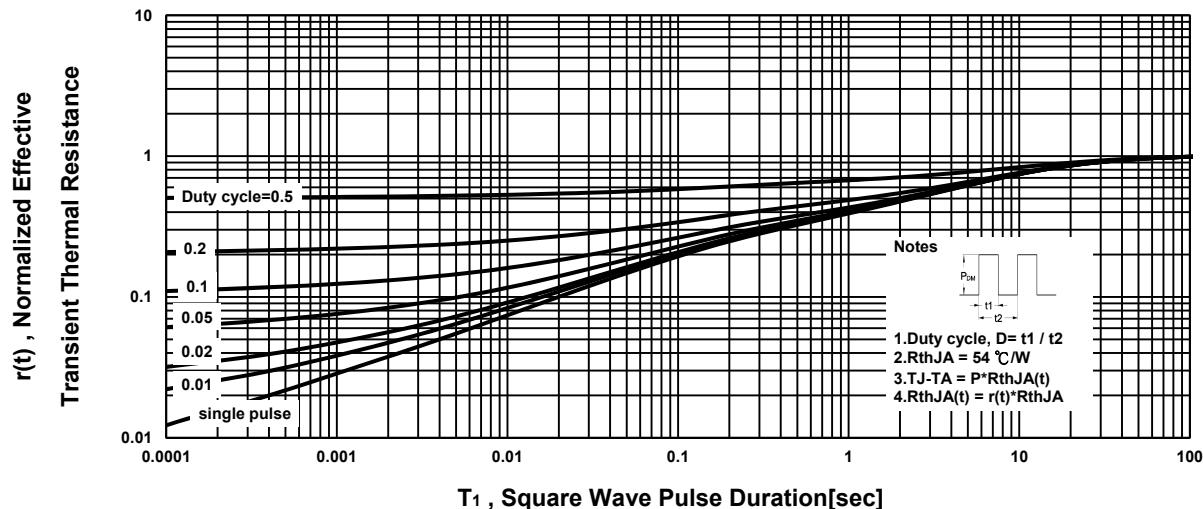


On-Resistance VS Gate-To-Source



On-Resistance VS Drain Current

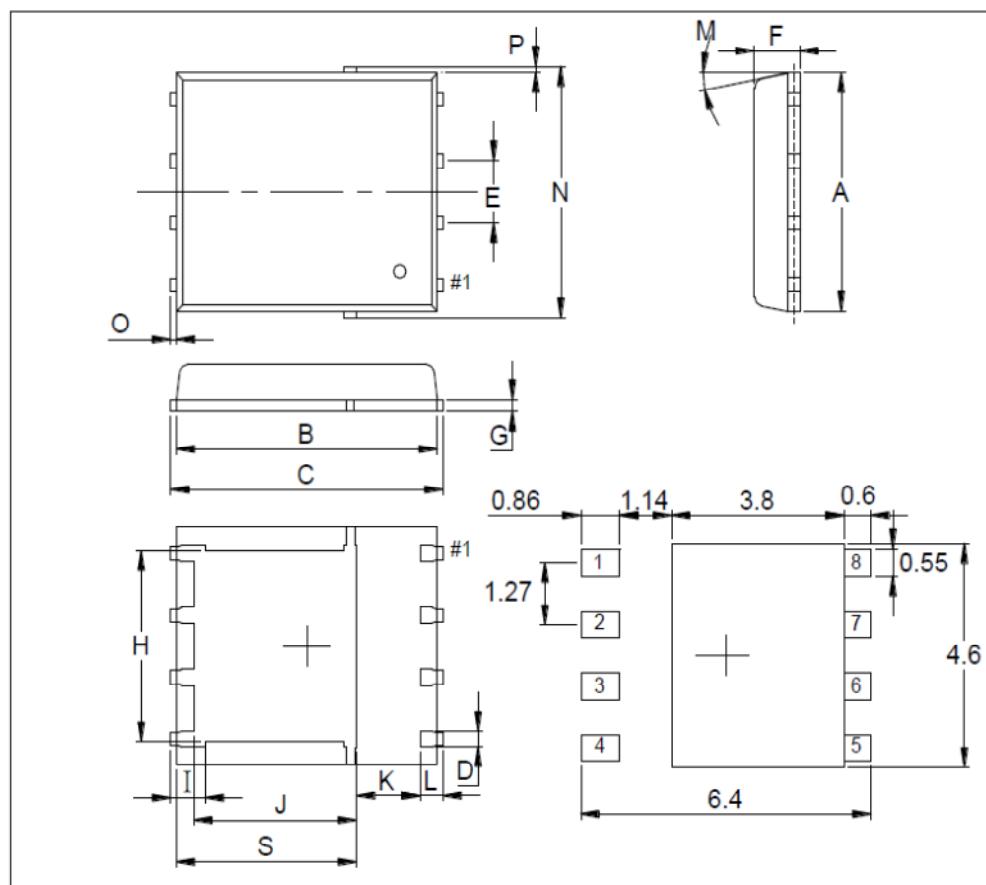


NIKO-SEM**P-Channel Logic Level Enhancement Mode
Field Effect Transistor****PK537BA
PDFN 5x6P
Halogen-Free & Lead-Free****On-Resistance VS Temperature****Source-Drain Diode Forward Voltage****Safe Operating Area****Single Pulse Maximum Power Dissipation****Transient Thermal Response Curve**

Package Dimension

PDFN 5x6P MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8		5.15	J	3.34		3.9
B	5.42		5.9	K	0.9		
C	5.9		6.35	L	0.38		0.711
D	0.3		0.51	M	0°		12°
E	1.17	1.27	1.37	N	4.8		5.4
F	0.8	1	1.2	O	0.05		0.36
G	0.15		0.35	P	0.05		0.25
H	3.67		4.31	S	3.73		4.19
I	0.38		0.71				



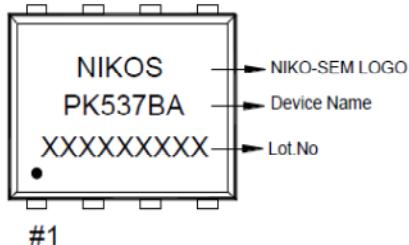
NIKO-SEM

**P-Channel Logic Level Enhancement Mode
Field Effect Transistor**

**PK537BA
PDFN 5x6P
Halogen-Free & Lead-Free**

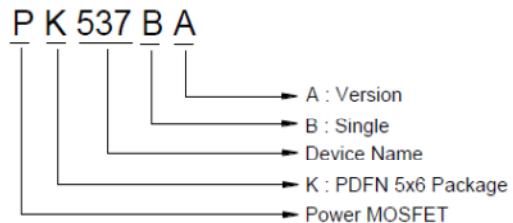
Marking Information:(Please see the corresponding data sheet)

1.零件Marking 文字面說明

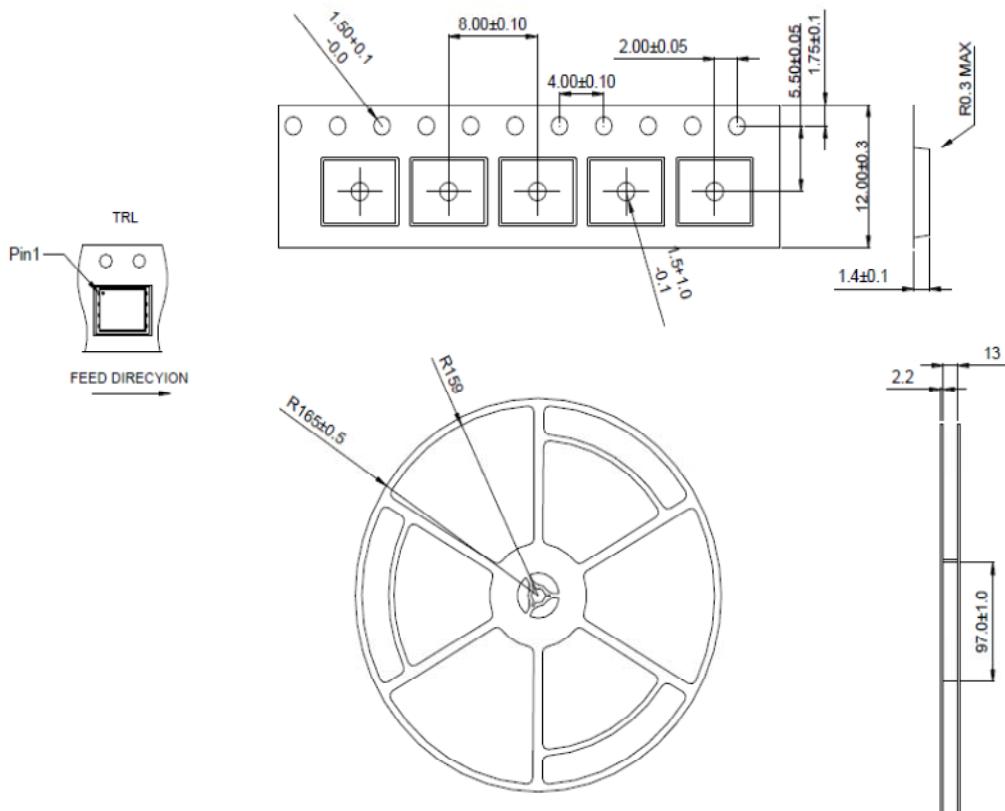


#1

2.零件 Part number 說明



Tape&Reel Information:3000pcs/Reel



附註:All Dimension in milimeter

NIKO-SEM

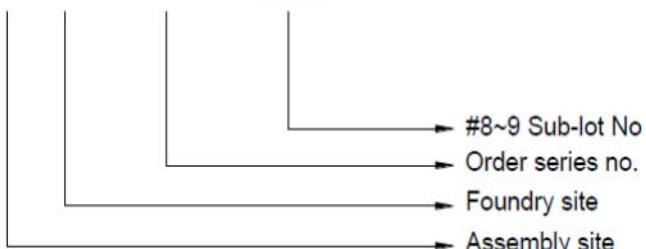
**P-Channel Logic Level Enhancement Mode
Field Effect Transistor**

**PK537BA
PDFN 5x6P
Halogen-Free & Lead-Free**

Lot.No. & Date Code rule

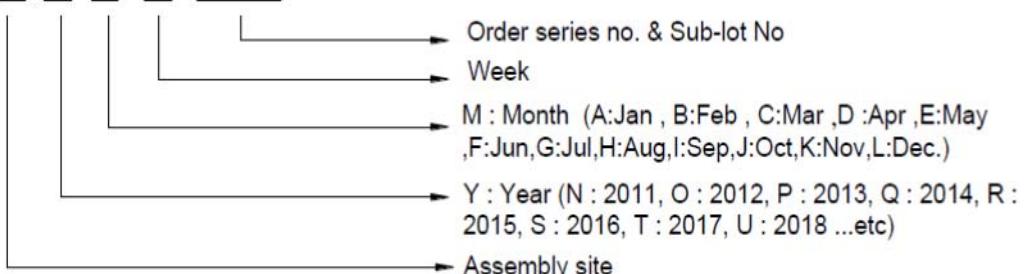
1.LOT.NO.

M N 15M21 03



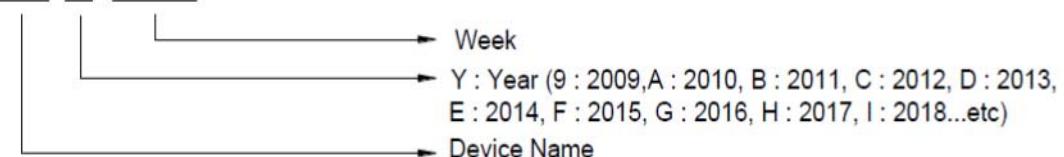
2.Date Code

D Y M X XXX



3.Date Code (for Small package)

XX Y WW



NIKO-SEM**P-Channel Logic Level Enhancement Mode
Field Effect Transistor****PK537BA
PDFN 5x6P
Halogen-Free & Lead-Free****Label rule**

標籤內容 (Label content)



1	Label Size	30 * 90 mm		
2	Font style	Times New Roman or Arial (或可區分英文”O”和數字”0”，”G 和”Q”的字型即可) (Or any font capable of being distinguished for Letter O and digital 0, and for G and Q))		
3	NIKO-SEM	Height: 4 mm		
4	NIKO SEMICONDUCTOR CO., LTD.	Height: 1 mm		
5	Package	Height: 2 mm		
6	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12		
7	Device	Height: 3 mm (Max: 16 Digit) Device Name not including Rev.		
8	Lot	Height: 3 mm (Max: 9 Digit) Sub lot		
9	D/C	Height: 3 mm (Max: 7 Digit)		
10	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed		
11	Pb Free label		Diameter: 1 cm Font color: Black Font style: Arial	bottom color: Green
12	Halogen Free label		Diameter: 1 cm Font color: Black Font style: Arial	bottom color: Green
13	Scan info	Device / Lot / D/C / QTY , Insert “ / ” between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least		