TCA9545A Low Voltage 4-channel I²C and SMbus Switch With Interrupt Logic and Reset Functions

1 Features

- 1-of-4 Bidirectional Translating Switches
- I²C Bus and SMBus Compatible
- Four Active-Low Interrupt Inputs
- Active-Low Interrupt Output
- Active-Low Reset Input
- Two Address Terminals, Allowing up to Four Devices on the I²C Bus
- Channel Selection via I²C Bus, in Any Combination
- Power-Up With All Switch Channels Deselected
- Low R_{ON} Switches
- Allows Voltage-Level Translation Between 1.8-V, 2.5-V, 3.3-V, and 5-V Buses
- No Glitch on Power-Up
- Supports Hot Insertion
- Low Standby Current
- Operating Power-Supply Voltage Range of 1.65 V to 5.5 V
- 5.5 V Tolerant Inputs
- 0 to 400-kHz Clock Frequency
- Latch-Up Performance Exceeds 100 mA per JESD 78
- ESD Protection Exceeds JESD 22
  - 4000-V Human-Body Model (A114-A)
  - 1500-V Charged-Device Model (C101)

2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products With I²C Slave Address Conflicts (e.g. Multiple, Identical Temp Sensors)

3 Description

The TCA9545A is a quad bidirectional translating switch controlled via the I²C bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register. Four interrupt inputs (INT3–INT0), one for each of the downstream pairs, are provided. One interrupt ($\overline{INT}$) output acts as an AND of the four interrupt inputs.

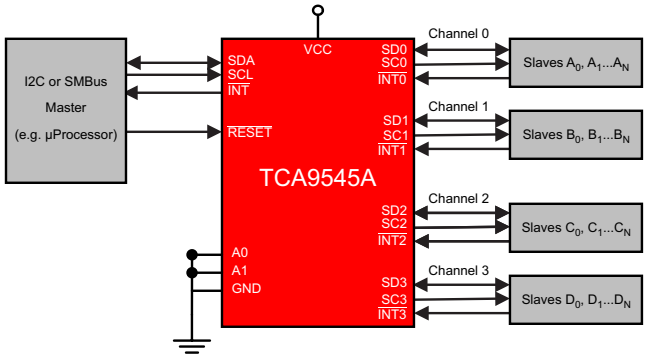
An active-low reset ($\overline{RESET}$) input allows the TCA9545A to recover from a situation in which one of the downstream I²C buses is stuck in a low state. Pulling $\overline{RESET}$ low resets the I²C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the VCC terminal can be used to limit the maximum high voltage, which will be passed by the TCA9545A. This allows the use of different bus voltages on each pair, so that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts, without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O terminals are 5.5 V tolerant.

Device Information

ORDER NUMBER	PACKAGE	BODY SIZE
TCA9545APWR	TSSOP (20)	6,5mm x 4,4mm

4 Simplified Application Diagram



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5 Revision History

Changes from Revision A (March 2014) to Revision B **Page**

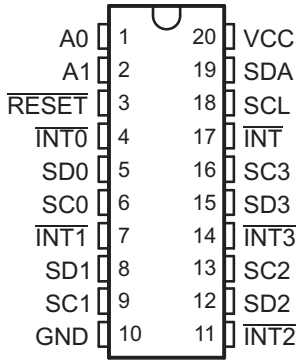
- Updated pin names in graphics. ... 1

Changes from Original (January 2014) to Revision A **Page**

- Updated PREVIEW document to full version. ... 1

6 Terminal Configuration and Functions

PW PACKAGE
(TOP VIEW)



Terminal Functions

NO.		DESCRIPTION
PW	NAME	
1	A0	Address input 0. Connect directly to V_{CC} or ground.
2	A1	Address input 1. Connect directly to V_{CC} or ground.
3	$\overline{\text{RESET}}$	Active-low reset input. Connect to V_{CC} or V_{DPUM}(1) through a pull-up resistor if not used.
4	$\overline{\text{INT0}}$	Active-low interrupt input 0. Connect to V_{DPU0}(1) through a pull-up resistor.
5	SD0	Serial data 0. Connect to V_{DPU0} (1) through a pul-up resistor.
6	SC0	Serial clock 0. Connect to V_{DPU0} (1) through a pull-up resistor.
7	$\overline{\text{INT1}}$	Active-low interrupt input 1. Connect to V_{DPU1}(1) through a pull-up resistor.
8	SD1	Serial data 1. Connect to V_{DPU1}(1) through a pull-up resistor.
9	SC1	Serial clock 1. Connect to V_{DPU1}(1) through a pull-up resistor.
10	GND	Ground
11	$\overline{\text{INT2}}$	Active-low interrupt input 2. Connect to V_{DPU2}(1) through a pull-up resistor.
12	SD2	Serial data 2. Connect to V_{DPU2}(1) through a pull-up resistor.
13	SC2	Serial clock 2. Connect to V_{DPU2}(1) through a pull-up resistor.
14	$\overline{\text{INT3}}$	Active-low interrupt input 3. Connect to V_{DPU3}(1) through a pull-up resistor.
15	SD3	Serial data 3. Connect to V_{DPU3}(1) through a pull-up resistor.
16	SC3	Serial clock 3. Connect to V_{DPU3}(1) through a pull-up resistor.
17	$\overline{\text{INT}}$	Active-low interrupt output. Connect to V_{DPUM}(1) through a pull-up resistor.
18	SCL	Serial clock line. Connect to V_{DPUM}(1) through a pull-up resistor.
19	SDA	Serial data line. Connect to V_{DPUM}(1) through a pull-up resistor.
20	VCC	Supply power

(1) V_{DPUX} is the pull-up reference voltage for the associated data line. V_{DPUM} is the master I^2C master reference voltage and V_{DPU0}–V_{DPU3} are the slave channel reference voltages.

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	7	V
V_I	Input voltage range(2)	–0.5	7	V
I_I	Input current		±20	mA
I_O	Output current		±25	mA
	Continuous current through V_{CC}		±100	mA
	Continuous current through GND		±100	mA
P_{tot}	Total power dissipation		400	mW
T_A	Operating free-air temperature range	–40	85	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 Handling Ratings

PARAMETER	DEFINITION		MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
V_{ESD}(1)	Human Body Model (HBM), ESD Stress Voltage(2)	All Terminals		4	kV
	Charged Device Model (CDM) ESD Stress Voltage(3)	All Terminals		1500	V

(1) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by assembly line electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. *Terminals listed as 250 V may actually have higher performance.*
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. *Terminals listed as 250 V may actually have higher performance.*

7.3 Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CC}	6	V
		A1, A0, $\overline{INT3}$–$\overline{INT0}$, $\overline{RESET}$	0.7 × V_{CC}	V_{CC} + 0.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	0.3 × V_{CC}	V
		A1, A0, $\overline{INT3}$–$\overline{INT0}$, $\overline{RESET}$	–0.5	0.3 × V_{CC}	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

7.4 Thermal Information

THERMAL METRIC(1)		TCA9545A PW 20 TERMINALS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	115.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	48.7	
θ_{JB}	Junction-to-board thermal resistance	66.4	
ψ_{JT}	Junction-to-top characterization parameter	6.5	
ψ_{JB}	Junction-to-board characterization parameter	65.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{PORR}	Power-on reset voltage, VCC rising		No load, $V_I = V_{CC}$ or GND(2)			1.2	1.5	V
V_{PORF}	Power-on reset voltage, VCC falling(3)		No load, $V_I = V_{CC}$ or GND(2)		0.8	1		V
V_{pass}	Switch output voltage		$V_{SWin} = V_{CC}$, $I_{SWout} = -100$ µA	5 V		3.6		V
				4.5 V to 5.5 V	2.6		4.5	
				3.3 V		1.9		
				3 V to 3.6 V	1.6		2.8	
				2.5 V		1.4		
				2.3 V to 2.7 V	1.0		1.8	
				1.8 V		0.8		
				1.65 V to 1.95 V	0.5		1.1	
I_{OH}	$\overline{INT}$		$V_O = V_{CC}$	1.65 V to 5.5 V			10	µA
I_{OL}	SDA		V_{OL} = 0.4 V	1.65 V to 5.5 V	3	7		mA
			V_{OL} = 0.6 V		6	10		
	$\overline{INT}$		V_{OL} = 0.4 V		3			
I_I	SCL, SDA		$V_I = V_{CC}$ or GND(2)	1.65 V to 5.5 V			±1	µA
	SC3–SC0, SD3–SD0						±1	
	A1, A0						±1	
	$\overline{INT3}$–$\overline{INT0}$						±1	
	$\overline{RESET}$						±1	
I_{CC}	Operating mode	f_{SCL} = 400 kHz	$V_I = V_{CC}$ or GND(2), I_O = 0, $t_{r,max}$ = 300 ns	5.5 V		50		µA
				3.6 V		20		
				2.7 V		11		
				1.65 V		6		
		f_{SCL} = 100 kHz	$V_I = V_{CC}$ or GND(2), I_O = 0, $t_{r,max}$ = 1 µs	5.5 V		35		
				3.6 V		14		
				2.7 V		5		
				1.65 V		2		
	Standby mode	Low inputs	V_I = GND(2), I_O = 0	5.5 V		1.6	2	
				3.6 V		1.0	1.3	
				2.7 V		0.7	1.1	
				1.65 V		0.4	0.55	
		High inputs	$V_I = V_{CC}$, I_O = 0	5.5 V		1.6	2	
				3.6 V		1.0	1.3	
				2.7 V		0.7	1.1	
				1.65 V		0.4	0.55	
ΔI_{CC}	Supply-current change	$\overline{INT3}$–$\overline{INT0}$	One $\overline{INT3}$–$\overline{INT0}$ input at 0.6 V, Other inputs at V_{CC} or GND(2)	1.65 V to 5.5 V		3	20	µA
			One $\overline{INT3}$–$\overline{INT0}$ input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND(2)			3	20	
		SCL, SDA	SCL or SDA input at 0.6 V, Other inputs at V_{CC} or GND(2)			2	15	
			SCL or SDA input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND(2)			2	15	

(1) All typical values are at nominal supply voltage (V_{CC} = 1.8 V, 2.5 V, 3.3 V, or 5 V), T_A = 25°C.
(2) $\overline{RESET}$ = V_{CC} (held high) when all other input voltages, V_I = GND
(3) The power-on reset circuit resets the I^2C bus logic with $V_{CC} < V_{PORF}$.

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
C_i	A1, A0	$V_I = V_{CC}$ or GND(2)		1.65 V to 5.5 V		4.5	6	pF
	$\overline{INT3}$–$\overline{INT0}$					4.5	6	
	$\overline{RESET}$					4.5	5.5	
$C_{io(OFF)}$ (4)	SCL, SDA	$V_I = V_{CC}$ or GND(2)	Switch OFF	1.65 V to 5.5 V		15	19	pF
	SC3–SC0, SD3–SD0					6	8	
R_{ON}	Switch on-state resistance	V_O = 0.4 V	I_O = 15 mA	4.5 V to 5.5 V	4	10	16	Ω
				3 V to 3.6 V	5	13	20	
		V_O = 0.4 V	I_O = 10 mA	2.3 V to 2.7 V	7	16	45	
				1.65 V to 1.95 V	10	25	70	

(4) $C_{io(ON)}$ depends on the device capacitance and load that is downstream from the device.

7.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

			STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency			100		400	kHz
t_{sch}	I²C clock high time		4		0.6		µs
t_{scl}	I²C clock low time		4.7		1.3		µs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial-data hold time		0(1)		0(1)		µs
t_{icr}	I²C input rise time			1000	20 + 0.1C_b (2)	300	ns
t_{icf}	I²C input fall time			300	20 + 0.1C_b (2)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	20 + 0.1C_b (2)	300	ns
t_{buf}	I²C bus free time between stop and start		4.7		1.3		µs
t_{sts}	I²C start or repeated start condition setup		4.7		0.6		µs
t_{sth}	I²C start or repeated start condition hold		4		0.6		µs
t_{sps}	I²C stop condition setup		4		0.6		µs
$t_{vdL(Data)}$	Valid-data time (high to low)(3)	SCL low to SDA output low valid		1		1	µs
$t_{vdH(Data)}$	Valid-data time (low to high)(3)	SCL low to SDA output high valid		0.6		0.6	µs
$t_{vd(ack)}$	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1		1	µs
C_b	I²C bus capacitive load			400		400	pF

(1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the V_{IH} min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.
(2) C_b = total bus capacitance of one bus line in pF
(3) Data taken using a 1-kΩ pullup resistor and 50-pF load (see Figure 5)

7.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted) (see Figure 7)

PARAMETER			FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd} (1)	Propagation delay time	R_{ON} = 20 Ω, C_L = 15 pF	SDA or SCL	SDn or SCn		0.3	ns
		R_{ON} = 20 Ω, C_L = 50 pF				1	
t_{iv}	Interrupt valid time (2)		$\overline{INTn}$	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time (2)		$\overline{INTn}$	$\overline{INT}$		2	µs

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
(2) Data taken using a 4.7-kΩ pullup resistor and 100-pF load (see Figure 7)

7.8 Interrupt and Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7)

PARAMETER		MIN	MAX	UNIT
t_{PWRL}	Low-level pulse duration rejection of $\overline{INTn}$ inputs	1		µs
t_{PWRH}	High-level pulse duration rejection of $\overline{INTn}$ inputs	0.5		µs
t_{WL}	Pulse duration, $\overline{RESET}$ low	6		ns
t_{rst} (1)	$\overline{RESET}$ time (SDA clear)		500	ns
$t_{REC(STA)}$	Recovery time from $\overline{RESET}$ to start	0		ns

(1) t_{rst} is the propagation delay measured from the time the $\overline{RESET}$ terminal is first asserted low to the time the SDA terminal is asserted high, signaling a stop condition. It must be a minimum of t_{WL}.

7.9 Typical Characteristics

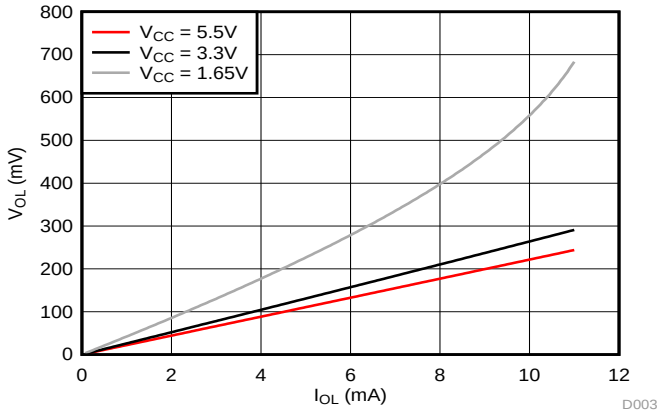


Figure 1. SDA Output Low Voltage (V_{OL}) vs Load Current (I_{OL}) at Three V_{CC} Levels

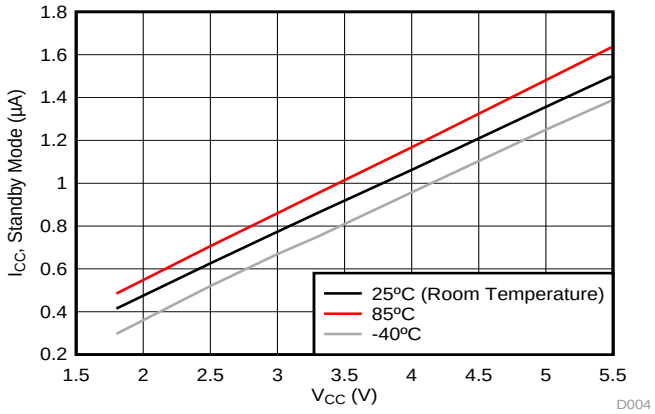


Figure 2. Standby Current (I_{CC}) vs Supply Voltage (V_{CC}) at Three Temperature Points

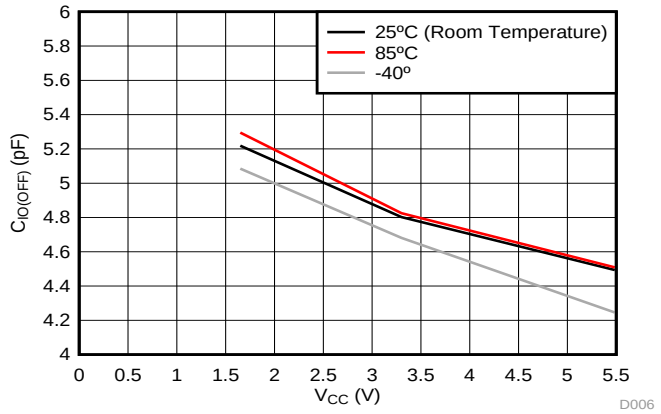


Figure 3. Slave channel (SCn/SDn) capacitance ($C_{io(OFF)}$) vs. Supply Voltage (V_{CC}) at Three Temperature Points

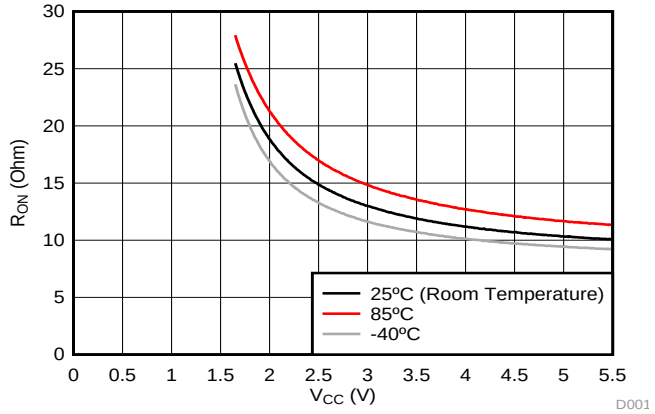
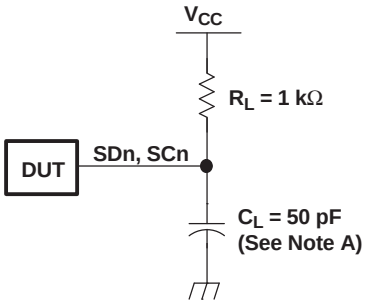
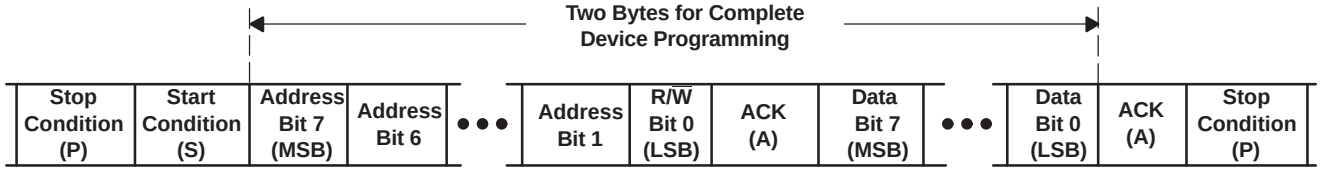


Figure 4. ON-Resistance (R_{ON}) vs Supply Voltage (V_{CC}) at Three Temperatures

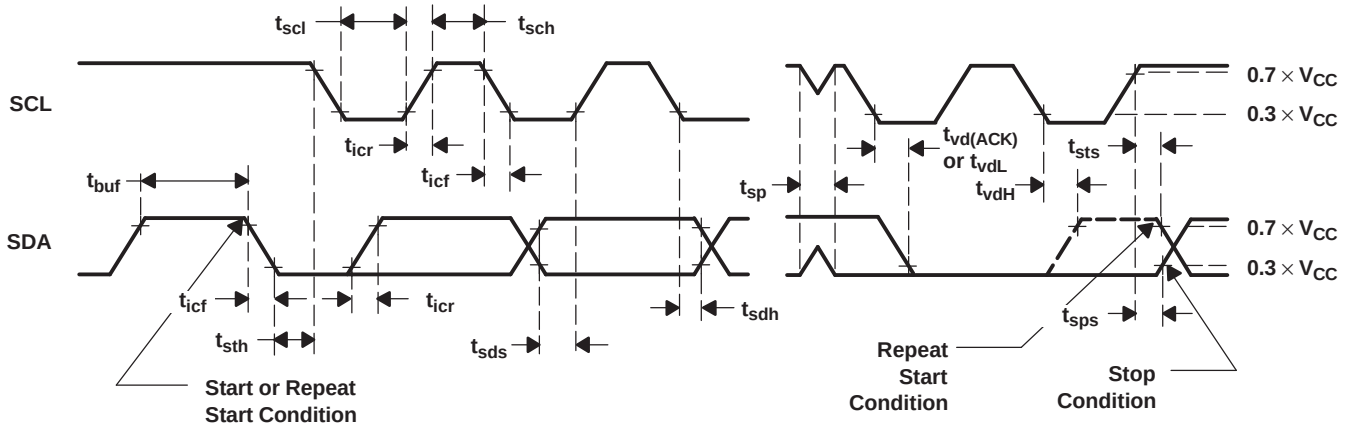
8 Parameter Measurement Information



I²C PORT LOAD CONFIGURATION



BYTE	DESCRIPTION
1	I²C address + R/W
2	Control register data



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 30 ns.

C. The outputs are measured one at a time, with one transition per measurement.

Figure 5. I²C Interface Load Circuit, Byte Descriptions, and Voltage Waveforms

Parameter Measurement Information (continued)

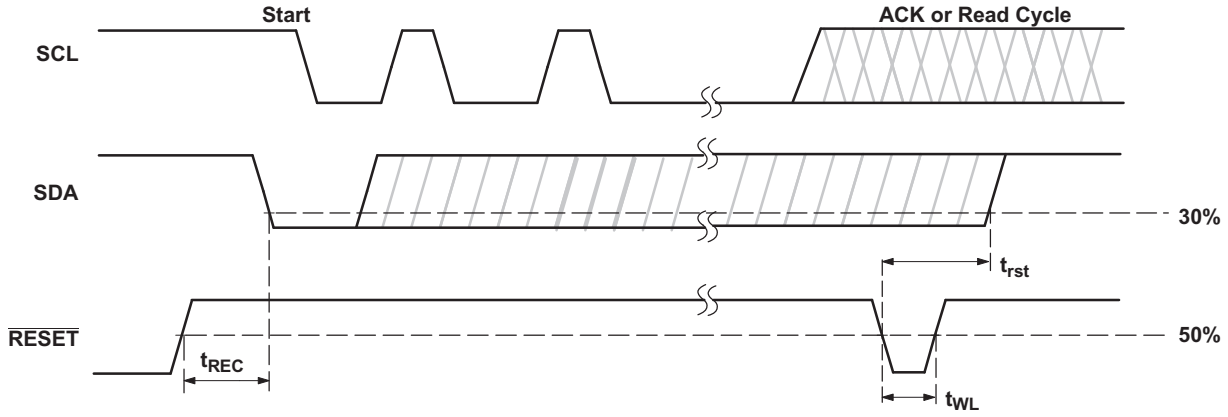
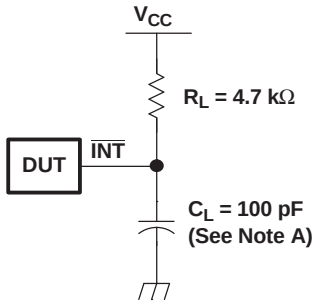
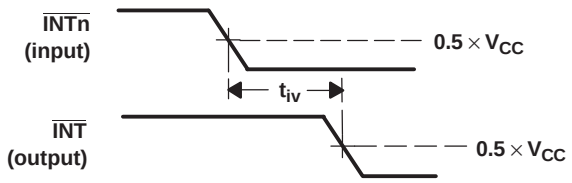


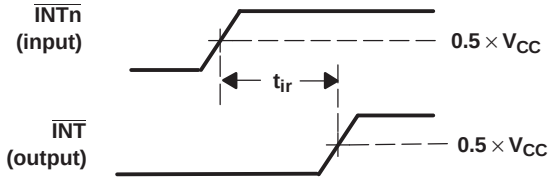
Figure 6. Reset Timing



INTERRUPT LOAD CONFIGURATION



VOLTAGE WAVEFORMS (t_{iv})



VOLTAGE WAVEFORMS (t_{ir})

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 30 ns.

Figure 7. Interrupt Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

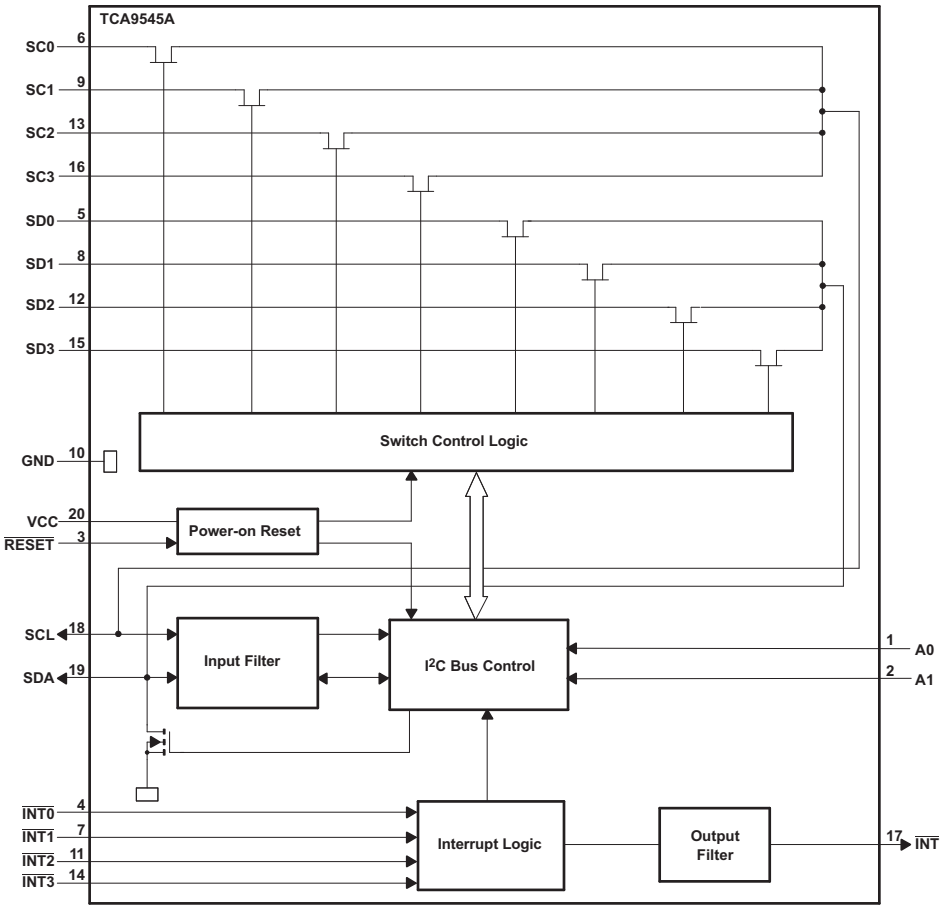
The TCA9545A is a 4-channel, bidirectional translating I^2C switch. The master SCL/SDA signal pair is directed to four channels of slave devices, SC0/SD0-SC3/SD3. Any individual downstream channel can be selected as well as any combination of the four channels. The TCA9545A also supports interrupt signals in order for the master to detect an interrupt on the $\overline{INT}$ output terminal that can result from any of the slave devices connected to the $\overline{INT3}$-$\overline{INT0}$ input terminals.

The device offers an active-low $\overline{RESET}$ input which resets the state machine and allows the TCA9545A to recover should one of the downstream I^2C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, V_{CC}, also known as a power-on reset (POR). Both the $\overline{RESET}$ function and a POR will cause all channels to be deselected.

The connections of the I^2C data path are controlled by the same I^2C master device that is switched to communicate with multiple I^2C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0 and A1 terminals), a single 8-bit control register is written to or read from to determine the selected channels and state of the interrupts.

The TCA9545A may also be used for voltage translation, allowing the use of different bus voltages on each SCn/SDn pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

9.2 Functional Block Diagram



9.3 Feature Description

The TCA9545A is a 4-channel, bidirectional translating switch for I^2C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The TCA9545A features I^2C control using a single 8-bit control register in which the four least significant bits control the enabling and disabling of the 4 switch channels of I^2C data flow. The TCA9545A also supports interrupt signals for each slave channel and this data is held in the four most significant bits of the control register. Depending on the application, voltage translation of the I^2C bus can also be achieved using the TCA9545A to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I^2C bus enters a fault state, the TCA9545A can be reset to resume normal operation using the $\overline{\text{RESET}}$ pin feature or by a power-on reset which results from cycling power to the device.

9.4 Device Functional Modes

9.4.1 $\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input can be used to recover the TCA9545A from a bus-fault condition. The registers and the I^2C state machine within this device initialize to their default states if this signal is asserted low for a minimum of t_{WL}. All channels also are deselected in this case. $\overline{\text{RESET}}$ must be connected to V_{CC} through a pull-up resistor.

9.4.2 Power-On Reset

When power is applied to VCC, an internal power-on reset holds the TCA9545A in a reset condition until V_{CC} has reached V_{PORR}. At this point, the reset condition is released and the TCA9545A registers and I^2C state machine are initialized to their default states, all zeroes, causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below at least V_{PORF} to reset the device.

9.5 Programming

9.5.1 I^2C Interface

The I^2C bus is for two-way two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer can be initiated only when the bus is not busy.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse, as changes in the data line at this time are interpreted as control signals (see Figure 8).

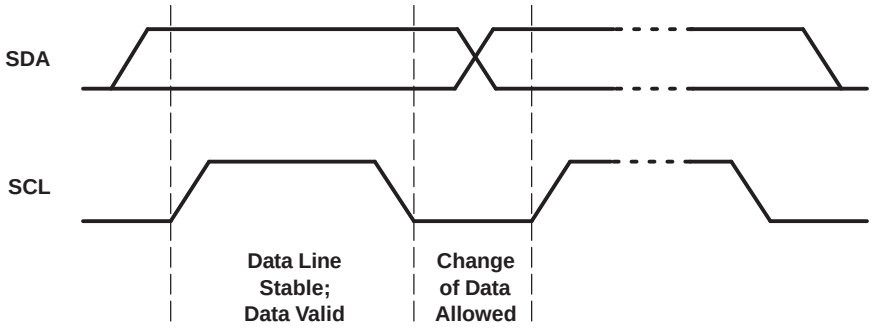


Figure 8. Bit Transfer

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the start condition (S). A low-to-high transition of the data line while the clock is high is defined as the stop condition (P) (see Figure 9).

Programming (continued)

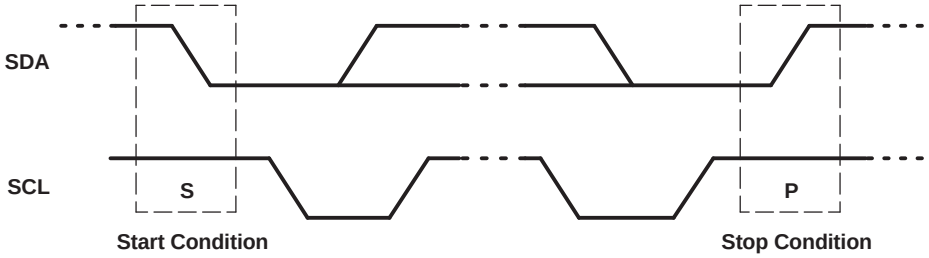


Figure 9. Definition of Start and Stop Conditions

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master, and the devices that are controlled by the master are the slaves (see Figure 10).

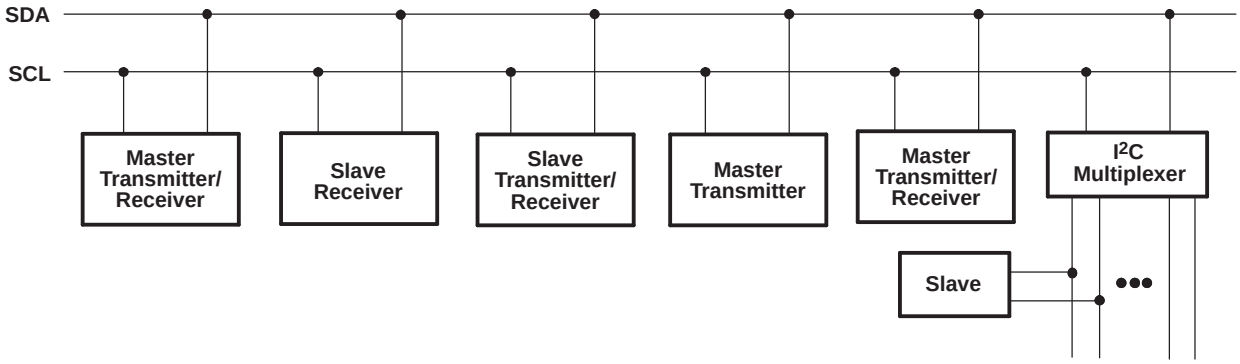


Figure 10. System Configuration

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge (ACK) bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

When a slave receiver is addressed, it must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 11). Setup and hold times must be taken into account.

Programming (continued)

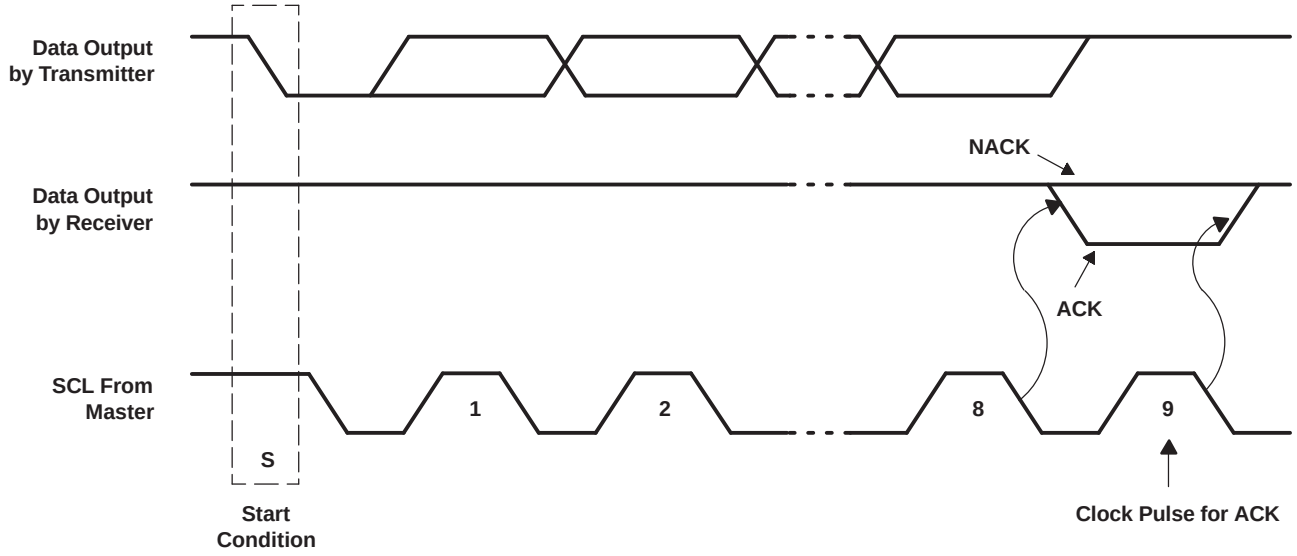


Figure 11. Acknowledgment on the I²C Bus

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

Data is transmitted to the TCA9545A control register using the write mode shown in Figure 12.

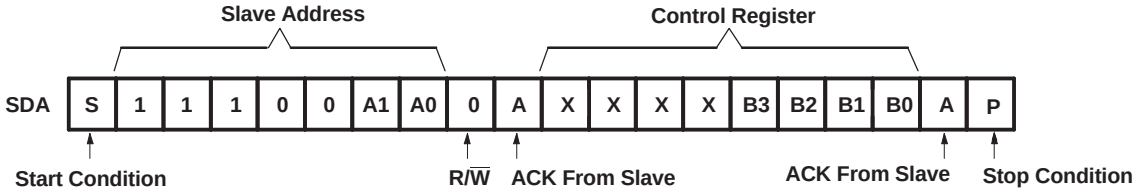


Figure 12. Write Control Register

Data is read from the TCA9545A control register using the read mode shown in Figure 13.

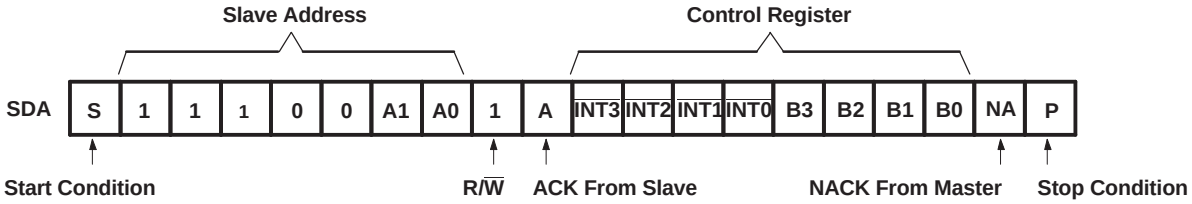


Figure 13. Read Control Register

9.6 Control Register

9.6.1 Device Address

Following a start condition, the bus master must output the address of the slave it is accessing. The address of the TCA9545A is shown in Figure 14. To conserve power, no internal pullup resistors are incorporated on the hardware-selectable address terminals, and they must be pulled high or low.

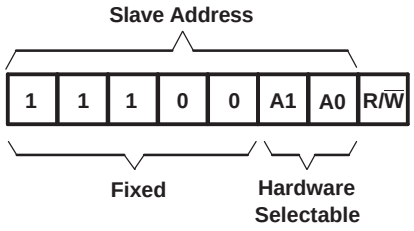


Figure 14. TCA9545A Address

The last bit of the slave address defines the operation to be performed. When set to a logic 1, a read is selected, while a logic 0 selects a write operation.

9.6.2 Control Register Description

Following the successful acknowledgment of the slave address, the bus master sends a byte to the TCA9545A, which is stored in the control register (see Figure 15). If multiple bytes are received by the TCA9545A, it saves the last byte received. This register can be written and read via the I^2C bus.

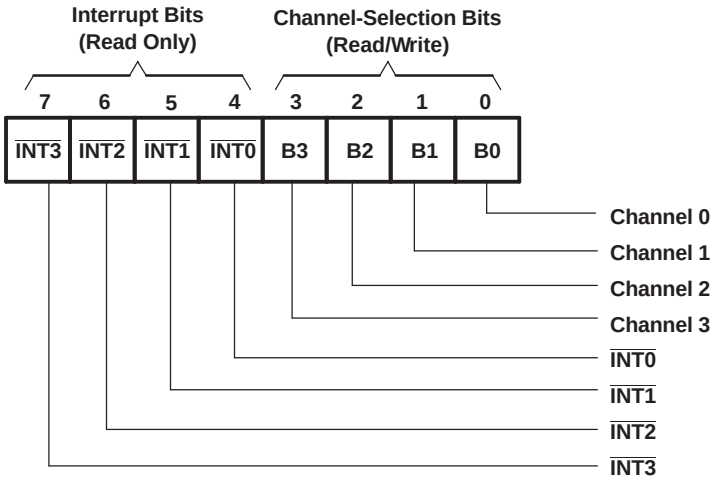


Figure 15. Control Register

9.6.3 Control Register Definition

One or several SCn/SDn downstream pairs, or channels, are selected by the contents of the control register (see Table 1). After the TCA9545A has been addressed, the control register is written. The four LSBs of the control byte are used to determine which channel or channels are to be selected. When a channel is selected, the channel becomes active after a stop condition has been placed on the I^2C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition must occur always right after the acknowledge cycle.

Control Register (continued)

Table 1. Control Register Write (Channel Selection), Control Register Read (Channel Status)(1)

$\overline{INT3}$	$\overline{INT2}$	$\overline{INT1}$	$\overline{INT0}$	B3	B2	B1	B0	COMMAND
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	0	X	Channel 1 disabled
						1		Channel 1 enabled
X	X	X	X	X	0	X	X	Channel 2 disabled
					1			Channel 2 enabled
X	X	X	X	0	X	X	X	Channel 3 disabled
				1				Channel 3 enabled
0	0	0	0	0	0	X	0	No channel selected, power-up/reset default state

(1) Several channels can be enabled at the same time. For example, B3 = 0, B2 = 1, B1 = 1, B0 = 0 means that channels 0 and 3 are disabled, and channels 1 are 2 and enabled. Care should be taken not to exceed the maximum bus capacity.

9.6.4 Interrupt Handling

The TCA9545A provides four interrupt inputs (one for each channel) and one open-drain interrupt output (see Table 2). When an interrupt is generated by any device, it is detected by the TCA9545A and the interrupt output is driven low. The channel does not need to be active for detection of the interrupt. A bit also is set in the control register.

Bits 4–7 of the control register correspond to channels 0–3 of the TCA9545A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master then can address the TCA9545A and read the contents of the control register to determine which channel contains the device generating the interrupt. The master then can reconfigure the TCA9545A to select this channel and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs can be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V_{CC}.

Table 2. Control Register Read (Interrupt)(1)

$\overline{INT3}$	$\overline{INT2}$	$\overline{INT1}$	$\overline{INT0}$	B3	B2	B1	B0	COMMAND
X	X	X	0	X	X	X	X	No interrupt on channel 0
			1					Interrupt on channel 0
X	X	0	X	X	X	X	X	No interrupt on channel 1
		1						Interrupt on channel 1
X	0	X	X	X	X	X	X	No interrupt on channel 2
	1							Interrupt on channel 2
0	X	X	X	X	X	X	X	No interrupt on channel 3
1								Interrupt on channel 3

(1) Several interrupts can be active at the same time. For example, $\overline{INT3}$ = 0, $\overline{INT2}$ = 1, $\overline{INT1}$ = 1, $\overline{INT0}$ = 0 means that there is no interrupt on channels 0 and 3, and there is interrupt on channels 1 and 2.

10 Application and Implementation

10.1 Application Information

Applications of the TCA9545A will contain an I^2C (or SMBus) master device and up to four I^2C slave devices. The downstream channels are ideally used to resolve I^2C slave address conflicts. For example, if four identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0, 1, 2, and 3. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I^2C master can move on and read the next channel.

In an application where the I^2C bus will contain many additional slave devices that do not result in I^2C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches will be enabled simultaneously, additional design requirements must be considered (See Design Requirements and Detailed Design Procedure).

10.2 Typical Application

A typical application of the TCA9545A will contain anywhere from 1 to 5 separate data pull-up voltages, V_{DPUX} , one for the master device (V_{DPUM}) and one for each of the selectable slave channels (V_{DPU0} – V_{DPU3}). In the event where the master device and all slave devices operate at the same voltage, then the pass voltage, V_{pass} = V_{DPUX}. Once the maximum V_{pass} is known, V_{cc} can be selected easily using Figure 17. In an application where voltage translation is necessary, additional design requirements must be considered (See Design Requirements).

Figure 16 shows an application in which the TCA9545A can be used.

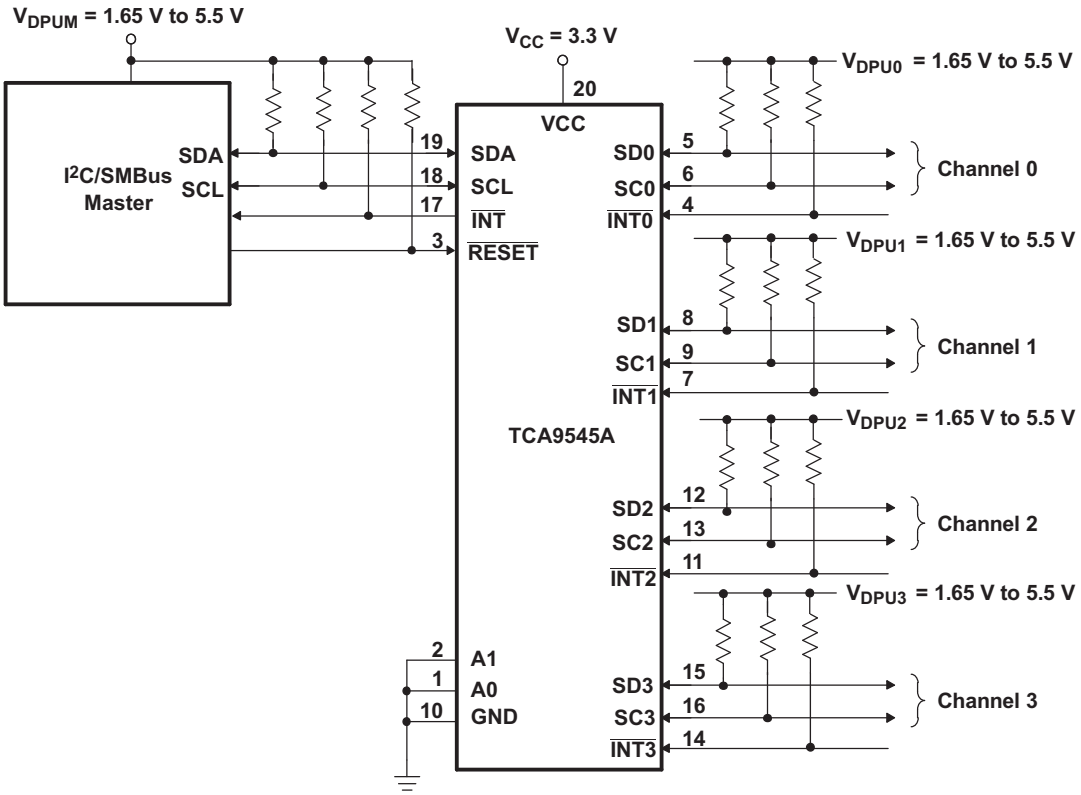


Figure 16. TCA9545A Typical Application Schematic

10.2.1 Design Requirements

The pull-up resistors on the $\overline{INT3}$-$\overline{INT0}$ terminals in the application schematic are not required in all applications. If the device generating the interrupt has an open-drain output structure or can be tri-stated, a pull-up resistor is required. If the device generating the interrupt has a push-pull output structure and cannot be tri-stated, a pull-up resistor is not required. The interrupt inputs should not be left floating in the application.

Typical Application (continued)

The A0 and A1 terminals are hardware selectable to control the slave address of the TCA9545A. These terminals may be tied directly to GND or V_{CC} in the application.

If multiple slave channels will be activated simultaneously in the application, then the total I_{OL} from SCL/SDA to GND on the master side will be the sum of the currents through all pull-up resistors, R_p.

The pass-gate transistors of the TCA9545A are constructed such that the V_{CC} voltage can be used to limit the maximum voltage that is passed from one I^2C bus to another.

Figure 17 shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the Electrical Characteristics section of this data sheet). In order for the TCA9545A to act as a voltage translator, the V_{pass} voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V, V_{pass} must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 17, $V_{pass(max)}$ is 2.7 V when the TCA9545A supply voltage is 4 V or lower, so the TCA9545A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see Figure 16).

10.2.2 Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors, R_p, for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of V_{DPUX}, $V_{OL,(max)}$, and I_{OL}:

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9545A, $C_{io(OFF)}$, the capacitance of wires/connections/traces, and the capacitance of each individual slave on a given channel. If multiple channels will be activated simultaneously, each of the slaves on all channels will contribute to total bus capacitance.

Typical Application (continued)

10.2.3 TCA9545A Application Curves

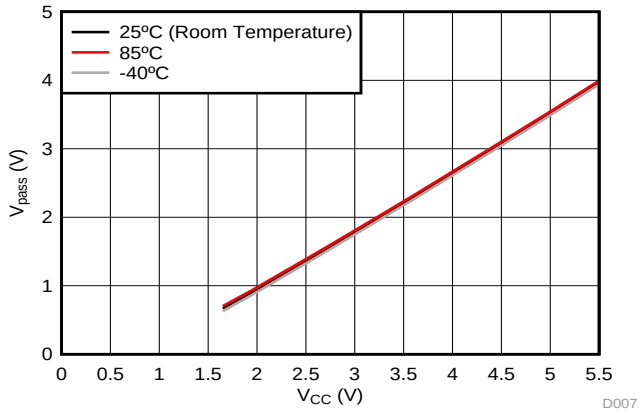
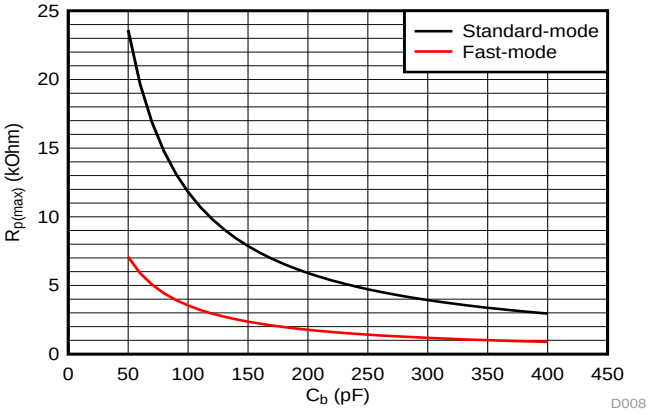


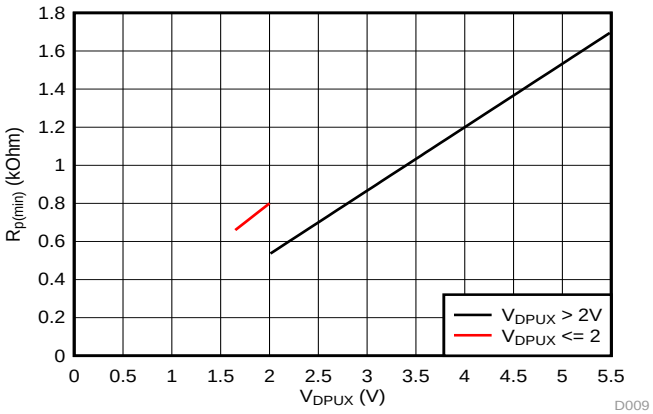
Figure 17. Pass-Gate Voltage (V_{pass}) vs Supply Voltage (V_{CC}) at Three Temperature Points



Standard-mode
(f_{SCL}= 100 kHz, t_r = 1 µs)

Fast-mode
(f_{SCL}= 400 kHz, t_r= 300 ns)

Figure 18. Maximum Pull-Up resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2*V_{DPUX}, I_{OL} = 2 mA when V_{DPUX} ≤ 2 V
V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{DPUX} > 2 V

Figure 19. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{DPUX})

11 Power Supply Recommendations

The operating power-supply voltage range of the TCA9545A is 1.65 V to 5.5 V applied at the VCC pin. When the TCA9545A is powered on for the first time or anytime the device needs to be reset by cycling the power supply, the power-on reset requirements must be followed to ensure the I^2C bus logic is initialized properly.

11.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA9545A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

A power-on reset is shown in Figure 20.

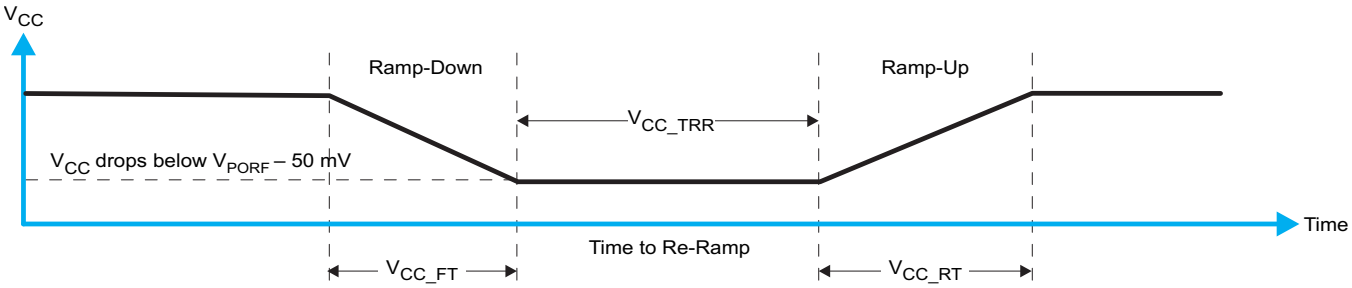


Figure 20. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

Table 3 specifies the performance of the power-on reset feature for TCA9545A for both types of power-on reset.

Table 3. Recommended Supply Sequencing And Ramp Rates(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall time	See Figure 20	1		100	ms
V_{CC_RT}	Rise time	See Figure 20	0.1		100	ms
V_{CC_TRR}	Time to re-ramp (when V_{CC} drops below $V_{PORF(min)}$ – 50 mV or when V_{CC} drops to GND)	See Figure 20	40			µs
V_{CC_GH}	Level that V_{CC} can glitch down to, but not cause a functional disruption when V_{CC_GW} = 1 µs	See Figure 21			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CC_GH} = 0.5 × V_{CC}	See Figure 21			10	µs
V_{PORF}	Voltage trip point of POR on falling V_{CC}	See Figure 22	0.8		1.25	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}	See Figure 22	1.05		1.5	V

(1) All supply sequencing and ramp rate values are measured at T_A = 25°C

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 21 and Table 3 provide more information on how to measure these specifications.

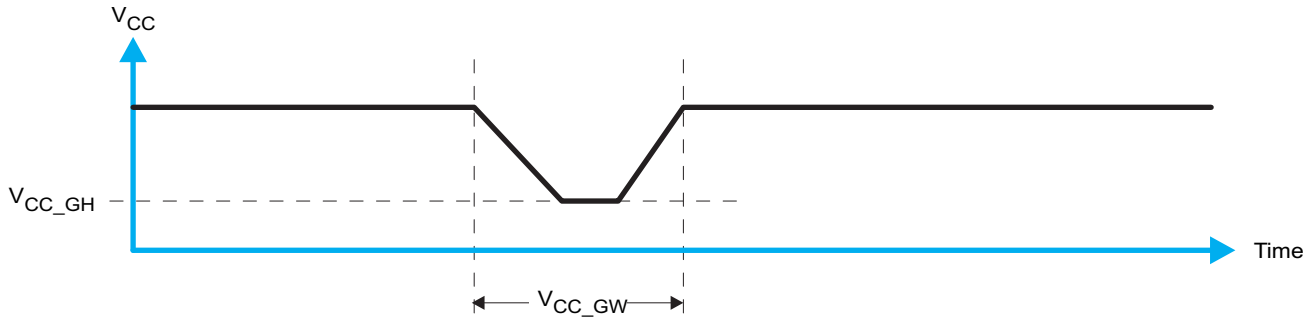


Figure 21. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 22 and Table 3 provide more details on this specification.

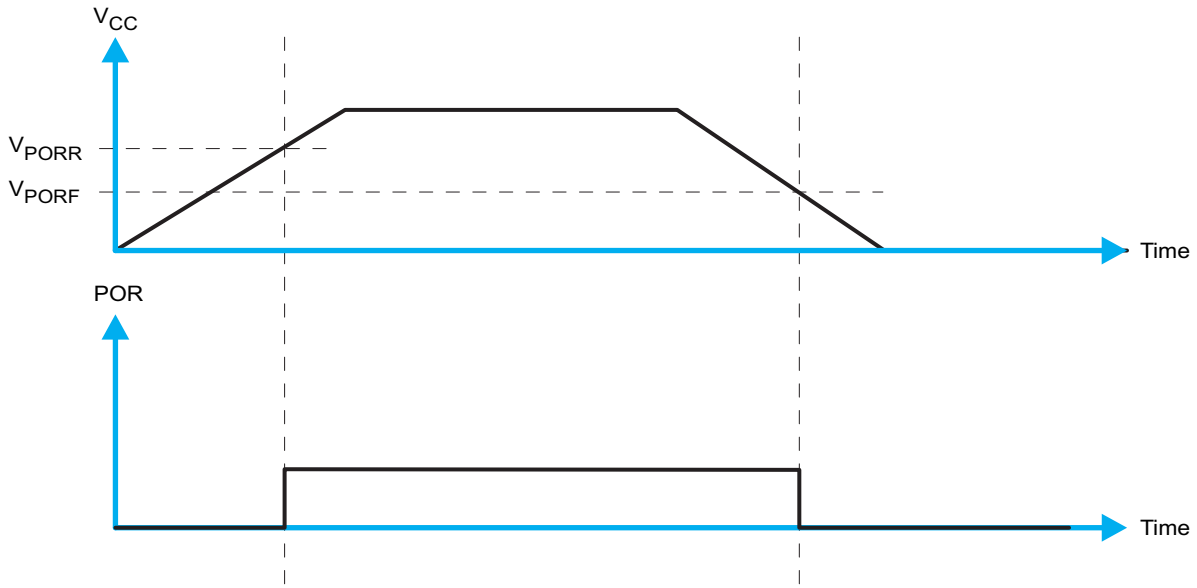


Figure 22. V_{POR}

12 Layout

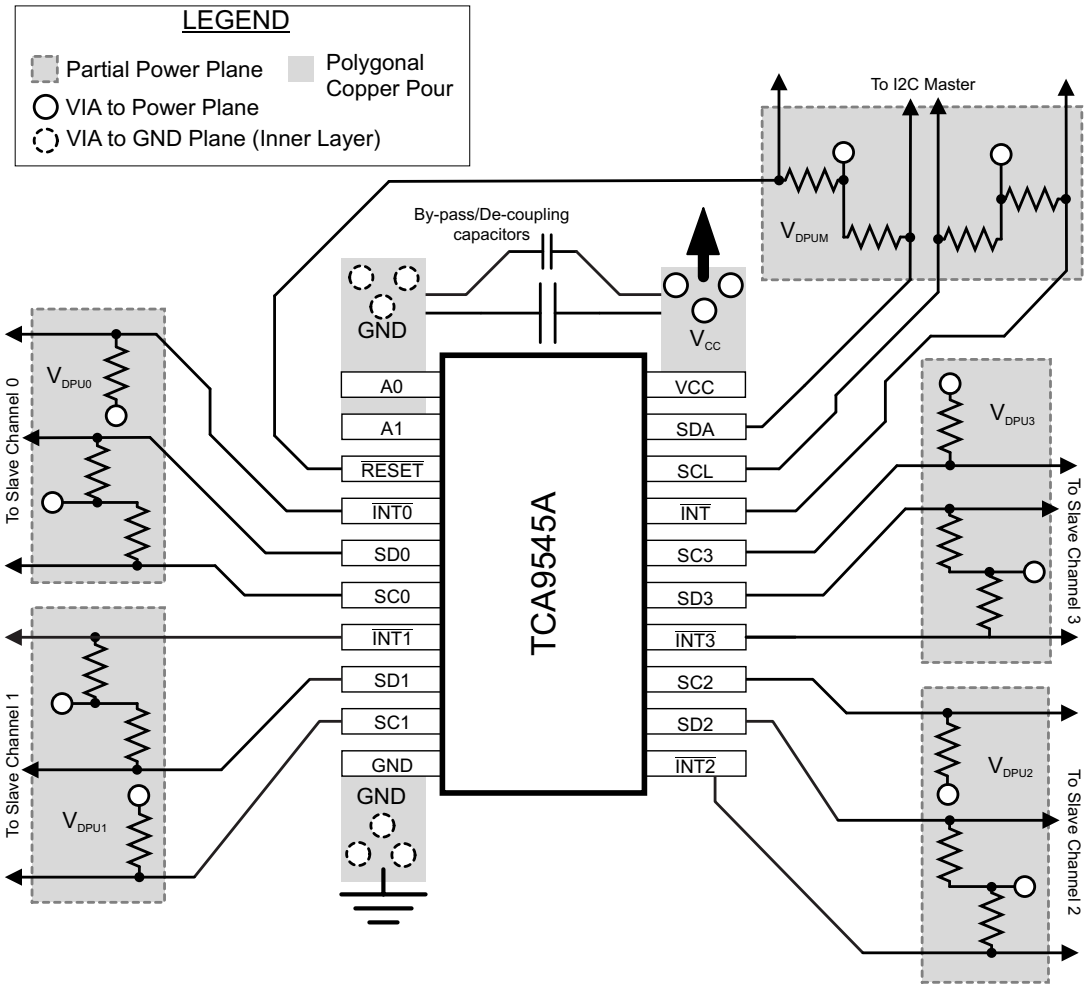
12.1 Layout Guidelines

For PCB layout of the TCA9545A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and terminals that are connected to ground should have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC terminal, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all V_{DPUX} voltages and V_{CC} could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V_{DPUM}, V_{DPU0}, V_{DPU1}, V_{DPU2}, and V_{DPU3} may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I^2C bus capacitance added by PCB parasitics, data lines (SCn, SDn and $\overline{INTn}$) should be a short as possible and the widths of the traces should also be minimized (e.g. 5-10 mils depending on copper weight).

12.2 Layout Example



13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following packaging information and addendum reflect the most current data available for the designated devices. This data is subject to change without notice and revision of this document.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9545APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW545A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

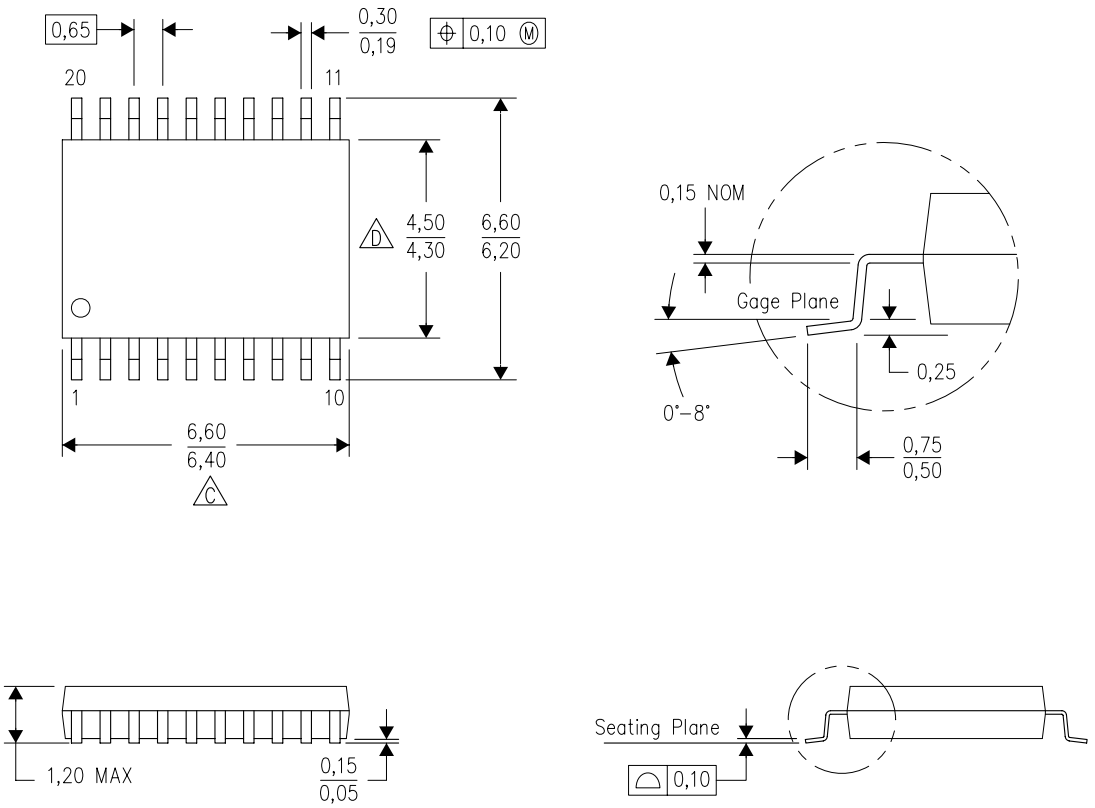
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

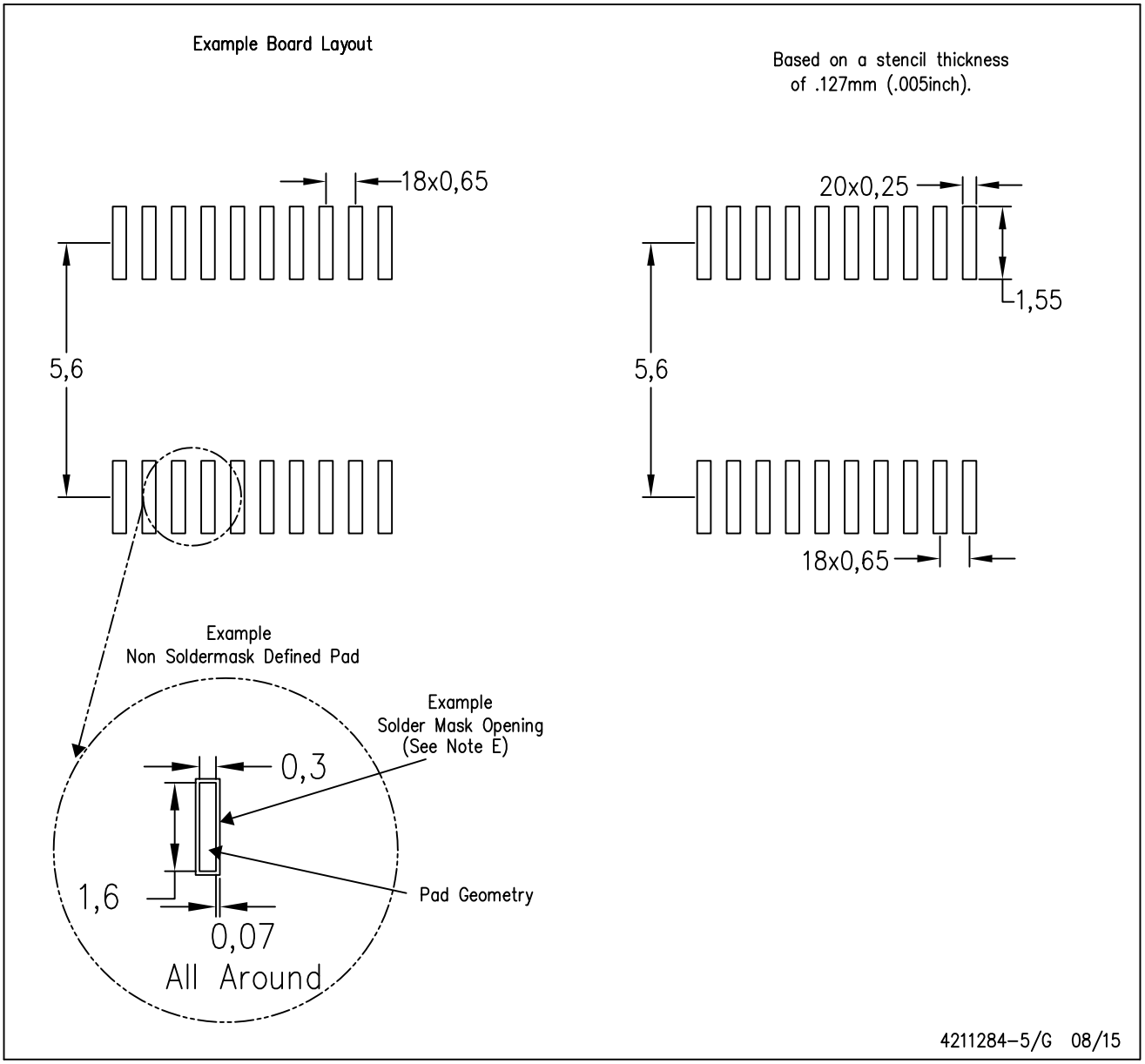
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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