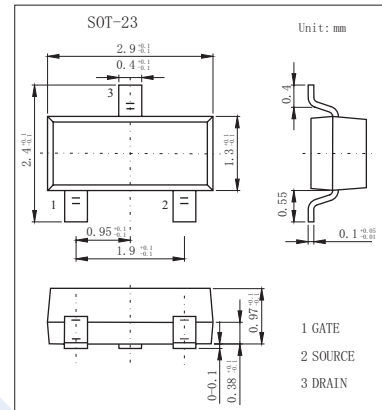
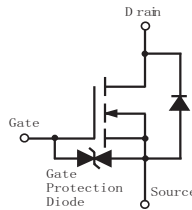


N-Channel Enhancement MOSFET

2N7002K

■ Features

- Low On-Resistance: $R_{DS(on)}$
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- ESD Protected 2KV HBM

■ Absolute Maximum Ratings $T_a=25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage -Continuous	V_{GS}	± 20	
Drain Current -Continuous (Note:1)	I_D	300	mA
		-Pulsed	
Power Dissipation (Note 1)	P_D	350	mW
Thermal Resistance.Junction- to-Ambient	R_{thJA}	357	$^\circ\text{C/W}$
Junction Temperature	T_J	150	$^\circ\text{C}$
Junction and Storage Temperature Range	T_{stg}	-55 to 150	

Notes: 1. Device mounted on FR-4 PCB.

■ Electrical Characteristics $T_a = 25^\circ\text{C}$

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage (Note.2)	V_{DSS}	$I_D=100\ \mu\text{A}, V_{GS}=0\text{V}$	60			V
Zero Gate Voltage Drain Current (Note.2)	I_{DSS}	$V_{DS}=60\text{V}, V_{GS}=0\text{V}$			1	μA
Gate-Body Leakage Current (Note.2)	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 10	μA
Gate Threshold Voltage (Note.2)	$V_{GS(th)}$	$V_{DS} = 10\text{V}, I_D = 1\text{mA}$	1	1.6	2.5	V
Static Drain-Source On-Resistance (Note.2)	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=500\text{mA}$			2	Ω
		$V_{GS}=10\text{V}, I_D=50\text{mA}$			3	
Forward Transfer Admittance (Note.2)	$ Y_{fs} $	$V_{GS}=10\text{V}, I_D=200\text{mA}$	80			ms
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}, V_{DS}=25\text{V}, f=1\text{MHz}$			50	pF
Output Capacitance	C_{oss}				25	
Reverse Transfer Capacitance	C_{rss}				5	
Total Gate Charge	Q_g	$V_{GS}=4.5\text{V}, V_{DS}=15\text{V}, I_D=200\text{mA}$			0.8	nC
Turn-On DelayTime	$t_{d(on)}$	$I_D=200\text{mA}, V_{DS}=30\text{V}, R_G=10\Omega, V_{GEN}=10\text{V}, R_L=150\Omega$			20	ns
Turn-Off DelayTime	$t_{d(off)}$				40	

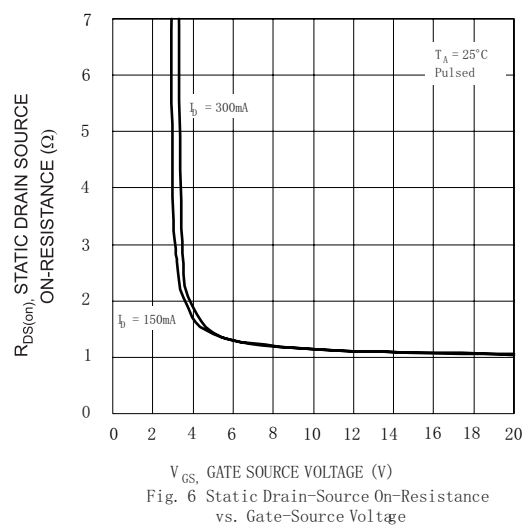
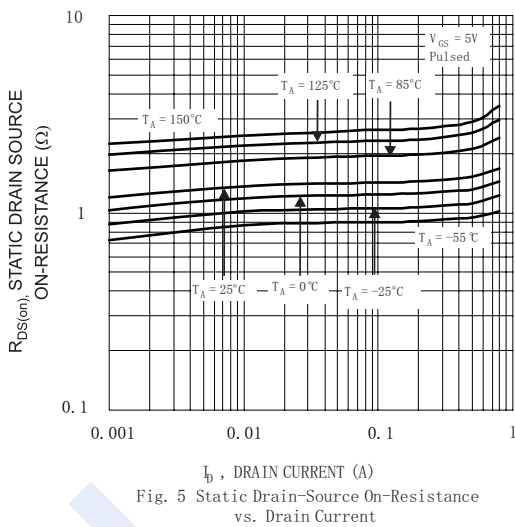
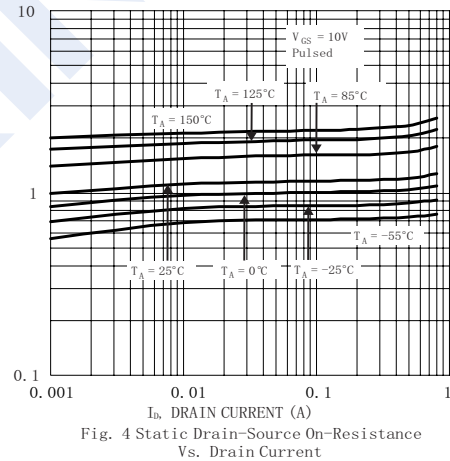
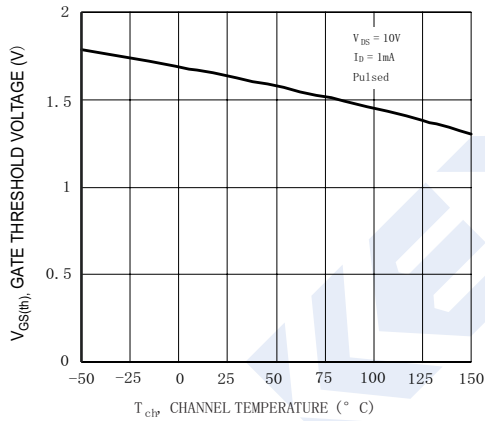
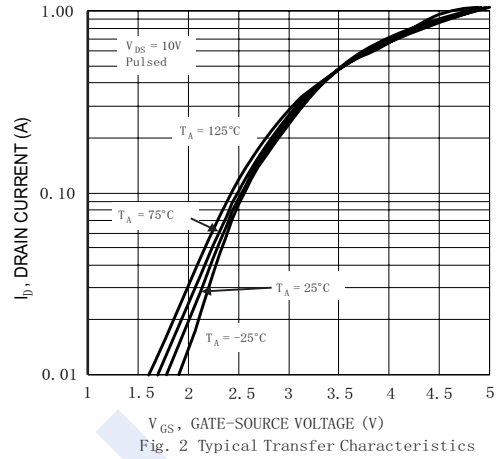
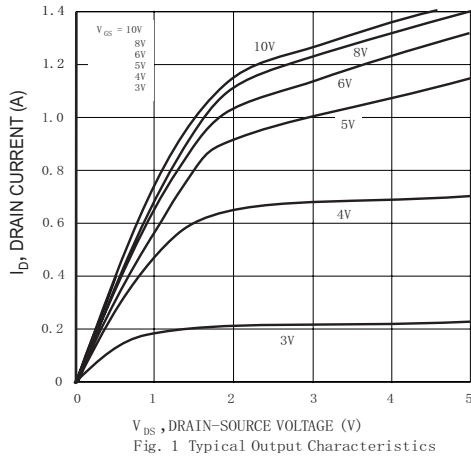
Note: 2. Short duration test pulse used to minimize self-heating effect.

■ Marking

Marking	K72R
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2N7002K

Typical Characteristics



2N7002K

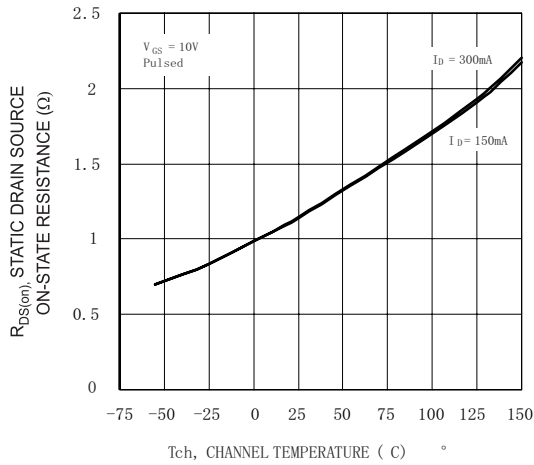


Fig. 7 Static Drain-Source On-State Resistance vs. Channel Temperature

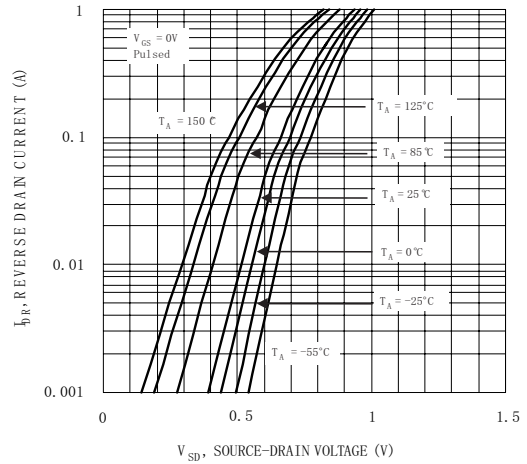


Fig. 8 Reverse Drain Current vs. Source-Drain Voltage

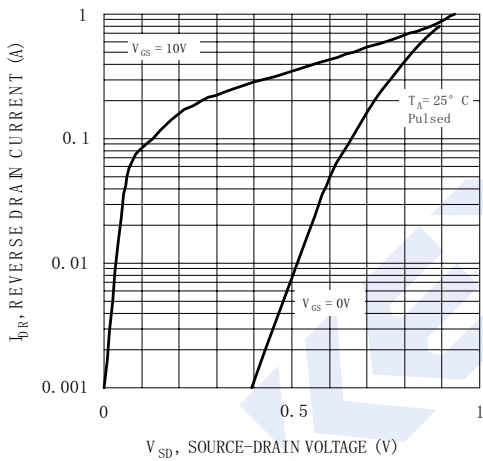


Fig. 9 Reverse Drain Current vs. Source-Drain Voltage

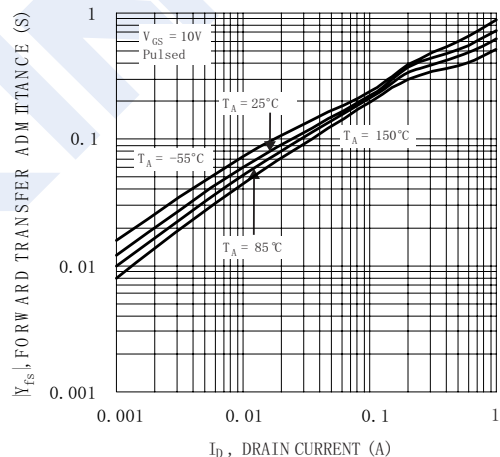


Fig. 10 Forward Transfer Admittance vs. Drain Current