

11A, 650V DP MOS POWER TRANSISTOR

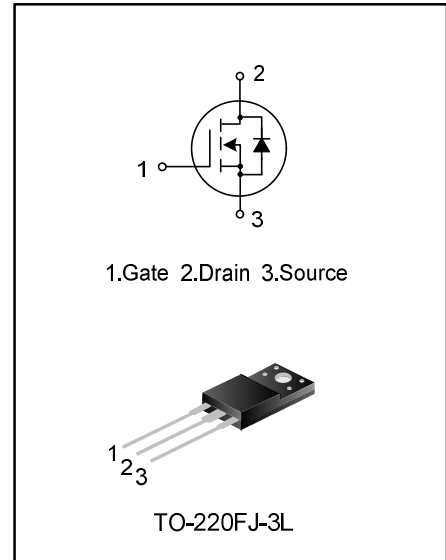
DESCRIPTION

SVS11N65FJD2 is an N-channel enhancement mode high voltage power MOSFETs produced using Silan's DP MOS technology. It achieves low conduction loss and switching losses. It leads the design engineers to their power converters with high efficiency, high power density, and superior thermal behavior.

Furthermore, it's universal applicable, i.e., suitable for hard and soft switching topologies.

FEATURES

- ◆ 11A, 650V, $R_{DS(on)(typ.)}=0.33\Omega@V_{GS}=10V$
- ◆ New revolutionary high voltage technology
- ◆ Ultra low gate charge
- ◆ Periodic avalanche rated
- ◆ Extreme dv/dt rated
- ◆ High peak current capability



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVS11N65FJD2	TO-220FJ-3L	11N65FJD2	Halogen free	Tube

ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, $T_C=25^\circ\text{C}$)

Characteristics	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	± 30	V
Drain Current	I_D	$T_C=25^\circ\text{C}$	11
		$T_C=100^\circ\text{C}$	7
Drain Current Pulsed	I_{DM}	44	A
Power Dissipation ($T_C=25^\circ\text{C}$) - Derate above 25°C	P_D	23	W
		0.18	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy (Note 1)	E_{AS}	250	mJ
Operation Junction Temperature Range	T_J	$-55\sim+150$	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	$-55\sim+150$	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	5.43	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^{\circ}C/W$

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $T_c=25^{\circ}C$)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=650V, V_{GS}=0V$	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30V, V_{DS}=0V$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	--	4.0	V
Static Drain- Source on State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=5.5A$	--	0.33	0.4	Ω
Input Capacitance	C_{iss}	$f=1MHz, V_{GS}=0V, V_{DS}=100V$	--	581.78	--	pF
Output Capacitance	C_{oss}		--	45.12	--	
Reverse Transfer Capacitance	C_{rss}		--	3.37	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=325V, V_{GS}=10V, R_G=24\Omega, I_D=11A$ (Note 2,3)	--	11.20	--	ns
Turn-on Rise Time	t_r		--	31.24	--	
Turn-off Delay Time	$t_{d(off)}$		--	62.20	--	
Turn-off Fall Time	t_f		--	31.24	--	
Total Gate Charge	Q_g	$V_{DD}=520V, V_{GS}=10V, I_D=11A$ (Note 2,3)	--	20.76	--	nC
Gate-Source Charge	Q_{gs}		--	4.13	--	
Gate-Drain Charge	Q_{gd}		--	10.88	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	11	A
Pulsed Source Current	I_{SM}		--	--	44	
Diode Forward Voltage	V_{SD}	$I_S=11A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=11A, V_{GS}=0V, di_F/dt=100A/\mu s$	--	450	--	ns
Reverse Recovery Charge	Q_{rr}		--	4.5	--	μC

Notes:

- $L=79mH, I_{AS}=2.4A, V_{DD}=100V, R_G=25\Omega$, starting temperature $T_J=25^{\circ}C$;
- Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;
- Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

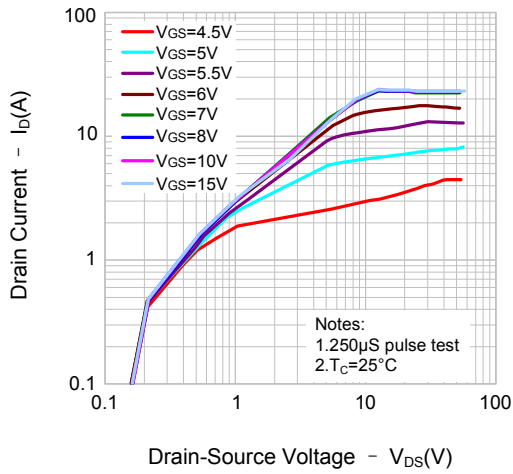


Figure 2. Transfer Characteristics

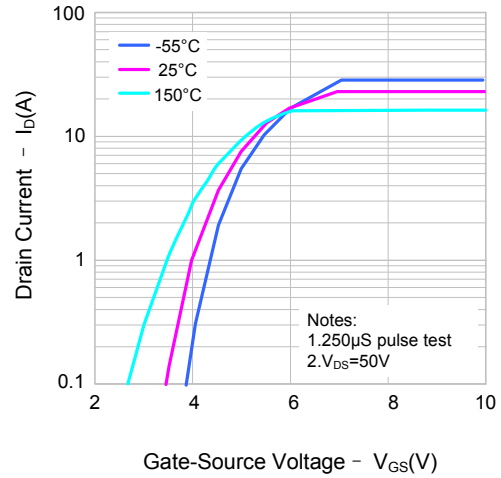


Figure 3. On-Resistance Variation vs. Drain Current

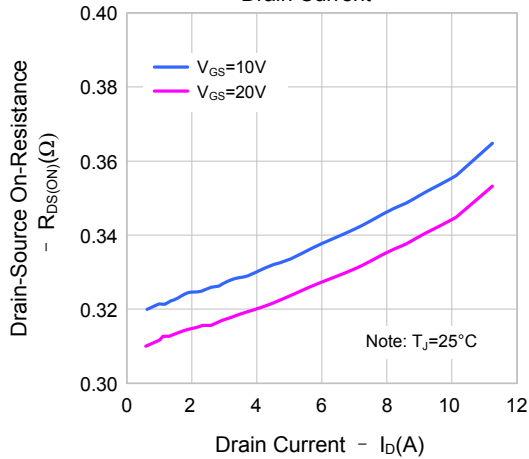


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

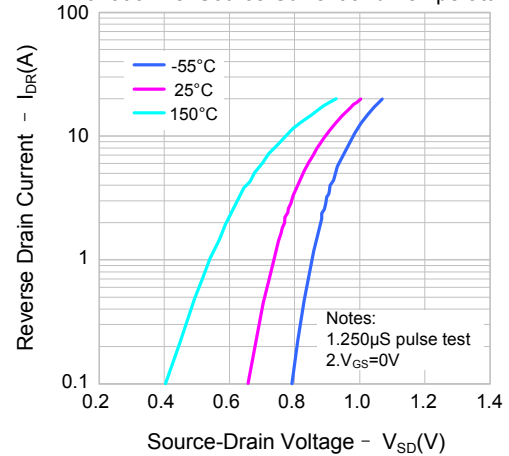


Figure 5. Capacitance Characteristics

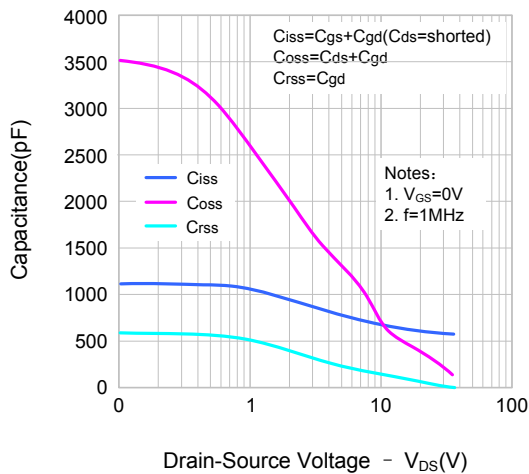
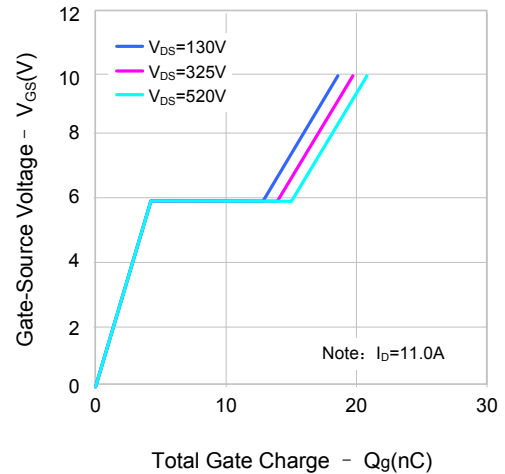


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

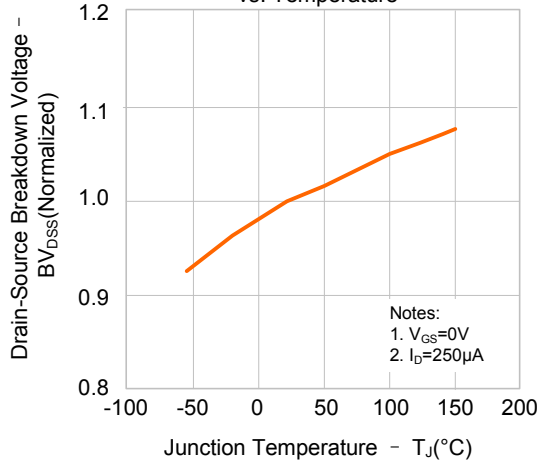


Figure 8. On-resistance Variation vs. Temperature

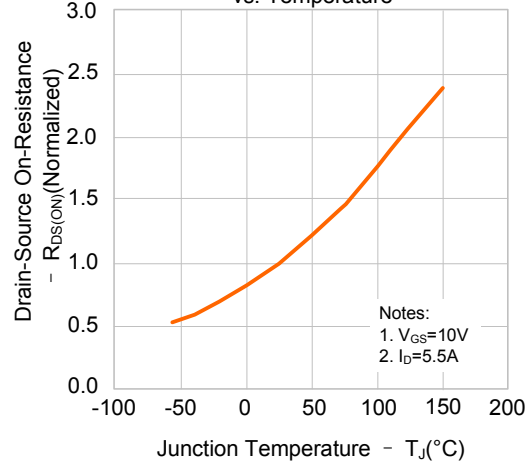
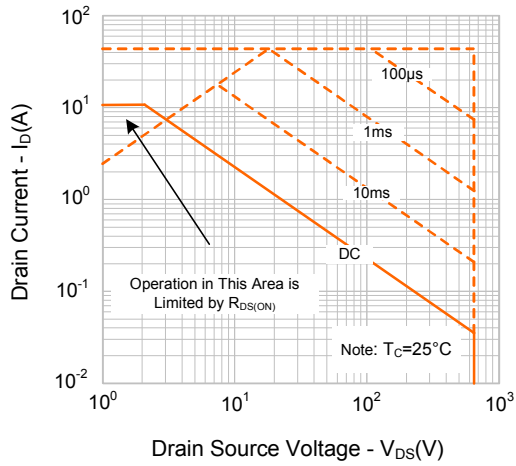
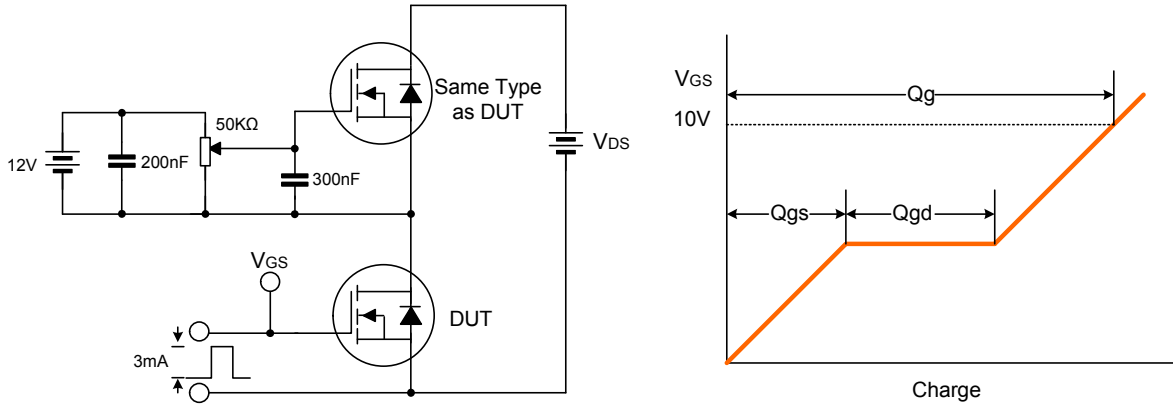


Figure 9. Max. Safe Operating Area

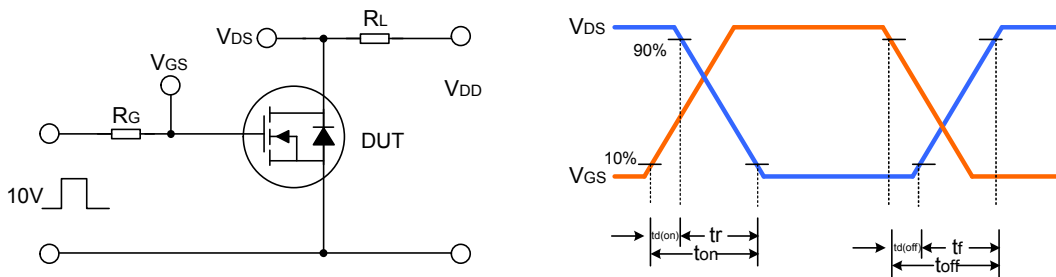


TYPICAL TEST CIRCUIT

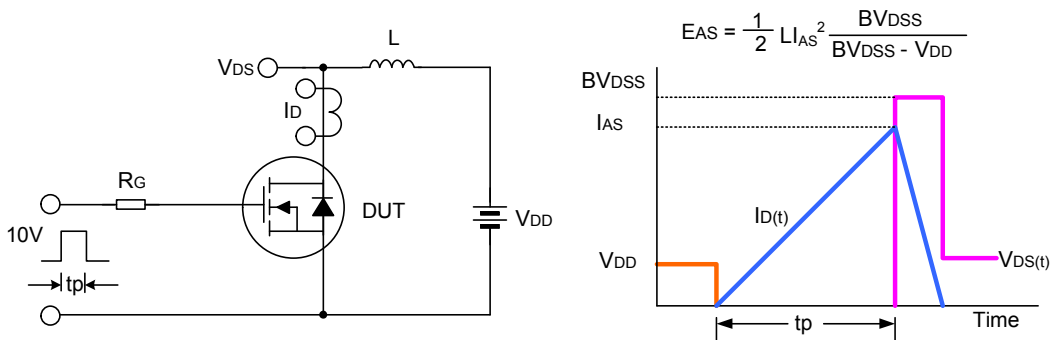
Gate Charge Test Circuit & Waveform



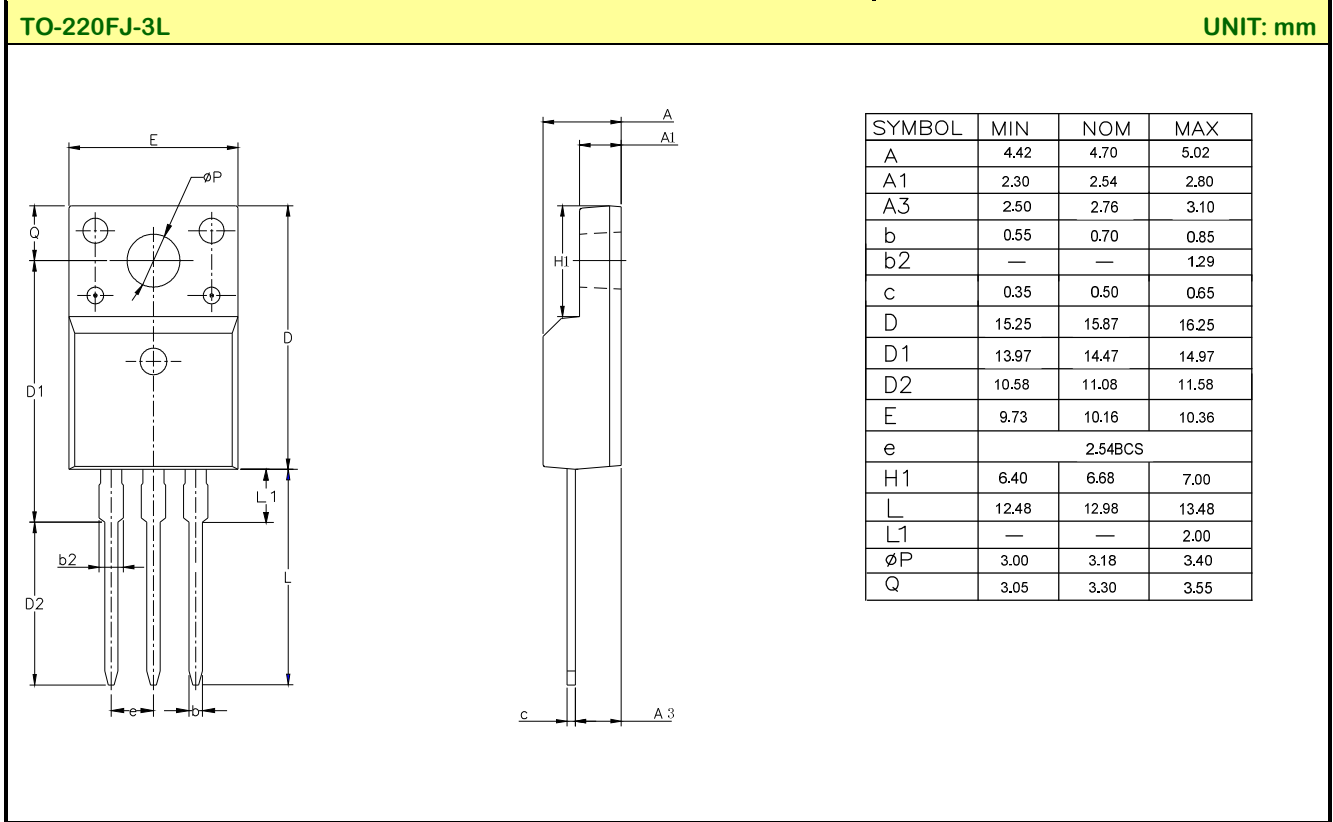
Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE(continued)



Disclaimer :

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without prior notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
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Part No.: SVS11N65FJD2 Document Type: Datasheet
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Rev.: 1.2

Revision History:

1. Modify Electrical characteristics
 2. Update Fig.5 and Fig.6
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Rev.: 1.0

Revision History:

1. Preliminary
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