Features

- ESD Protect for Transition Minimized Differential Signaling (TMDS) channels
- Protects four I/O lines
- Provide ESD protection for each line to
  IEC 61000-4-2 (ESD) ±18kV (air), ±16kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 6A (8/20μs)
- **For operating voltage of 3.3V and below**
- **Ultra low capacitance : 0.45pF typical**
- Fast turn-on and Low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS (Transient Voltage Suppression) diode
- Simplified layout for HDMI connectors
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- **High Definition Multi-Media Interface (HDMI) 1.3 & 1.4 and 2.0 version**
- **DisplayPort interface**
- **SATA and eSATA interface**
- **USB3.0**
- **V-By-One**
- **LVDS interfaces**
- IEEE 1394 up to 3.2 Gb/s
- Ethernet port: 10/100/1000 Mb/s
- Desktop and Notebooks PCs
- Consumer Electronics
- Set Top Box
- DVDRW Players
- Graphics Cards

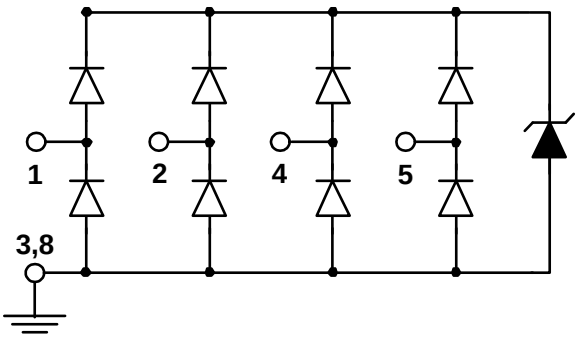
Description

AZ1143-04F is a design which includes ESD rated diode arrays to protect high speed data interfaces. The AZ1143-04F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

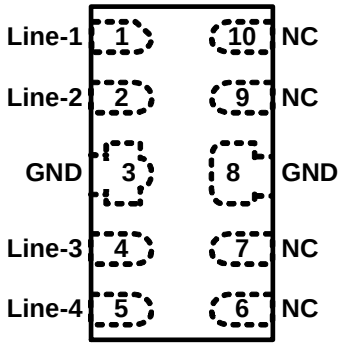
AZ1143-04F is a unique design which includes ESD rated, ultra low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the internal ESD line or to ground line. The internal unique design of clamping cell prevents over-voltage on the internal ESD line and on the I/O line, which is protecting any downstream components.

AZ1143-04F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



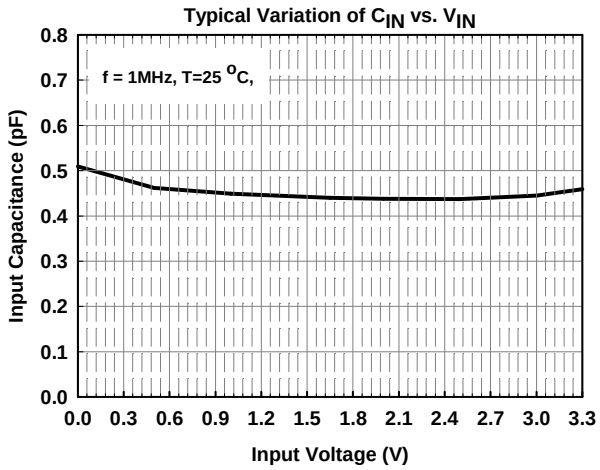
DFN2510P10E (Top View)

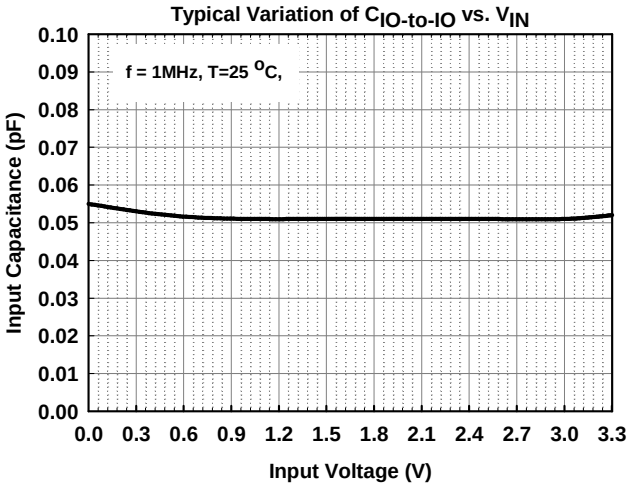
SPECIFICATIONS

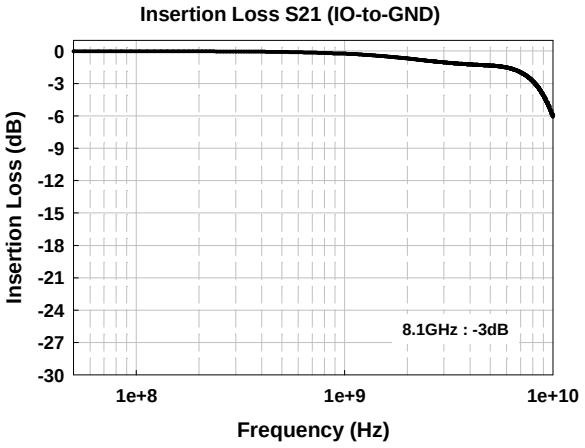
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp= 8/20μs)	I_{PP}	6	**A**
Operating Voltage (I/O pin-GND)	V_{DC}	(GND – 0.5) to 3.6	**V**
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	18 16	**kV**
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	**°C**
Operating Temperature	T_{OP}	-55 to +85	**°C**
Storage Temperature	T_{STO}	-55 to +150	**°C**

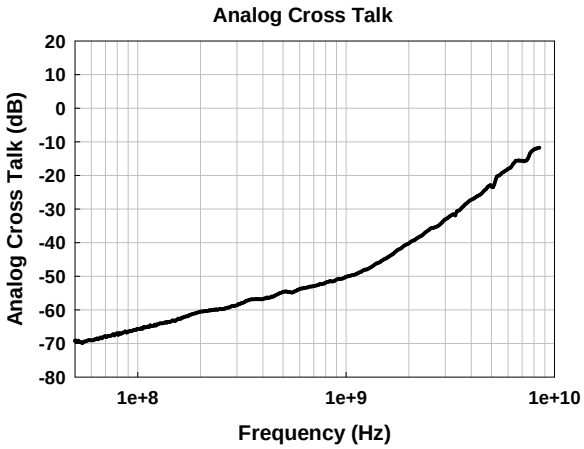
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1,-2,-4,-5 to pin-3,-8, T=25 °C			3.3	**V**
Channel Leakage Current	$I_{CH-Leak}$	$V_{Pin-1,-2,-4,-5}$ = 3.3V, $V_{Pin-3,-8}$ = 0V, T=25 °C			1.0	**μA**
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, pin-1,-2,-4,-5 to pin-3,-8	4.5			**V**
Forward Voltage	V_F	I_F = 15mA, T=25 °C, pin-3,-8 to pin-1,-2,-4,-5		0.9	1.1	**V**
ESD Clamping Voltage	V_{clamp}	IEC 61000-4-2 +6kV, T=25 °C, Contact mode, any I/O pin to Ground		9		**V**
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+6kV, T=25 °C, Contact mode, any I/O pin to Ground		0.24		**Ω**
Channel Input Capacitance	C_{IN}	$V_{pin-3,-8}$ = 0V, **V_{IN} = 1.65V**, f = 1MHz, T=25 °C, any I/O pin to Ground		0.45	0.65	**pF**
Channel to Channel Input Capacitance	C_{CROSS}	$V_{pin-3,-8}$ = 0V, **V_{IN} = 1.65V**, f = 1MHz, T=25 °C, between I/O pins		0.05	0.1	**pF**

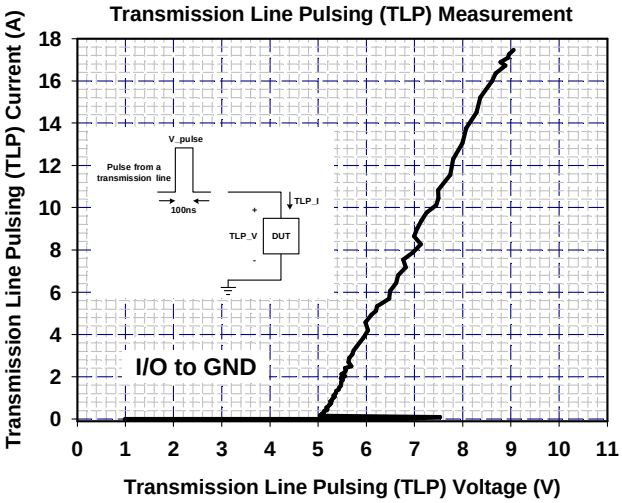
Typical Characteristics











Applications Information

The AZ1143-04F is designed to protect four data lines from transient over-voltage (such as ESD stress pulse). The device connection of AZ1143-04F is shown in the Fig. 1. In Fig. 1, the four protected data lines are connected to the ESD protection pins (pin1, pin2, pin4, and pin5) of AZ1143-04F. The ground pins (pin3 and pin8) of AZ1143-04F are the negative reference pins. These pins should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible.

AZ1143-04F can provide ESD protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

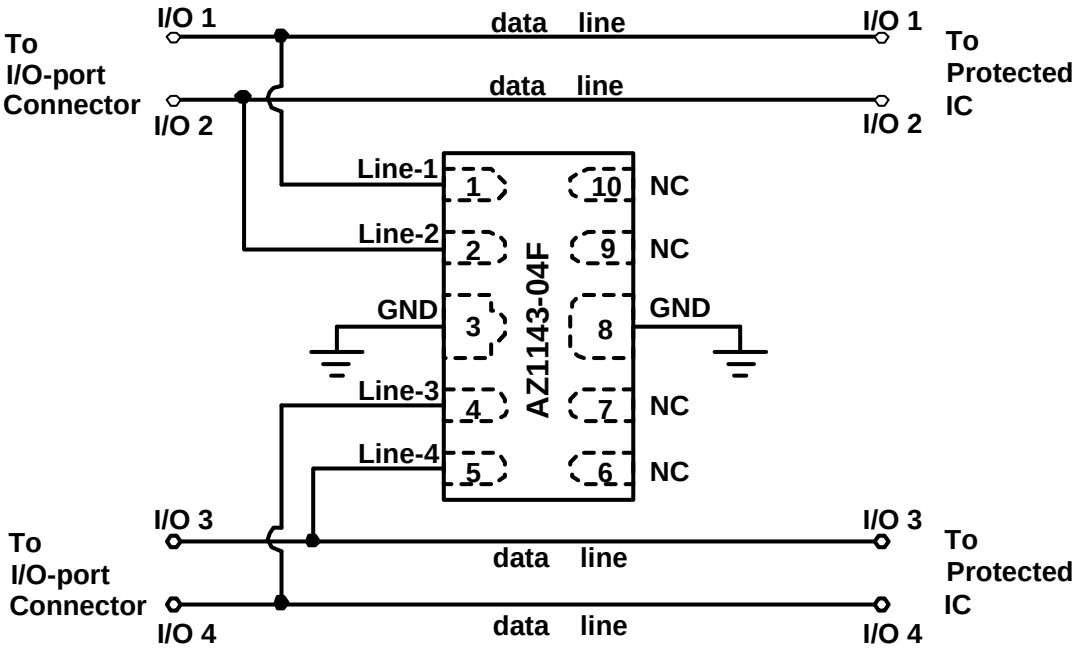


Fig. 1 Data lines connection of AZ1143-04F.

B. Application

AZ1143-04F is designed for protecting high speed I/O ports from over-voltage caused by Electrostatic Discharging (ESD). Thus, a lot of kinds of high speed I/O ports can be the applications of AZ1143-04F, especially, the HDMI port.

HDMI Protection for High and Low speed signals

The HDMI Compliance Test Specification (CTS) requires sink (receiver) ports maintain a differential impedance of 100 Ohms +/- 15%.

ESD protection devices have an inherent junction capacitance. Even a small amount of added capacitance on a HDMI port will cause the impedance of the differential pair to drop. Thus, some form of compensation to the layout will be required to bring the differential pairs back within the required 100 Ohm +/- 15% range. The higher the added capacitance, the more extreme the modifications will need to be. If the added capacitance is too high, compensation may not even be possible. The AZ1143-04F presents **0.45pF** capacitance to each differential signal while being rated to handle >8kV ESD contact discharges (>15kV air discharge) as outlined in IEC 61000-4-2. Therefore, it is possible to **make**

none adjustment to the board layout parameters to compensate for the added capacitance of the AZ1143-04F. Figure 2 shows how to implement the AZ1143-04F in a HDMI application.

The AZ1143-04F is designed for allowing the traces to run straight through the device to simplify the PCB layout. As shown in Figure 2, the best way to design the PCB trace is using the flow through layout. The solid line represents the PCB trace. Note that the PCB traces are used to connect the pin pairs for each line (pin 1 to pin 10, pin 2 to pin 9, pin 4 to pin 7, pin 5 to pin 6). For example, line 1 enters at pin 1 and exits at Pin 10 and the PCB trace connects pin 1 and 10 together. Lines 2, 3, and 4 have the same way of connection. The ground pins (pin3 and pin8) of AZ1143-04F are the negative reference pins. These pins should be directly connected to the GND plane of PCB. To get minimum parasitic inductance, the path length should keep as short as possible. **In Figure 2, the none-TMDS signals, DDC_CLK, DDC_DAT, CE_REMOTE, and HOTPLUG_DET, can be protected with another low cost part, e.g., AZC199-04S.**

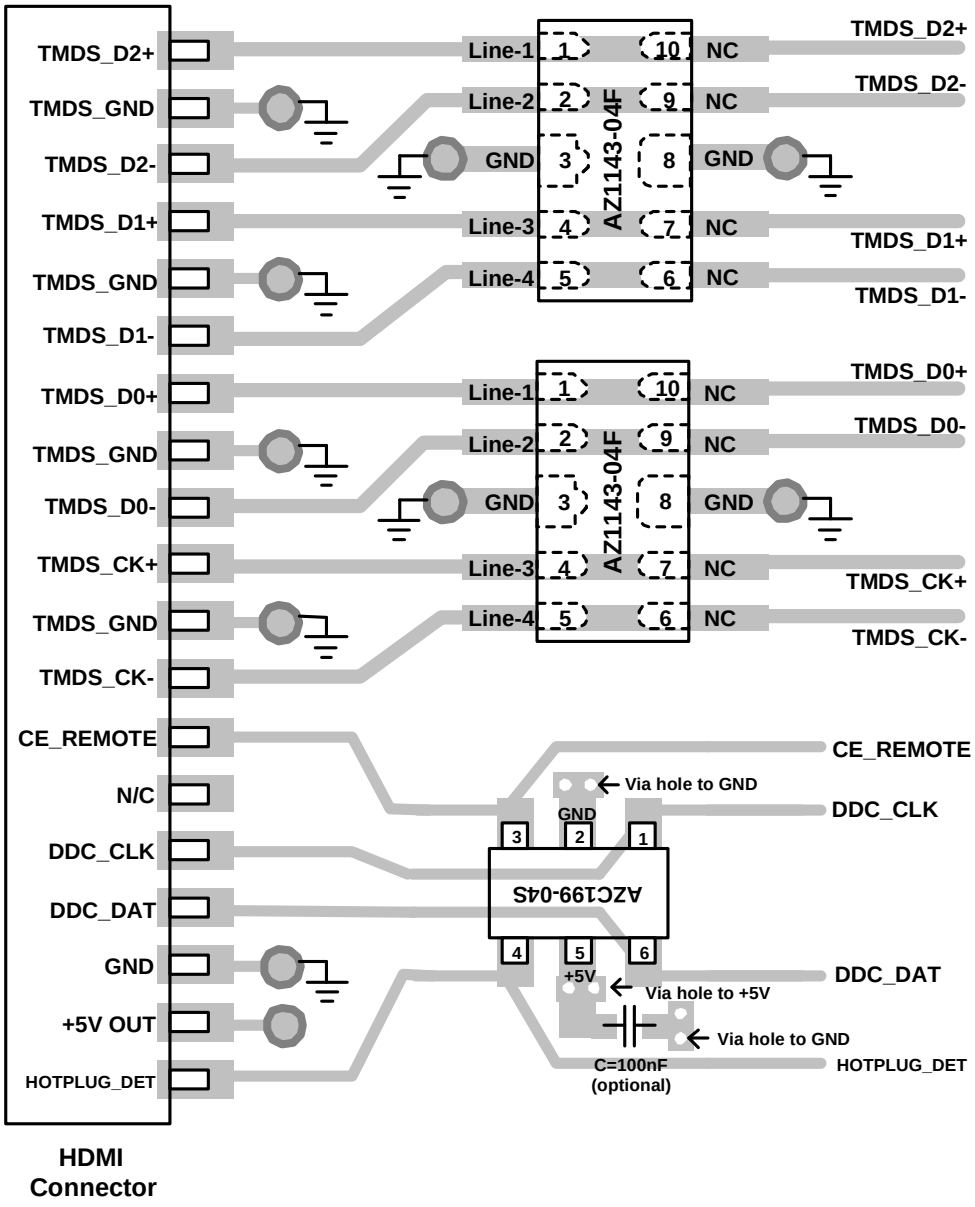
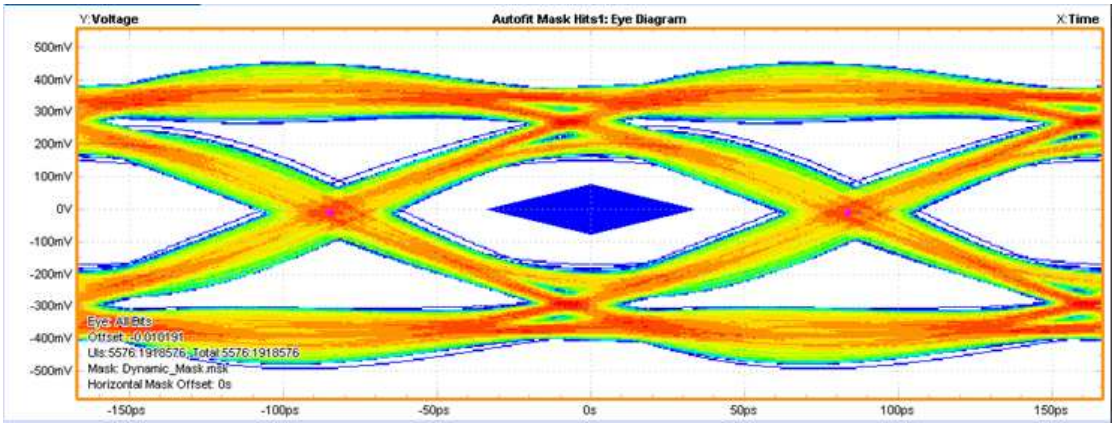
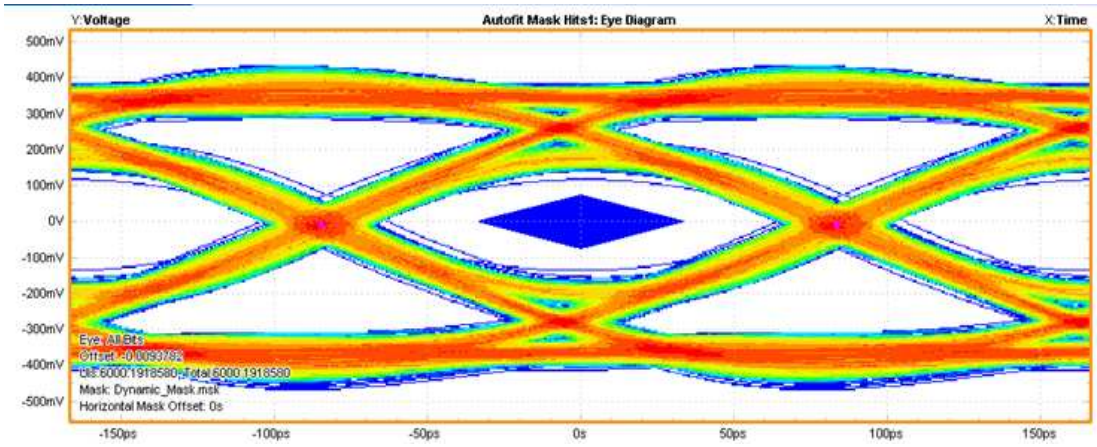


Fig. 2 HDMI Protection for High and Low speed signals.

Fig. 3 shows the HDMI 2.0 (6 Gb/s) eye diagrams with and without AZ1143-04F. Due to ultra low capacitance of AZ1143-04F, no degradation is observed.



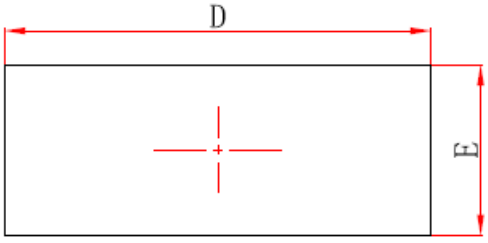
Without AZ1143-04F



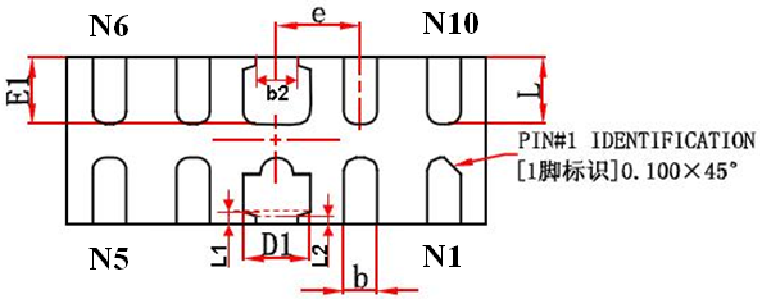
With AZ1143-04F

Fig. 3 HDMI 2.0 (6 Gb/s) Eye Diagrams with and without AZ1143-04F.

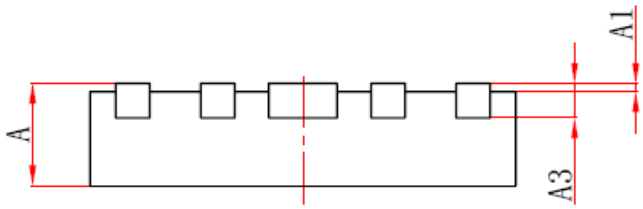
PACKAGE OUTLINE (DFN2510P10E)



TOP VIEW (unit in mm)



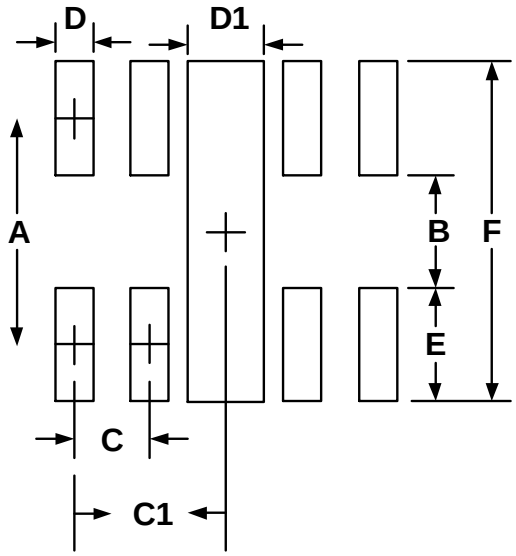
BOTTOM VIEW (unit in mm)



SIDE VIEW (unit in mm)

Symbol	Millimeters		Inches	
	min	max	min	max
A	0.40	0.55	0.016	0.022
A1	0.00	0.05	0.000	0.002
A3	0.152REF.		0.006 BSC	
D	2.45	2.55	0.096	0.100
E	0.95	1.05	0.037	0.041
D1	0.35	0.45	0.014	0.018
E1	0.35	0.45	0.014	0.018
b	0.15	0.25	0.006	0.010
e	0.5 BSC		0.019 BSC	
L1	0.075 REF		0.0029 REF	
L2	0.05 REF		0.0019 REF	
b2	0.20	0.30	0.0079	0.012
L	0.35	0.45	0.014	0.018

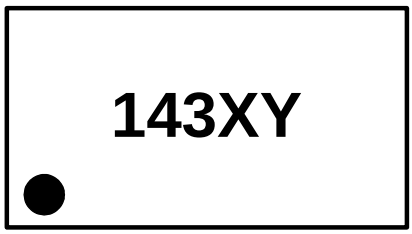
LAND LAYOUT



Dimensions		
Index	**Millimeter**	**Inches**
A	0.875	0.034
B	0.20	0.008
C	0.50	0.02
C1	1.00	0.039
D	0.25	0.01
D1	0.4	0.016
E	0.675	0.027
F	1.55	0.061

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



143 = Device Code
X = Date Code
Y= Control Code

Part Number	Marking Code
AZ1143-04F (Green part)	**143XY**

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ/internal box	MOQ/carton
AZ1143-04F.R7G	Green	T/R	7 inch	4 reel= 12,000/box	6 box =72,000/carton

Revision History

Revision	Modification Description
Revision 2014/06/16	Preliminary Release.
Revision 2014/10/02	Formal Release.