High-Side Power Distribution Controller

Features

- **High-Side Driver for an External N-Channel MOSFET**
- **Under-Voltage Lockout (UVLO)**
- **Wrong VIN Input Voltage Protection**
- **Output Under-Voltage Protection (UVP)**
- **Short-Circuit Protection During Power-Up (SCP)**
- **Over-Current Protection (OCP)**
- **Shutdown Function**
- **Power-Ok (POK) Function**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

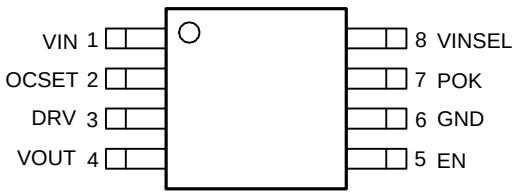
- **Desktop PCs**

General Description

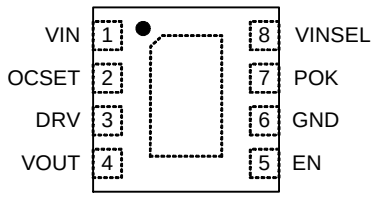
APL3540 is a high-side power distribution controller for an external N-channel MOSFET, allow for +12V and +19V power-supply rails. The wrong input voltage protection function protects a wrong input adapter insertion. When input voltage is out of the target input voltage range, the IC is off.

The built-in under-voltage protection monitors the output voltage for short-circuit conditions. When output voltage is less than 70% of VIN voltage, the IC will be shut down. The over-current protection monitors the output current by using the voltage drop across the external MOSFET's $R_{DS(ON)}$. When output current reaches the trip point, the IC will be shut down. The APL3540 also provides a short-circuit protection during power-up. The device monitors DRV and VOUT voltages for a short-circuit detection. If a short-circuit condition is detected, the IC will be shut down. Other features, including a POK output which indicates that the output voltage is ready and a logic-controlled shutdown mode.

Pin Configuration



SOP-8
(Top View)



TDFN2x2-8
(Top View)

=Exposed Pad
(Please connect to the ground)

Ordering and Marking Information

APL3540 □□□□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code
- SCP Threshold Code

Package Code
K : SOP-8 QB : TDFN2x2-8
Operating Ambient Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
SCP Threshold Code
26 : 2.6V 28 : 2.8V 30 : 3.0V Blanking : 3.5V
Assembly Material
G : Halogen and Lead Free Device

APL3540 K :	APL3540 XXXXX ●	APL3540 XXXXX SS ●
APL3540 QB :	3540 X ●	3540 X SS ●

XXXXX - Date Code SS : SCP Threshold Code

X - Date Code SS : SCP Threshold Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant)and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN Input Voltage (VIN to GND)	-0.3 to 35	V
V_{OUT}, V_{DRV}, V_{OCSET}, V_{POK}, V_{VINSEL}	VOUT, DRV, POK, OCSET and VINSEL to GND Voltage	-0.3 to 40	V
V_{EN}	EN to GND Voltage	-0.3 to 7	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
T_{SDR}	Maximum Lead Soldering Temperature,10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air SOP-8 TDFN2x2-8	 150 80	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage (VIN to GND)	10 to 26	V
V_{EN}	EN to GND Voltage	0 to 5	V
T_A	Ambient Temperature	-40 to 85	°C
T_J	Junction Temperature	-40 to 125	°C

Note 3: Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=19V, V_{EN} =5V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3540			Unit
			Min.	Typ.	Max.	
UNDER-VOLTAGE LOCKOUT (UVLO) AND SUPPLY CURRENT						
V_{UVLO}	VIN UVLO Threshold Voltage	V_{IN} rising, T_A= -40 to 85 °C	7.0	7.5	8.0	V
	VIN UVLO Hysteresis		0.3	0.4	0.5	V
$T_{D(ON)}$	Power-On Delay Time	V_{IN} >V_{UVLO}, V_{EN}=5V, and $V_{VINSEL(H)}$>V_{VINSEL}> $V_{VINSEL(L)}$	5	8.5	12	ms
I_{VIN}	VIN Supply Current	No load, V_{EN} =5V	-	750	1200	µA
		No load, V_{EN} =0V	-	400	600	µA
WRONG VIN INPUT VOLTAGE PROTECTION						
$V_{VINSEL(L)}$	VINSEL Low Detection Rising Threshold	V_{IN} rising, IC is on, V_{IN}=10V to 21V	1.223	1.275	1.305	V
	VINSEL Low Detection Falling Threshold	V_{IN} falling, IC is off, V_{IN}=10V to 21V	1.148	1.200	1.230	V
$V_{VINSEL(H)}$	VINSEL High Detection Rising Threshold	V_{IN} rising, IC is off, V_{IN}=10V to 21V	1.748	1.800	1.830	V
	VINSEL High Detection Falling Threshold	V_{IN} falling, IC is on, V_{IN}=10V to 21V	1.673	1.725	1.755	V
	VINSEL Input Current	V_{VINSEL}=40V	-	-	1	µA
	VINSEL Low Detection Debounce	V_{VINSEL} falling, V_{VINSEL} < $V_{VINSEL(L)}$	-	10	-	µs
	VINSEL High Detection Debounce	V_{VINSEL} rising, V_{VINSEL} > $V_{VINSEL(H)}$	-	10	-	µs
GATE DRIVER						
$V_{DRV-OUT}$	DRV to VOUT Voltage	V_{DRV}-V_{OUT}, V_{IN}=19	4.3	4.6	4.9	V
	DRV Source Current	V_{DRV}=10V, V_{DRV}-V_{OUT}=2.5	155	185	215	µA
	DRV Discharge Resistance	Any fault condition and shutdown (connected from DRV to VOUT), V_{DRV}=5V, V_{OUT}=GND	1.8	2.0	2.2	kΩ
PROTECTIONS						
	Under-Voltage Protection Threshold	V_{OUT} falling, V_{OUT}/V_{IN}	65	70	75	%
	Under-Voltage Protection Debounce		-	5	-	µs
I_{OCSET}	OCSET Source Current	No load, V_{VINSEL}=1.5V, V_{EN}=5V, V_{OCSET}=18.9V	45	50	55	µA
	OCSET Offset Voltage		-10	0	10	mV
	Over-Current Debounce		-	10	-	µs

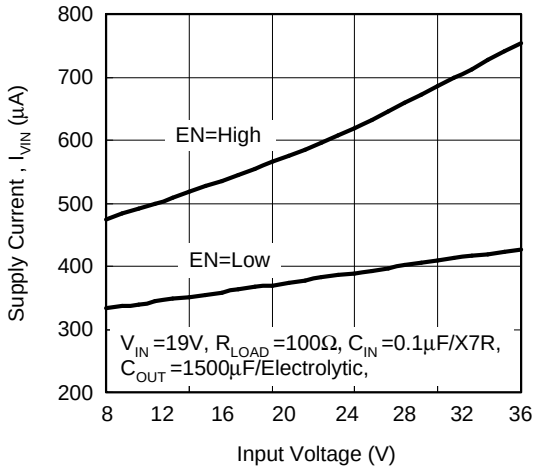
Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{IN}=19V, V_{EN} =5V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

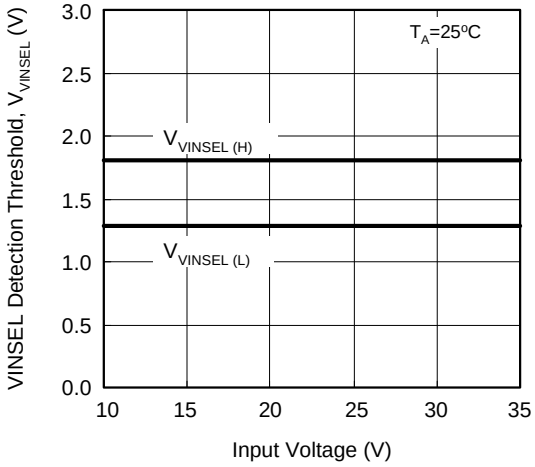
Symbol	Parameter	Test Conditions	APL3540			Unit
			Min.	Typ.	Max.	
PROTECTIONS (CONT.)						
$V_{DRV(SC)}$	Short Circuit Protection Threshold Accuracy	V_{DRV} -V_{OUT} SCP threshold tunable range: 2.5~3.5V, 0.1V/step	-100	-	+100	mV
	VOUT Input Current	V_{OUT}=19V	-	60	80	μA
	VOUT Discharge Resistance	Any fault condition and shutdown, V_{OUT}=1V	1.5	1.75	2.0	kΩ
EN INPUT						
	EN Logic High Threshold Voltage	V_{IN}=10V to 21V	0.8	-	1.5	V
	EN Hyteresis		-	0.2	-	V
	EN Pull-up Current		-	5	-	μA
POK OUTPUT						
$V_{POK(TH)}$	POK Threshold	V_{OUT} rising, V_{OUT}/V_{IN}, V_{POK}=High	85	90	95	%
	POK Hysteresis	V_{OUT} falling, V_{POK}=Low	-	5	-	%
	POK Low Voltage	I_{POK}=10mA	-	0.2	0.5	V
	POK Leakage Current	V_{POK}=40V	-	-	1	μA
$T_{D(POK)}$	POK Rising Delay Time	V_{OUT} rising, POK assertion	8	11.5	15	ms

Typical Operating Characteristics

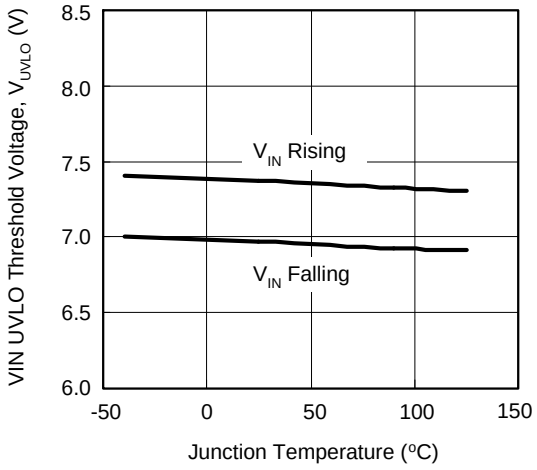
Supply Current vs. Input Voltage



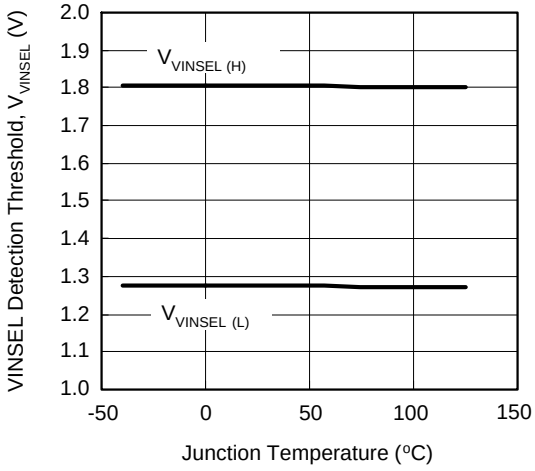
VINSEL Detection Threshold Voltage vs. Input Voltage



VIN UVLO Threshold Voltage vs. Junction Temperature



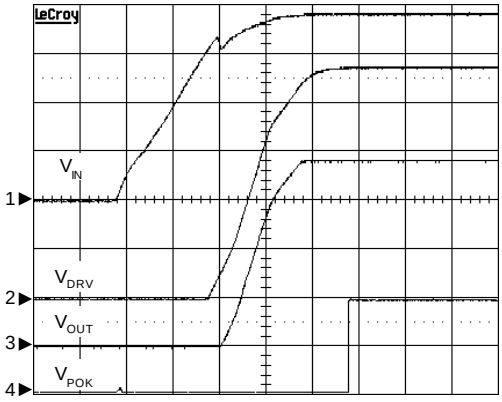
VINSEL Detection Threshold Voltage vs. Junction Temperature



Operating Waveforms

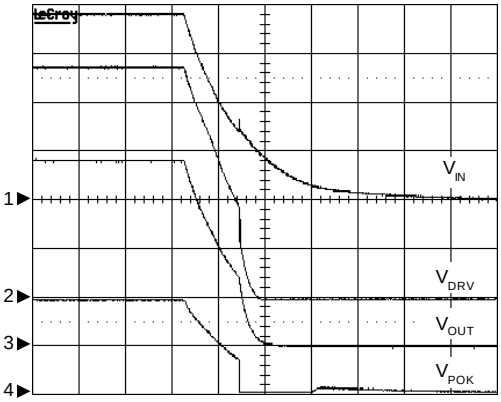
The test condition is V_{IN}=19V, T_A=25°C unless otherwise specified.

Power On



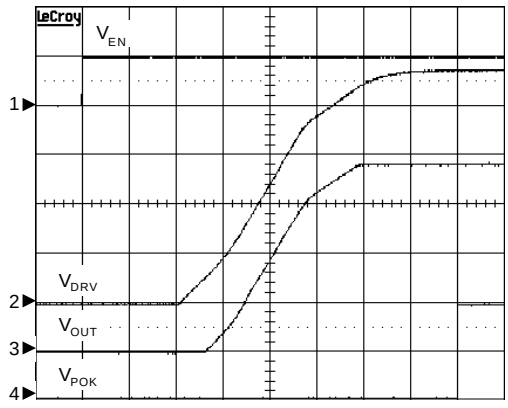
V_{IN} =19V, R_{LOAD} =100Ω, R3 =51kΩ,
C_{IN} =0.1µF/X7R, C_{OUT} =1500µF/Electrolytic,
CH1: V_{IN}, 5V/Div, DC
CH2: V_{DRV}, 5V/Div, DC
CH3: V_{OUT}, 5V/Div, DC
CH4: V_{POK}, 10V/Div, DC
TIME: 10ms/Div

Power Off



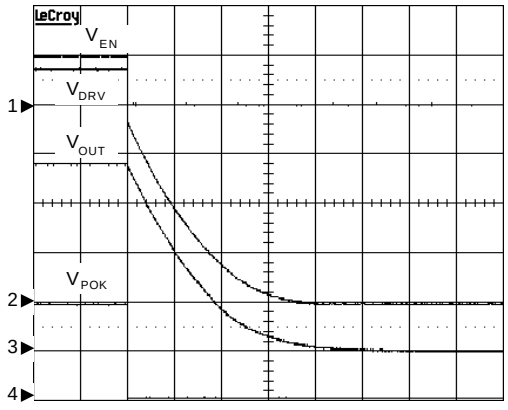
V_{IN} =19V, R_{LOAD} =100Ω, R3 =51kΩ,
C_{IN} =0.1µF/X7R, C_{OUT} =1500µF/Electrolytic,
CH1: V_{IN}, 5V/Div, DC
CH2: V_{DRV}, 5V/Div, DC
CH3: V_{OUT}, 5V/Div, DC
CH4: V_{POK}, 10V/Div, DC
TIME: 0.5s/Div

Enable



V_{IN} =19V, R_{LOAD} =100Ω, R3 =51kΩ,
C_{IN} =0.1µF/X7R, C_{OUT} =1500µF/Electrolytic,
CH1: V_{EN}, 5V/Div, DC
CH2: V_{DRV}, 5V/Div, DC
CH3: V_{OUT}, 5V/Div, DC
CH4: V_{POK}, 10V/Div, DC
TIME: 5ms/Div

Disable

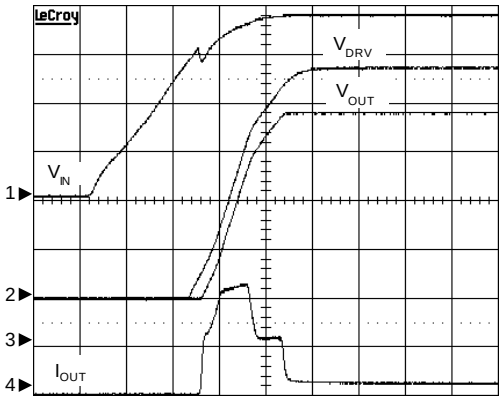


V_{IN} =19V, R_{LOAD} =100Ω, R3 =51kΩ,
C_{IN} =0.1µF/X7R, C_{OUT} =1500µF/Electrolytic,
CH1: V_{EN}, 5V/Div, DC
CH2: V_{DRV}, 5V/Div, DC
CH3: V_{OUT}, 5V/Div, DC
CH4: V_{POK}, 10V/Div, DC
TIME: 50ms/Div

Operating Waveforms (Cont.)

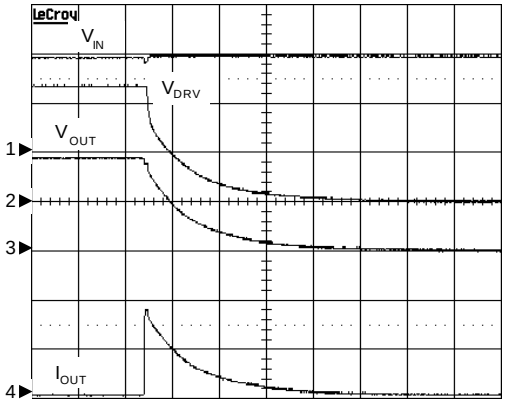
The test condition is V_{IN}=19V, T_A=25°C unless otherwise specified.

Soft-Start



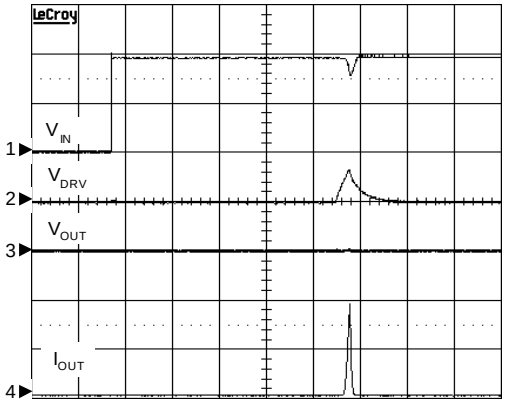
V_{IN} =19V, R_{LOAD} =100Ω, C1=100nF,
C_{IN} =0.1µF/X7R, C_{OUT} =1500µF/Electrolytic,
CH1: V_{IN}, 5V/Div, DC
CH2: V_{DRV}, 5V/Div, DC
CH3: V_{OUT}, 5V/Div, DC
CH4: I_{OUT}, 1A/Div, DC
TIME: 10ms/Div

Over-Current Protection



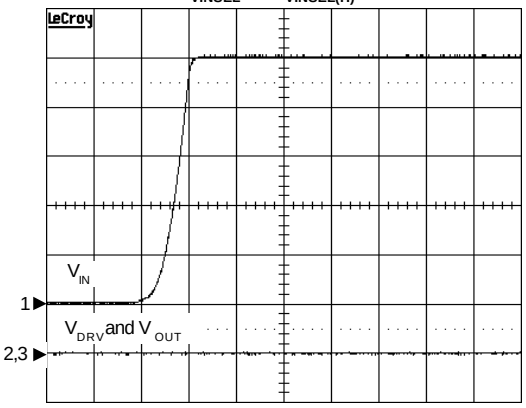
V_{IN} =19V, R_{LOAD} =1Ω, R_{OCSET} =1.5kΩ,
C_{IN} =0.1µF/X7R, C_{OUT} =470µF/Electrolytic,
CH1: V_{IN}, 10V/Div, DC
CH2: V_{DRV}, 10V/Div, DC
CH3: V_{OUT}, 10V/Div, DC
CH4: I_{OUT}, 10A/Div, DC
TIME: 0.5ms/Div

Short-Circuit Protection



V_{IN} =19V, R_{LOAD} =Short to GND before power-up,
C_{IN} =0.1µF/X7R, C_{OUT} =470µF/Electrolytic
CH1: V_{IN}, 10V/Div, DC
CH2: V_{DRV}, 5V/Div, DC
CH3: V_{OUT}, 5V/Div, DC
CH4: I_{OUT}, 10A/Div, DC
TIME: 2ms/Div

Wrong VIN Input Voltage Protection, $V_{VINSEL} > V_{VINSEL(H)}$



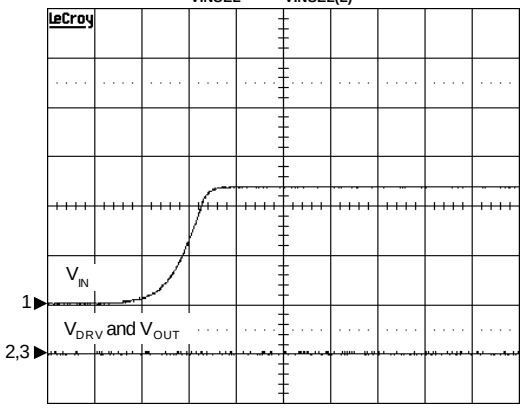
V_{IN} =25V, R1=24kΩ, R2 =2kΩ
CH1: V_{IN}, 5V/Div, DC
CH2: V_{DRV}, 5V/Div, DC
CH3: V_{OUT}, 5V/Div, DC
TIME: 50ms/Div

Operating Waveforms (Cont.)

The test condition is V_{IN}=19V, T_A=25°C unless otherwise specified.

Wrong VIN Input Voltage Protection,

$V_{VINSEL} < V_{VINSEL(L)}$



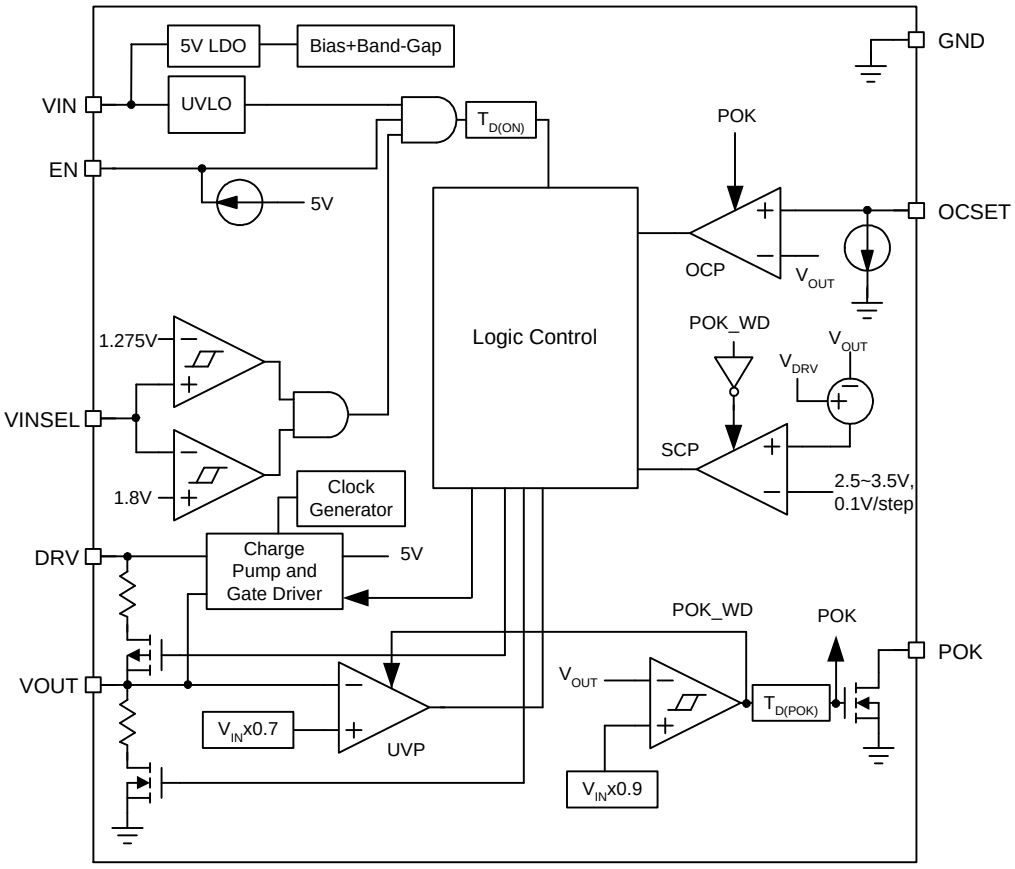
V_{IN} =12V, R1=24kΩ, R2 =2kΩ

CH1: V_{IN}, 5V/Div, DC
CH2: V_{DRV}, 5V/Div, DC
CH3: V_{OUT}, 5V/Div, DC
TIME: 20ms/Div

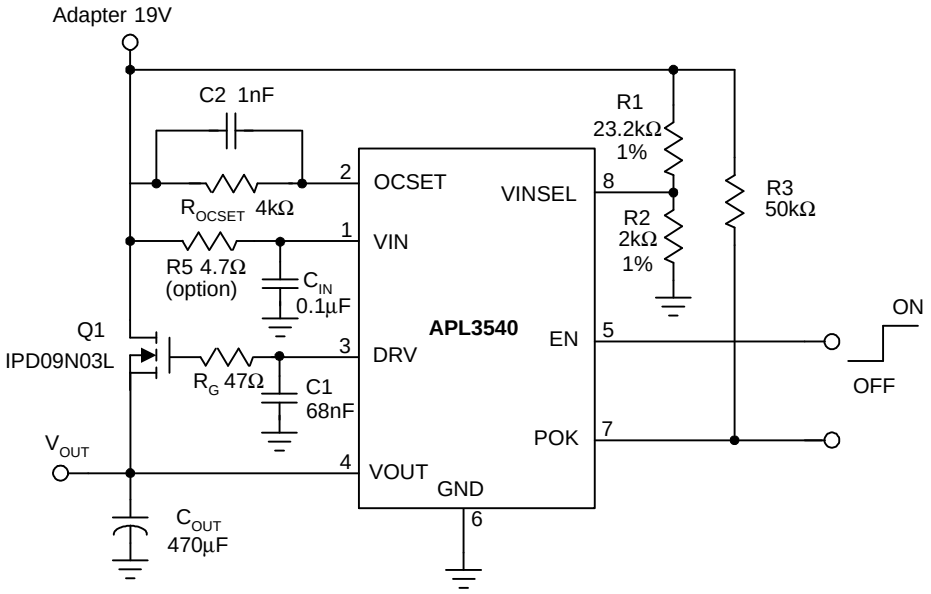
Pin Description

PIN		FUNCTION
NO.	NAME	
1	VIN	Input Supply Pin. Provides power to the IC, V_{IN} can range from 10V to 21V and should be bypassed with at least a 0.1µF capacitor.
2	OCSET	Over-Current Trip Point Adjustment Pin. Connect a resistor (R_{OCSET}) from this pin to the drain of the external MOSFET to set the OCP trip point.
3	DRV	Gate Driver Output. The gate driver for the external N-channel MOSFET.
4	VOUT	Output Voltage Sense Pin. Connect this pin to the source of external N-channel MOSFET to monitor the output voltage.
5	EN	Enable Input. Pulling the V_{EN} above 2V will enable the IC; pulling V_{EN} below 0.6V will disable the IC. This pin is pulled high by an internal current source.
6	GND	Ground.
7	POK	Power-Okay Indicator Output. The POK is an open-drain pull-down device. When VOUT voltage is below the POK threshold, the POK output is pulled low; when VOUT voltage is above the POK threshold, the POK output is high impedance.
8	VINSEL	Input Voltage Sense Pin. Connect a resistive divider from VIN to VINSEL to GND to monitor the input voltage. This pin cannot be left floating.

Block Diagram



Typical Application Circuit



Function Description

Wrong VIN Input Voltage Protection

The APL3540 provides an input voltage detection function to protect a wrong input adapter insertion. Connect a resistive divider from VIN to VINSEL to GND to set the target input voltage. The target input voltage is set at:

$V_{IN(target)}$=1.5V x (1+R1/R2)

The IC is enabled when input voltage is within the $V_{IN(target)}$ ±15% (V_{IN} also must above V_{UVLO} and EN is high); the device shuts down when input voltage is outside the $V_{IN(target)}$±20%.

Power-Up

The APL3540 has a built-in under-voltage lockout circuitry to keep the DRV output shutting off until internal circuitry operates properly. The UVLO circuit has a hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold (V_{IN} also must within the $V_{IN(target)}$±10% and EN is high) and after 7ms delay time, the DRV output starts to charge the C1.

The voltage at DRV rises with a slope equals to 185µA/C1 and the VOUT output voltage rise time is set at:

T_{SS}=C1 x V_{IN} / 185µA

where

T_{SS} is the rise time of VOUT output voltage

Under-Voltage Protection (UVP)

The VOUT pin monitors the output voltage. If the V_{OUT} is under 70% of VIN input voltage because of the short circuit or other influences, it will cause the under-voltage protection and turn off IC, the VOUT voltage is also discharged to the GND by an internal resistor, requiring a VIN UVLO or EN re-enable again to restart IC. Note that the UVP is active after the power-up and POK are asserted.

Over-Current Protection (OCP)

The APL3540 monitors the voltage across the external MOSFET and uses the OCSET pin to set the over-current trip point.

A resistor (R_{OCSET}) connected between OCSET pin and the drain of the MOSFET will determine the over current trip point. An internal 50µA current source will flow through this resistor, creating a voltage drop, which will be compared with the voltage across the MOSFET.

When the voltage across the MOSFET exceeds the voltage drop across the R_{OCSET}, an over-current will be detected.

The threshold of the over current is therefore given by:

I_{OCP}= I_{OCSET} x R_{OCSET} / $R_{DS(ON)}$

For the over-current is never occurred in the normal operating load range, the variation of all parameters in the above equation should be determined.

- The MOSFET's $R_{DS(ON)}$ is varied by temperature, the user should determine the maximum $R_{DS(ON)}$ in manufacturer's datasheet.
- The minimum I_{OCSET} (45µA) and minimum R_{OCSET} should be used in the above equation.

An over-current condition will shut down the device and pull the $V_{DRV-OUT}$ to low, the VOUT voltage is also discharged to the GND by an internal resistor, requiring a VIN UVLO or EN re-enable again to restart IC. Note that the OCP is active after the power-up and POK are asserted.

POK Output

The power okay function monitors the output voltage and drives the POK low to indicate a fault. When a fault condition such as over-current or under-voltage is occurred, the VOUT output voltage falls to 85% of VIN input voltage and the POK is pulled low. When the VOUT output voltage reaches to 90% of VIN input voltage and after 10ms delay time, the POK is pulled high. Since the POK is an open-drain device, connecting a resistor to a pull high voltage is necessary.

Short-Circuit Protection

The APL3540 monitors DRV and VOUT voltages for the short circuit detection during power-up. When the difference in voltage between DRV pin and VOUT pin is above short circuit protection threshold, a short-circuit condition is detected and the device will be shut down. Requiring a VIN UVLO or EN re-enable again to restart IC.

Caution must be taken when selecting a power MOSFET. If an unsuitable MOSFET is used, the SCP will be falsely activated during power-up. A complete power-up partly relies on the current driving capacity of the MOSFET. In the startup of V_{DRV} while gate voltage starts to rise, the MOSFET starts to conduct. If the current via the MOSFET is insufficient to supply for the needs of C_{OUT} and R_{LOAD},

Function Description (Cont.)

Short-Circuit Protection (Cont.)

the V_{OUT} voltage will not follow the V_{DRV} to rise, eventually, when V_{DRV} - V_{OUT} > short circuit protection threshold, the SCP happens. Since the C_{OUT} demands the most current during power-up, the supplying current via the MOSFET should satisfy the following equation for a completion of power-up.

$I_{SUPPLY(max)} > I_{CHARGING}$

where:

$I_{CHARGING} = C_{OUT}$ x (185µA/C1)

- $I_{SUPPLY(max)}$ is the maximum supply current via the MOSFET in the conditions of V_{GS} = short circuit protection threshold and $V_{DS} = V_{IN} - V_{OUT}$.
- $I_{CHARGING}$ is the charging current of C_{OUT} during soft-start.
- C_{OUT} is output capacitor.
- C1, placed on the gate of MOSFET is the capacitor that controls the ramp-up rate of output voltage during soft-start.
- 185µA is the soft-start current driving from the DRV pin during the power-up process.

For example, If C_{OUT}=1500µF, C1=100nF, short circuit protection threshold=3.0V and V_{IN}=19V, the $I_{CHARGING}$ demanded by the output capacitor is 2.78A. The $I_{SUPPLY(max)}$ in the conditions of V_{GS} = 3.0V and V_{DS} = 19V (while V_{IN} -V_{OUT} V_{IN}) should be greater than the $I_{CHARGING}$. We set the safety margin that is 1.5 times greater than the demanded 2.78A, therefore, we can choose a MOSFET that can deliver at least 4.17A in such conditions.

Shutdown Control

The APL3540 has an active-low shutdown function. Pulling the V_{EN} above 2V will enable the IC; pulling V_{EN} below 0.6V will disable the IC and the POK is pulled low immediately (ignore the $V_{POK(TH)}$ and $T_{D(POK)}$), the VOUT voltage is also discharged to the GND by an internal resistor. EN pin is pulled high by an internal current source and can be left floating.

Application Information

Input Capacitor

While hot plug-in an AC adapter, the inductive peak voltage seen in the VIN pin could be very high if there is no any filtering measure taken. It is recommended to place a 0.1 to 1μF ceramic bypass capacitor as close as possible to the VIN pin. An RC-filter, depicted in the application circuit, is preferable because better performance in filtering the peak voltage and noise. Note that the voltage rating of the input capacitor must be greater than the maximum V_{IN} voltage.

Gate and Output Capacitor

It is recommended to place a capacitor in the gate of external power MOSFET to control the soft-start rate of output voltage, especially when a high-value output capacitor is used. The gate capacitor can reduce the inrush current to the output capacitor during soft-start. If the power supply cannot support the inrush current, the C_{OUT} voltage will be clamped during soft-start and SCP will be falsely activated. The inrush current must be controlled within power supply current capability by using this gate capacitor. Note that the voltage rating of the gate capacitor must be greater than the maximum V_{DRV} voltage, where the V_{DRV} approximately equals V_{IN}+5V.

A bulk output capacitor, placed close to the load, is recommended to support load transient current. Precautions should be taken when a high-value output capacitor is used the gate capacitor C1 (shown in the application circuit) must be matched. A high-value output capacitor with a small-value C1 would probably lead to inrush current and end up SCP latched-off in the soft-start period. Please make sure that the gate capacitor C1 is matched with a high-value output capacitor. Note that the voltage rating of the output capacitor must be greater than the maximum V_{IN} voltage.

Gate Resistor

It is recommended to place a resistor R_G, as shown in the Typical Application Circuit, in the gate of external power MOSFET to prevent occurrence of oscillation during powering on. If the oscillation occurs, the SCP or VINSEL wrong voltage detection might be activated unexpectedly. The R_G literally could stabilize the external MOSFET to avoid oscillation. The R_G can be in the range of 10~100Ω. The recommended value is 47Ω.

Power MOSFETs

APL3540 requires an N-channel MOSFET that is utilized as an on/off switch. When a MOSEFT is selected, please make sure that the $R_{DS(ON)}$ of this MOSFET can meet your maximum voltage droop requirement in full load conditions. And also make sure that the MOSFET you select can satisfy the current delivering requirement, described in the paragraph of Short-Circuit Protection in Function Description. Another important criterion for selection of MOSFET is the MOSFET must be operated within its safe operation area in your application. The package type of the MOSFET must be chosen for efficient heat removal. Note that the V_{DS} rating of the MOSFET you selected must be greater than the V_{IN} voltage and the V_{GS} rating must be greater than V_{IN}+5V. The power dissipated in the MOSFET while on is shown in the following equation:

$$P_D = I_O^2 \times R_{DS(on)}$$

Select a package type and heatsink that maintains the junction temperature below the rating.

Layout Consideration

Figure 1 illustrates the layout, with bold lines indicating high current paths; and these traces must be short and wide. The layout guidelines are listed as below.

1. Place the input capacitors C_{IN} for VIN near pin as close as possible.
2. The trace from DRV to the gate of power MOSFETs should be wide and short.
3. Place output capacitor C_{OUT} near the load as close as possible.
4. Large current paths must have wide and thick traces, depicted as the bold lines.
5. The drain of the power MOSFETs should be a large plane for heatsinking.

Application Information (Cont.)

Layout Consideration (Cont.)

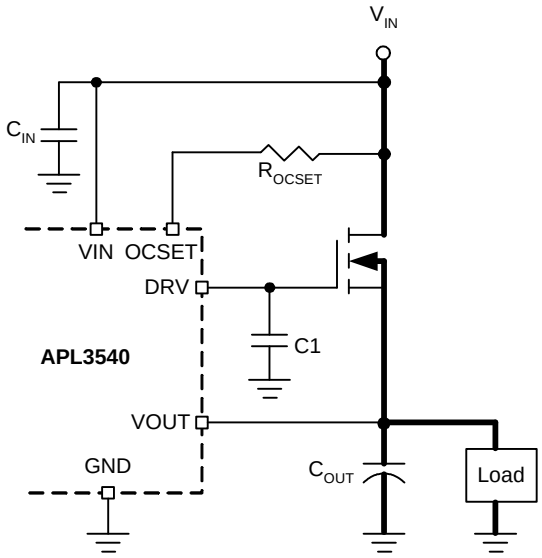
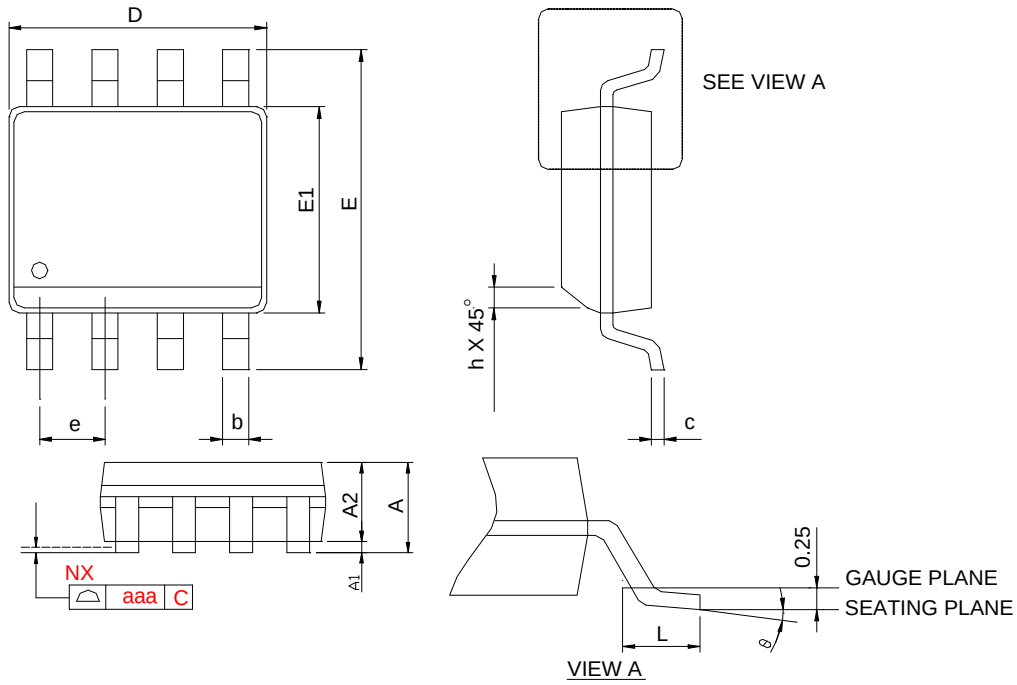


Figure 1. Layout Guidelines

Package Information

SOP-8

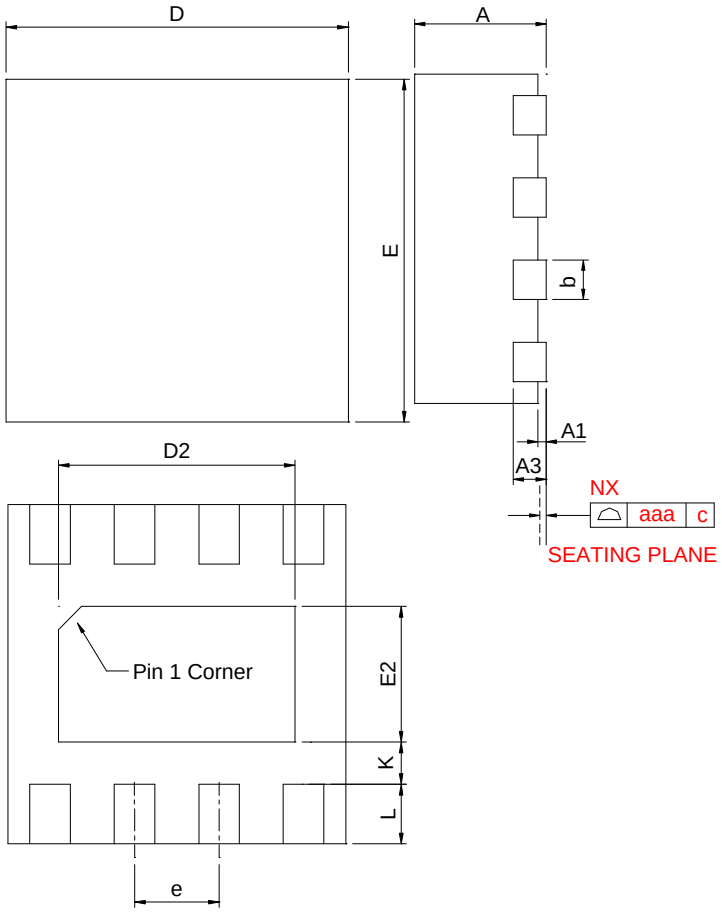


SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
aaa	0.10		0.004	

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

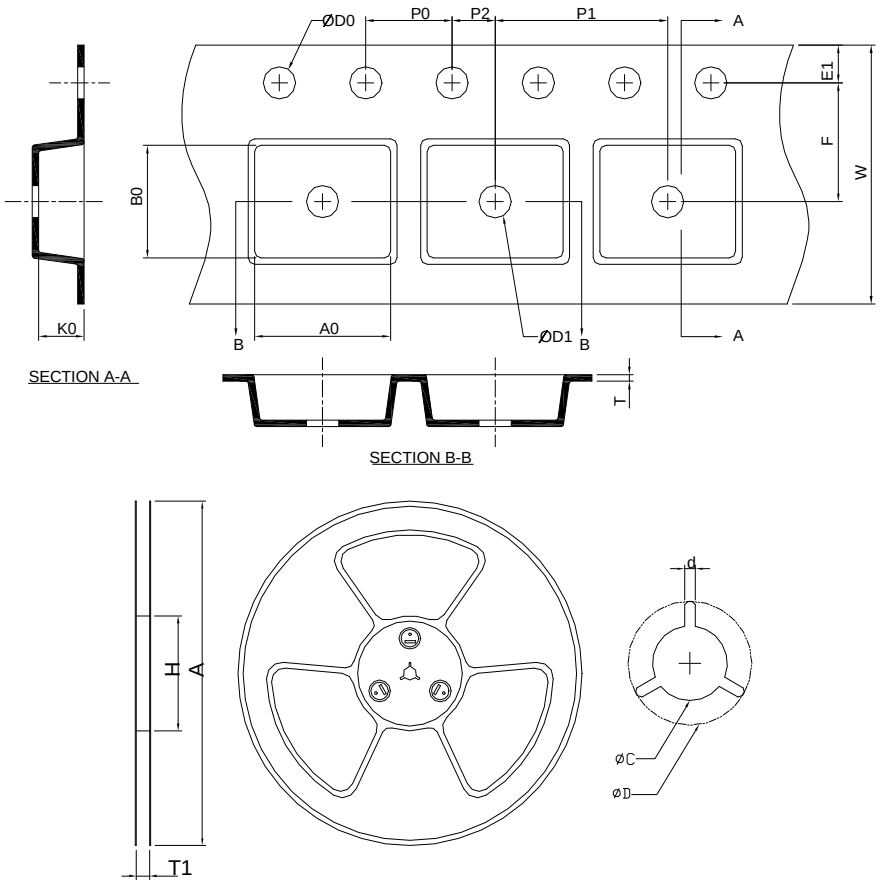
TDFN2x2-8



SYMBOL	TDFN2x2-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.50 BSC		0.020 BSC	
L	0.30	0.45	0.012	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-229 WCCD-3.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TDFN2x2-8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.50±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.4	3.35 MIN	3.35 MIN	1.30±0.20

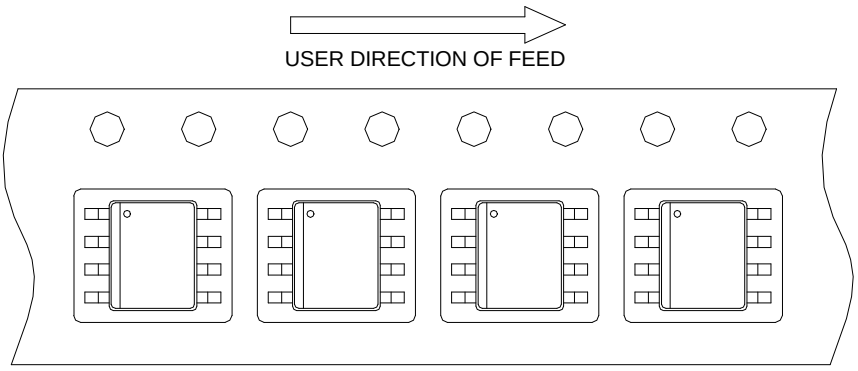
(mm)

Devices Per Unit

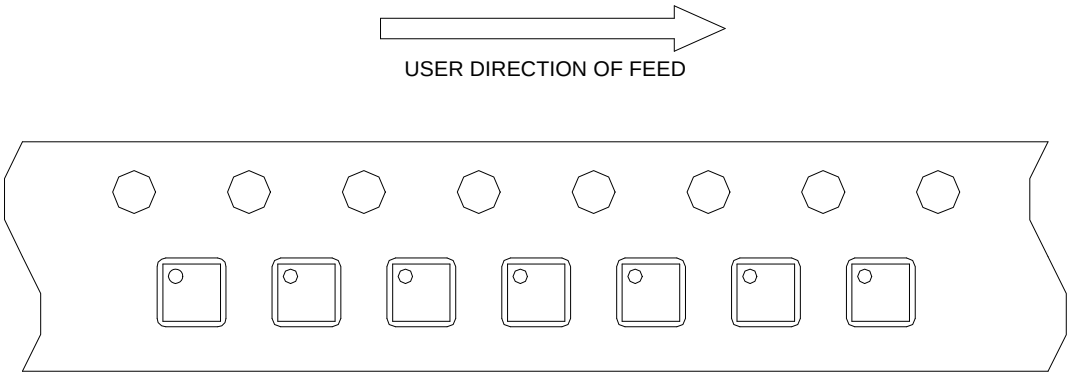
Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500
TDFN2x2-8	Tape & Reel	3000

Taping Direction Information

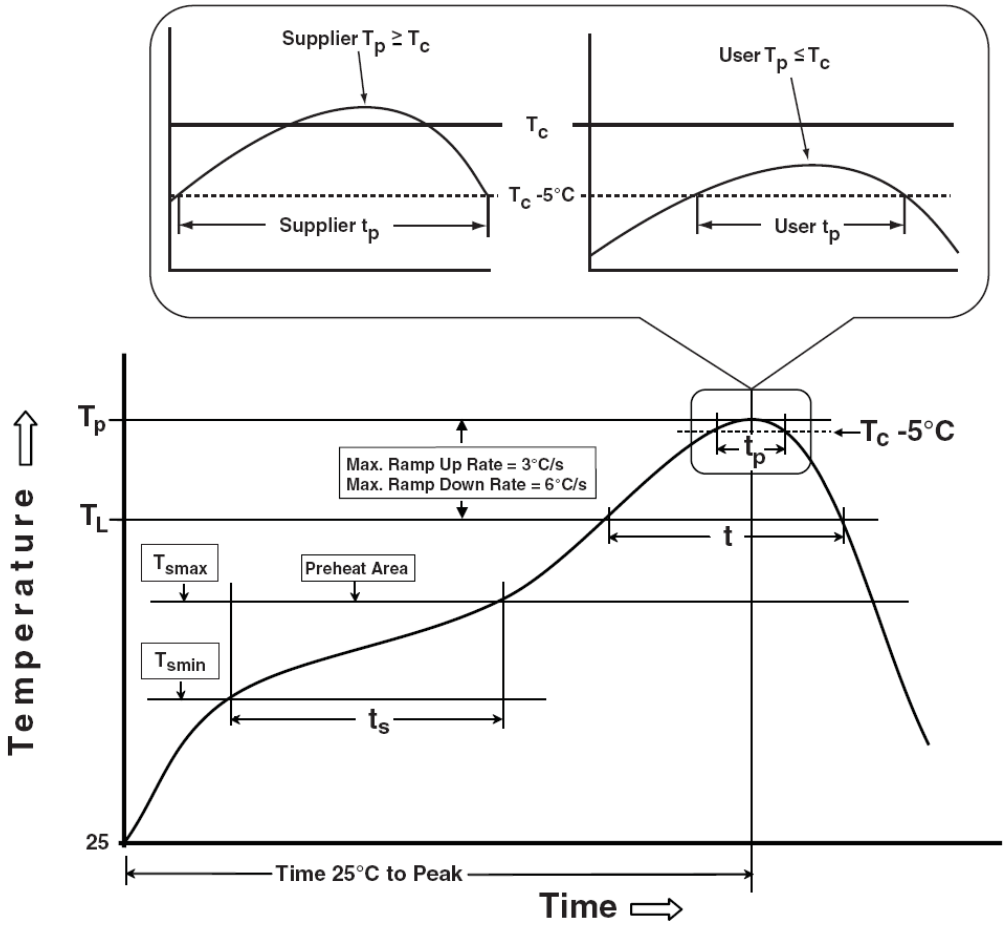
SOP-8



TDFN2x2-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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