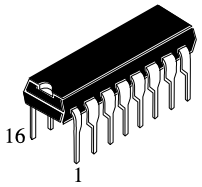
Stepping Motor Driver IC

IK6502

General Description

IK6502 is stepping motor driver ICs with MOS output transistors.

The ICs can control two-phase stepping motor forward and reverse by bipolar driving. They have a power-saving circuit and a standby circuit.



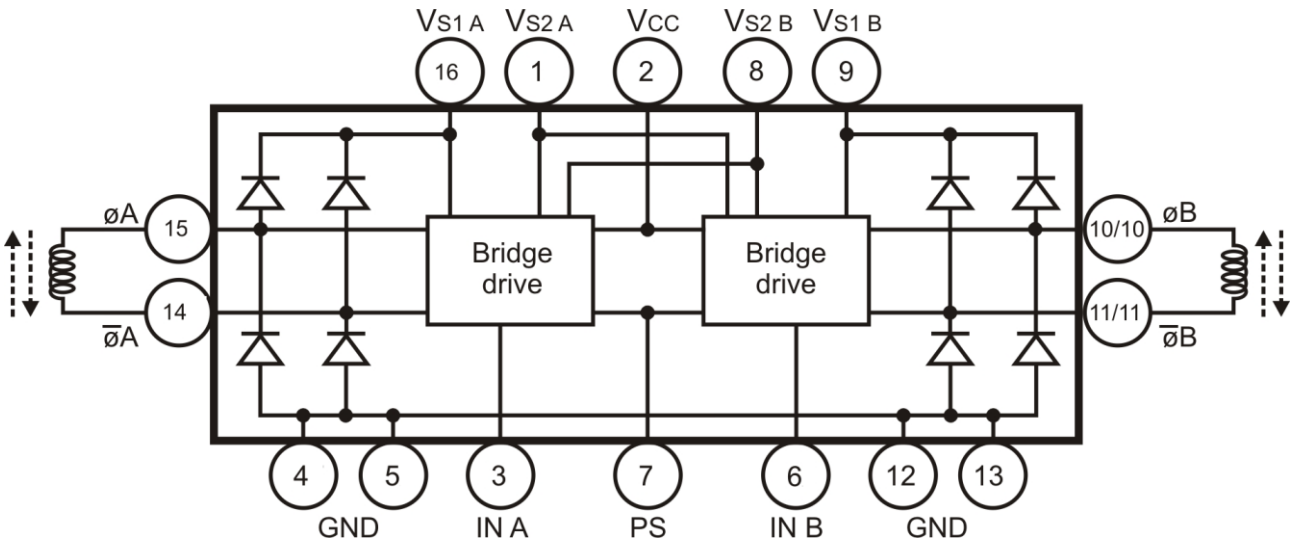
Ordering Information

IK6502N DIP-16

Features

- They are similar substituting products of TB6674.
  Both products have same packages and same pin assignments.
- One-chip two-phase bipolar stepping motor driver (including two bridge drivers)
- Power saving operation is available
- Standby operation is available
  Current consumption ≤ 20 μA (typ.)
- Built-in punch-through current restriction circuit for system reliability and noise suppression
- TTL-compatible inputs INA, INB, PS, and V_{S2B} terminals
- ON resistance PS = L: 3.0 Ω (Typ.)
  PS = H: 8.5 Ω (Typ.)
- High driving ability
  : $I_{O\ (START)}$ 350 mA (MAX.): V_{S1} ENABLE
  : $I_{O\ (HOLD)}$ 100 mA (MAX.): V_{S2} ENABLE
- Typical PKG DIP16
- GND terminal = HEAT SINK
- Over current shutdown circuit (ISD)
- Thermal shutdown circuit (TSD)
- Under voltage lockout circuit (UVLO)
- Pull-down resistance for input terminal (250 kΩ)

Block Diagram



Pin Description

Pin	No.	Symbol
1	V_{S2A}	Low-voltage power supply terminal
2	V_{CC}	Power voltage supply terminal for control
3	IN A	A-ch forward rotation / reverse rotation signal terminal, Truth Table 1
4	GND	GND terminal
5	GND	GND terminal
6	IN B	B-ch forward rotation / reverse rotation signal terminal, Truth Table 1
7	PS	Power saving signal input terminal
8	V_{S2B}	Standby signal input terminal, Truth Table 2
9	V_{S1B}	High-voltage power supply terminal
10	φB	Output B
11	$\Phi\overline{B}$	Output $\overline{B}$
12	GND	GND terminal
13	GND	GND terminal
14	$\Phi\overline{A}$	Output $\overline{A}$
15	φA	Output A
16	$V_{S1\ A}$	High-voltage power supply terminal

Truth Table 1

Input		Output		
PS	**IN**	**φ**	**$\bar{\Phi}$**	
L	L	L	H	ENABLE V_{S1}
L	H	H	L	ENABLE V_{S1}
H	L	L	H	ENABLE V_{S2} (Power saving)
H	H	H	L	ENABLE V_{S2} (Power saving)

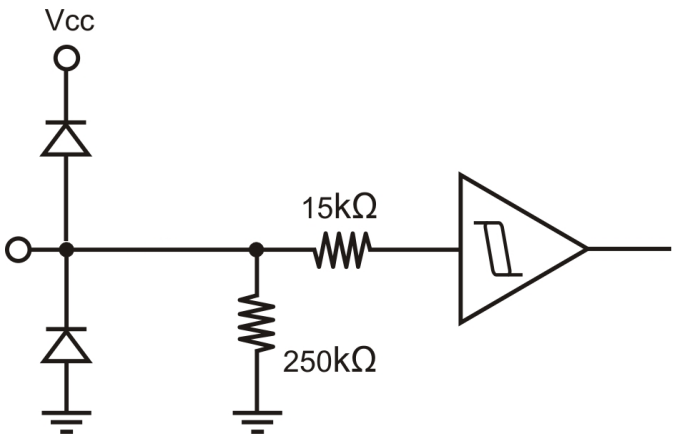
Truth Table 2

V_{S2B}	**Mode**
L	POWER OFF (Standby mode)
H	OPERATION

Note: Apply 5V to V_{S2A} as a supply terminal.

Terminal circuit

Input terminal
(INA, INB, PS, and V_{S2B})



The diagram is partly-provided and omitted or simplified for explanatory purposes.

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Supply voltage		V_{CC}	6.0	V
		V_{S1}	24.0	
		V_{S2}	Up to V_{CC}	
Output current	IK6502N	$I_{O\ (PEAK)}$	±400	mA
		$I_{O\ (START)}$	±350	
		$I_{O\ (HOLD)}$	±100	
Input voltage		V_{IN}	Up to V_{CC}	V
Power dissipation	IK6502N	P_D	1.4 (Note 1)	W
			2.7 (Note 2)	
Operating temperature		Topr	-30 to 75	°C
Storage temperature		Tstg	-55 to 150	°C

Note 1: IC only
Note 2: This value is obtained if mounting is on a 50 mm × 50 mm × 0.8 mm PCB, 60 % or more of which is occupied by copper.

Operating Conditions (Ta = 25°C)

Characteristic		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		VCC	4.5	-	5.5	V
		V_{S1}	8.0	-	22.0	
		V_{S2A}	2.7	-	5.5	
Output current	IK6502N	I_O	-	-	±350	mA
Input voltage		V_{IN}	0	-	V_{CC}	V
Maximum frequency of input pulse		f_{IN}	-	-	25	kHz
Minimum resolution of input pulse		tw	20	-	-	μs

Value of ON resistance tends to increase when the difference between V_{S1} and V_{S2A} becomes 5 V or less.

Electrical Characteristics

Unless otherwise specified, Ta = 25°C, V_{CC} = 5 V, V_{S1} = 12 V, and V_{S2A} = 5 V

Characteristic		Symbol	Test Cir-cuit	Test Condition		Min	Typ.	Max	Unit
Supply current		I_{CC1}	1	PS: H, V_{S2B}: H			3	5	mA
		I_{CC2}		PS: L, V_{S2B}: H			3	5	
		I_{CC3}		V_{S2B}: L			1	20	μA
Input voltage	High	$V_{IN\ H}$		INA, INB, PS, V_{S2B}		2.0		Vcc	V
	Low	$V_{IN\ L}$				-0.2		0.8	
Input hysteresis voltage*		V_{IN}hys	1				90		mV
Input current		$I_{IN\ (H)}$	1	INA, INB, PS, V_{S2B} V_{IN} = 5.0 V Built in pull-down resistance		5	20	38	μA
		$I_{IN\ (L)}$		V_{IN} = 0 V				1	μA
Output ON resistance (Note)	IK6502N	Ron $_{1H}$	2	PS: L, V_{S2B}: H	I_{OUT}=400mA		3	5	Ω
		Ron $_{2H}$	3	PS: H, V_{S2B}: H	I_{OUT}=100mA		8.5	16	
		Ron $_{L}$	2	V_{S2B}: H	I_{OUT}=400mA		0.9	3.5	
Diode forward voltage		$V_{F\ U}$	4	I_F = 350 mA, PS = L			1.2	2.5	V
		$V_{F\ L}$					1.0	2.2	
Delay time		tp_{LH}		IN − φ			0.5		μs
		tp_{HL}					0.5		
Thermal shutdown circuit*		TSD		(Design target only)			160		°C
TSD hysteresis *		TSDhys		(Design target only)			20		°C

* ： IK Semicon does not implement testing before shipping.

Under voltage Lockout Circuit (UVLO)

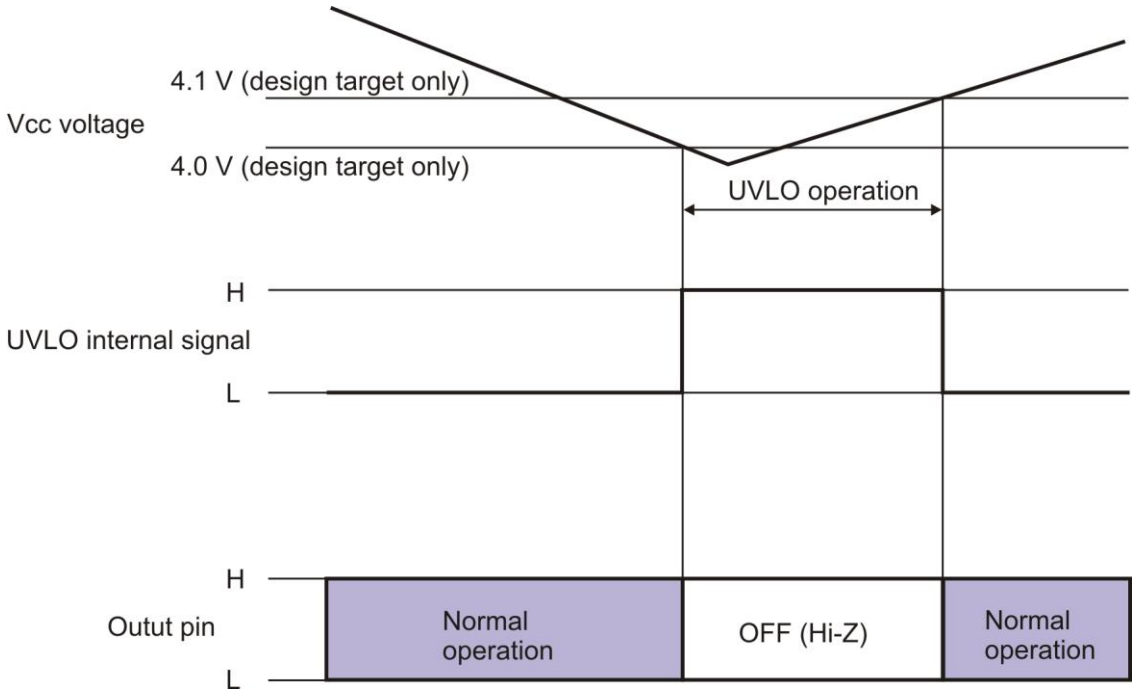
The IK6502 incorporates an under voltage lockout circuit.
Outputs are turned off (Hi-Z) under the conditions as follows;

V_{CC} ≤ 4.0 V (Design target) or
V_{S1A} ≤ 6.0 V (Design target) and V_{S1B} ≤ 6.0 V (Design target) or
V_{S2A} ≤ 2.2 V (Design target)

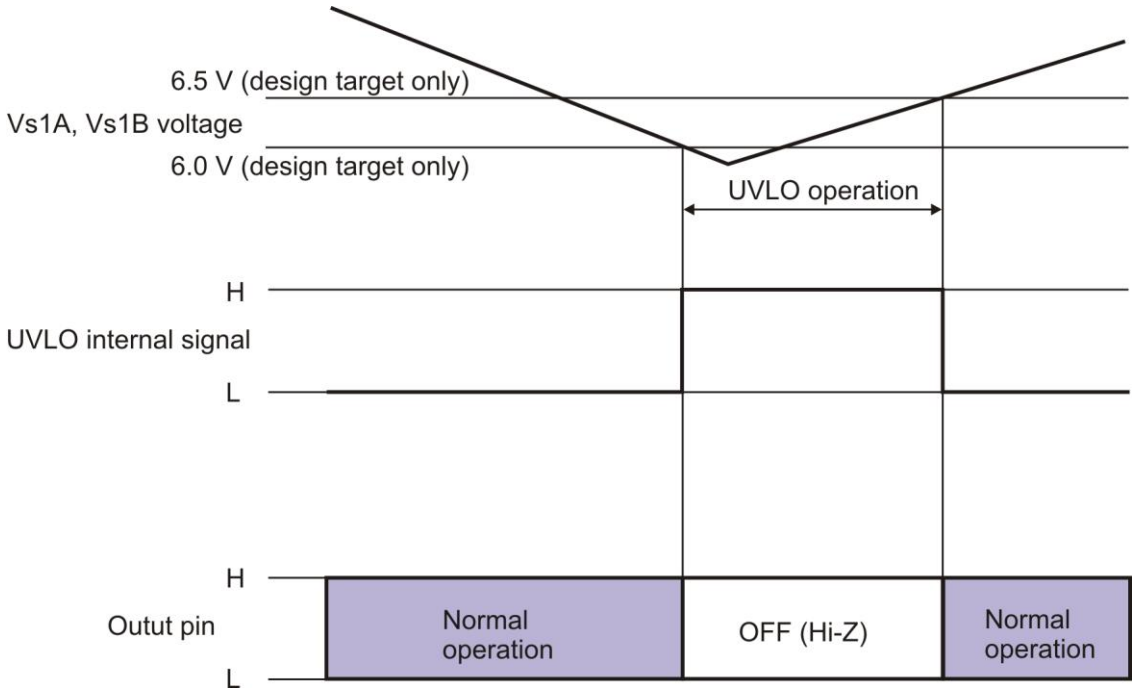
The UVLO circuit has a hysteresis and the function recovers under the conditions as follows;

V_{CC} = 4.1 V (Design target), $V_{S1A/\ VS1B}$ = 6.5 V (Design target), V_{S2A} = 2.3 V (Design target)

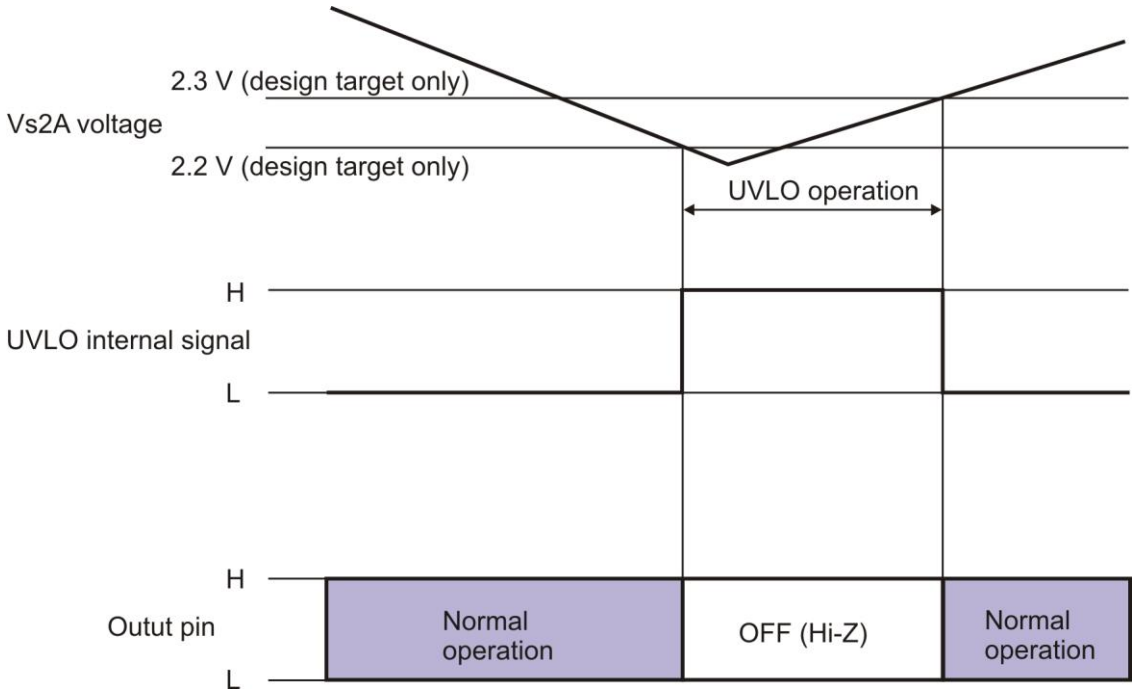
UVLO operation



UVLO operation



UVLO operation



Over Current Protection (ISD) Circuit

The IC incorporates the over current protection circuit that monitors the current flowing through each output power transistor. If a current, which is out of the detecting current, is sensed at any one of these transistors, all output transistors are turned off (Hi-Z). (However, ISD is not incorporated in upper PchDMOS when PS is high level (V_{S2A} is 5V usage) because ON resistance is large.

Masking time is 20 µs. The operation does not recover automatically (latch method). There are two recovery methods written below.

(1) Power monitor turns on when any of the power supply decreases and reaches the specified voltage.

(2) V_{S2B} is set low level for 20 µs or more and then set high. The operation recovers in 10 µs.

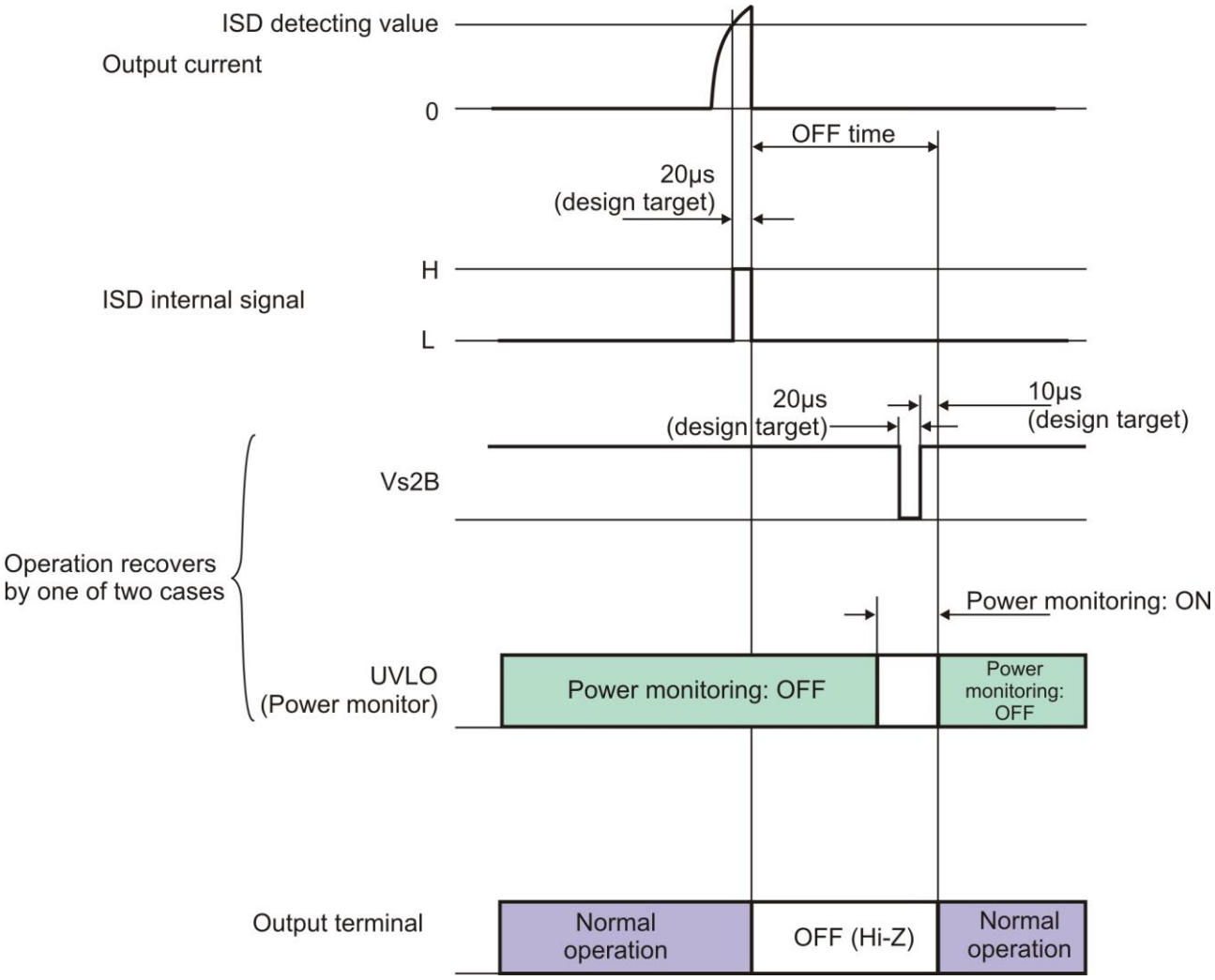
Reference design target of detecting current is as follows;

PS = L, V_{S1A} (12 V) : PchDMOS = 0.8 A

PS = H/PS = L in common : Lower NchDMOS = 1.1 A

Please reduce the external noise to prevent malfunction for ISD.

ISD operation



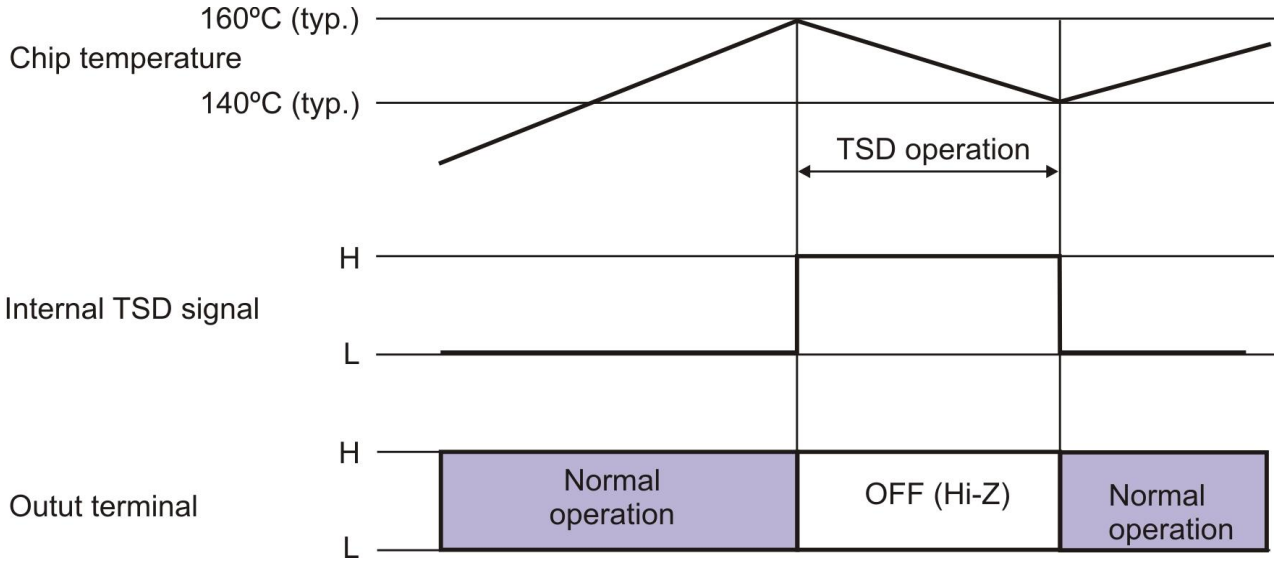
Thermal Shutdown Circuit (TSD)

The IK6502 incorporates a thermal shutdown circuit. If the junction temperature (Tj) exceeds 160°C (design target only), all the outputs are tuned off (Hi-Z).

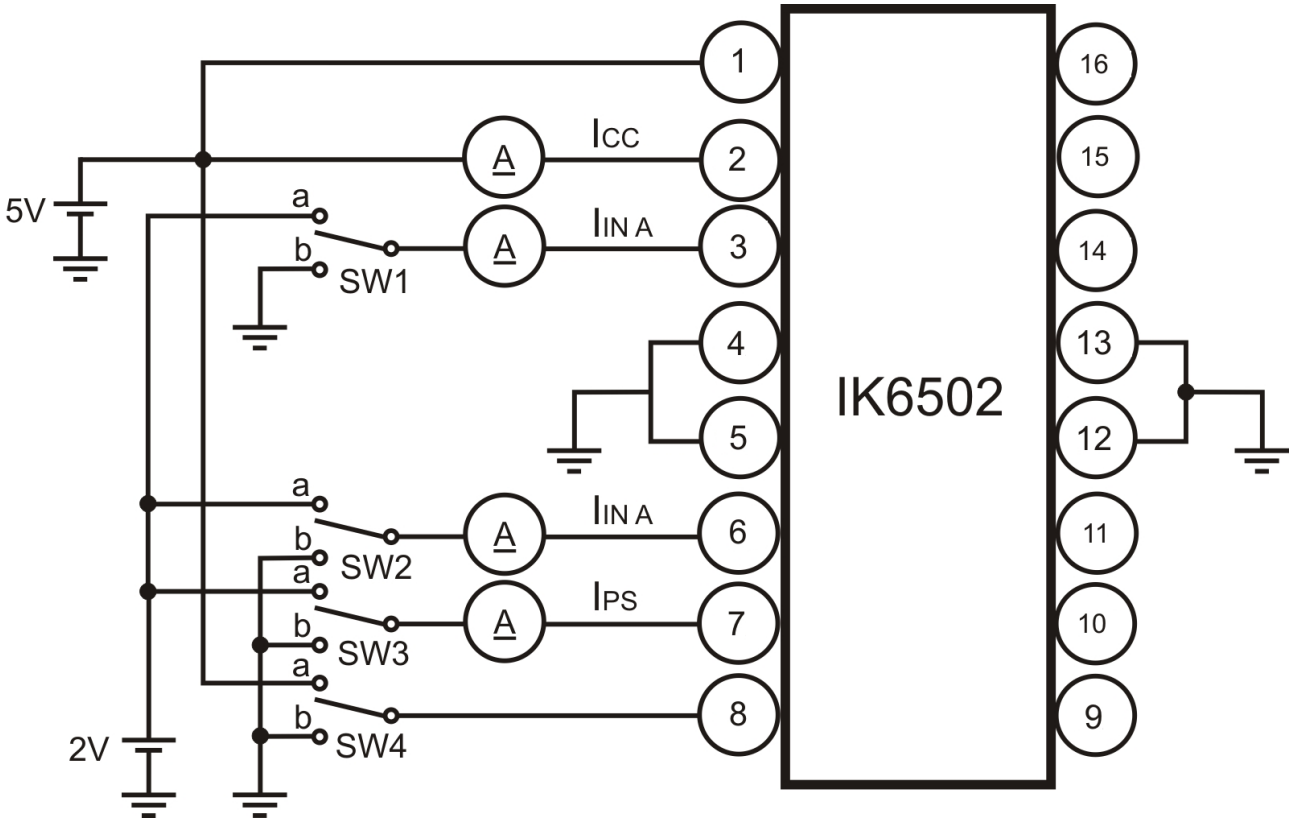
It recovers automatically at 140ºC. It has a hysteresis width of 20ºC.

TSD = 160°C (design target only)

TSD operation



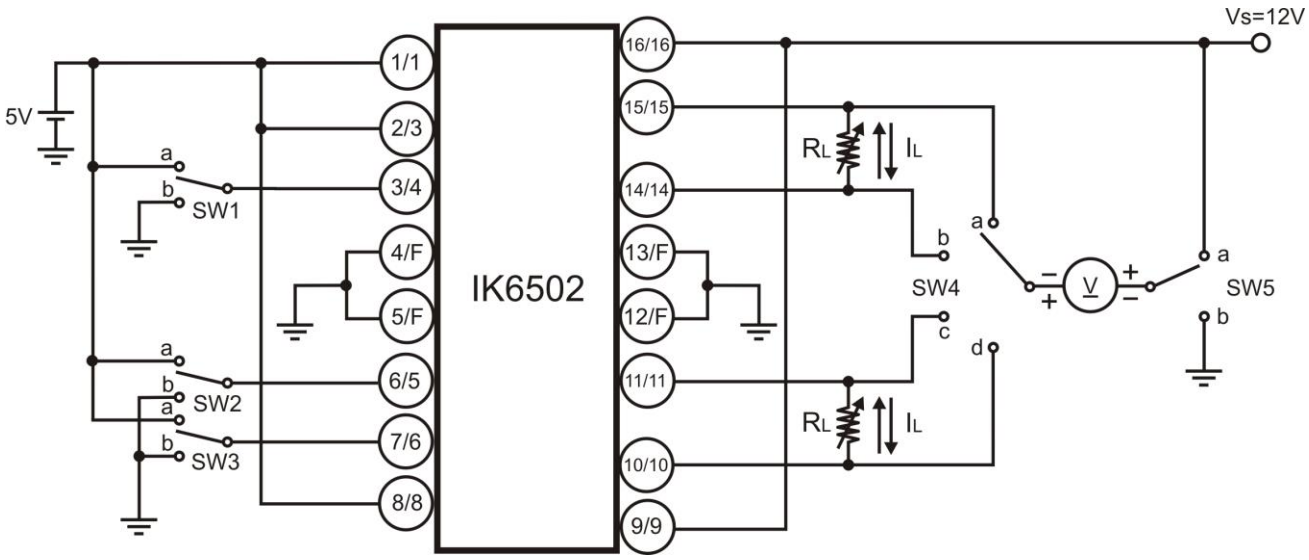
Test Circuit 1. I_{CC1}, I_{CC2}, I_{CC3}, $I_{IN\ A}$, $I_{IN\ B}$, and I_{PS}



Item	SW_1	SW_2	SW_3	SW_4
I_{CC1}	b	b	a	a
I_{CC2}	b	b	b	a
I_{CC3}	b	b	—	b
$I_{IN\ A}$	a	—	—	a
$I_{IN\ B}$	—	a	—	a
I_{PS}	—	—	a	a

All terminals of INA, INB, and PS should output low or be connected to the ground terminal in measuring I_{CC3}.

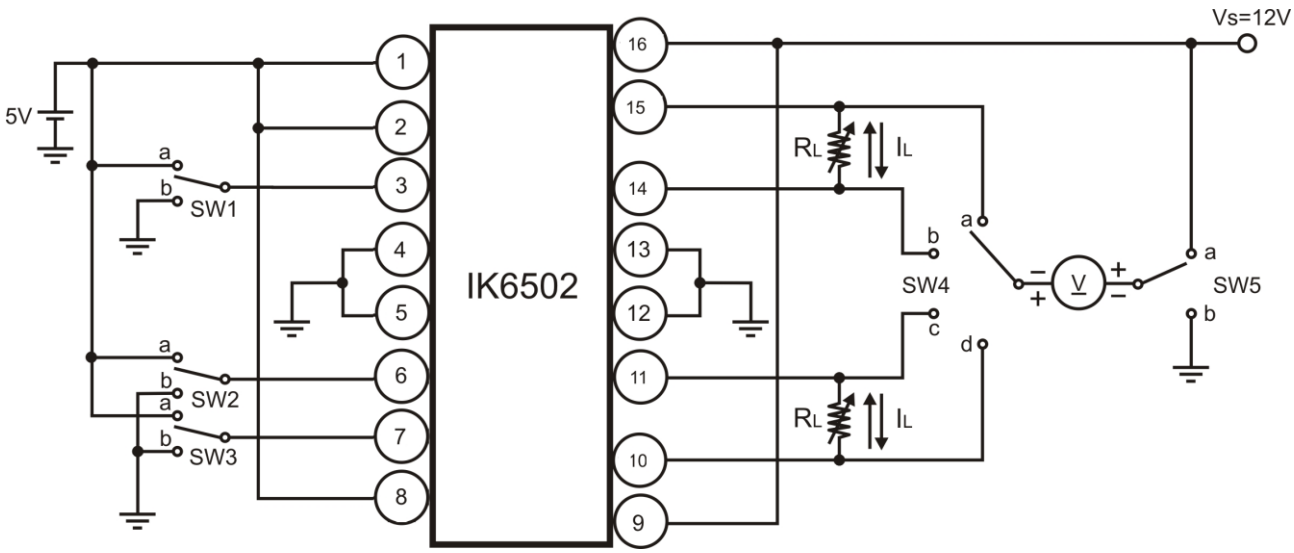
$_{\text{Test Circuit 2. Ron}}$1H1, $_{\text{Ron}}$1H2, $_{\text{Ron}}$L2, $_{\text{and Ron}}$L3



*: Adjust R_L to correspond to I_L.

Item	SW_1	SW_2	SW_3	SW_4	SW_5	I_L (mA)
$V_{SAT\ 1H1}$	a	—	b	a	a	100
	b	—		b		
	—	a		d		
	—	b		c		
$V_{SAT\ 1H2}$	a	—	b	a	a	400
	b	—		b		
	—	a		d		
	—	b		c		
$V_{SAT\ L2}$	a	—	—	b	b	100
	b	—		a		
	—	a		d		
	—	b		c		
$V_{SAT\ L3}$	a	—	b	b	b	400
	b	—		a		
	—	a		d		
	—	b		c		

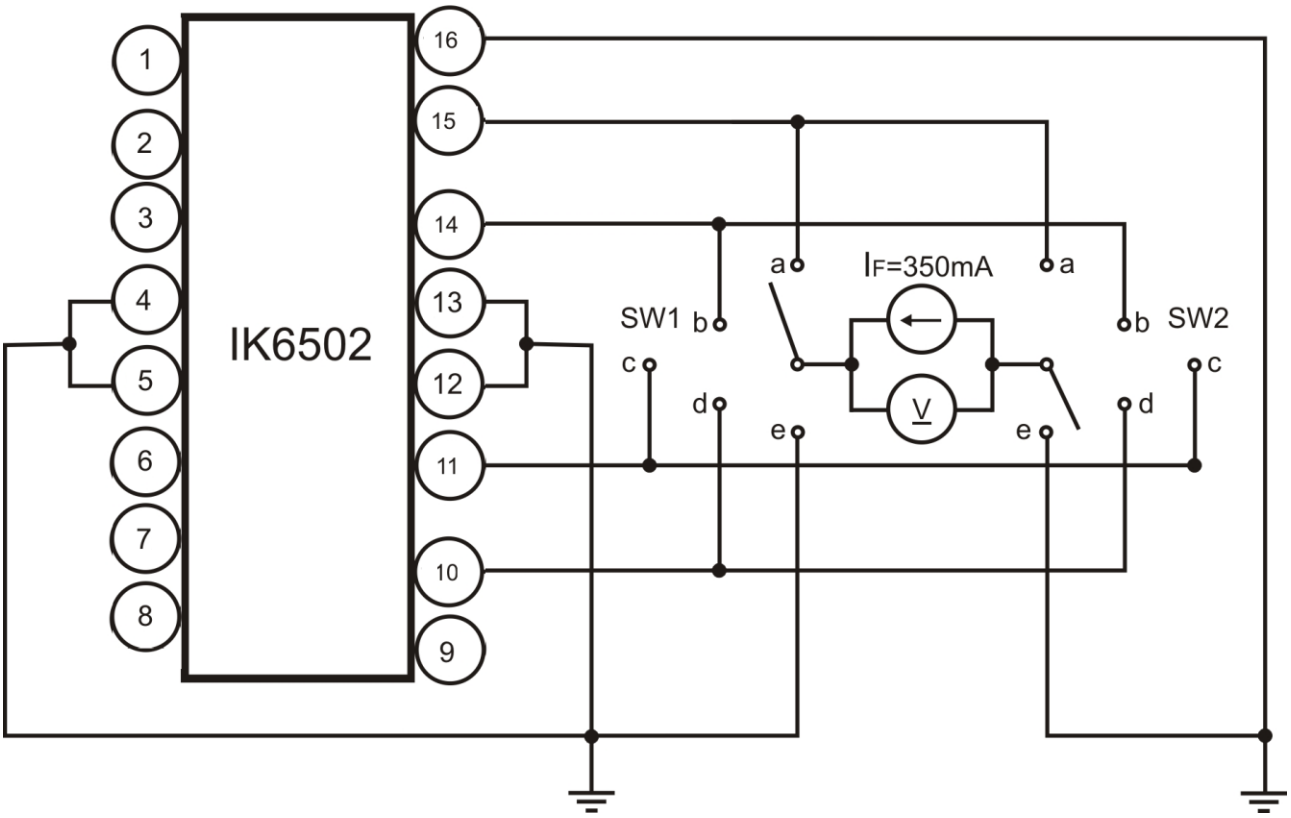
Test Circuit 3. Ron $_{2H1}$, Ron $_{2H2}$, and Ron $_{L1}$



*: Adjust R_L to correspond to I_L.

Item	SW_1	SW_2	SW_3	SW_4	SW_5	I_L (mA)
$V_{SAT\ 2H1}$	a	—	a	a	a	20
	b	—		b		
	—	a		d		
	—	b		c		
$V_{SAT\ 2H2}$	a	—	a	a	a	100
	b	—		b		
	—	a		d		
	—	b		c		
$V_{SAT\ L1}$	a	—	a	b	b	20
	b	—		a		
	—	a		c		
	—	b		d		

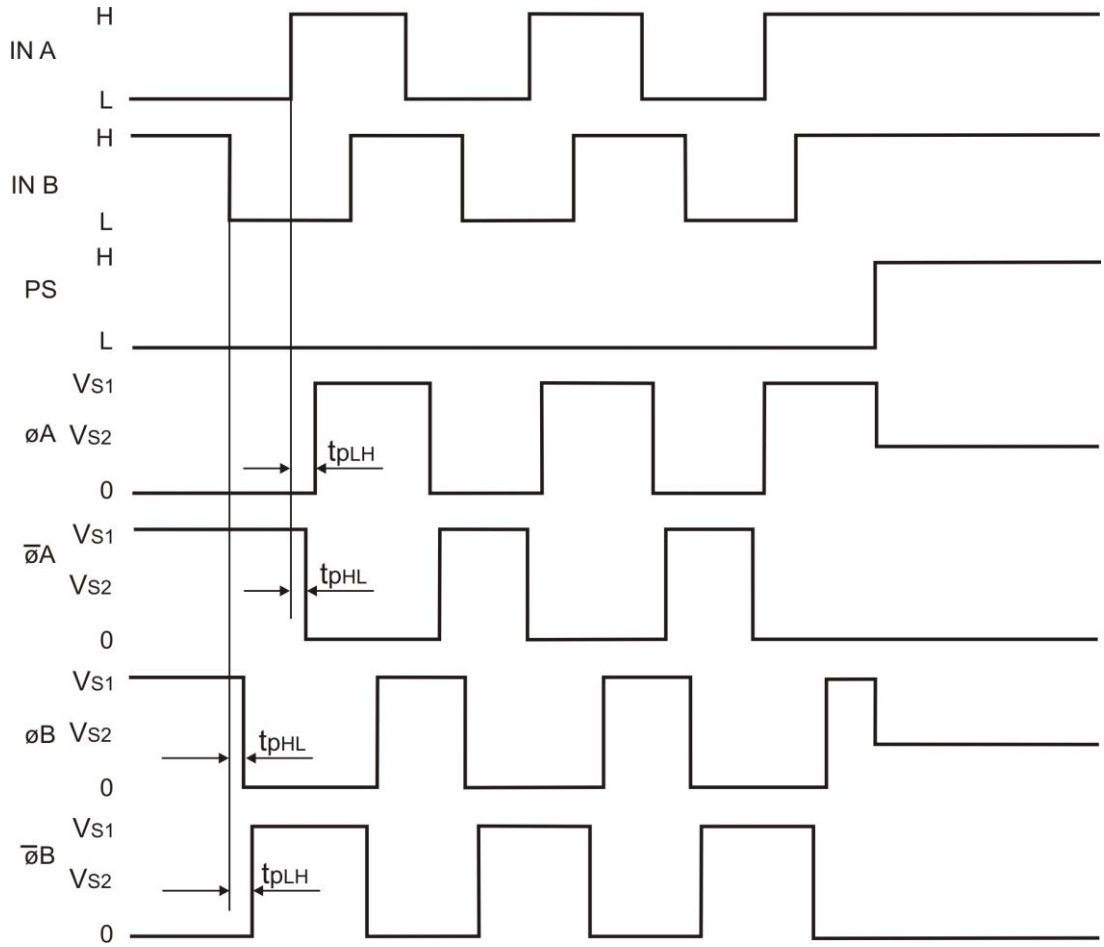
Test Circuit 4. V_{FU}, and V_{FL}



Measuring Method

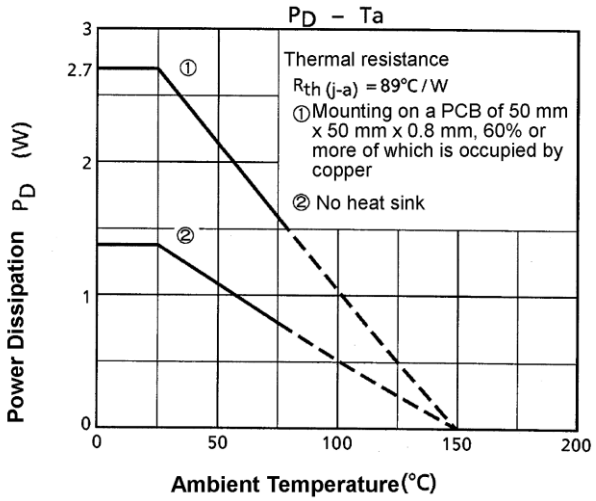
Item	SW_1	SW_2
V_{FU}	a	e
	b	
	c	
	d	
V_{FL}	e	a
		b
		c
		d

Timing Chart (two-phase excitation)

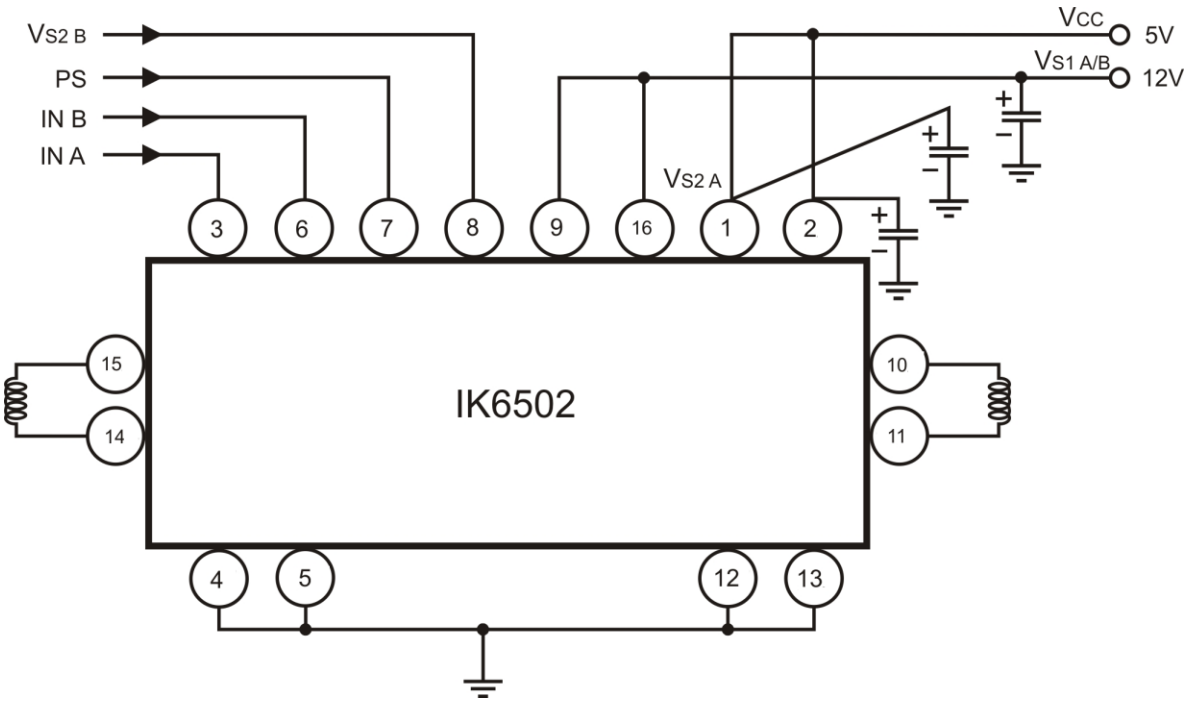


Thermal Performance Characteristics

IK6502N (DIP-16)



Application Circuit



Note 1: Connect the V_{S2A} terminal to the lower supply voltage (5 V).

Note 2: Supply smoothing capacitor***** should be connected between each supply terminal (Vcc, V_{S2A}, and $V_{S1A/B}$) and GND terminal.
*****: (Ex.): Capacitors of tens of μF and 0.1 μF which are connected in parallel.

Note 3: Utmost care is necessary in the design of the output, Vcc, V_M, and GND lines since the IC may be destroyed by short-circuiting between outputs, air contamination faults, or faults due to improper grounding, or by short-circuiting between contiguous terminals.

Note 4: By our short-circuited examination of neighboring terminals, when 9 and 10 terminals or 15 and 16 terminals are short-circuited, in any case might to be destroyed and cause the trouble of smoking etc. Please use an appropriate fuse to the power supply line.

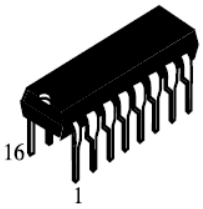
Note 5: Connect V_{S1A} terminal and V_{S1B} terminal externally.

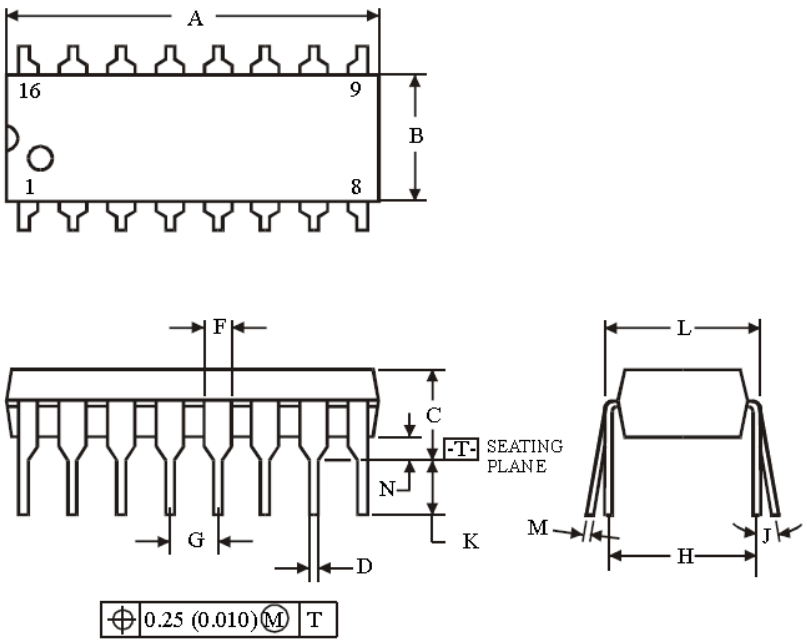
Note 6: Connect each GND terminal externally.

Package Dimensions

N SUFFIX DIP

(MS - 001BB)





	Dimension, mm	
Symbol	MIN	MAX
A	18.67	19.69
B	6.10	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.20	0.36
N	0.38	

NOTES:

1. Dimensions "A", "B" do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.