



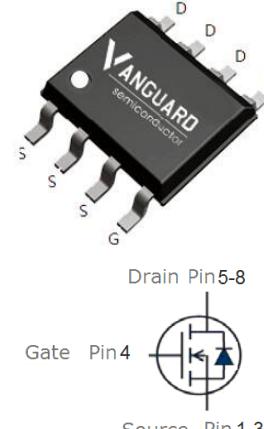
Features

- ◆ Low On-Resistance
- ◆ Fast Switching
- ◆ 100% Avalanche Tested
- ◆ Repetitive Avalanche Allowed up to T_{jmax}
- ◆ Lead-Free, RoHS Compliant

V_{DS}	40	V
$R_{DS(on),TYP}$ @ $V_{GS}=10\text{ V}$	6.0	$\text{m}\Omega$
$R_{DS(on),TYP}$ @ $V_{GS}=4.5\text{ V}$	7.5	$\text{m}\Omega$
I_D	18	A

Description

VS4020AS designed by the trench processing techniques to achieve extremely low on-resistance. Additional features of this design are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Motor applications and a wide variety of other applications.



Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Rating	Unit
Common Ratings (T_c=25°C Unless Otherwise Noted)			
V _{GS}	Gate-Source Voltage	±20	V
V _{(BR)DSS}	Drain-Source Breakdown Voltage	40	V
ESD	Human Body Mode	±800	V
T _J	Maximum Junction Temperature	150	°C
T _{STG}	Storage Temperature Range	-55 to 150	°C
I _S	Diode Continuous Forward Current	T _c =25°C 2.6	A
EAS	Avalanche energy, single pulsed ②	58	mJ
Mounted on Large Heat Sink			
I _{DM}	Pulse Drain Current Tested (Silicon Limit) ①	T _c =25°C 72	A
I _D	Continuous Drain current@V _{GS} =10V	T _c =25°C 18	A
P _D	Maximum Power Dissipation	T _c =25°C 3.1	W
		T _c =75°C 1.9	W
R _{θJA}	Thermal Resistance-Junction to Ambient	40	°C/W



Typicle Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	40	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current($T_J=25^\circ\text{C}$)	$V_{\text{DS}}=32\text{V}, V_{\text{GS}}=0\text{V}$	--	--	1	μA
	Zero Gate Voltage Drain Current($T_J=125^\circ\text{C}$)	$V_{\text{DS}}=32\text{V}, V_{\text{GS}}=0\text{V}$	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	--	--	± 100	nA
$V_{\text{GS(TH)}}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1.0	2.0	2.5	V
$R_{\text{DS(ON)}}$	Drain-Source On-State Resistance ^③	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=10\text{A}$	--	6.0	7.5	$\text{m}\Omega$
$R_{\text{DS(ON)}}$	Drain-Source On-State Resistance ^③	$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=6\text{A}$	--	7.5	8.5	$\text{m}\Omega$
Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise stated)						
C_{iss}	Input Capacitance	$V_{\text{DS}}=20\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$	--	2250	--	pF
C_{oss}	Output Capacitance		--	320	--	pF
C_{rss}	Reverse Transfer Capacitance		--	195	--	pF
Q_g	Total Gate Charge	$V_{\text{GS}}=10\text{V}$	--	42	--	nC
		$V_{\text{GS}}=4.5\text{V}$	--	25	--	nC
Q_{gs}	Gate-Source Charge	$V_{\text{DS}}=20\text{V}, I_{\text{D}}=10\text{A}, V_{\text{GS}}=10\text{V}$	--	7	--	nC
Q_{qd}	Gate-Drain Charge		--	9.5	--	nC
Switching Characteristics						
$t_{\text{d(on)}}$	Turn-on Delay Time	$V_{\text{DD}}=20\text{V}, I_{\text{D}}=9\text{A}, R_{\text{G}}=6.8\Omega, V_{\text{GS}}=10\text{V}$	--	16.5	--	nS
t_r	Turn-on Rise Time		--	17.5	--	nS
$t_{\text{d(off)}}$	Turn-Off Delay Time		--	24	--	nS
t_f	Turn-Off Fall Time		--	16	--	nS
Source- Drain Diode Characteristics@ $T_J = 25^\circ\text{C}$ (unless otherwise stated)						
V_{SD}	Forward on voltage	$I_{\text{SD}}=10\text{A}, V_{\text{GS}}=0\text{V}$	--	--	1.2	V
t_{rr}	Reverse Recovery Time	$T_J=25^\circ\text{C}, I_{\text{sd}}=9\text{A}, V_{\text{GS}}=0\text{V}, \frac{di}{dt}=100\text{A}/\mu\text{s}$	--	28	--	nS
Q_{rr}	Reverse Recovery Charge		--	16	--	nC

NOTE:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by $T_{J\text{max}}$, starting $T_J = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 12\text{A}$, $V_{GS} = 10\text{V}$. Part not recommended for use above this value

③ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.



Typical Characteristics

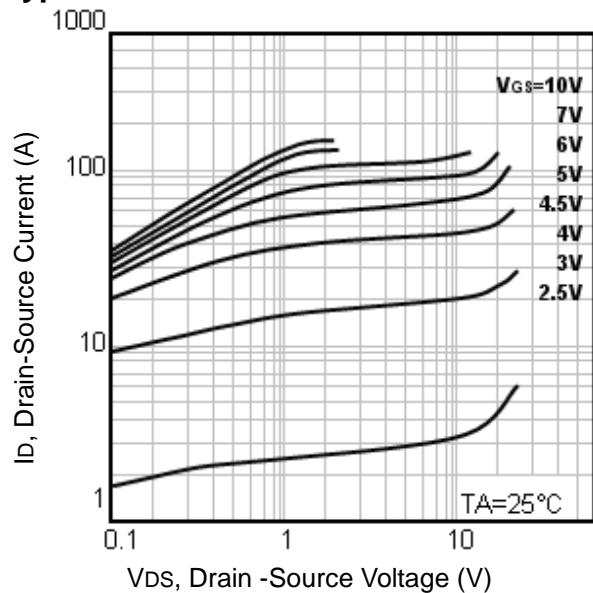


Fig1. Typical Output Characteristics

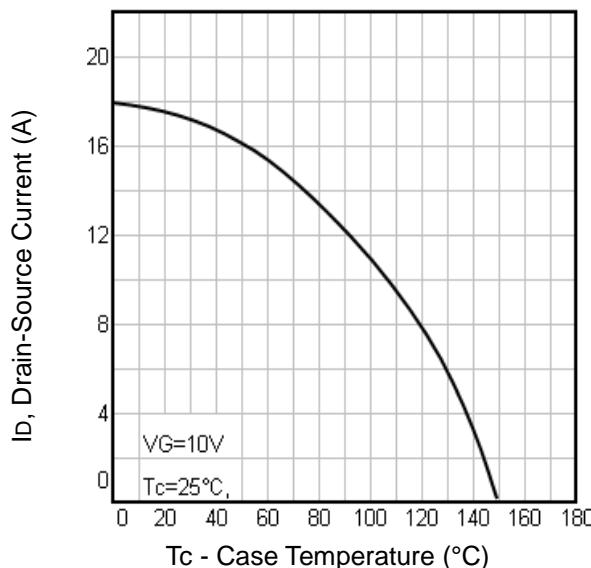


Fig2. Maximum Drain Current Vs. Case Temperature

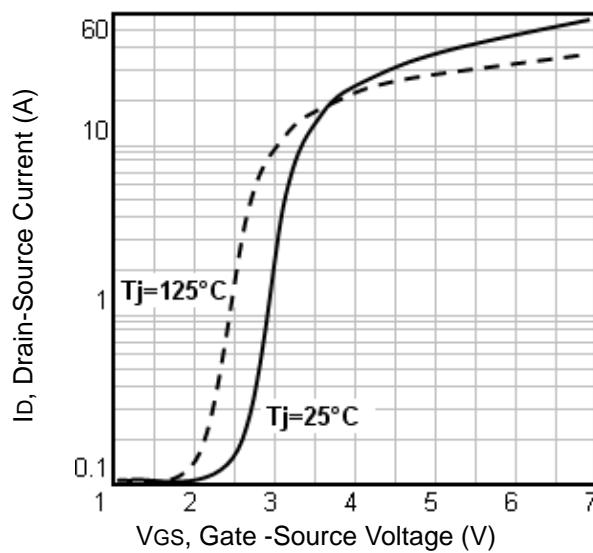


Fig3. Typical Transfer Characteristics

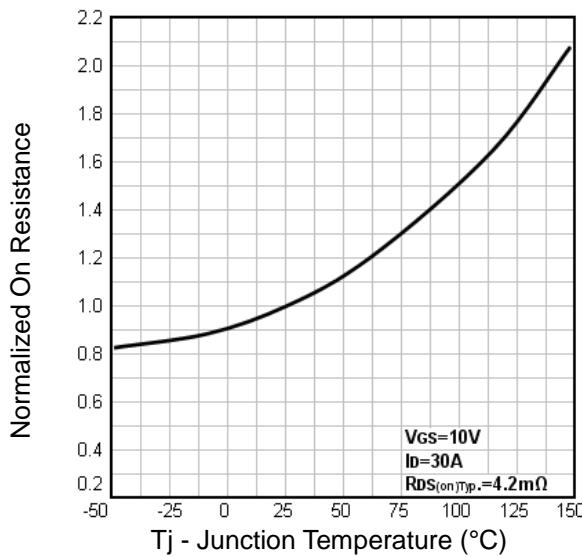


Fig4. Normalized On-Resistance Vs. Temperature

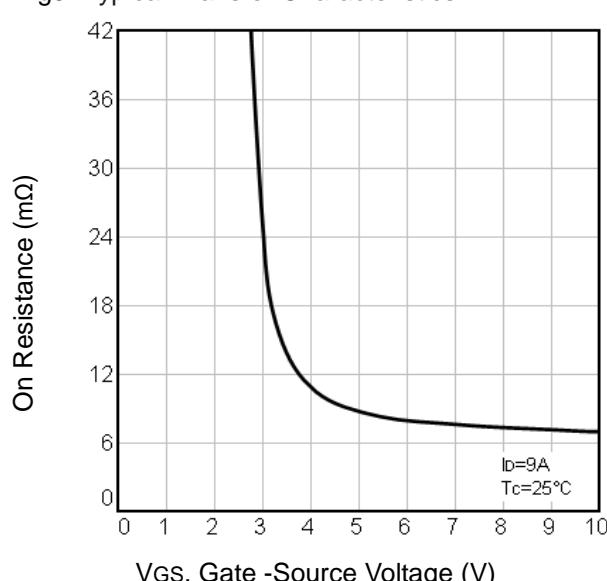


Fig5. On Resistance Vs. Gate-Source Voltage

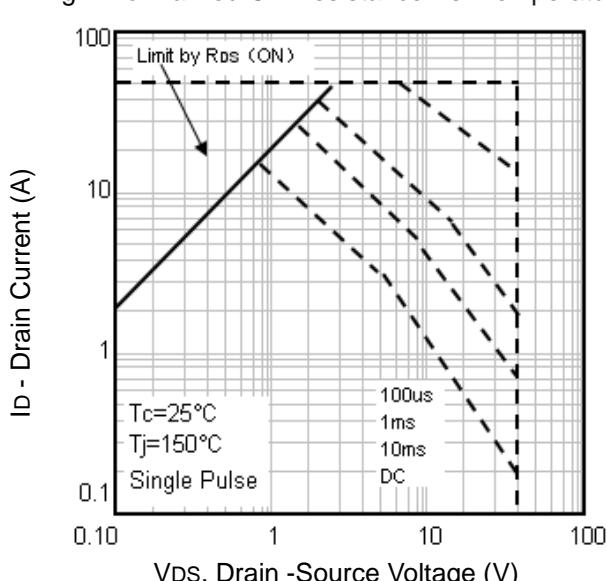


Fig6. Maximum Safe Operating Area



Typical Characteristics

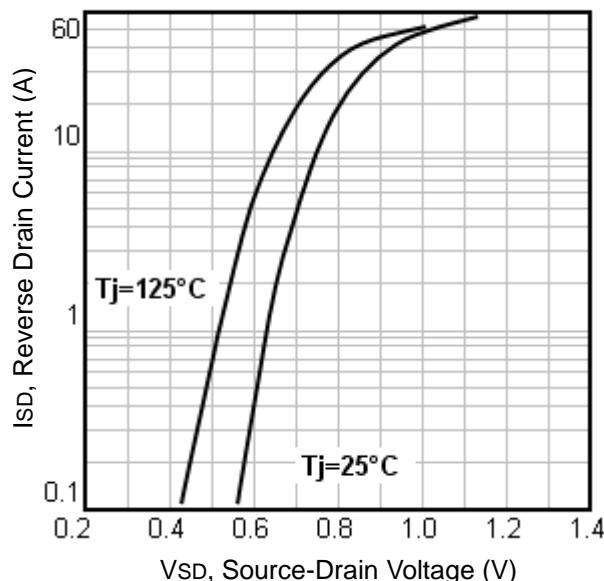


Fig7. Typical Source-Drain Diode Forward Voltage

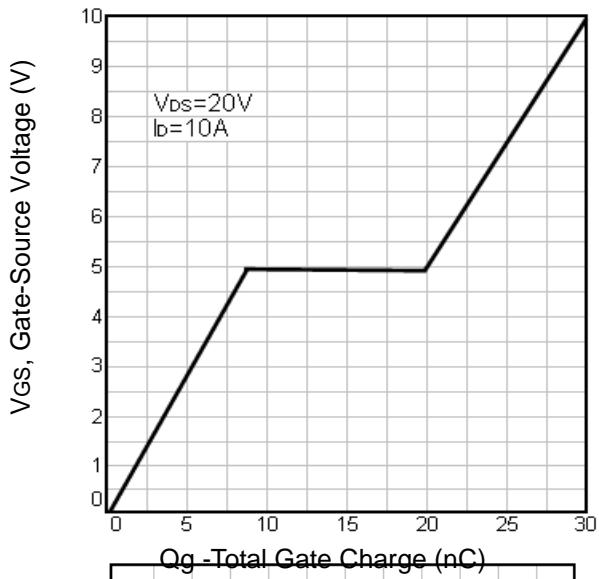


Fig8.16. Typical Gate Charge Vs. Gate-Source Voltage

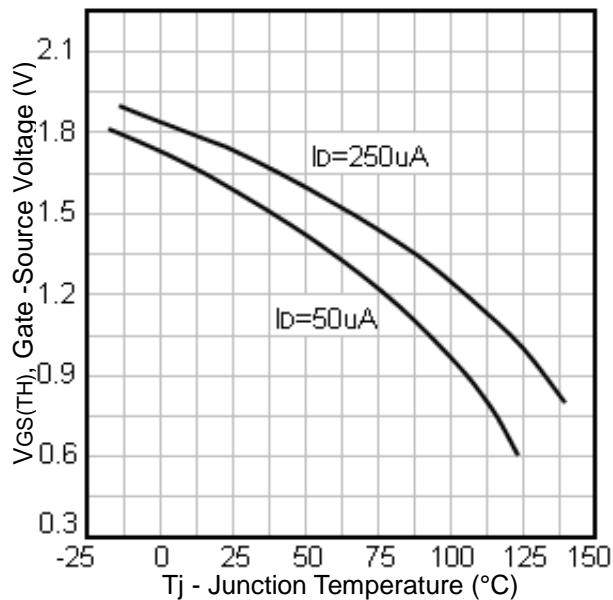


Fig9. Threshold Voltage Vs. Temperature

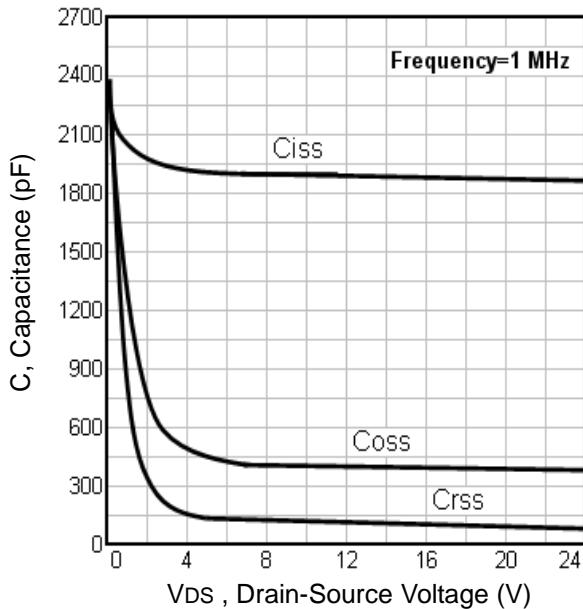


Fig10. Typical Capacitance Vs. Drain-Source Voltage

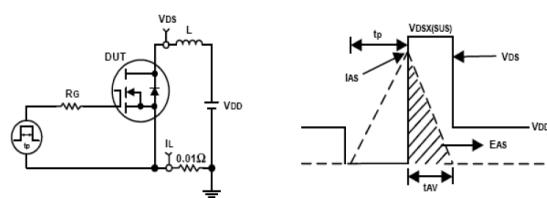


Fig11. Unclamped Inductive Test Circuit and waveforms

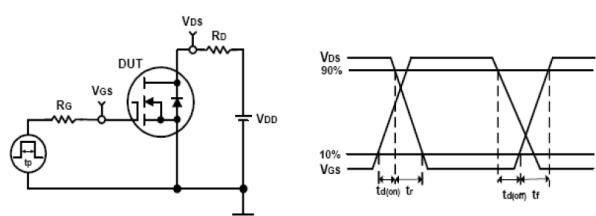
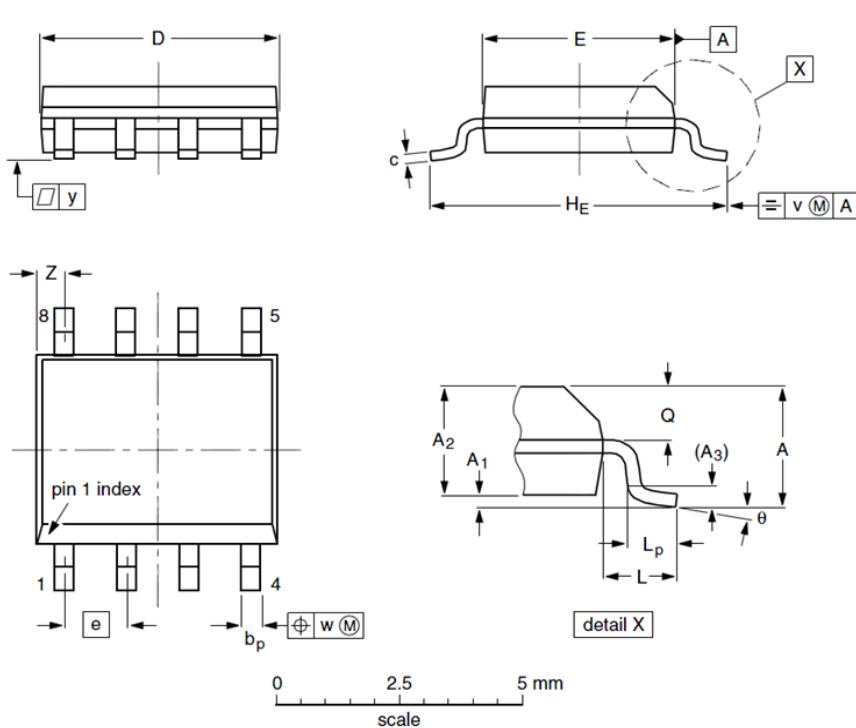


Fig12. Switching Time Test Circuit and waveforms



SOP8 Package Outline Data



Label	Dimensions (unit: mm)		
	Min	Typ	Max
A	--	--	1.75
A ₁	0.10	0.18	0.25
A ₂	1.25	1.35	1.50
A ₃	--	0.25	--
b _p	0.36	0.42	0.51
c	0.19	0.22	0.25
D	4.80	4.92	5.00
E	3.80	3.90	4.00
e	--	1.27	--
H _E	5.80	6.00	6.20
L	--	1.05	--
L _p	0.40	0.68	1.00
Q	0.60	0.65	0.725
v	--	0.25	--
w	--	0.25	--
y	--	0.10	--
z	0.30	0.50	0.70
θ	0°		8°

Notes:

1. Follow JEDEC MS-012.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. Dimension "bp" does NOT include dambar protrusion. Allowable dambar protrusion shall be 0.1mm total in excess of "bp" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

Customer Service

Sales and Service:

sales@vgsemi.com

Vanguard Semiconductor CO., LTD

TEL: (86-755) -26902410

FAX: (86-755) -26907027

WEB: www.vgsemi.com