

## Multi-Mode PWM Controller of Flyback with MOSFET Integrated

REV. 02

### General Description

The LD9534 is built in a multi-mode PWM controller and integrated a 650V MOSFET. The multi-mode PWM controller which consists of Quasi-Resonant (QR) PWM control for light load condition and Continue Conduction Mode (CCM) for heavy load condition. Moreover, the QR controller not only gains the system performance, but also brings the worse EMI capability, while the frequency swapping function of LD9534 can reduce the EMI emission of SMPS and helps the power circuit designers to simply deal with EMI filter and saves several component and developing time.

The LD9534 is implemented in DIP-8 package, and includes the comprehensive protection function, such as Over Load Protection (OLP), Over Voltage Protection (OVP), Output Short Circuit Protection (OSCP) and internal Over Temperature Protection (OTP).

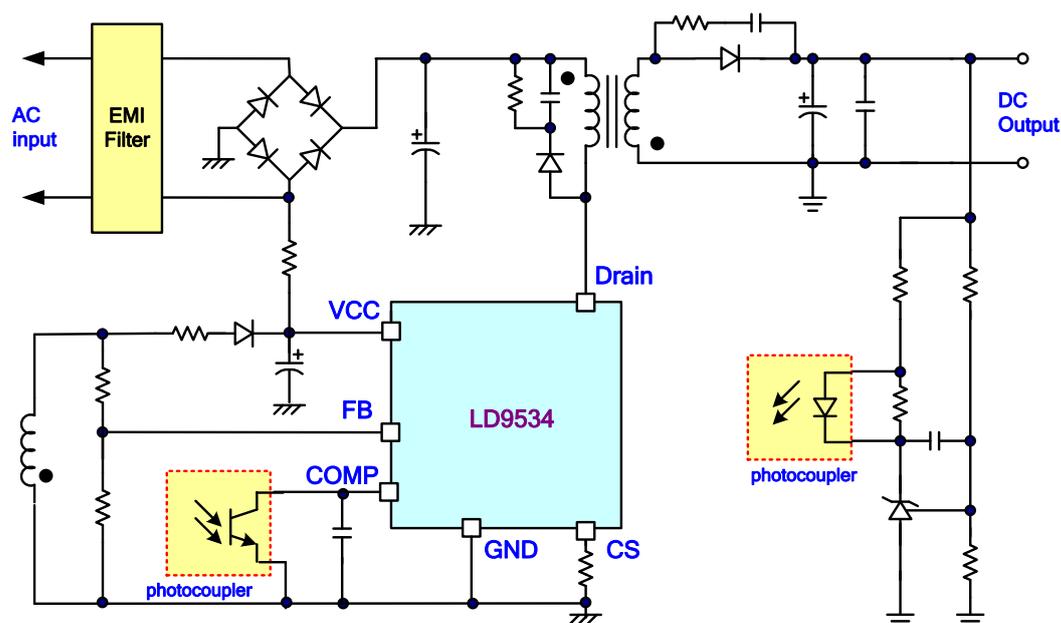
### Features

- Secondary-side feedback control with quasi-resonant + CCM operation
- Built-in 650V MOSFET Switch
- Low Startup Current ( $<1\mu\text{A}$ )
- Ultra-low operating current at light load
- Current Mode Control with Cycle-by-Cycle Current Limit
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- VCC OVP (Over Voltage Protection)
- Adj. OVP (Over Voltage Protection) on FB pin.
- Adj. UVP (Under Voltage Protection) on FB pin.
- OLP (Over Load Protection)
- Internal OTP (Over Temperature Protection)

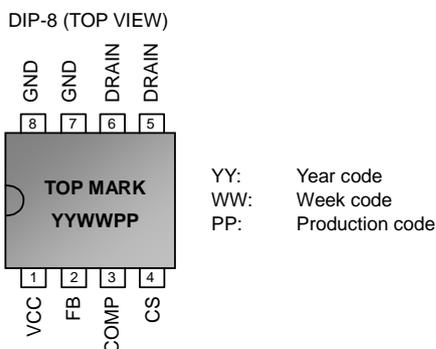
### Applications

- Switching AC/DC Adaptor

### Typical Application



## Pin Configuration



## Ordering Information

Part number	Package	TOP MARK	Shipping
LD9534 GN	DIP-8 (Green Package)	LD9534GN	3600 /tube /carton

The LD9534 is RoHs compliant/ green packaged.

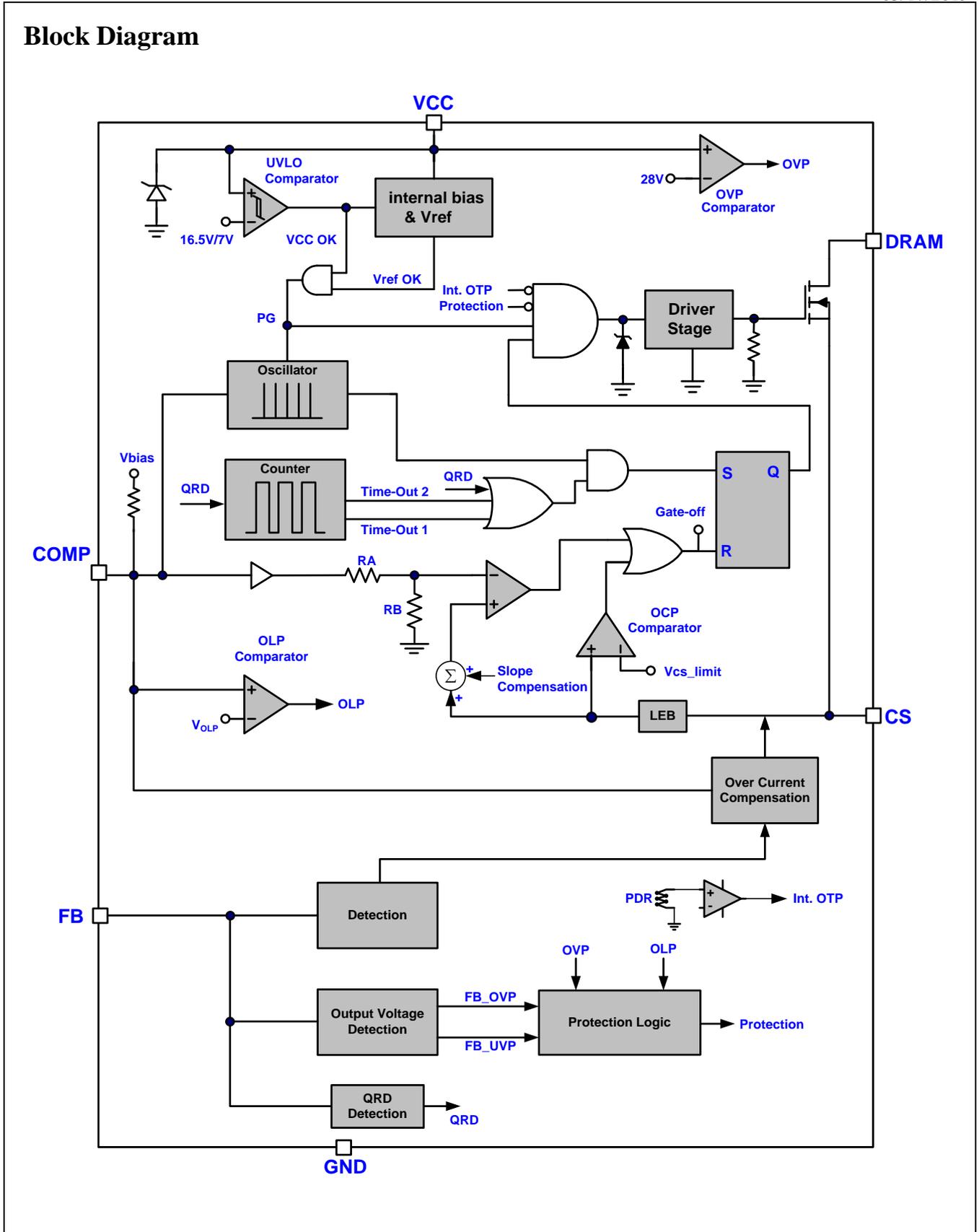
## Protection Mode

Product Name	Switching Freq.	VCC_OVP	FB_OVP	OSCP	OLP	Int. OTP
LD9534	65kHz	Auto recovery				

## Pin Descriptions

NAME	Pin (DIP-8)	FUNCTION
GND	8,7	Ground
DRAIN	5,6	The drain of internal power MOSFET
CS	4	Current sense pin, connect to sense the MOSFET current
COMP	3	Output of the error amplifier for voltage compensation
FB	2	Auxiliary voltage sense and Quasi Resonant detection
VCC	1	Supply voltage pin

Block Diagram



## Absolute Maximum Ratings

Supply Voltage VCC.....	-0.3V ~ 30V
COMP.....	-0.3V ~ 12V
FB, CS.....	-0.3V ~ 7V
DRAIN.....	-0.3V ~ 650V
Drain Peak Current.....	4A
Maximum Junction Temperature.....	150°C
Storage Temperature Range.....	-65°C ~ 150°C
Package Thermal Resistance (DIP-8, $\theta_{JA}$ ).....	80°C/W
Package Thermal Resistance (DIP-8, $\theta_{JC}$ ).....	30°C/W
Total Power Dissipation (DIP-8, at Ambient Temperature = 85°C).....	500mW
Lead temperature (Soldering, 10sec).....	260°C
ESD Voltage Protection, Human Body Model (Except Drain Pin).....	2.5 KV
ESD Voltage Protection, Human Body Model (Drain Pin).....	1 KV
ESD Voltage Protection, Machine Model (Except Drain Pin).....	250 V
ESD Voltage Protection, Machine Model (Drain Pin).....	200 V

### Caution:

Stress exceeding maximum ratings may damage the device. Maximum ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stress above recommended operating conditions may affect device reliability.

Note 1: The value of  $\theta_{JA}$  is measured with the device mounted on 1oz one layer FR-4 board, in a still air environment with TA = 25°C. The value in any given application depends on the user's specific board design.

## Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	8.0	26.5	V
VCC Capacitor	3.3	10	μF
Start-up resistor Value (AC Side, Half Wave)	400K	2M	Ω
Comp Pin Capacitor (X7R type)	330	4700	pF
CS Pin Capacitor Value		30	pF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF ~ 0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible.
2. It's also essential to connect a capacitor to COMP to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed close to IC pin as possible.

## Electrical Characteristics

( $T_A = +25^\circ\text{C}$  unless otherwise stated,  $V_{CC}=15.0\text{V}$ )

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
<b>Supply Voltage (VCC Pin)</b>						
Startup Current		$I_{CC\_ST}$			1	$\mu\text{A}$
Operating Current	$V_{COMP}=0\text{V}$	$I_{CC\_OP1}$		0.295		mA
	$V_{COMP}=1.7\text{V}, I_{FB}=200\mu\text{A}$	$I_{CC\_OP2}$		1.95		mA
	Auto current protection	$I_{CC\_OPA1}$		0.6		mA
UVLO(OFF)		$V_{CC\_OFF}$	6	7	8	V
UVLO(ON)		$V_{CC\_ON}$	15.5	16.5	17.5	V
VCC OVP Level		$V_{CC\_OVP}$	27	28	29	V
VCC OVP de-bounce time		$T_{VCC\_OVP}$		8		Cycle
<b>Voltage Feedback (COMP Pin)</b>						
Short Circuit Current	$V_{COMP}=0\text{V}$	$I_{COMP}$	0.08	0.116	0.15	mA
Open Loop Voltage	(1)	$V_{COMP\_OPEN}$		3.15		V
<b>Current Sensing (CS Pin)</b>						
Maximum Input Voltage	$I_{FB}=0\mu\text{A}$	$V_{CS\_LIMIT}$	0.45	0.5	0.55	V
Leading Edge Blanking Time	(1)	$T_{LEB}$		450		ns
Internal Slope Compensation	$t_{on}>3\mu\text{s}$ to $D_{MAX}$ . (Linearly increase), (1)	$V_{SLP\_L}$		165		mV
<b>QRD (Quasi Resonant Detection, FB Pin)</b>						
FB OVP Trip voltage Level		$V_{FB\_OVP}$	3.3	3.5	3.7	V
FB OVP De-bounce Time		$T_{FB\_OVP}$		8		Cycle
FB UVP Trip voltage Level	(1)	$V_{FB\_UVP}$		0.8		V
QRD Trip Level	(1)	$I_{QRD}$		20		$\mu\text{A}$
<b>Oscillator for Switching Frequency</b>						
CCM Frequency		$F_{CCM}$	60	65	70	kHz
Frequency Swapping	(1)	$F_{SW\_MOD}$		$\pm 8$		%
Green Mode Frequency		$F_{SW\_GREEN}$	21	24	27	kHz
Temp. Stability	(1)	$F_{SW\_TS}$		3	5	%
Voltage Stability	$V_{CC} = 9\text{V} \sim 24\text{V}$ (1)	$F_{SW\_VS}$			1	%
Maximum Duty	(1)	$D_{MAX}$		81		%
<b>Soft Start</b>						
Soft Start Time	$V_{CS\_OFF}$ from 0.2V to 0.5V (1)	$T_{SS}$		7		ms

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
<b>BNO Protection (FB Pin)</b>						
Brown In Trip Level		I <sub>BNI</sub>	85	95	105	μA
BNO Hysteresis		I <sub>BNO_HYS</sub>		10		μA
Brown Out De-bounce Time	V <sub>COMP</sub> =1.7V	T <sub>DB_BNO</sub>		75		ms
<b>Open Loop Protection</b>						
OLP Trip Level		V <sub>OLP</sub>	2.65	2.8	2.95	V
OLP delay time	After soft-start	T <sub>D_OLP</sub>		88		ms
<b>On Chip OTP (Over Temperature Protection)</b>						
OTP Level	(1,2)	T <sub>INOTP</sub>		140		°C
OTP Hysteresis	(1,2)	T <sub>INOTP_HYS</sub>		12		°C

## Electrical Characteristics for MOSFET

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
<b>LD9534 MOSFET Drain (DRAIN Pin)</b>						
Breakdown Voltage	VCC=0V , COMP=0V, ID=250μA , Tj=25°C	BV <sub>DS</sub>	650			V
	VCC=0V , COMP=0V, ID=250μA , Tj=125°C <sup>(1)</sup>		700			V
Continuous Drain Current	VCC=15V , Tj=25°C	I <sub>D</sub>			4	A
On Resistance	ID=2A , VCC=15V , Tj=25°C	R <sub>DS_ON</sub>		2.15	2.65	Ω

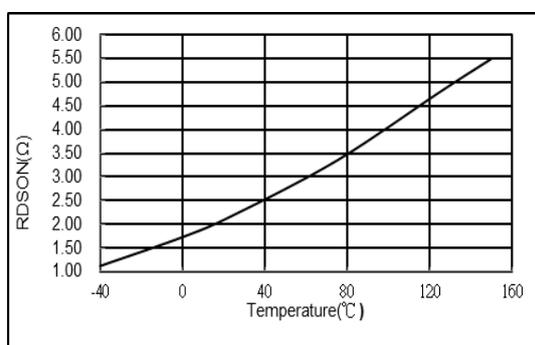


Fig. 1 LD9534 R<sub>DS\_ON</sub> vs. Temperature

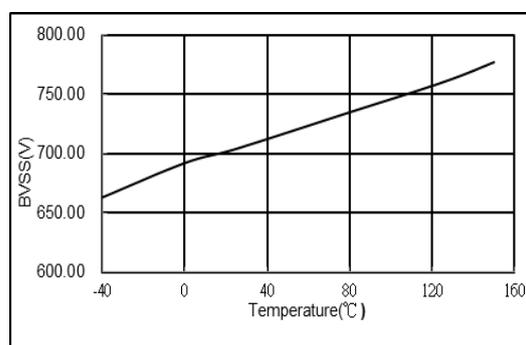


Fig. 2 LD9534 Breakdown Voltage vs. Temperature

**Notes:**

1. Guaranteed by design.
2. The threshold temperature for enabling the output again and resetting the latch after OTP has been activated.

## Typical Performance Characteristics

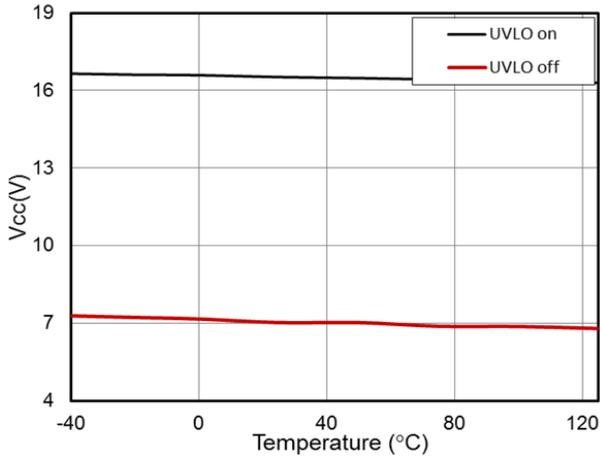


Fig 3. UVLO Level vs. Temperature

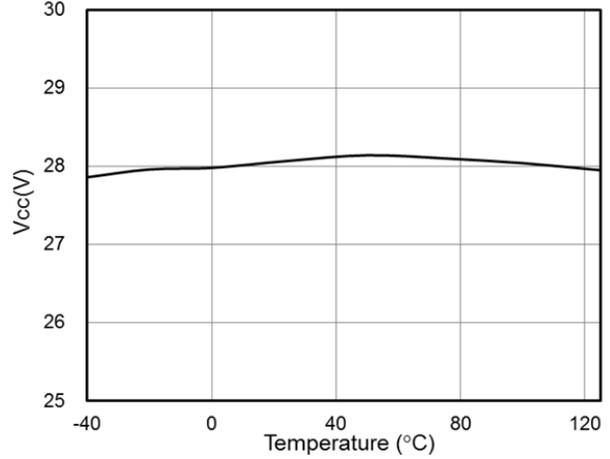


Fig 4. Vcc OVP Level vs. Temperature

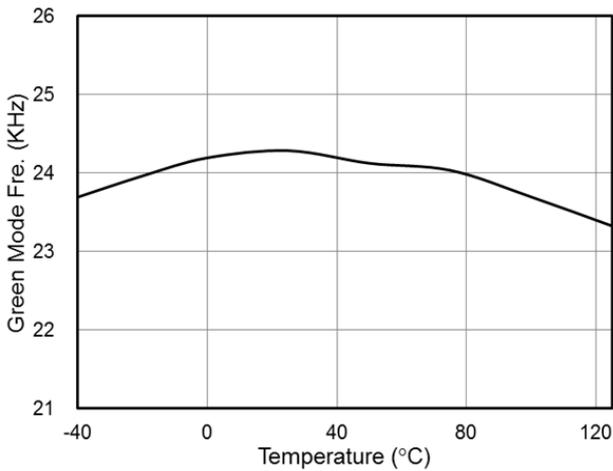


Fig 5. Green Mode Fre. vs. Temperature

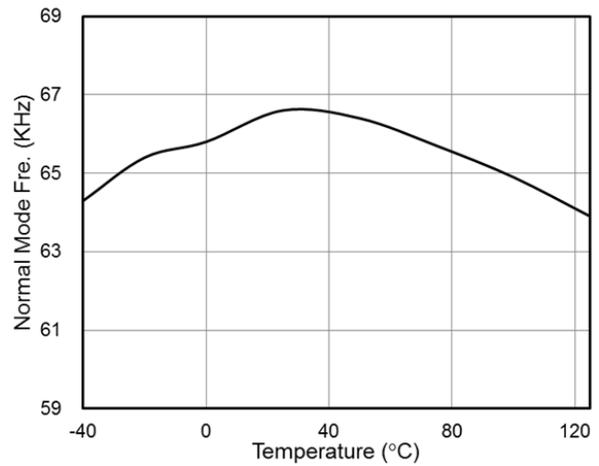


Fig 6. Normal Mode Fre. vs. Temperature

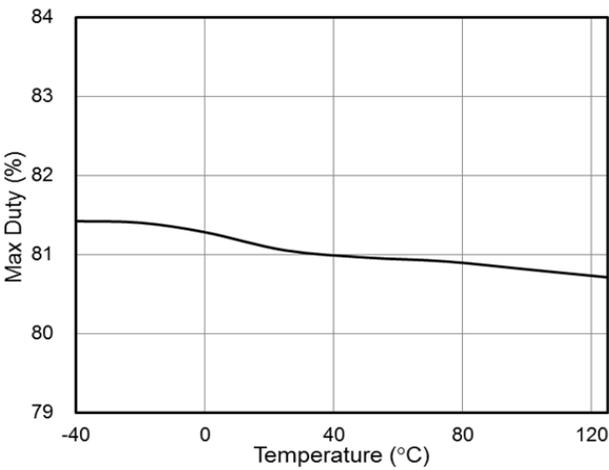


Fig 7. Max Duty vs. Temperature

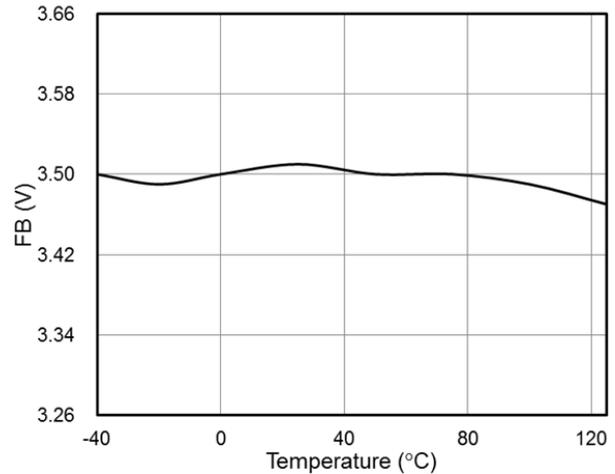


Fig 8. FB OVP Level vs. Temperature

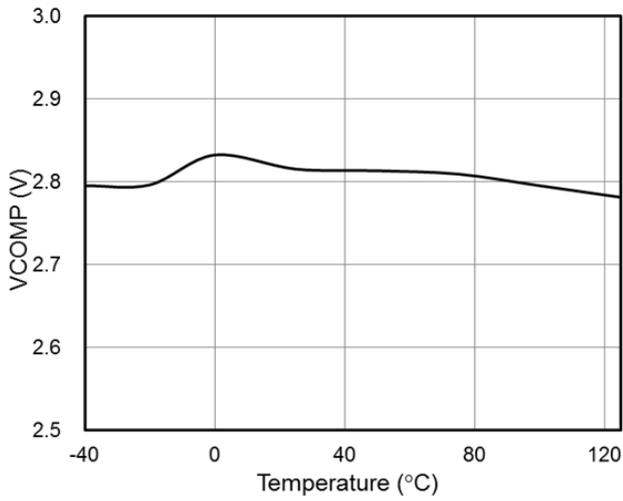


Fig 9. VOLP Level vs. Temperature

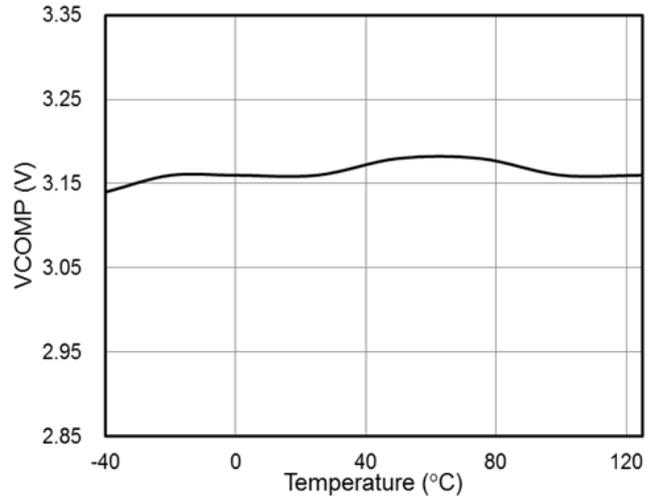


Fig 10. Open Loop Voltage vs. Temperature

## Application Information

### Operation Overview

The LD9534 is built in a multi-mode PWM controller and integrated a 650V MOSFET. The LD9534 operates a constant frequency to achieve the CCM as heavy load. For demanding higher power efficiency and power-saving in light load condition, the LD9534 implements QR function to allow the valley switching and accomplish zero voltage switching (ZVS). Under different load conditions, LD9534 provides the different solutions for achieving higher efficiency and performance.

### Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD9534. As shown in Fig. 11, a hysteresis is built in to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16.5V and 7V, respectively.

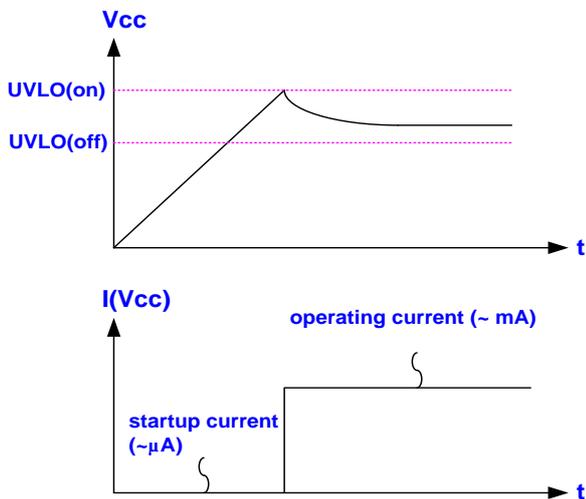


Fig. 11

### Startup Current and Startup Circuit

The typical startup circuit to generate the LD9534 VCC is shown in Fig. 12. During the startup transient, the VCC is lower than the UVLO threshold thus LD9534 will

not to turn on. Therefore, the current through R1 will provide the startup current and to charge the capacitor C1. Whenever the VCC voltage is high enough to turn on the LD9534 the supply current is provided from the auxiliary winding of the transformer.

Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current of LD9534 is only 1µA. If a higher resistance value of R1 is chosen, it usually takes more time to start up. To select the value of R1 and C1 carefully will optimize the power consumption and startup time.

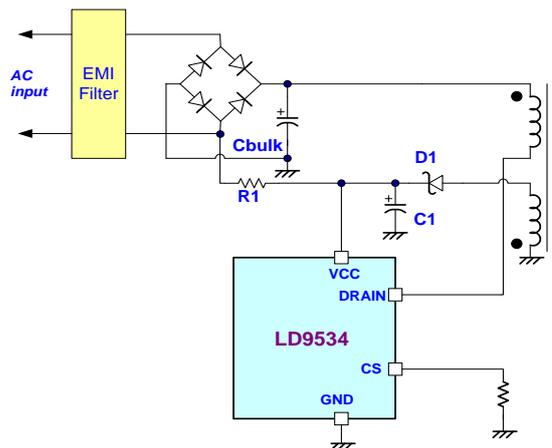


Fig. 12

### QR Mode Detection

The transformer will be demagnetized after the main power MOSFET turns off. A quasi resonant signal will be detected from auxiliary winding by FB pin through the external resistor.

As soon as the current of the secondary side diode is down to zero during MOSFET-off period, the transformer's core is demagnetized completely.  $V_{DS}$  of MOSFET will resonate in discontinuous current mode.

The resonance frequency ( $F_{QR}$ ) will be obtained as below.

$$F_{QR} = \frac{1}{2\pi\sqrt{L_M * C_R}} \text{ (HZ)}$$

$L_M$  = Inductance of primary winding

$C_R$  = Resonance equivalent parasitic capacitance

If  $V_{DS}$  voltage falls to resonant valley level from max plateau value, the QRD comparator will be tripped while FB pin current is close to  $20\mu A$ .

However, the QR detection will be influenced by propagation delay. If inductance of primary winding is less than  $500\mu H$ , there is barb in  $V_{ds}$  (as shown in Fig. 13).

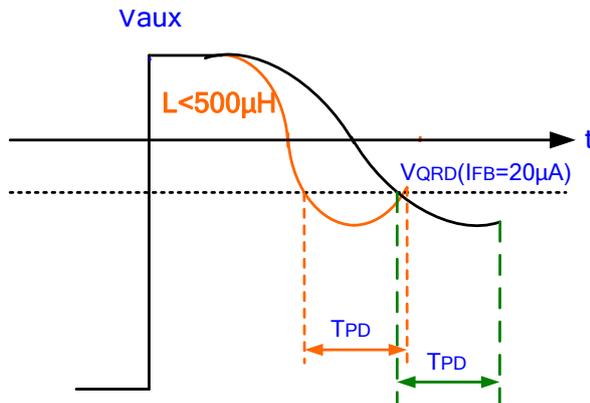


Fig. 13

### Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD9534. Similar to UC3842, the LD9534 would without voltage offset to feed the voltage divider at the ratio of  $R_A$  and  $R_B$ , that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{R_B}{R_A + R_B} \times V_{COMP}$$

A pull-high resistor is embedded internally and therefore no external one is required.

The LD9534 integrates the multi-mode PWM controller, and for enhance the light load efficiency, the comp pin value corresponding to the frequency is as shown in Fig. 14.

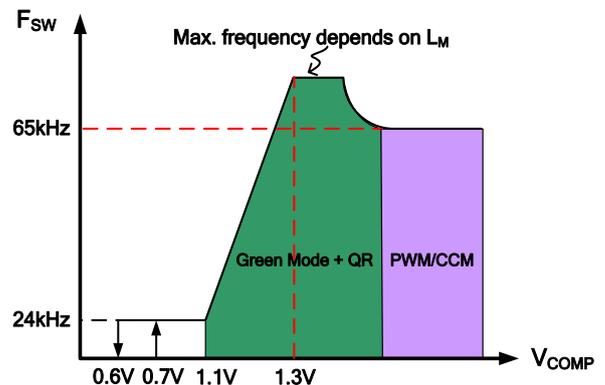


Fig. 14

### Current Sensing, Leading Edge Blanking

The typical current mode of PWM controller feeds back both current signal and voltage signal to close the control loop and achieve regulation. The LD9534 detect the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin sets at  $0.5V$ . From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.5V}{R_{CS}}$$

A leading-edge blanking (LEB) timer is included in the input of CS pin to prevent false trigger from the turn-on current spike (as shown in Fig. 15).

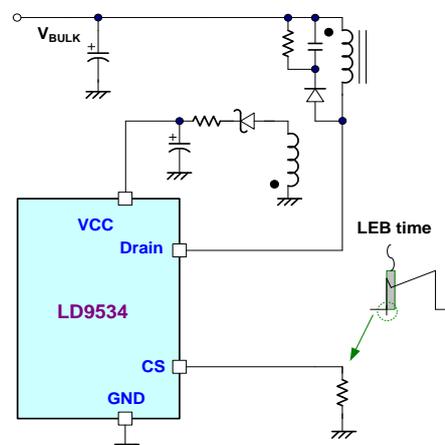


Fig. 15

## CCM Switching Frequency Clamp

According to the QR operation principle, the switching frequency is inversely proportional to the output power. Therefore, as the output power increases, the switching frequency can become rather low without limiting. The CCM switching frequency of LD9534 is clamped at 65 kHz internally to provide the optimized operations by considering the EMI performance, thermal treatment, component sizes and transformer design.

## Over Voltage Protection on VCC Pin (VCC OVP) – Auto Recovery

LD9534 is implemented with an OVP function on VCC. Whenever the VCC voltage is higher than the OVP threshold voltage, the LD9534 will be shutdown simultaneously thus to stop the switching of the power MOSFET until the next UVLO(ON). The VCC OVP function in LD9534 is an auto-recovery type protection. The Fig. 16 shows its operation.

On the other hand, if the OVP condition is removed, the VCC level will get back to normal level and the output will automatically return to the normal operation.

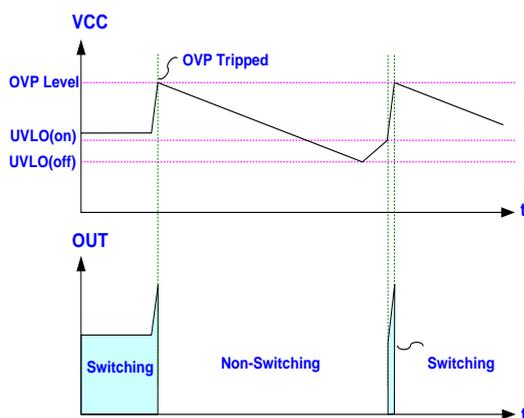


Fig. 16

## Over Load Protection (OLP) – Auto Recovery

To protect the circuit from damage due to over-load condition and short or open-loop condition, the LD9534 is implemented with smart OLP function. It also features

auto-recovery function, see Fig. 17 for the waveform. In case of fault condition, the feedback system will force the voltage loop toward the saturation and then pull the voltage high on COMP pin (V<sub>COMP</sub>). When the V<sub>COMP</sub> ramps up to the OLP threshold of 2.8V and continues over OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

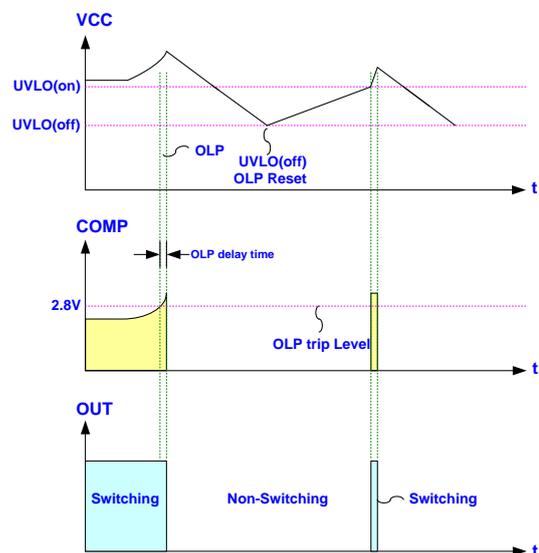


Fig. 17

## Brown-In/ Brown-Out Protection (BNI/BNO) – Auto Recovery

The LD9534 integrates the brown in, brownout protection and valley detection into FB pin. The auxiliary voltage reflects a proportional bulk voltage during the on time. Fix the internal current at the BNI and BNO, the BNI level could be set by modulating the FB divided resistors and auxiliary voltage, as shown in Fig. 18. For preventing the abnormal condition of line voltage to causing damage, BNO function is implemented, while turns off the gate signal after de-bounce time 75ms as BNO occurring, as shown in Fig. 19. The relationship of

input voltage and BNI/BNO is expressed in following equation.

$$V_{DC\_BNI} = \frac{N_p}{N_a} \cdot I_{BNI} \cdot R_1$$

$$V_{DC\_BNO} = \frac{N_p}{N_a} \cdot I_{BNO} \cdot R_1$$

,where

$V_{DC\_BNI}$  is predicted BNI DC value of input voltage.

$V_{DC\_BNO}$  is predicted BNO DC value of input voltage.

$I_{BNI}$  is BNI trip current.

$I_{BNO}$  is BNO trip current.

$N_p$  is turns ration of primary-side winding.

$N_a$  is turns ration of auxiliary winding.

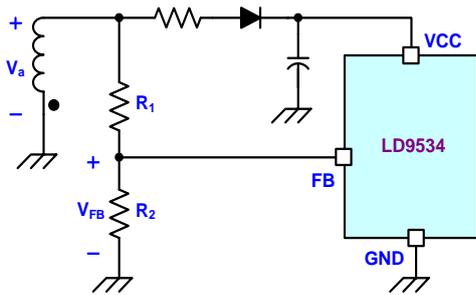


Fig. 18

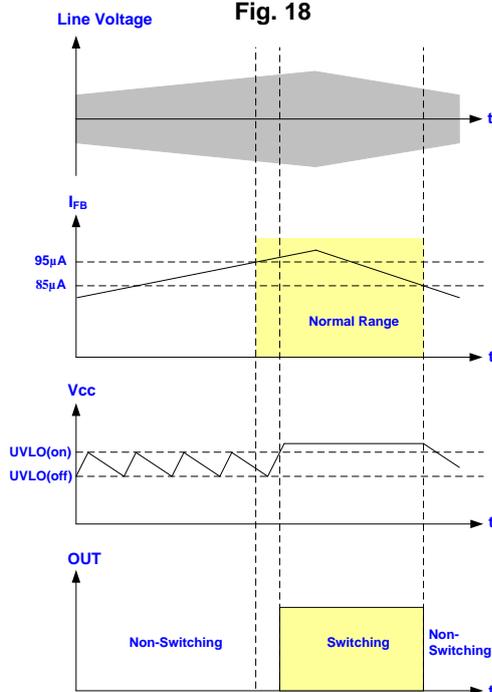


Fig. 19

## Over Voltage Protection on FB Pin (FB OVP) – Auto Recovery

An output overvoltage protection is implemented in the LD9534. The auxiliary winding voltage can be reflected from secondary winding, in which the FB pin voltage is proportional to output voltage during the gate off time. OVP is worked by sensing the auxiliary voltage via the divided resistors R2, refereeing to Fig. 18. The equation of FB OVP is shown as follows.

$$R_2 = \frac{R_1 \cdot V_{FB\_OVP}}{V_a - V_{FB\_OVP}}$$

$$V_a = \frac{N_a}{N_s} (V_o + V_F)$$

$V_{FB\_OVP}$  is the FB pin OVP trip voltage level.  $V_a$  is the auxiliary winding voltage which reflects from the forward voltage  $V_F$  of Schottky diode and output voltage  $V_o$ .  $N_s$  is turns ration of secondary-side winding.

If  $V_{FB}$  overs the FB OVP trip level, the internal counter starts counting 8 cycles, and then LD9534 goes to auto-recovery protection mode till the FB OVP status is defused.

## Output Short Circuit Protection (OSCP) – Auto Recovery

The OSCP function can prevent the damage from output short circuit. Once the output is shorted,  $V_o$  and  $V_{CC}$  drop immediately, which always reflects the auxiliary winding during the gate off region. Therefore, as  $V_{FB}$  is lower than 0.8V during gate off region, then the  $FB\_UVP$  is triggered, and skips one cycle. According to the close loop control, COMP voltage will pull high in the meanwhile. If the  $V_{COMP}$  pulls higher than 2.8V over 15 ms and  $V_{CC}$  drops below 9.6V. At this time, the OSCP protection will be triggered and turn off the gate driving.

## Oscillator and Switching Frequency

The LD9534 is implemented with frequency swapping function which helps the power supply designers to both

optimize EMI performance and lower system cost.

### **Green Mode Operation**

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency in light load conditions. The green-mode control is Leadtrend Technology's own property.

### **Fault Protection**

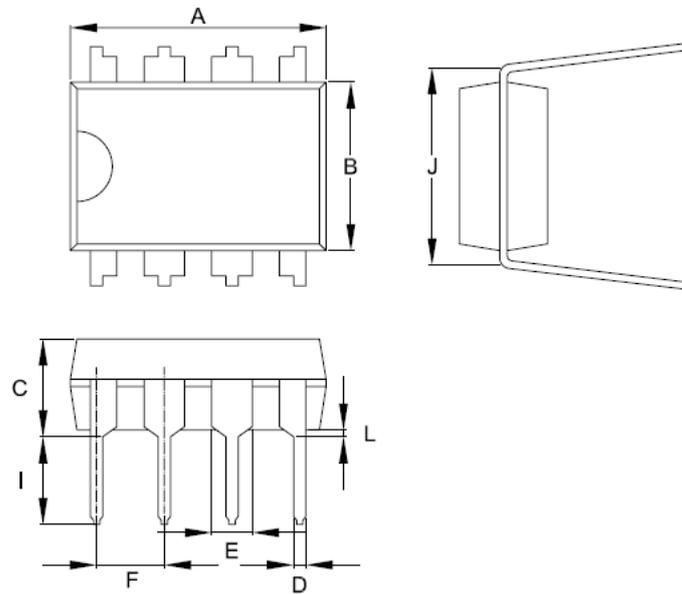
There are several critical protections integrated in the LD9534 to prevent from damage to the power supply. Those damages usually come from open or short conditions on the pins of LD9534.

In case under such conditions listed below, the gate output will turn off immediately to protect the power circuit.

1. CS pin floating
2. COMP pin floating

## Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	-----	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	-----	0.015	-----

**Revision History**

REV.	Date	Change Notice
00	01/14/2019	Original Specification
01	03/28/2019	Modify "block diagram".
02	05/17/2109	Modify absolute maximum ratings values.

**Important Notice**

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Customers should verify the datasheets are current and complete before placing order.