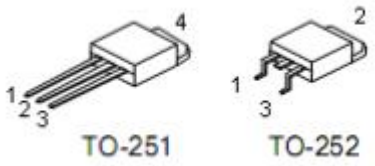
1. Description

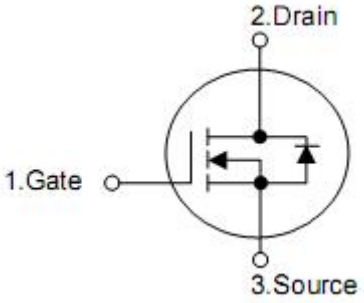
The KNX4820B-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology

2. Features

- Proprietary New Planar Technology
- RDS(ON),typ.=250m Ω@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

3. Pin configuration





Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Ordering Information

Part Number	Package	Brand
KNU4820B	TO-251	KIA
KND4820B	TO-252	KIA

5. Absolute maximum ratings

TC=25℃ unless otherwise specified

Parameter	Symbol	Ratings	Unit
		TO251/TO252	
Drain-to-Source Voltage	V_{DSS}	200	V
Gate-to-Source Voltage	V_{GSS}	±20	
Continuous Drain Current	I_D	9.0	A
Pulsed Drain Current at VGS=10V	I_{DM}	36	
Single Pulse Avalanche Energy	E_{AS}	300	mJ
Power Dissipation	P_D	83	W
Derating Factor above 25℃		0.59	W/ ºC
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	T_L	300	ºC
Operating and StorageTemperatureRange	T_J& T_{STG}	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Ratings		Units
		TO251	TO252	
Thermal resistance, junction-ambient	$R_{\theta JA}$	75		ºC/W
Thermal resistance, Junction-case	$R_{\theta JC}$	1.5		

7. Electrical characteristics

(T_J=25°C,unless otherwise notes)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Off characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	200	-	-	V
Drain-to-source Leakage Current	I_{DSS}	V_{DS}=200V ,V_{GS}=0V	-	-	1	μA
		V_{DS}=160 V_{GS}=0V T_C=125℃,	-	-	10	μA
Gate-body leakage current	I_{GSS}	V_{GS}=20V,V_{DS}=0V	-	-	+100	nA
		V_{GS}=-20V,V_{DS}=0V	-	-	-100	nA
On characteristics						
Static drain-source on-resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=4.5A	-	250	300	mΩ
		V_{GS}=4.5V, I_D=4.5A	-	270	320	mΩ
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.0	-	3.0	V
Forward Transconductance	gfs	V_{DS}=20V,I_D=9A	-	9.0	-	S
Dynamic characteristics						
Input capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1MHz	-	418	-	pF
Output capacitance	C_{oss}		-	94	-	pF
Reverse transfer capacitance	C_{rss}		-	55	-	pF
Total gate charge						
Turn-on delay time	$t_{d(on)}$	V_{DD}=100V,I_D=9.0A, V_{GS}=10V,R_G=12Ω	-	7.0	-	ns
Rise time	t_r		-	6.0	-	ns
Turn-off delay time	$t_{d(off)}$		-	20	-	ns
Fall time	t_f		-	6.0	-	ns
Total gate charge	Q_g	V_{DD}=100V,I_D=9.0A , V_{GS}=0 to10V	-	28	-	nC
Gate-source charge	Q_{gs}		-	12	-	nC
Gate-drain charge	Q_{gd}		-	2.0	-	nC
Drain-source diode characteristics						
Drain-source diode forward voltage	V_{SD}	V_{GS}=0V,I_s=9.0A	-	-	1.5	V
Continuous drain-source current [2]	I_{SD}	Integral pn-diode In MOSFET	-	-	9	A
Pulsed drain-source current[2]	I_{SM}		-	-	36	A
Reverse recovery time	t_{rr}	V_{GS}=0V,I_F=9.0A d_{IF}/dt=100A/μs	-	238	-	ns
Reverse recovery charge	Q_{rr}		-	1.0	-	μC

Note: [1] TJ=+25 ℃ to +150 ℃
[2] Pulse width≤380μs; duty cycle≤2%.

8. Typical Characteristics

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

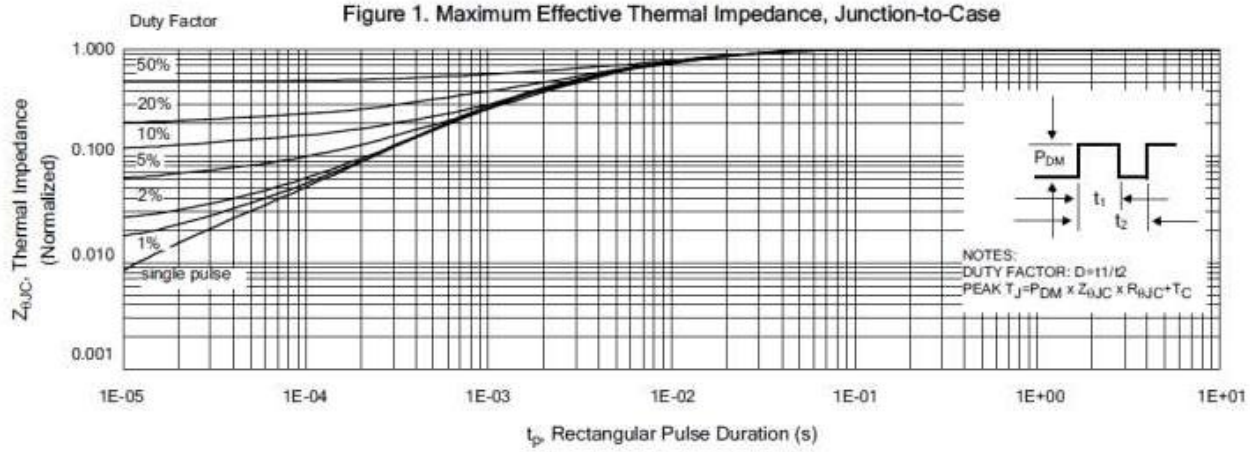


Figure 2. Maximum Power Dissipation vs Case Temperature

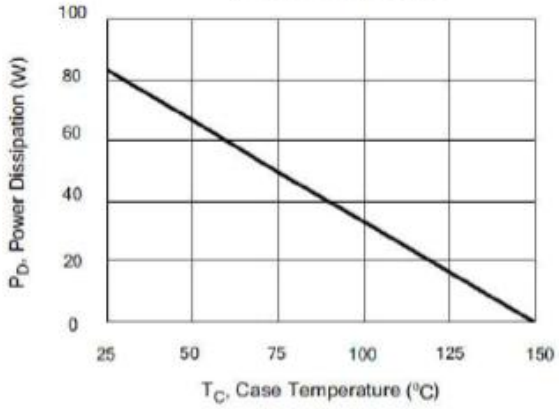


Figure3. Maximum Continuous Drain Current vs Case Temperature

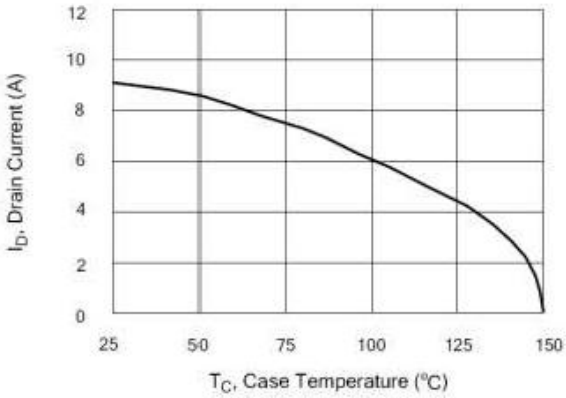


Figure 4. Typical Output Characteristics

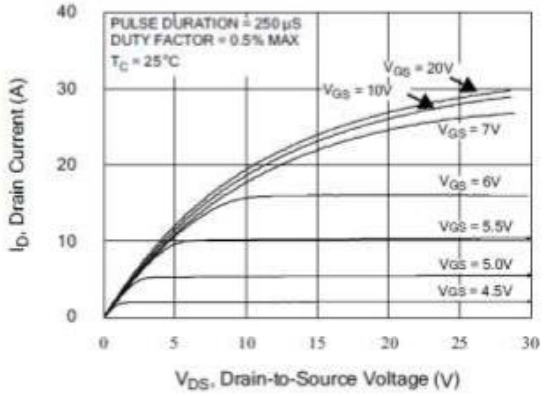


Figure5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

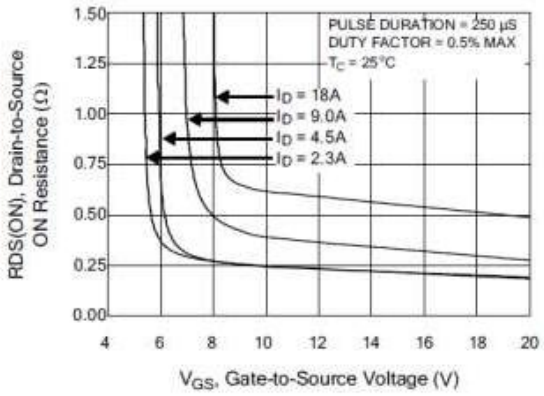


Figure 6. Maximum Peak Current Capability

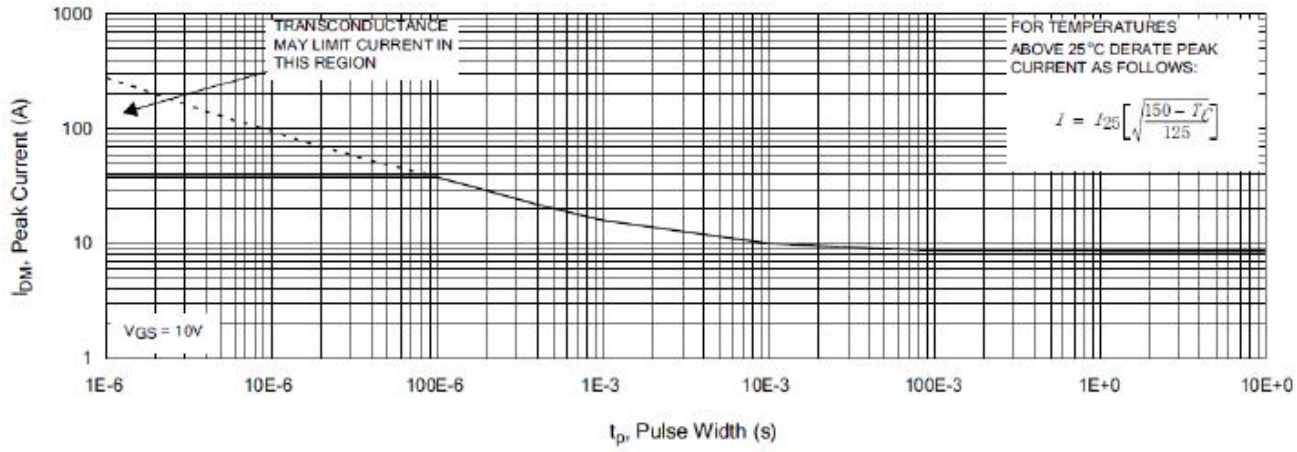


Figure 7. Typical Transfer Characteristics

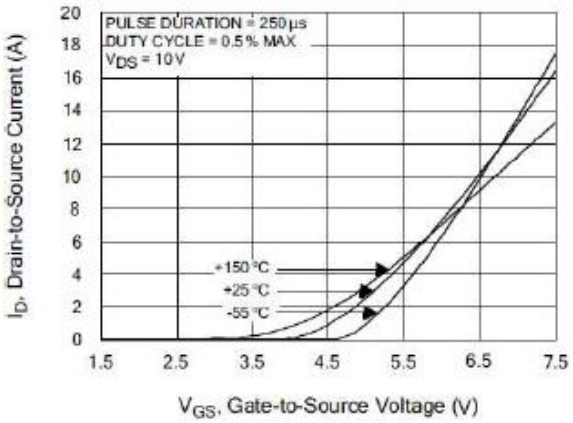


Figure8. Unclamped Inductive Switching Capability

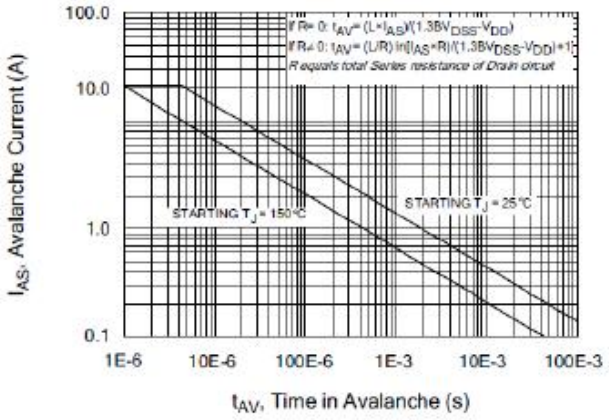


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

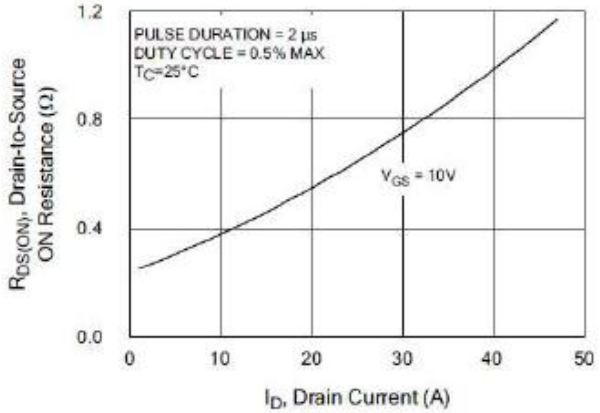


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

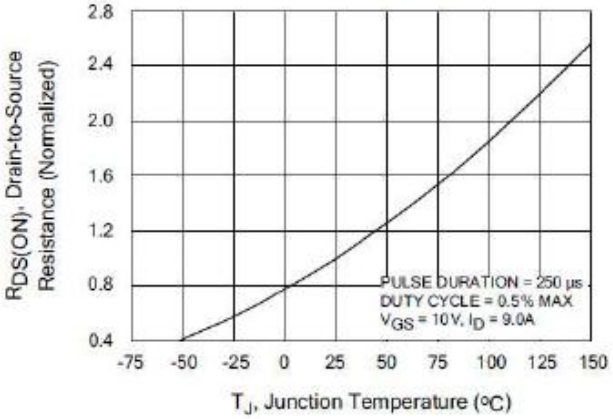


Figure 11. Typical Breakdown Voltage vs Junction Temperature

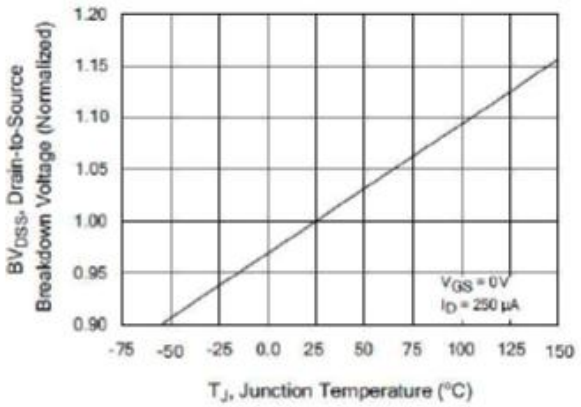


Figure 12. Typical Threshold Voltage vs Junction Temperature

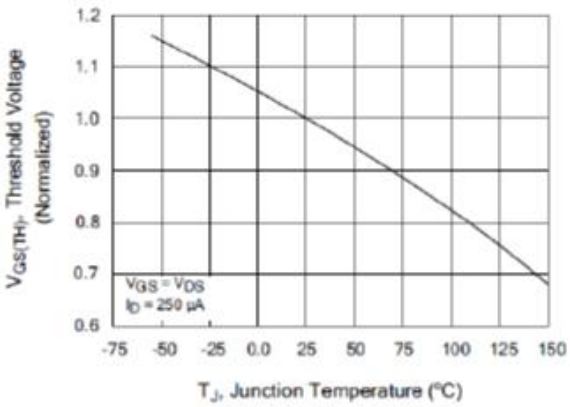


Figure 13. Maximum Forward Bias Safe Operating Area

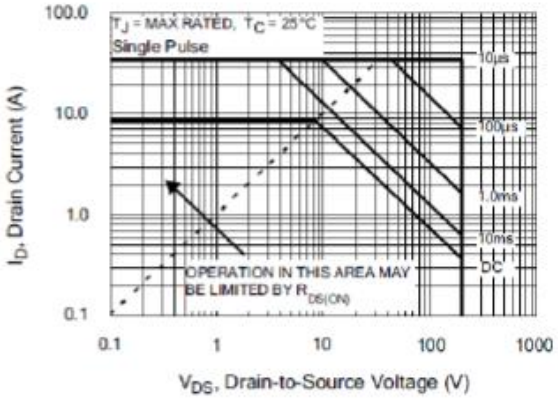


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

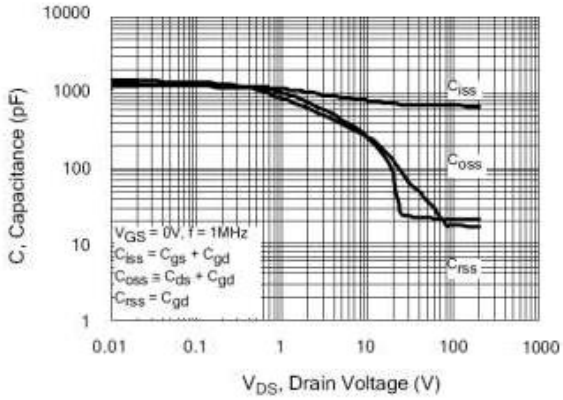


Figure 15 .Typical Gate Charge

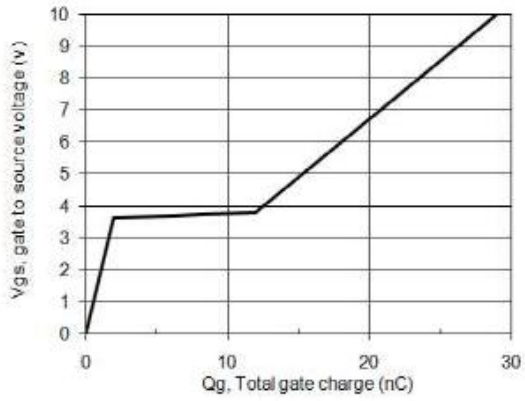
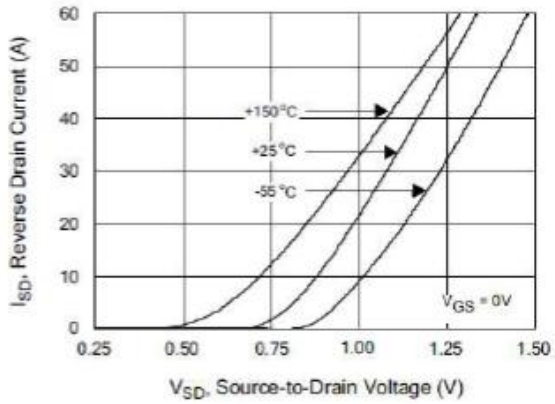


Figure 16. Typical Body Diode Transfer Characteristics



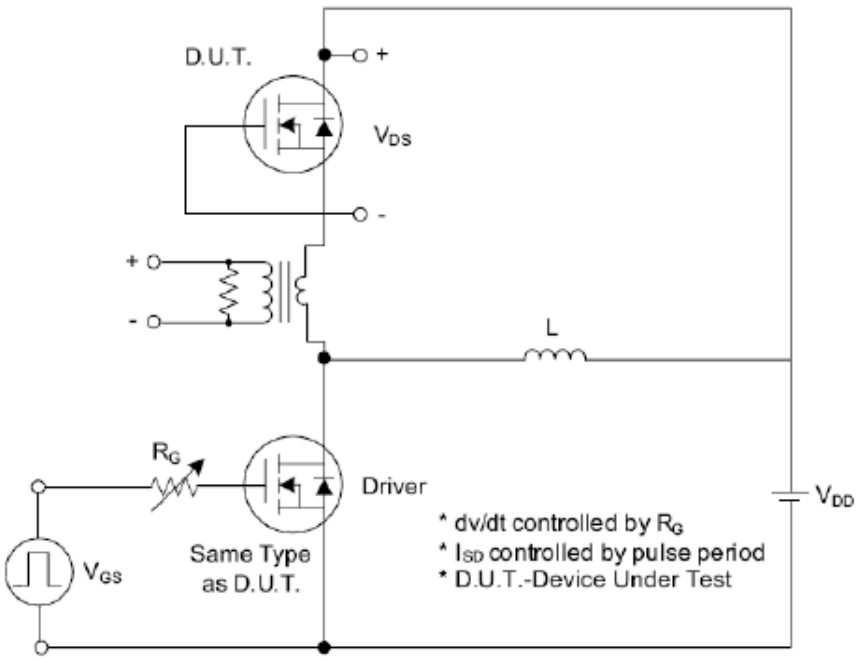


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

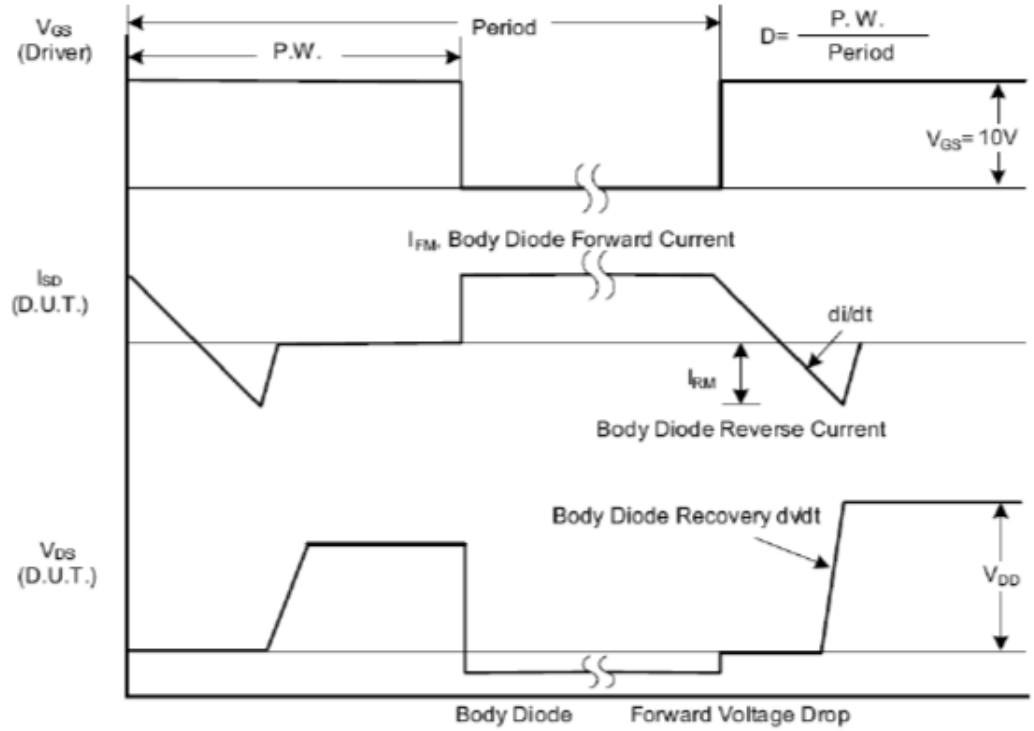


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

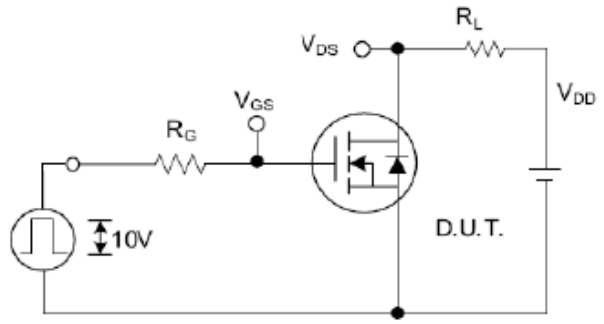


Fig. 2.1 Switching Test Circuit

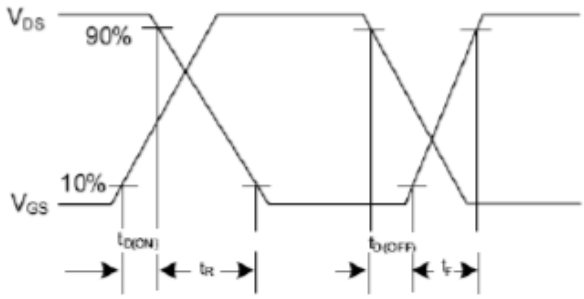


Fig. 2.2 Switching Waveforms

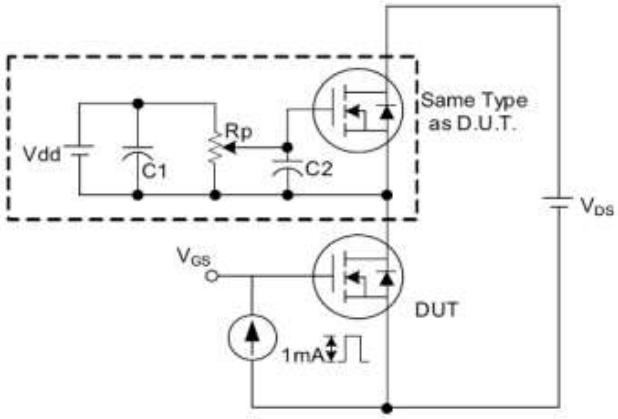


Fig. 3 . 1 Gate Charge Test Circuit

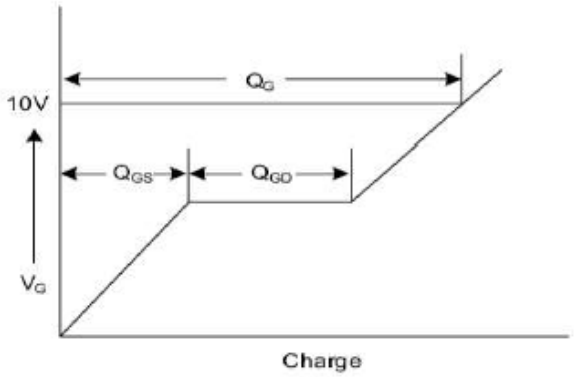


Fig. 3 . 2 Gate Charge Waveform

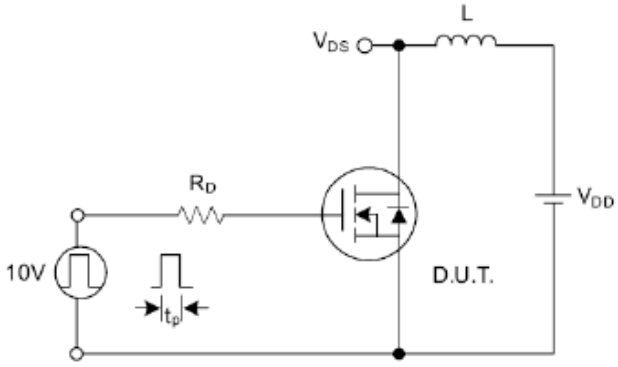


Fig. 4.1 Unclamped Inductive Switching Test Circuit

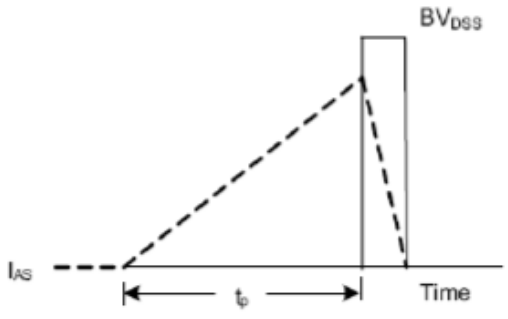


Fig. 4.2 Unclamped Inductive Switching Waveforms