Automotive Grade Start-Stop Non-Synchronous Boost Controller

NCV8878

The NCV8878 is a Non-Synchronous Boost controller designed to supply a minimum output voltage during Start-Stop vehicle operation battery voltage sags. The controller drives an external N-channel MOSFET. The device uses peak current mode control with internal slope compensation. The IC incorporates an internal regulator that supplies charge to the gate driver.

Protection features include, cycle-by-cycle current limiting and thermal shutdown.

Additional features include low quiescent current sleep mode operation. The NCV8878 is enabled when the supply voltage drops below the wake up threshold. Boost Operation is initiated when the supply voltage drops below the regulation set point.

Features

- Automatic Enable Below Wake Up Threshold Voltage (Factory Programmable)
- Status Pin Diagnostic Function
- Override Disable Function
- Boost Mode Operation at Regulation Set Point
- ±2% Output Accuracy Over Temperature Range
- Peak Current Mode Control with Internal Slope Compensation
- Wide Input Voltage Range of 2 V to 40 V, 45 V Load Dump
- Low Quiescent Current in Sleep Mode (<12 μA Typical)
- Cycle−by−Cycle Current Limit Protection
- Hiccup−Mode Overcurrent Protection (OCP)
- Thermal Shutdown (TSD)
- This is a Pb−Free Device
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100

Typical Applications

- Applications Requiring Regulated Voltage through Cranking and Start−Stop Operation

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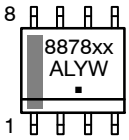
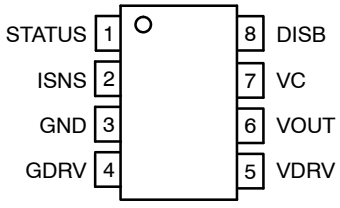
SOIC−8
D SUFFIX
CASE 751
STYLE N/A

MARKING DIAGRAM



8878xx	= Specific Device Code
	xx = 01
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCV887801D1R2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

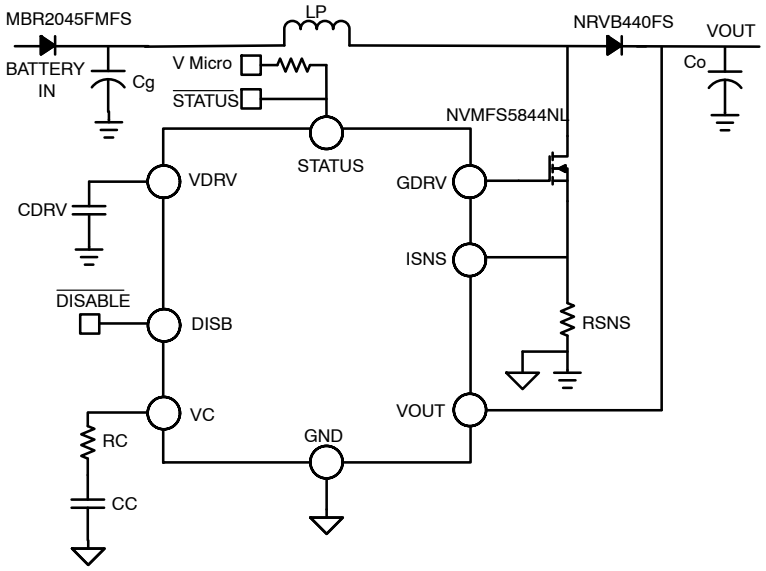


Figure 1. Typical Application

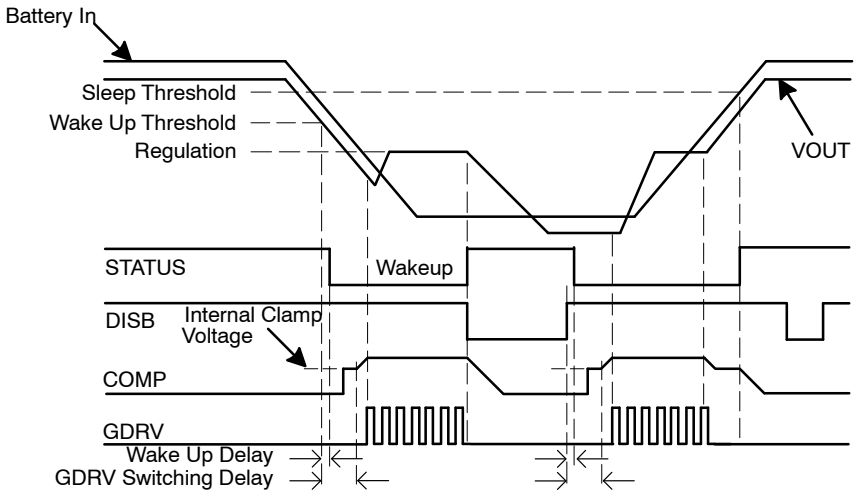


Figure 2. Functional Waveforms

PACKAGE PIN DESCRIPTIONS

Pin No.	Pin Symbol	Function
1	STATUS	This is an open−drain diagnostic. IC status operation flag indicator. This output is a logic low when IC VOUT is below the wake up threshold voltage ($Th_{ic,en}$) and device is active. A pull−up resistor of around 80 kΩ should be connected between STATUS and a microcontroller reference. This output is a logic high when the IC is disabled or in UVLO.
2	ISNS	Current sense input. Connect this pin to the source of the external N−MOSFET, through a current−sense resistor to ground to sense the switching current for regulation and current limiting.
3	GND	Ground reference.
4	GDRV	Gate driver output. Connect to gate of the external N−MOSFET. A series resistance can be added from GDRV to the gate to tailor EMC performance.
5	VDRV	Driving voltage. Internally−regulated supply for driving the external N−MOSFET, sourced from VOUT. Bypass with a 1.0 μF ceramic capacitor to ground.
6	VOUT	Monitors output voltage and provides IC input voltage.
7	VC	Output of the voltage error transconductance amplifier. An external compensator network from VC to GND is used to stabilize the converter.
8	DISB	Disable input. This part is disabled when this pin is brought low.

ABSOLUTE MAXIMUM RATINGS (Voltages are with respect to GND, unless otherwise indicated)

Rating	Value	Unit
Dc Supply Voltage (VOUT)	−0.3 to 40	V
Peak Transient Voltage (Load Dump on VOUT)	45	V
Dc Supply Voltage (VDRV, GDRV)	12	V
Dc Voltage (VC, ISNS)	−0.3 to 3.6	V
Dc Voltage (DISB, STATUS)	−0.3 to 6	V
Dc Voltage Stress (VOUT − VDRV)	−0.7 to 40	V
Operating Junction Temperature	−40 to 150	°C
Storage Temperature Range	−65 to 150	°C
Peak Reflow Soldering Temperature: Pb−Free, 60 to 150 seconds at 217°C	265 peak	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

PACKAGE CAPABILITIES

Characteristic		Value	Unit
ESD Capability (All Pins)	Human Body Model	≥2.0	kV
Moisture Sensitivity Level		1	
Package Thermal Resistance	Junction−to−Ambient, $R_{\theta JA}$ (Note 1)	100	°C/W

1. 1 in^2, 1 oz copper area used for heatsinking.

TYPICAL VALUES

Part No.	D_{max}	f_S	S_a	V_{cl}	I_{src}	I_{sink}	VOUT	SCE
NCV887801	83%	450 kHz	53 mV/μs	200 mV	800 mA	600 mA	6.8 V	N

ELECTRICAL CHARACTERISTICS (−40°C < T_J < 150°C, 3.6 V < V_{OUT} < 40 V, unless otherwise specified) Min/Max values are guaranteed by test, design or statistical correlation.

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
GENERAL						
Quiescent Current, Sleep Mode	$I_{q,sleep}$	V_{OUT} = 13.2 V, T_J = 25°C, DISB = 0 V	–	12	14	μA
Quiescent Current, No switching	$I_{q,off}$	Into V_{OUT} pin, VOUT,reg < V_{OUT} < VOUT,des, No switching	–	2.2	4.0	mA
OSCILLATOR						
Switching Frequency	F_{SW}	NCV887801	405	450	495	kHz
Minimum Pulse Width	$t_{on,min}$		90	115	145	ns
Maximum Duty Cycle	D_{max}		81	83	85	%
Slope Compensating Ramp (Note 2)	S_a	NCV887801	46	53	60	mV/ μs
STATUS FLAG						
STATUS Wake Up Delay		V_{OUT} < 7.3 V $Th_{ic,en}$	–	9.3	14	μs
STATUS Pull−down Capability		Sinking 1.0 mA	–	–	400	mV
DISABLE						
DISB Pull−down Current (Note 2)	I_{DIS}	V_{DIS} = 5 V	–	0.6	1.0	μA
DISB Input High Voltage	$V_{d,ih}$		2.0	–	5.0	V
DISB Input High Voltage Hysteresis	$V_{d,hys}$		–	500	–	mV
DISB Input Low Voltage	$V_{d,il}$		0	–	800	mV
CURRENT SENSE AMPLIFIER						
Low−Frequency Gain	A_{csa}	Input−to−output gain at dc, ISNS ≤ 1 V	0.9	1.0	1.1	V/V
Bandwidth	BW_{csa}	Gain of A_{csa} − 3 dB	2.5	–	–	MHz
ISNS Input Bias Current	$I_{sns,bias}$	Out of ISNS pin	–	30	50	μA
Current Limit Threshold Voltage	V_{cl}	Voltage on ISNS pin NCV887801	180	200	220	mV
Current Limit, Response Time (Note 2)	t_{cl}	CL tripped until GDRV falling edge, V_{ISNS} = V_{cl}(typ) + 60 mV	–	80	125	ns
Overcurrent Protection, Threshold Voltage	$\%V_{ocp}$	Percent of V_{cl}	125	150	175	%
Overcurrent Protection, Response Time (Note 2)	t_{ocp}	From overcurrent event, Until switching stops, V_{ISNS} = V_{OCP} + 40 mV	–	80	125	ns
VOLTAGE ERROR OPERATIONAL TRANSCONDUCTANCE AMPLIFIER						
Transconductance	$g_{m,vea}$	V_{OUT} = ±100 mV	0.8	1.2	1.63	mS
VEA Output Resistance (Note 2)	$R_{o,vea}$		2.0	–	–	MΩ
VEA Maximum Output Voltage	$V_{c,max}$		2.5	–	–	V
VEA Sourcing Current	$I_{src,vea}$	VEA output current, Vc = 2.0 V	80	100	–	μA
VEA Sinking Current	$I_{snk,vea}$	VEA output current, Vc = 1.5 V	80	100	–	μA
VEA Clamp Voltage	$V_{c,clamp}$	V_{OUT} < VOUT,des	–	1.1	–	V
GDRV Switching Delay		V_{OUT} < VOUT,des or when IC DISB goes from low to high with Vc pin compensation network disconnected	–	55	64	μs
GATE DRIVER						
Sourcing Current	I_{src}	V_{DRV} ≥ Typical Driving Voltage Specification, V_{DRV} − V_{GDRV} = 2 V	550	800	–	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Not tested in production. Limits are guaranteed by design.

ELECTRICAL CHARACTERISTICS (−40°C < T_J < 150°C, 3.6 V < V_{OUT} < 40 V, unless otherwise specified) Min/Max values are guaranteed by test, design or statistical correlation.

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
GATE DRIVER						
Sinking Current	I_{sink}	$V_{GDRV} \geq 2$ V	480	600	–	mA
Driving Voltage Dropout (Note 2)	$V_{drv,do}$	$V_{OUT} - V_{DRV}$, Iv_{DRV} = 25 mA	–	0.3	0.6	V
Driving Voltage Source Current	I_{drv}	$V_{OUT} - V_{DRV}$ = 1 V	35	45	–	mA
Backdrive Diode Voltage Drop	$V_{d,bd}$	$V_{DRV} - V_{OUT}$, $I_{d,bd}$ = 5 mA	–	–	0.7	V
Driving Voltage	V_{DRV}	I_{VDRV} = 0.1 – 25 mA	5.8	6.0	6.2	V
Pull−down Resistance			–	21	–	kΩ
UVLO						
Undervoltage Lock−out, Threshold Voltage	$V_{uvlo,fall}$	V_{OUT} falling	3.40	3.59	3.80	V
Undervoltage Lock−out	$V_{uvlo,\ rise}$	V_{OUT} rising	3.90	4.05	4.20	V
THERMAL SHUTDOWN						
Thermal Shutdown Threshold (Note 2)	T_{sd}	T_J rising	160	170	180	°C
Thermal Shutdown Hysteresis (Note 2)	$T_{sd,hys}$	T_J falling	10	15	20	°C
Thermal Shutdown Delay (Note 2)	$t_{sd,dly}$	From $T_J > T_{sd}$ to stop switching	–	–	100	ns
VOLTAGE REGULATION						
Voltage Regulation	$VOUT_{,reg}$	NCV887801	6.66	6.80	6.94	V
Threshold IC Enable		V_{OUT} descending NCV887801	7.10	7.30	7.50	V
Threshold IC Disable		V_{OUT} ascending NCV887801	7.55	7.75	7.95	V
Threshold IC Enable – Voltage Regulation		NCV887801	0.32	0.5	–	V
Threshold IC Disable – Threshold IC Enable		NCV887801	–	0.4	–	V

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2. Not tested in production. Limits are guaranteed by design.

TYPICAL CHARACTERISTICS

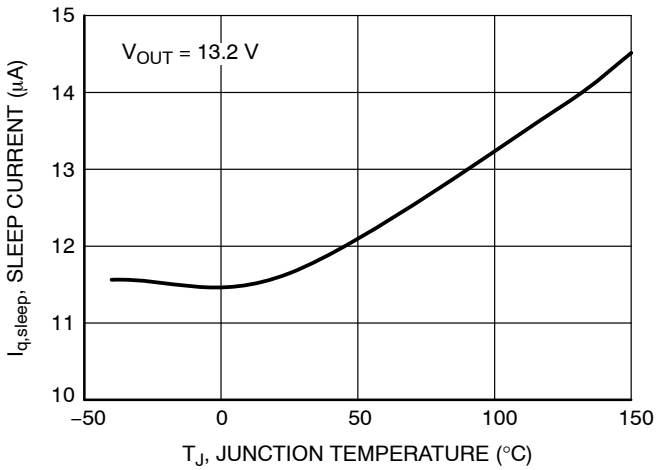


Figure 3. Sleep Current vs. Temperature

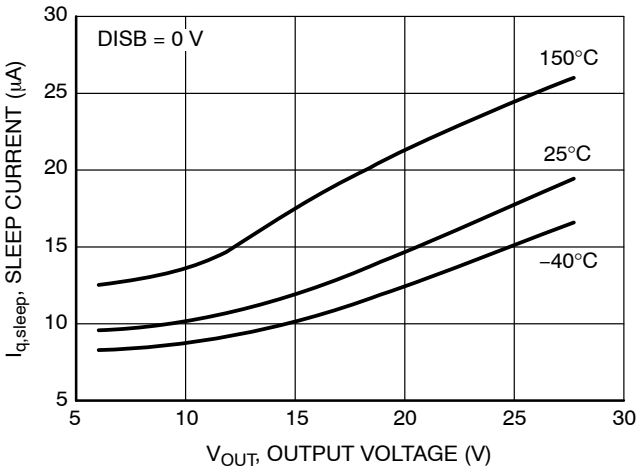


Figure 4. Sleep Current vs. V_{OUT}

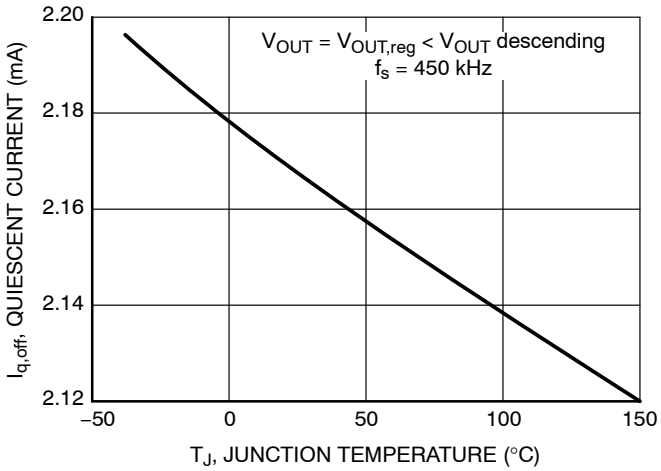


Figure 5. Quiescent Current vs. Temperature

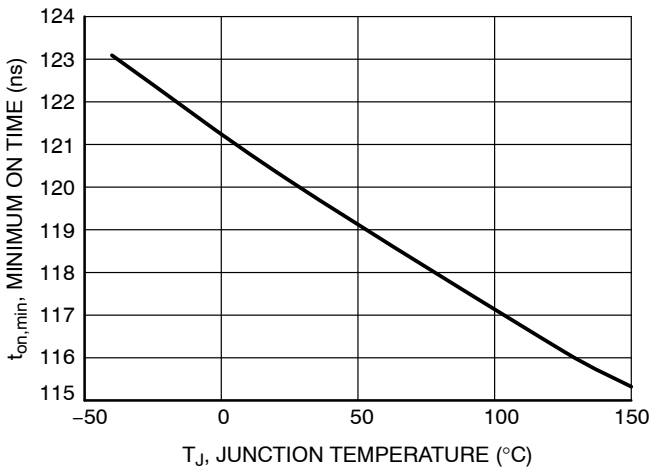


Figure 6. Minimum On Time vs. Temperature

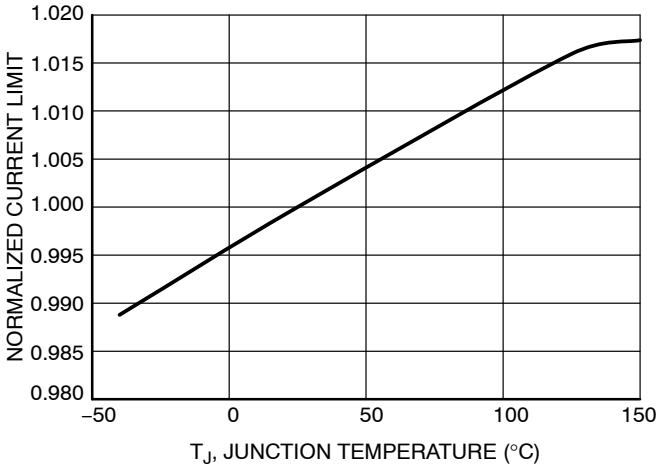


Figure 7. Normalized Current vs. Temperature

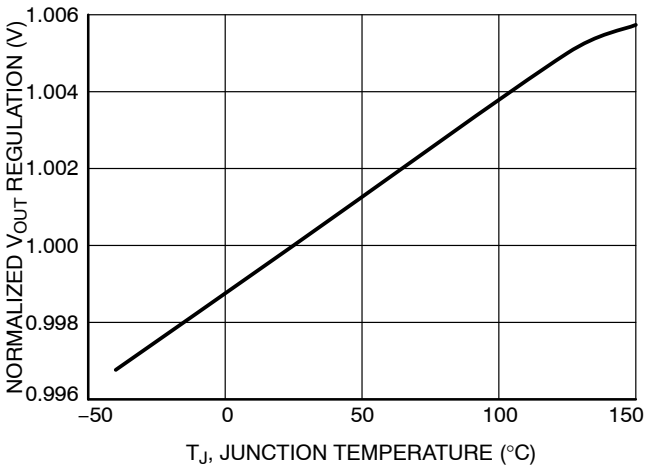


Figure 8. V_{OUT} Regulation vs. Temperature

TYPICAL CHARACTERISTICS

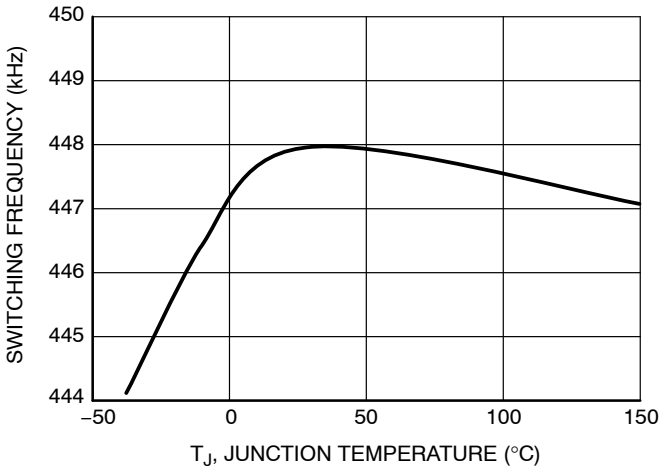


Figure 9. Switching Frequency vs. Temperature

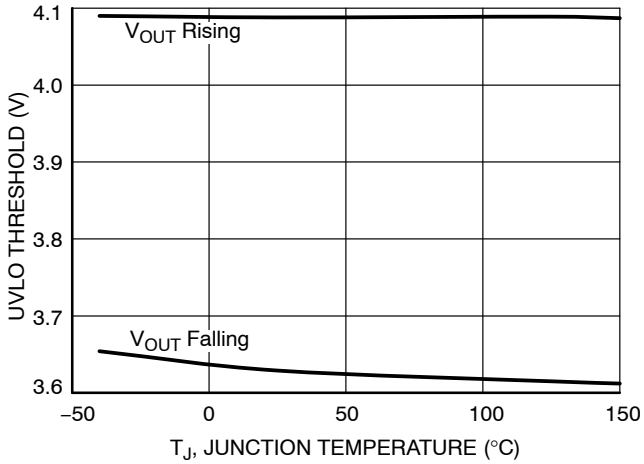


Figure 10. UVLO Threshold vs. Temperature

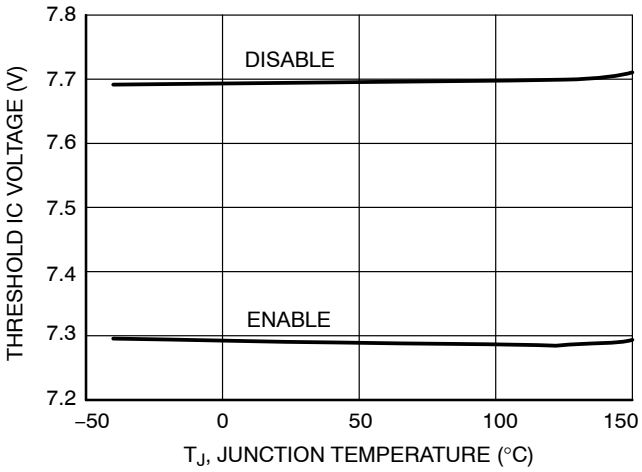


Figure 11. NCV887801 Threshold IC Voltage vs. Temperature

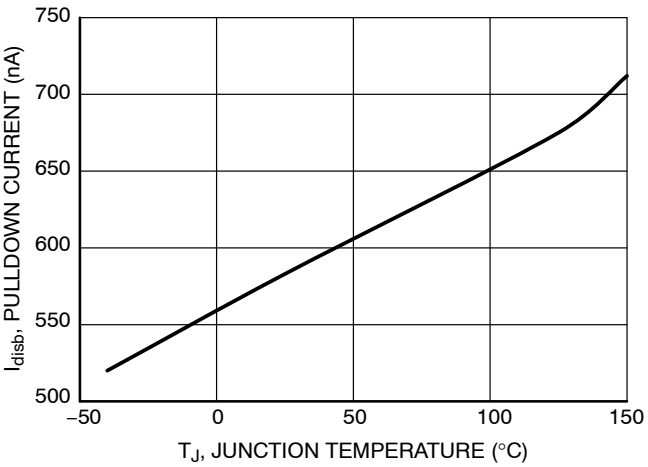


Figure 12. DISB Pulldown Current vs. Temperature

THEORY OF OPERATION

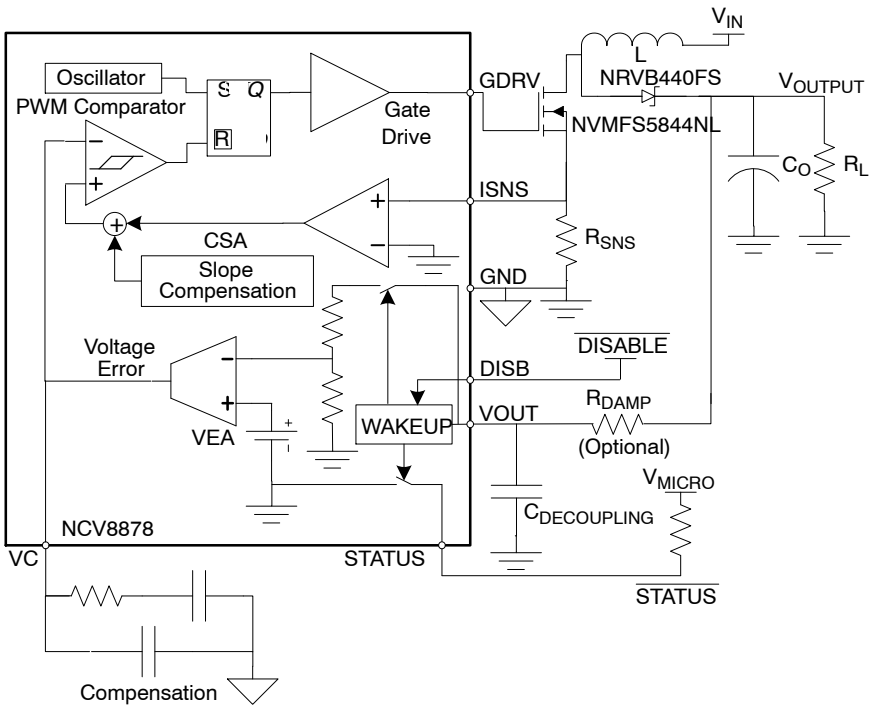


Figure 13. Current Mode Control Schematic

DISB

The DISB pin provides an IC disable function. When a DC logic-low voltage is applied to this pin, the NCV8878 enters a low quiescent sleep mode, permitting an external signal to either shutdown the IC or disable the wakeup function.

Regulation

The NCV8878 is a non−synchronous boost controller designed to supply a minimum output voltage during Start−Stop vehicle operation battery voltage sags. The NCV8878 is in low quiescent current sleep mode under normal battery operation (12 V) and is enabled when the supply voltage drops below the descending threshold (7.3 V for the NCV887801). Boost operation is initiated when the supply voltage is below the regulation set point (6.8 V for the NCV887801). Once the supply voltage sag condition ends and begins to increase, the NCV8878 boost operation will cease when the supply voltage increases beyond the regulation set point. The NCV8878 low quiescent current sleep mode resumes once the supply voltage increases beyond the ascending voltage threshold (7.7 V for the NCV887801).

The NCV8878 VOUT pin serves the dual purpose: (1) powering the NCV8878 and (2) providing the regulation feedback signal. The feedback network is imbedded within the IC to eliminate the constant current battery drain that would exist with the use of external voltage feedback resistors.

There is no soft−start operating mode. The NCV8878 will instantly respond to a voltage sag so as to maintain normal operation of downstream loads. Once the NCV8878 is enabled, the voltage error operational transconductance amplifier supplies current to set VC to 1.1 V to minimize the feedback loop response time when the battery voltage sag goes below the regulation set point.

Current Mode Control

The NCV8878 incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on−time of the power switch. The oscillator is used as a fixed−frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and the error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse−by−pulse current limiting by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows for a simpler compensation.

The NCV8878 also includes a slope compensation scheme in which a fixed ramp generated by the oscillator is added to the current ramp. A proper slope rate is provided to improve circuit stability without sacrificing the advantages of current mode control.

Current Limit

The NCV8878 features two current limit protections, peak current mode and over current latch off. When the current sense amplifier detects a voltage above the peak current limit between ISNS and GND after the current limit

leading edge blanking time, the peak current limit causes the power switch to turn off for the remainder of the cycle. Set the current limit with a resistor from ISNS to GND, with $R = V_{CL} / I_{limit}$.

If the voltage across the current sense resistor exceeds the over current threshold voltage the device enters over current hiccup mode. The device will remain off for the hiccup time and then go through the soft−start procedure.

UVLO

Input Undervoltage Lockout (UVLO) is provided to ensure that unexpected behavior does not occur when VIN is too low to support the internal rails and power the controller. The IC will start up when enabled and VIN surpasses the UVLO threshold plus the UVLO hysteresis and will shut down when VIN drops below the UVLO threshold or the part is disabled.

VDRV

An internal regulator provides the drive voltage for the gate driver. Bypass with a ceramic capacitor to ground to ensure fast turn on times. The capacitor should be between 0.1 μF and 1 μF, depending on switching speed and charge requirements of the external MOSFET.

VDRV uses an internal linear regulator to charge the VDRV bypass capacitor. VOUT must be decoupled at the IC by a capacitor that is equal or larger in value than the VDRV decoupling capacitor.

APPLICATION INFORMATION

Design Methodology

This section details an overview of the component selection process for the NCV8878 in continuous conduction mode boost. It is intended to assist with the design process but does not remove all engineering design work. Many of the equations make heavy use of the small ripple approximation. This process entails the following steps:

1. Define Operational Parameters
2. Select Current Sense Resistor
3. Select Output Inductor
4. Select Output Capacitors
5. Select Input Capacitors
6. Select Compensator Components
7. Select MOSFET(s)
8. Select Diode
9. Design Notes
10. Determine Feedback Loop Compensation Network

1. Define Operational Parameters

Before beginning the design, define the operating parameters of the application. These include:

$V_{IN(min)}$: minimum input voltage [V]
$V_{IN(max)}$: maximum input voltage [V]
V_{OUT}: output voltage [V]
$I_{OUT(max)}$: maximum output current [A]
I_{CL}: desired typical cycle-by-cycle current limit [A]

From this the ideal minimum and maximum duty cycles can be calculated as follows:

$$D_{min} = 1 - \frac{V_{IN(max)}}{V_{OUT}}$$

$$D_{max} = 1 - \frac{V_{IN(min)}}{V_{OUT}}$$

Both duty cycles will actually be higher due to power loss in the conversion. The exact duty cycles will depend on conduction and switching losses. If the maximum input voltage is higher than the output voltage, the minimum duty cycle will be negative. This is because a boost converter cannot have an output lower than the input. In situations where the input is higher than the output, the output will follow the input, minus the diode drop of the output diode and the converter will not attempt to switch.

If the calculated D_{max} is higher the D_{max} of the NCV8878, the conversion will not be possible. It is important for a boost converter to have a restricted D_{max}, because while the ideal conversion ration of a boost converter goes up to infinity as D approaches 1, a real converter's conversion ratio starts to decrease as losses overtake the increased power transfer. If the converter is in this range it will not be able to regulate properly.

If the following equation is not satisfied, the device will skip pulses at high V_{IN}:

$$\frac{D_{min}}{f_s} \geq t_{on(min)}$$

Where: f_s: switching frequency [Hz]
$t_{on(min)}$: minimum on time [s]

2. Select Current Sense Resistor

Current sensing for peak current mode control and current limit relies on the MOSFET current signal, which is measured with a ground referenced amplifier. The easiest method of generating this signal is to use a current sense resistor from the source of the MOSFET to device ground. The sense resistor should be selected as follows:

$$R_S = \frac{V_{CL}}{I_{CL}}$$

Where: R_S: sense resistor [Ω]
V_{CL}: current limit threshold voltage [V]
I_{CL}: desire current limit [A]

3. Select Output Inductor

The output inductor controls the current ripple that occurs over a switching period. A high current ripple will result in excessive power loss and ripple current requirements. A low current ripple will result in a poor control signal and a slow current slew rate in case of load steps. A good starting point for peak to peak ripple is around 20−40% of the inductor current at the maximum load at the worst case V_{IN}, but operation should be verified empirically. The worst case V_{IN}

is half of V_{OUT}, or whatever V_{IN} is closest to half of V_{OUT}. After choosing a peak current ripple value, calculate the inductor value as follows:

$$L = \frac{V_{IN(WC)}\, D_{WC}}{\Delta I_{L,max}\, f_s}$$

Where: $V_{IN(WC)}$: V_{IN} value as close as possible to half of V_{OUT} [V]
D_{WC}: duty cycle at $V_{IN(WC)}$
$\Delta I_{L,max}$: maximum peak to peak ripple [A]

The maximum average inductor current can be calculated as follows:

$$I_{L,AVG} = \frac{V_{OUT} I_{OUT(max)}}{V_{IN(min)} \eta}$$

The Peak Inductor current can be calculated as follows:

$$I_{L,peak} = I_{L,avg} + \frac{\Delta I_{L,max}}{2}$$

Where: $I_{L,peak}$: Peak inductor current value [A]

4. Select Output Capacitors

The output capacitors smooth the output voltage and reduce the overshoot and undershoot associated with line transients. The steady state output ripple associated with the output capacitors can be calculated as follows:

$$V_{OUT(ripple)} = \frac{D I_{OUT(max)}}{f C_{OUT}} + \left(\frac{I_{OUT(max)}}{1 - D} + \frac{V_{IN(min)} D}{2 f L} \right) R_{ESR}$$

The capacitors need to survive an RMS ripple current as follows:

$$I_{Cout(RMS)} = I_{OUT} \sqrt{\frac{D_{WC}}{D'_{WC}} + \frac{D_{WC}}{12} \left(\frac{D'_{WC}}{\frac{L}{R_{OUT} \times T_{SW}}} \right)^2}$$

The use of parallel ceramic bypass capacitors is strongly encouraged to help with the transient response.

5. Select Input Capacitors

The input capacitor reduces voltage ripple on the input to the module associated with the ac component of the input current.

$$I_{Cin(RMS)} = \frac{V_{IN(WC)}^{\,2}\, D_{WC}}{L f_s V_{OUT} 2\sqrt{3}}$$

6. Select Compensator Components

Current Mode control method employed by the NCV8878 allows the use of a simple, Type II compensation to optimize the dynamic response according to system requirements.

7. Select MOSFET(s)

In order to ensure the gate drive voltage does not drop out the MOSFET(s) chosen must not violate the following inequality:

$$Q_{g(total)} \le \frac{I_{drv}}{f_s}$$

Where: $Q_{g(total)}$: Total Gate Charge of MOSFET(s) [C]
I_{drv}: Drive voltage current [A]
f_s: Switching Frequency [Hz]

The maximum RMS Current can be calculated as follows:

$$I_{Q(max)} = I_{out} \frac{\sqrt{D}}{D'}$$

The maximum voltage across the MOSFET will be the maximum output voltage, which is the higher of the maximum input voltage and the regulated output voltaged:

$$V_{Q(max)} = V_{OUT(max)}$$

8. Select Diode

The output diode rectifies the output current. The average current through diode will be equal to the output current:

$$I_{D(avg)} = I_{OUT(max)}$$

Additionally, the diode must block voltage equal to the higher of the output voltage and the maximum input voltage:

$$V_{D(max)} = V_{OUT(max)}$$

The maximum power dissipation in the diode can be calculated as follows:

$$P_D = V_{f(max)}\, I_{OUT(max)}$$

Where: P_d: Power dissipation in the diode [W]
$V_{f(max)}$: Maximum forward voltage of the diode [V]

9. Design Notes

- VOUT serves a dual purpose (feedback and IC power). The VDRV circuit has a current pulse power draw resulting in current flow from the output sense location to the IC. Trace ESL will cause voltage ripple to develop at IC pin VOUT which could affect performance.
  - Use a 1 μF IC VOUT pin decoupling capacitor close to IC in addition to the VDRV decoupling capacitor.
- Classic feedback loop measurements are not possible (VOUT pin serves a dual purpose as a feedback path and IC power). Feedback loop computer modeling recommended.
  - A step load test for stability verification is recommended.
- Compensation ground must be dedicated and connected directly to IC ground.
  - Do not use vias. Use a dedicated ground trace.
- IC ground & current sense resistor ground sense point must be located on the same side of PCB.
  - Vias introduce sufficient ESR/ESL voltage drop which can degrade the accuracy of the current feedback signal amplitude (signal bounce) and should be avoided.
- Star ground should be located at IC ground pad.
  - This is the location for connecting the compensation and current sense grounds.
- The IC architecture has a leading edge ISNS blanking circuit. In some instances, current pulse leading edge current spike RC filter may be required.
  - If required, 330 pF + 250 Ω are a recommended evaluation starting point.
- $R_{DAMPING}$ (optional)
  - The IC-VOUT pin may be located a few cm from the output voltage sensing point. Parasitic inductance from the feedback trace (roughly 5 nH/cm) results in the requirement for a decoupling capacitor ($C_{decoupling}$ = 1 μF recommended) next to the IC-VOUT pin to support the VDRV charging pulses. The IC-VDRV energy is replenished from current pulses by an internal linear regulator whose charging frequency corresponds to that of the IC oscillator (phase lag may occur; some charging pulses may occasionally be skipped depending on the state of the VDRV voltage). The trace's parasitic inductance can introduce a low amplitude damped voltage oscillation between the IC-VOUT and the output voltage sense location which may result in minor frequency jitter.
  - If the measured frequency jitter is objectionable, it may be attenuated by placing a series damping resistor (R_{damp}) in the feedback path between the output voltage sense and IC-VOUT. The resulting filter introduced by R_{damp} introduces a high frequency pole in the feedback loop path. The RC filter 3 dB pole frequency must be chosen at a minimum of 1 decade above the design's feedback loop cross-over frequency (at minimum power supply input voltage where the worst case phase margin will occur) to avoid deteriorating the feedback loop cross-over frequency phase margin.
  - The average operating current demand from the IC is dominated by the MOSFET gate drive power energy consumption ($I_{VDRV} = Q_g(tot)\_6V \times f_{osc}$). The $I_{VDRV} \times R_{damp}$ voltage drop results in a corresponding increase in power supply regulation voltage. R_{damp} is typically 0.68 Ω, so the resulting increase in output voltage regulation will be minimal (10-30 mV may be typical).

10. Determine Feedback Loop Compensation Network

The purpose of a compensation network is to stabilize the dynamic response of the converter. By optimizing the compensation network, stable regulation response is achieved for input line and load transients.

Compensator design involves the placement of poles and zeros in the closed loop transfer function. Losses from the boost inductor, MOSFET, current sensing and boost diode losses also influence the gain and compensation expressions. The OTA has an ESD protection structure ($R_{ESD} \approx 502$ Ω, data not provided in the datasheet) located on the die between the OTA output and the IC package compensation pin (VC). The information from the OTA PWM feedback control signal (V_{CTRL}) may differ from the IC−VC signal if R_2 is of similar order of magnitude as R_{ESD}. The compensation and gain expressions which follow take influence from the OTA output impedance elements into account.

Type−I compensation is not possible due to the presence of R_{ESD}. The Figure 14 compensation network corresponds to a Type−II network in series with R_{ESD}. The resulting control−output transfer function is an accurate mathematical model of the IC in a boost converter topology. The model does have limitations and a more accurate SPICE model should be considered for a more detailed analysis:

- The attenuating effect of large value ceramic capacitors in parallel with output electrolytic capacitor ESR is not considered in the equations.
- The efficiency term η should be a reasonable operating condition estimate.

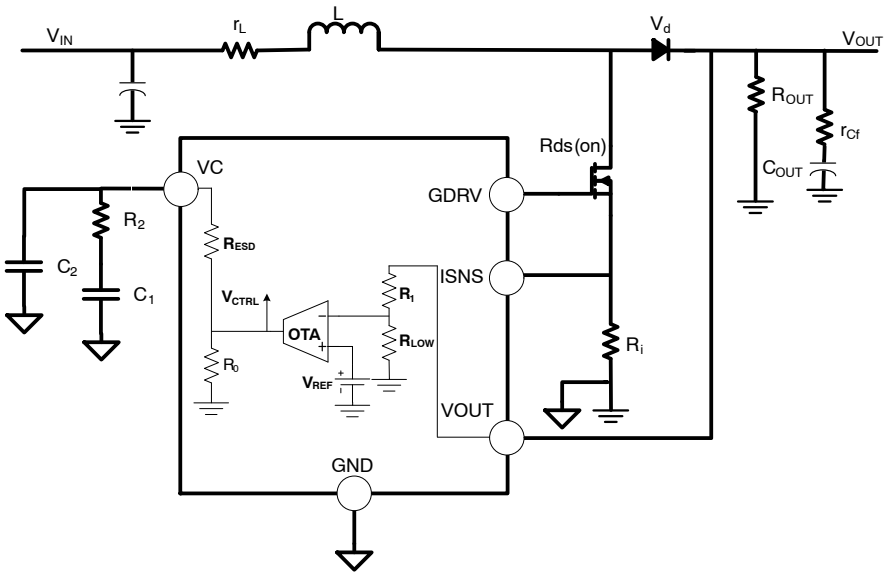


Figure 14. NCV8878 OTA and Compensation

A worksheet as well as a SPICE model which may be used for selecting compensation components R_2, C_1, C_2 is available at the ON Semiconductor web site (http://onsemi.com/PowerSolutions/product.do?id=NCV8878). The following equations may be used to analyze the Figure 10 boost converter. Required input design parameters for analysis are:

V_d = Boost diode V_f (V)
V_{IN} = Boost supply input voltage (V)
R_i = Current sense resistor (Ω)
$R_{DS(on)}$ = MOSFET $R_{DS(on)}$ (Ω)
C_{OUT} = Bulk output capacitor value (F)
R_{sw_eq} = $R_{DS(on)}$ + R_i, for the boost continuous conduction mode (CCM) expressions
r_{CF} = Bulk output capacitor ESR (Ω)
R_{OUT} = Equivalent resistance of output load (Ω)
P_{out} = Output Power (W)
L = Boost inductor value (H)
r_L = Boost inductor ESR (Ω)
$T_s = 1/f_s$, where f_s = clock frequency (Hz)
V_{OUT} = Device specific output voltage (e.g. 6.8 V for NCV887801) (V)
V_{ref} = OTA internal voltage reference = 1.2 V
R_0 = OTA output resistance = 3 MΩ
S_a = IC slope compensation (e.g. 53 mV/μs for NCV887801)
g_m = OTA transconductance = 1.2 mS
D = Controller duty ratio
D' = 1 − D

Necessary equations for describing the modulator gain (V_{ctrl}−to−V_{out} gain) $H_{ctrl\_output(f)}$ are described in Table 1.

Table 1. BOOST CCM TRANSFER FUNCTION EXPRESSIONS

Duty ratio (D)	$\frac{\left(2R_{OUT}V_dV_{IN} - \left[R_{sw\_eq} + R_{OUT}\left(\frac{V_{IN}}{V_{OUT}} - 2\right)\right]V_{OUT}^2 - V_{OUT}\sqrt{R_{OUT}\left(\begin{matrix}R_{OUT}V_{IN}^2 + 2R_{sw\_eq}V_{IN}V_{OUT} - 4V_dR_{sw\_eq}V_{IN} \\ -4R_{sw\_eq}V_{OUT}^2 - 4r_LV_dV_{IN} - 4r_LV_{OUT}^2\end{matrix}\right) + R_{sw\_eq}^2V_{OUT}^2}\right)}{2R_{OUT}(V_{OUT}^2 + V_dV_{IN})}$
V_{out}/V_{in} Power Supply DC Conversion Ratio (M)	$\frac{1}{1-D}\left[1 - \frac{(1-D)V_d}{V_{OUT}}\right]\left[\frac{1}{1 + \frac{1}{(1-D)^2\left(\frac{r_L + DR_{sw\_eq}}{R_{OUT}}\right)}}\right]$
Average Inductor Current (I_{lave})	$\frac{P_{OUT}}{V_{IN}\eta}$
Inductor On−slope (S_n)	$\frac{V_{IN} - I_{Lave}\left(r_L + R_{sw\_eq}\right)}{L}R_i$
Compensation Ramp (m_c)	$1 + \frac{S_a}{S_n}$
C_{out} ESR Zero (ω_{z1})	$\frac{1}{r_{CF}C_{OUT}}$
Right−half−plane Zero (ω_{z2})	$\frac{(1-D)^2}{L}\left(R_{OUT} - \frac{r_{CF}R_{OUT}}{r_{CF} + R_{OUT}}\right) - \frac{r_L}{L}$
Low Frequency Modulator Pole (ω_{p1})	$\frac{\frac{2}{R_{OUT}} + \frac{T_s}{LM^3}m_c}{C_{OUT}}$
Sampling Double Pole (ω_n)	$\frac{\pi}{T_s}$
Sampling Quality Coefficient (Q_p)	$\frac{1}{\pi(m_c(1-D) - 0.5)}$
F_m	$\frac{1}{2M + \frac{R_{OUT}T_s}{LM^2}\left(\frac{1}{2} + \frac{S_a}{S_n}\right)}$
H_d	$\frac{\eta R_{OUT}}{R_i}$
Control−output Transfer Function ($H_{ctrl\_output(f)}$)	$F_mH_d\frac{\left(1 + j\frac{2\pi f}{\omega_{z1}}\right)}{\left(1 + j\frac{2\pi f}{\omega_{p1}}\right)}\frac{\left(1 - j\frac{2\pi f}{\omega_{z2}}\right)}{\left(1 + j\frac{2\pi f}{\omega_nQ_p} + \left(j\frac{2\pi f}{\omega_n}\right)^2\right)}$

Once the desired cross−over frequency (f_c) gain adjustment and necessary phase boost are determined from the $H_{ctrl\_output}(f)$ gain and phase plots, the Table 2 equations may be used. It should be noted that minor compensation component value adjustments may become necessary when $R_2 \le \sim 10 \cdot R_{esd}$ as a result of approximations for determining components R_2, C_1, C_2.

Table 2. OTA COMPENSATION TRANSFER FUNCTION AND COMPENSATION VALUES

Desired OTA Gain at Cross−over Frequency f_c (G)	$10^{\frac{desired\_G_{fc\_gain\_db}}{20}}$
Desired Phase Boost at Cross−over Frequency f_c (boost)	$\left(\theta_{margin} - \arg\left(H_{ctrl\_output}(fc)\right)\frac{180^\circ}{\pi} - 90^\circ\right)\frac{\pi}{180^\circ}$
Select OTA Compensation Zero to Coincide with Modulator Pole at f_{p1} (f_z)	$\frac{\omega_{p1e}}{2\pi}$
Resulting OTA High Frequency Pole Placement (f_p)	$\frac{f_z f_c + f_c^{\,2}\tan(boost)}{f_c - f_z\tan(boost)}$
Compensation Resistor (R_2)	$\frac{f_p G}{f_p - f_z}\,\frac{V_{OUT}}{1.2\,g_m}\,\frac{\sqrt{1+\left(\frac{f_c}{f_p}\right)^2}}{\sqrt{1+\left(\frac{f_z}{f_p}\right)}}$
Compensation Capacitor (C_1)	$\frac{1}{2\pi f_z R_2}$
Compensation Capacitor (C_2)	$\frac{1}{2\pi f_p G}\,\frac{1.2\,g_m}{V_{OUT}}$
OTA DC Gain (G_{0_OTA})	$\frac{V_{ref}}{V_{OUT}} g_m R_0$
Low Frequency Zero (ω_{z1e})	$\frac{1}{2}\,\frac{\left(R_2 + R_{esd}\right)}{R_2 R_{esd} C_2}\left[1 - \sqrt{1 - 4\frac{R_2 R_{esd} C_2}{\left(R_2 + R_{esd}\right)^2 C_1}}\right]$
High Frequency Zero (ω_{z2e})	$\frac{1}{2}\,\frac{\left(R_2 + R_{esd}\right)}{R_2 R_{esd} C_2}\left[1 + \sqrt{1 - 4\frac{R_2 R_{esd} C_2}{\left(R_2 + R_{esd}\right)^2 C_1}}\right]$
Low Frequency Pole (ω_{p1e})	$\frac{1}{2}\,\frac{\left(R_0 + R_2 + R_{esd}\right)}{R_2\left(R_0 + R_{esd}\right) C_2}\left[1 - \sqrt{1 - 4\frac{R_2\left(R_0 + R_{esd}\right) C_2}{\left(R_0 + R_2 + R_{esd}\right)^2 C_1}}\right]$
High Frequency Pole (ω_{p2e})	$\frac{1}{2}\,\frac{\left(R_0 + R_2 + R_{esd}\right)}{R_2\left(R_0 + R_{esd}\right) C_2}\left[1 + \sqrt{1 - 4\frac{R_2\left(R_0 + R_{esd}\right) C_2}{\left(R_0 + R_2 + R_{esd}\right)^2 C_1}}\right]$
OTA Transfer Function ($G_{OTA}(f)$)	$-G_{0\_OTA}\frac{1 + j\frac{2\pi f}{\omega_{z1e}}}{1 + j\frac{2\pi f}{\omega_{p1e}}}\,\frac{1 + j\frac{2\pi f}{\omega_{z2e}}}{1 + j\frac{2\pi f}{\omega_{p2e}}}$

The open−loop−response in closed−loop form to verify the gain/phase margins may be obtained from the following expressions.

$$T(f) = G_{OTA}(f) H_{ctrl\_output}(f)$$

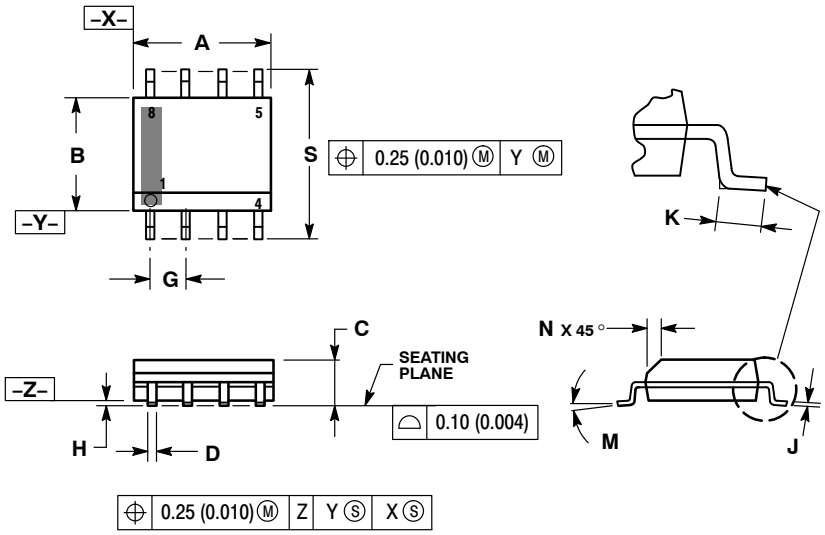
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

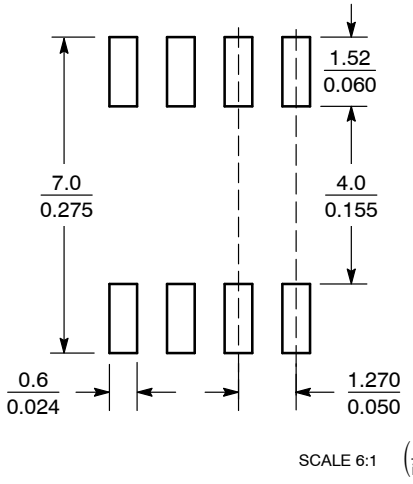
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

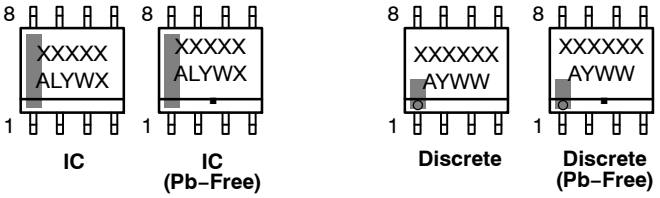
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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