# 2Pai Semi

# Enhanced ESD, 3.0 kV rms/6.0 kV rms 150Kbps Triple-Channel Digital Isolators

Data Sheet **π130U/π131U**

## FEATURES

**Ultra low power consumption (150Kbps):**
**0.62mA/Channel**
**High data rate:** **π13xAxx: 600Mbps**
**π13xExx: 200Mbps**
**π13xMxx: 10Mbps**
**π13xUxx: 150kbps**
**High common-mode transient immunity: 150 kV/μs typical**
**High robustness to radiated and conducted noise**
**Isolation voltages:**
**π13xx3x: AC 3000Vrms**
**π13xx6x: AC 6000Vrms**
**High ESD rating:**
**ESDA/JEDEC JS-001-2017**
**Human body model (HBM) ±8kV, all pins**
**Safety and regulatory approvals (Pending):**
**UL certificate number: E494497**
**3000Vrms/6000Vrms for 1 minute per UL 1577**
**CSA Component Acceptance Notice 5A**
**VDE certificate number: 40047929**
**DIN V VDE V 0884-10 (VDE V 0884-10):2006-12**
**$V_{IORM}$ = 707V peak/1200V peak**
**CQC certification per GB4943.1-2011**
**3 V to 5.5 V level translation**
**AEC-Q100 qualification**
**Wide temperature range: -40°C to 125°C**
**16-lead, RoHS-compliant, SOIC_N, SOIC_W and SSOP package**

## APPLICATIONS

**General-purpose multichannel isolation**
**Industrial field bus isolation**

## GENERAL DESCRIPTION

The π1xxxxx is a 2PaiSemi digital isolators product family that includes over hundreds of digital isolator products. By using maturated standard semiconductor CMOS technology and 2PaiSEMI ***i*Divider** technology, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators.

Intelligent voltage divider technology (***i*Divider** technology) is a new generation digital isolator technology invented by 2PaiSEMI. It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

The π1xxxxx isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 6.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide). The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The fail-safe state is available in which the outputs transition to a preset state when the input power supply is not applied.

## FUNCTIONAL BLOCK DIAGRAMS

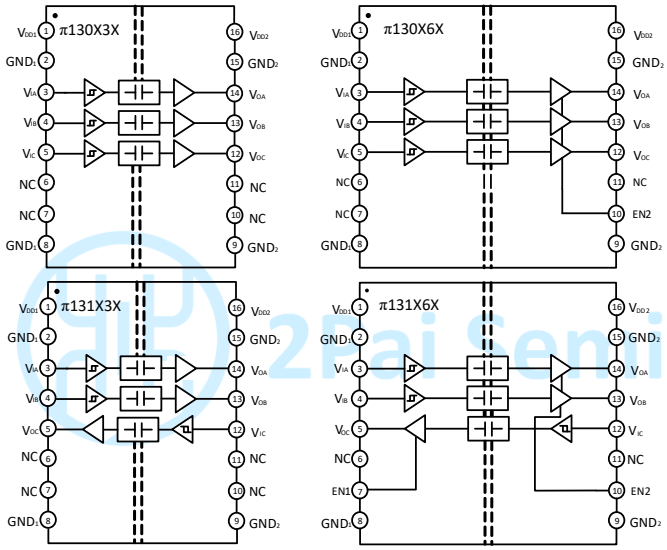



*Figure1. π130xxx/π131xxx functional Block Diagram*

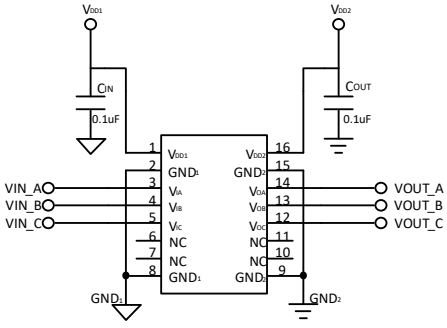



*Figure2. π130x3x Typical Application Circuit*





Room 308−309, No.22, Boxia Road, Pudong New District, Shanghai, 201203, China
021-50850681

http://www.rpsemi.com/

# PIN CONFIGURATIONS AND FUNCTIONS

**π130Uxx Pin Function Descriptions**

| Pin No. | Name | Description |
|---|---|---|
| 1 | $V_{DD1}$ | Supply Voltage for Isolator Side 1. |
| 2 | $GND_1$ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 3 | $V_{IA}$ | Logic Input A. |
| 4 | $V_{IB}$ | Logic Input B. |
| 5 | $V_{IC}$ | Logic Input C. |
| 6 | NC | No connect. |
| 7 | NC | No connect. |
| 8 | $GND_1$ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 9 | $GND_2$ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 10 | NC/EN2 | No connect for π130U3X.<br>Output enable for π130U6X. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low. |
| 11 | NC | No connect. |
| 12 | $V_{OC}$ | Logic Output C. |
| 13 | $V_{OB}$ | Logic Output B. |
| 14 | $V_{OA}$ | Logic Output A. |
| 15 | $GND_2$ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 16 | $V_{DD2}$ | Supply Voltage for Isolator Side 2. |

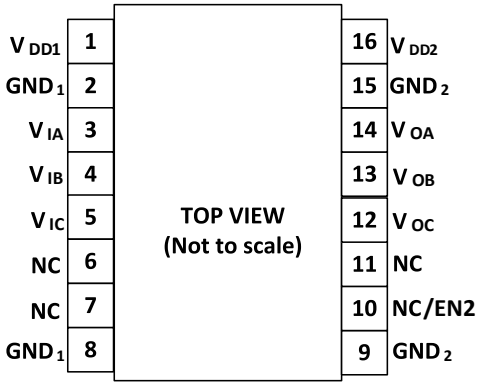



*Figure3 π130Uxx Pin Configuration*

**π131Uxx Pin Function Descriptions**

| Pin No. | Name | Description |
|---|---|---|
| 1 | $V_{DD1}$ | Supply Voltage for Isolator Side 1. |
| 2 | $GND_1$ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 3 | $V_{IA}$ | Logic Input A. |
| 4 | $V_{IB}$ | Logic Input B. |
| 5 | $V_{OC}$ | Logic Output C. |
| 6 | NC | No connect. |
| 7 | NC | No connect for π131U3X.<br>Output enable for π131U6X. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low. |
| 8 | $GND_1$ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 9 | $GND_2$ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 10 | NC | No connect for π131U3X.<br>Output enable for π131U6X. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low. |
| 11 | NC | No connect. |
| 12 | $V_{IC}$ | Logic Input C. |
| 13 | $V_{OB}$ | Logic Output B. |
| 14 | $V_{OA}$ | Logic Output A. |
| 15 | $GND_2$ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 16 | $V_{DD2}$ | Supply Voltage for Isolator Side 2. |

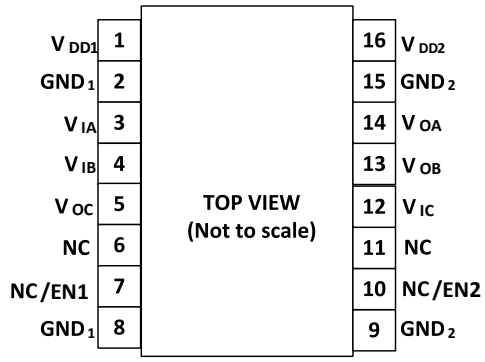



*Figure4. π131Uxx Pin Configuration*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 1. Absolute Maximum Ratings[4]**

| Parameter | Rating |
|---|---|
| Supply Voltages ($V_{DD1}$-$GND_1$, $V_{DD2}$-$GND_2$) | −0.5 V to +7.0 V |
| Input Voltages ($V_{IA}$, $V_{IB}$)[1] | −0.5 V to $V_{DDx}$ + 0.5 V |
| Output Voltages ($V_{OA}$, $V_{OB}$)[1] | −0.5 V to $V_{DDx}$ + 0.5 V |
| Average Output Current per Pin[2] Side 1 Output Current ($I_{O1}$) | −10 mA to +10 mA |
| Average Output Current per Pin[2] Side 2 Output Current ($I_{O2}$) | −10 mA to +10 mA |
| Common-Mode Transients Immunity[3] | −150 kV/µs to +150 kV/µs |
| Storage Temperature ($T_{ST}$) Range | −65°C to +150°C |
| Ambient Operating Temperature ($T_A$) Range | −40°C to +125°C |

Notes:
[1] $V_{DDx}$ is the side voltage power supply $V_{DD}$, where x = 1 or 2.
[2] See Figure 6 for the maximum rated current values for various temperatures.
[3] See Figure 16 for Common-mode transient immunity (CMTI) measurement.
[4] Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

# RECOMMENDED OPERATING CONDITIONS

**Table 2. Recommended Operating Conditions**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DDx}$ [1] | 3 | | 5.5 | V |
| High Level Input Signal Voltage | $V_{IH}$ | 0.7*$V_{DDx}$[1] | | $V_{DDx}$[1] | V |
| Low Level Input Signal Voltage | $V_{IL}$ | 0 | | 0.3*$V_{DDx}$[1] | V |
| High Level Output Current | $I_{OH}$ | -6 | | | mA |
| Low Level Output Current | $I_{OL}$ | | | 6 | mA |
| Maximum Data Rate | | 0 | | 150 | Kbps |
| Junction Temperature | $T_J$ | -40 | | 150 | °C |
| Ambient Operating Temperature | $T_A$ | -40 | | 125 | °C |

Notes:
[1] $V_{DDx}$ is the side voltage power supply $V_{DD}$, where x = 1 or 2.

# Truth Tables

**Table 3. π130U3x/π131U3x Truth Table**

| $V_{Ix}$ Input[1] | $V_{DDI}$ State[1] | $V_{DDO}$ State[1] | Default Low $V_{Ox}$ Output[1] | Default High $V_{Ox}$ Output[1] | Test Conditions /Comments |
|---|---|---|---|---|---|
| Low | Powered[2] | Powered[2] | Low | Low | Normal operation |
| High | Powered[2] | Powered[2] | High | High | Normal operation |
| Open | Powered[2] | Powered[2] | Low | High | Default output |
| Don't Care[4] | Unpowered[3] | Powered[2] | Low | High | Default output[5] |
| Don't Care[4] | Powered[2] | Unpowered[3] | High Impedance | High Impedance | |

Notes:
[1] $V_{Ix}$/$V_{Ox}$ are the input/output signals of a given channel (A or B). $V_{DDI}$/$V_{DDO}$ are the supply voltages on the input/output signal sides of this given channel.

[2] Powered means $V_{DDx}$≥ 2.9 V
[3] Unpowered means $V_{DDx}$ < 2.3V
[4] Input signal ($V_{Ix}$) must be in a low state to avoid powering the given $V_{DDI}$[1] through its ESD protection circuitry.
[5] If the $V_{DDI}$ goes into unpowered status, the channel outputs the default logic signal after around 1us. If the $V_{DDI}$ goes into powered status, the channel outputs the input status logic signal after around 3us.

**Table 4. π130U6x/π131U6x Truth Table**

| $V_{Ix}$ Input[1] | EN1/2 State | $V_{DDI}$ State[1] | $V_{DDO}$ State[1] | Default Low $V_{Ox}$ Output[1] | Default High $V_{Ox}$ Output[1] | Test Conditions /Comments |
|---|---|---|---|---|---|---|
| Low | High or NC | Powered[2] | Powered[2] | Low | Low | Normal operation |
| High | High or NC | Powered[2] | Powered[2] | High | High | Normal operation |
| Don't Care[4] | L | Powered[2] | Powered[2] | High Impedance | High Impedance | Disabled |
| Open | High or NC | Powered[2] | Powered[2] | Low | High | Default output[5] |
| Don't Care[4] | High or NC | Unpowered[3] | Powered[2] | Low | High | Default output[5] |
| Don't Care[4] | L | Unpowered[3] | Powered[2] | High Impedance | High Impedance | |
| Don't Care[4] | Don't Care[4] | Powered[2] | Unpowered[3] | High Impedance | High Impedance | |

Notes:
[1] $V_{Ix}$/$V_{Ox}$ are the input/output signals of a given channel (A or B). $V_{DDI}$/$V_{DDO}$ are the supply voltages on the input/output signal sides of this given channel.
[2] Powered means $V_{DDx}$≥ 2.9 V
[3] Unpowered means $V_{DDx}$ < 2.3V
[4] Input signal ($V_{Ix}$) must be in a low state to avoid powering the given $V_{DDI}$[1] through its ESD protection circuitry.
[5] If the $V_{DDI}$ goes into unpowered status, the channel outputs the default logic signal after around 1us. If the $V_{DDI}$ goes into powered status, the channel outputs the input status logic signal after around 3us.

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

**Table 5. Switching Specifications**

$V_{DD1}$ - $V_{GND1}$ = $V_{DD2}$ - $V_{GND2}$ = 3.3$V_{DC}$±10% or 5$V_{DC}$±10%, $T_A$=25°C, unless otherwise noted.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| Minimum Pulse Width | PW | | | 6.5 | us | Within pulse width distortion (PWD) limit |
| Maximum Data Rate | | 150 | | | Kbps | Within PWD limit |
| Propagation Delay Time[1,4] | $t_{pHL}$, $t_{pLH}$ | | 3.0 | 4.5 | us | The different time between 50% input signal to 50% output signal 50% @ 5$V_{DC}$ supply |
| | | | 3.2 | 4.8 | us | @ 3.3$V_{DC}$ supply |
| Pulse Width Distortion[4] | PWD | 0 | 0.02 | 0.2 | us | The max different time between $t_{pHL}$ and $t_{pLH}$@ 5$V_{DC}$ supply. And The value is \| $t_{pHL}$ - $t_{pLH}$ \| |
| | | 0 | 0.02 | 0.2 | us | @ 3.3$V_{DC}$ supply |
| Part to Part Propagation Delay Skew[4] | $t_{PSK}$ | | | 0.3 | us | The max different propagation delay time between any two devices at the same temperature, load and voltage @ 5$V_{DC}$ supply |
| | | | | 0.3 | us | @ 3.3$V_{DC}$ supply |
| Channel to Channel Propagation Delay Skew[4] | $t_{CSK}$ | | 0 | 0.2 | us | The max amount propagation delay time differs between any two output channels in the single device @ 5$V_{DC}$ supply. |
| | | | 0 | 0.2 | us | @ 3.3$V_{DC}$ supply |
| Output Signal Rise/Fall Time[4] | $t_r$/$t_f$ | | 1.5 | | ns | 10% to 90% signal terminated 50Ω， See figure13. |
| Common-Mode Transient Immunity[3] | CMTI | 100 | 150 | | kV/μs | $V_{IN}$ = $V_{DDx}$[2] or 0V, $V_{CM}$ = 1000 V |
| ESD（HBM - Human body model） | ESD | | ±8 | | kV | All pins |

Notes:
[1] $t_{pLH}$ = low-to-high propagation delay time, $t_{pHL}$ = high-to-low propagation delay time. See figure 14.
[2] $V_{DDx}$ is the side voltage power supply $V_{DD}$, where x = 1 or 2.
[3] See Figure 16 for Common-mode transient immunity (CMTI) measurement.
[4] Output Signal Terminated 50Ω.

### Table 6. DC Specifications

$V_{DD1}$ - $V_{GND1}$ = $V_{DD2}$ - $V_{GND2}$ = 3.3$V_{DC}$±10% or 5$V_{DC}$±10%, $T_A$=25°C, unless otherwise noted.

| | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| Rising Input Signal Voltage Threshold | $V_{IT+}$ | | 0.6*$V_{DDx}$[1] | 0.7*$V_{DDx}$[1] | V | |
| Falling Input Signal Voltage Threshold | $V_{IT-}$ | 0.3* $V_{DDX}$[1] | 0.4* $V_{DDX}$[1] | | V | |
| High Level Output Voltage | $V_{OH}$ [1] | $V_{DDx}$ – 0.1 | $V_{DDx}$ | | V | −20 µA output current |
| | | $V_{DDx}$ – 0.2 | $V_{DDx}$ – 0.1 | | V | −2 mA output current |
| Low Level Output Voltage | $V_{OL}$ | | 0 | 0.1 | V | 20 µA output current |
| | | | 0.1 | 0.2 | V | 2 mA output current |
| Input Current per Signal Channel | $I_{IN}$ | −10 | 0.5 | 10 | µA | 0 V ⩽ Signal voltage ⩽ $V_{DDx}$[1] |
| $V_{DDx}$[1] Undervoltage Rising Threshold | $V_{DDxUV+}$ | 2.45 | 2.65 | 2.9 | V | |
| $V_{DDx}$[1] Undervoltage Falling Threshold | $V_{DDxUV-}$ | 2.3 | 2.5 | 2.75 | V | |
| $V_{DDx}$[1] Hysteresis | $V_{DDxUVH}$ | | 0.15 | | V | |

Notes:
[1] $V_{DDx}$ is the side voltage power supply $V_{DD}$, where x = 1 or 2.



### Table 7. Quiescent Supply Current

$V_{DD1}$ - $V_{GND1}$ = $V_{DD2}$ - $V_{GND2}$ = 3.3$V_{DC}$±10% or 5$V_{DC}$±10%, $T_A$=25°C, $C_L$ = 0 pF, unless otherwise noted.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| π130Uxx Quiescent Supply Current @ 5$V_{DC}$ Supply | $I_{DD1 (Q)}$ | 279 | 349 | 453 | µA | 0V Input signal |
| | $I_{DD2 (Q)}$ | 1123 | 1404 | 1825 | µA | 0V Input signal |
| | $I_{DD1 (Q)}$ | 112 | 140 | 182 | µA | 5V Input signal |
| | $I_{DD2 (Q)}$ | 1205 | 1506 | 1958 | µA | 5V Input signal |
| @ 3.3$V_{DC}$ Supply | $I_{DD1 (Q)}$ | 214 | 268 | 348 | µA | 0V Input signal |
| | $I_{DD2 (Q)}$ | 1101 | 1376 | 1789 | µA | 0V Input signal |
| | $I_{DD1 (Q)}$ | 104 | 130 | 169 | µA | 3.3V Input signal |
| | $I_{DD2 (Q)}$ | 1191 | 1489 | 1936 | µA | 3.3V Input signal |
| π131Uxx Quiescent Supply Current @ 5$V_{DC}$ Supply | $I_{DD1 (Q)}$ | 556 | 695 | 904 | µA | 0V Input signal |
| | $I_{DD2 (Q)}$ | 846 | 1058 | 1375 | µA | 0V Input signal |
| | $I_{DD1 (Q)}$ | 489 | 611 | 794 | µA | 5V Input signal |
| | $I_{DD2 (Q)}$ | 852 | 1065 | 1385 | µA | 5V Input signal |
| @ 3.3$V_{DC}$ Supply | $I_{DD1 (Q)}$ | 506 | 632 | 822 | µA | 0V Input signal |
| | $I_{DD2 (Q)}$ | 810 | 1012 | 1316 | µA | 0V Input signal |
| | $I_{DD1 (Q)}$ | 484 | 605 | 787 | µA | 3.3V Input signal |
| | $I_{DD2 (Q)}$ | 842 | 1053 | 1369 | µA | 3.3V Input signal |

**Table 8. Total Supply Current vs. Data Throughput ($C_L$ = 0 pF)**

$V_{DD1}$ - $V_{GND1}$ = $V_{DD2}$ - $V_{GND2}$ = 3.3$V_{DC}$±10% or 5$V_{DC}$±10%, $T_A$=25°C, $C_L$ = 0 pF, unless otherwise noted.

| Parameter | Symbol | 2 Kbps | | | 50Kbps | | | 150Kbps | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| π130Uxx Supply Current@ 5$V_{DC}$ | $I_{DD1}$ | | 0.24 | 0.36 | | 0.24 | 0.36 | | 0.25 | 0.38 | mA |
| | $I_{DD2}$ | | 1.45 | 2.18 | | 1.47 | 2.21 | | 1.49 | 2.24 | mA |
| @ 3.3$V_{DC}$ | $I_{DD1}$ | | 0.18 | 0.27 | | 0.18 | 0.27 | | 0.18 | 0.27 | mA |
| | $I_{DD2}$ | | 1.41 | 2.12 | | 1.42 | 2.13 | | 1.43 | 2.15 | mA |
| π131Uxx Supply Current@ 5$V_{DC}$ | $I_{DD1}$ | | 0.60 | 0.90 | | 0.61 | 0.92 | | 0.62 | 0.93 | mA |
| | $I_{DD2}$ | | 1.05 | 1.58 | | 1.07 | 1.61 | | 1.09 | 1.64 | mA |
| @ 3.3$V_{DC}$ | $I_{DD1}$ | | 0.55 | 0.83 | | 0.56 | 0.84 | | 0.57 | 0.86 | mA |
| | $I_{DD2}$ | | 1.03 | 1.55 | | 1.05 | 1.58 | | 1.07 | 1.61 | mA |

## INSULATION AND SAFETY RELATED SPECIFICATIONS

**Table 9. Insulation Specifications**

| Parameter | Symbol | Value | | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| | | π13xU3x | π13xU6x | | |
| Rated Dielectric Insulation Voltage | | 3000 | 6000 | V rms | 1-minute duration |
| Minimum External Air Gap (Clearance) | L (CLR) | 4 | 8 | mm min | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L (CRP) | 4 | 8 | mm min | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | 11 | 21 | µm min | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >400 | >400 | V | DIN IEC 112/VDE 0303 Part 1 |
| Material Group | | II | II | | Material Group (DIN VDE 0110, 1/89, Table 1) |



## PACKAGE CHARACTERISTICS

**Table 10. Package Characteristics**

| Parameter | Symbol | Typical Value | | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| | | π13xU3x | π13xU6x | | |
| Resistance (Input to Output)[1] | $R_{I-O}$ | $10^{11}$ | $10^{11}$ | Ω | |
| Capacitance (Input to Output)[1] | $C_{I-O}$ | 0.6 | 0.6 | pF | @1MHz |
| Input Capacitance[2] | $C_I$ | 3 | 3 | pF | @1MHz |
| IC Junction to Ambient Thermal Resistance | $\theta_{JA}$ | 100 | 45 | °C/W | Thermocouple located at center of package underside |

Notes:

[1]The device is considered a 2-terminal device; SOIC-16 Pin 1 - Pin 8(WSOIC-16 Pin 1-Pin8 and SSOP16 Pin 1-Pin8) are shorted together as the one terminal, and SOIC-16 Pin 9- Pin 16(WSOIC-16 Pin 9-Pin16 and SSOP16 Pin 9-Pin16) are shorted together as the other terminal.

[2]Testing from the input signal pin to ground.

## REGULATORY INFORMATION

See Table 11 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

**Table11. Regulatory**

| Regulatory | π13xU3x | π13xU6x |
|---|---|---|
| **UL** | Recognized under UL 1577 | Recognized under UL 1577 |

| | | |
|---|---|---|
| | Component Recognition Program[1]<br>Single Protection, 3000 V rms Isolation Voltage<br>File (E494497) | Component Recognition Program[1]<br>Single Protection, 6000 V rms Isolation Voltage<br>File (pending) |
| **CSA** | Approved under CSA Component Acceptance Notice 5A<br>CSA 60950-1-07+A1+A2 and<br>IEC 60950-1, second edition, +A1+A2:<br>Basic insulation at 500 V rms (707 V peak)<br>Reinforced insulation at 250 V rms<br>(353 V peak)<br>File (pending) | Approved under CSA Component Acceptance Notice 5A<br>CSA 60950-1-07+A1+A2 and<br>IEC 60950-1, second edition, +A1+A2:<br>Basic insulation at 845 V rms (1200 V peak)<br>Reinforced insulation at 422 V rms<br>(600 V peak)<br>File (pending) |
| **VDE** | DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]<br>Basic insulation, $V_{IORM}$ = 707 V peak, $V_{IOSM}$ = 4615 V peak<br>File (40047929) | DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]<br>Basic insulation, $V_{IORM}$ = 1200 V peak, $V_{IOSM}$ = 7000V peak<br>File (pending) |
| **CQC** | Certified under<br>CQC11-471543-2012<br>GB4943.1-2011<br>Basic insulation at 500 V rms (707 V peak) working voltage<br>Reinforced insulation at<br>250 V rms (353 V peak)<br>File (pending) | Certified under<br>CQC11-471543-2012<br>GB4943.1-2011<br>Basic insulation at 845 V rms (1200 V peak) working voltage<br>Reinforced insulation at<br>422 V rms (600 V peak)<br>File (pending) |

Notes:

[1] In accordance with UL 1577, each π130U3X/π131U3X is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec; each π130U6X/π131U6X is proof tested by applying an isulation test voltage ≥ 7200 V rms for 1 sec

[2] In accordance with DIN V VDE V 0884-10, each π130U3X/π131U3X is proof tested by applying an insulation test voltage ≥ 1326 V peak for 1 sec (partial discharge detection limit = 5 pC); each π130U6X/π131U6X is proof tested by ≥ 2250 V peak for 1 sec. The * marking branded on the component designates DIN V VDE V 0884-10 approval.



## DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

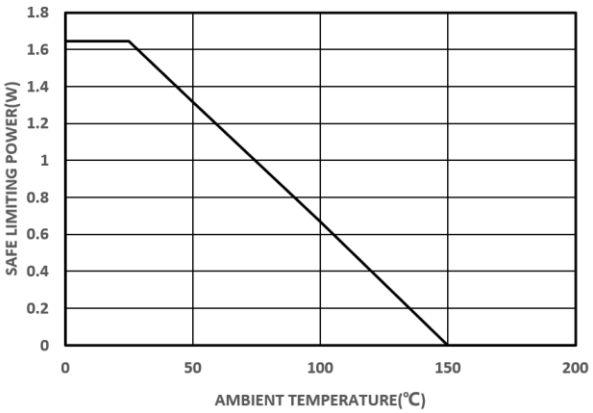
These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The * marking on packages denotes DIN V VDE V 0884-10 approval.

**Table 12. VDE Insulation Characteristics**

| Description | Test Conditions/Comments | Symbol | Characteristic | | Unit |
|---|---|---|---|---|---|
| | | | π13xU3x | π13xU6x | |
| Installation Classification per DIN VDE 0110 | | | | | |
| For Rated Mains Voltage ⩽ 150 V rms | | | I to IV | I to IV | |
| For Rated Mains Voltage ≤ 300 V rms | | | I to III | I to III | |
| For Rated Mains Voltage ≤ 400 V rms | | | I to III | I to III | |
| Climatic Classification | | | 40/105/21 | 40/105/21 | |
| Pollution Degree per DIN VDE 0110, Table 1 | | | 2 | 2 | |
| Maximum Working Insulation Voltage | | $V_{IORM}$ | 707 | 1200 | V peak |
| Input to Output Test Voltage, Method B1 | $V_{IORM}$ × 1.875 = $V_{pd\ (m)}$, 100% production test, tini = $t_m$ = 1 sec, partial discharge < 5 pC | $V_{pd\ (m)}$ | 1326 | 2250 | V peak |
| Input to Output Test Voltage, Method A | | | | | |
| After Environmental Tests Subgroup 1 | $V_{IORM}$ × 1.5 = $V_{pd\ (m)}$, $t_{ini}$ = 60 sec, $t_m$ = 10 sec, partial discharge < 5 pC | $V_{pd\ (m)}$ | 1061 | 1800 | V peak |

| | | | | | |
|---|---|---|---|---|---|
| After Input and/or Safety Test Subgroup 2 and Subgroup 3 | $V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini}$ = 60 sec, $t_m$ = 10 sec, partial discharge < 5 pC | | 849 | 1440 | V peak |
| Highest Allowable Overvoltage | | $V_{IOTM}$ | 4200 | 8500 | V peak |
| Surge Isolation Voltage Basic | Basic insulation, 1.2 µs rise time, 50 µs, 50% fall time | $V_{IOSM}$ | 4615 | 7000 | V peak |
| Surge Isolation Voltage Reinforced | Reinforced insulation, 1.2 µs rise time, 50 µs, 50% fall time | $V_{IOSM}$ | | | V peak |
| Safety Limiting Values | Maximum value allowed in the event of a failure (see Figure 6) | | | | |
| Maximum Junction Temperature | | $T_S$ | 150 | 150 | °C |
| Total Power Dissipation at 25°C | | $P_S$ | 1.56 | 2.78 | W |
| Insulation Resistance at $T_S$ | $V_{IO}$ = 800 V | $R_S$ | >$10^9$ | >$10^9$ | Ω |

**π13xU3x**




**π13xU6x**

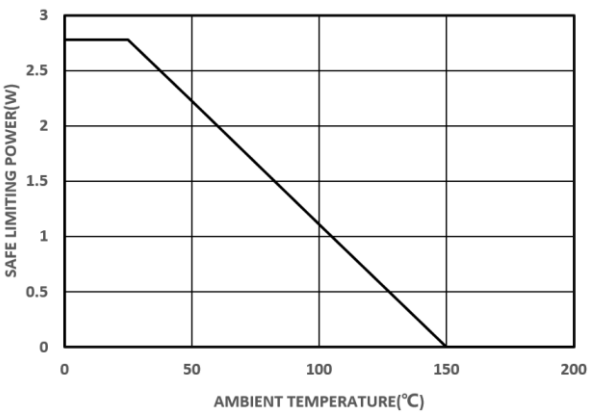



*Figure6. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per VDE*

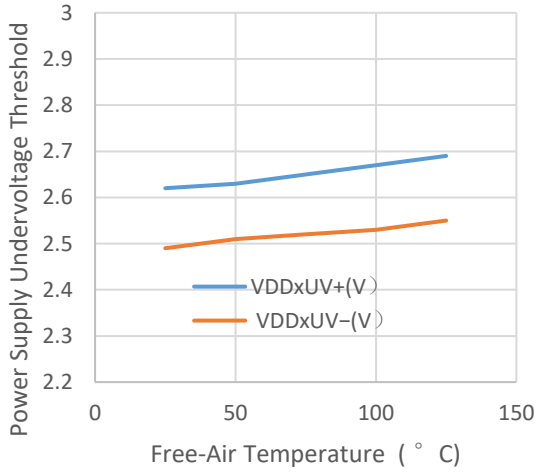



*Figure7. UVLO vs. Free-Air Temperature*

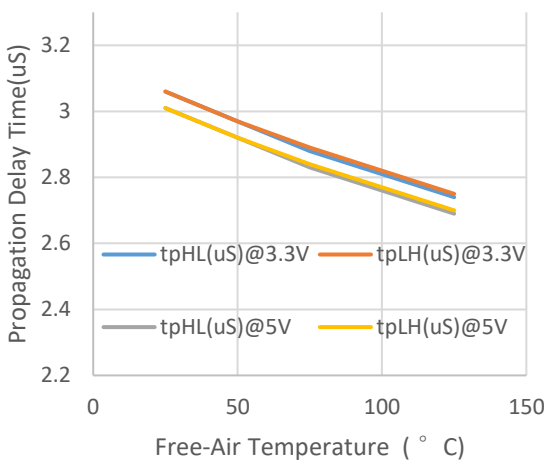



*Figure8. Propagation Delay Time vs. Free-Air Temperature*

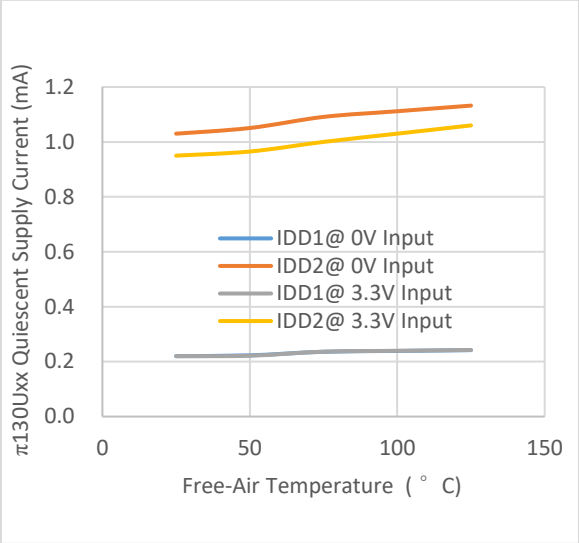



*Figure9 π130Uxx Quiescent Supply Current with 3.3V Supply vs.Free-Air Temperature*

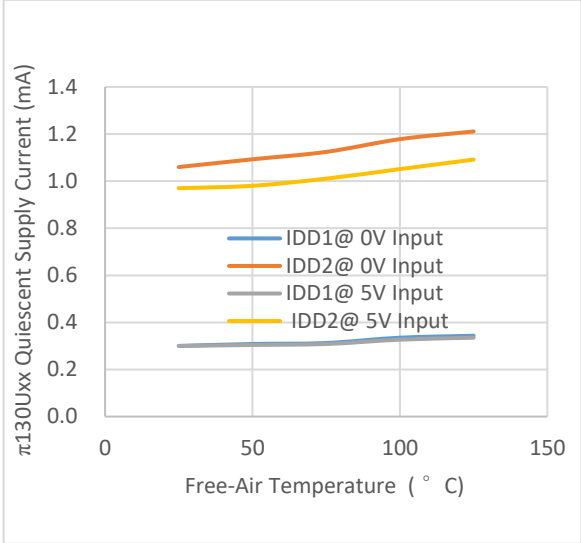



*Figure10 π130Uxx Quiescent Supply Current with 5V Supply vs. Free-Air Temperature*

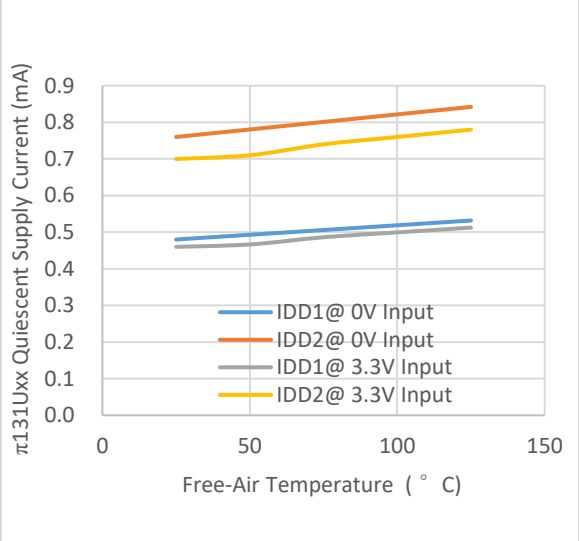



*Figure 11 π131Uxx Quiescent Supply Current with 3.3V Supply vs.Free-Air Temperature*

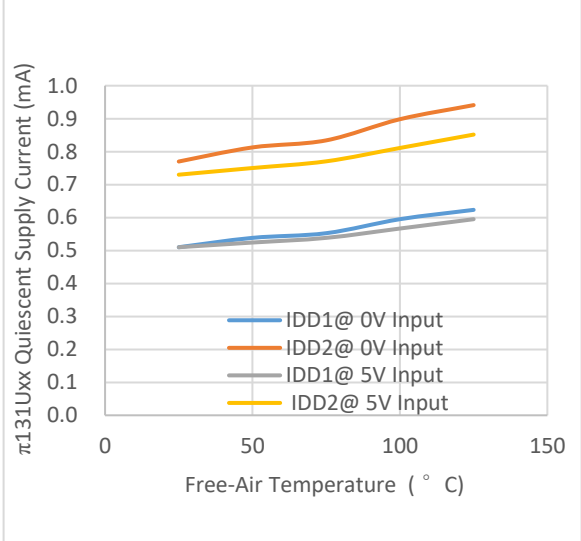



*Figure 12 π131Uxx Quiescent Supply Current with 5V Supply vs.Free-Air Temperature*

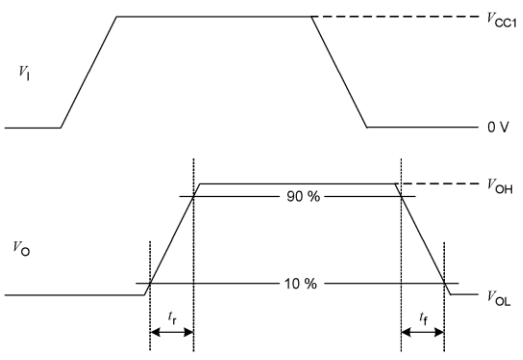



*Figure13. Transition time waveform measurement*

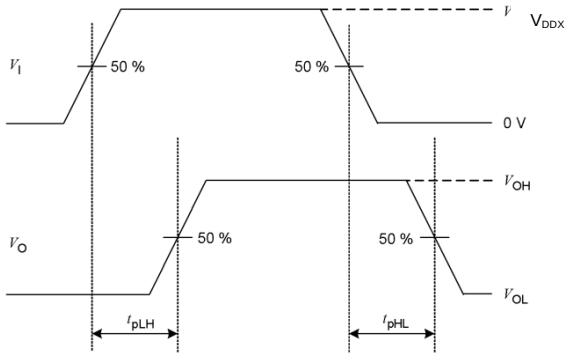



*Figure14. Propagation delay time waveform measurement*

# APPLICATIONS INFORMATION

## OVERVIEW

The π1xxxxx are 2PaiSemi digital isolators product family based on 2PaiSEMI unique ***i*Divider** technology. Intelligent voltage **Divider** technology (***i*Divider** technology) is a new generation digital isolator technology invented by 2PaiSEMI. It uses the principle of capacitor voltage divider to transmit signal directly cross the isolator capacitor without signal modulation and demodulation. Compare to the traditional Opto-couple technology, icoupler technology, OOK technology, ***i*Divider** is a more essential and concise isolation signal transmit technology which leads to greatly simplification on circuit design and therefore significantly improves device performance, such as lower power consumption, faster speed, enhanced anti-interference ability, lower noise.

By using maturated standard semiconductor CMOS technology and the innovative ***i*Divider** design, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators. The π1xxxxx isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 6.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide).

The π130Uxx/π131Uxx are the outstanding 150Kbps Triple-channel digital isolators with the enhanced ESD capability. the devices transmit data across an isolation barrier by layers of silicon dioxide isolation.

The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, offering voltage translation of 3.3 V, and 5 V logic.

The π130Uxx/π131Uxx have very low propagation delay and high speed. The input/output design techniques allow logic and supply voltages over a wide range from 3.0 V to 5.5 V, offering voltage translation of 3.3 V and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference.

See the Ordering Guide for the model numbers that have the fail-safe output state of low or high.

## PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between $V_{DD1}$ and $GND_1$ and between $V_{DD2}$ and $GND_2$. The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value is between 0.1 µF and 10 µF. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

Avoid reducing the isolation capability, Keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To reduce the rise time degradation, keep the length of input/output signal traces as short as possible, and route low inductance loop for the signal path and It's return path.

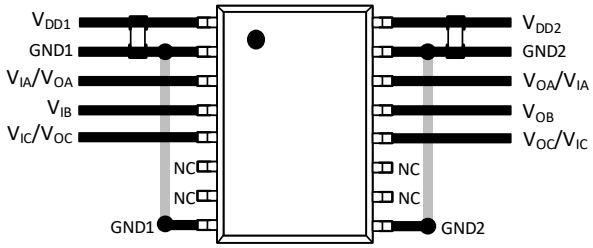



*Figure15.Recommended Printed Circuit Board Layout*

## CMTI MEASUREMENT

To measure the Common-Mode Transient Immunity (CMTI) of π1xxxxx isolator under specified common-mode pulse magnitude ($V_{CM}$) and specified slew rate of the common-mode pulse ($dV_{CM}/dt$) and other specified test or ambient conditions, The common-mode pulse generator ($G_1$) will be capable of providing fast rising and falling pulses of specified magnitude and duration of the common-mode pulse ($V_{CM}$) and the maximum common-mode slew rates ($dV_{CM}/dt$) can be applied to π1xxxxx isolator coupler under measurement. The common-mode pulse is applied between one side ground GND1 and the other side ground GND2 of π1xxxxx isolator and shall be capable of providing positive transients as well as negative transients.

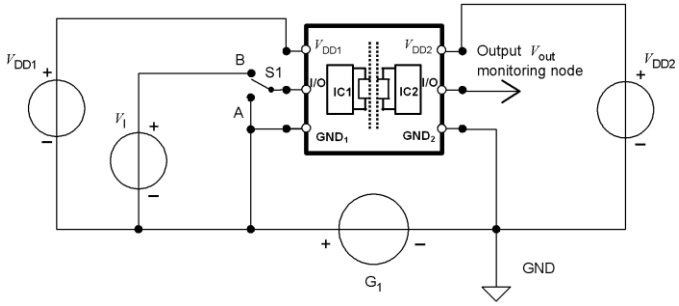



*Figure16 Common-mode transient immunity (CMTI) measurement*

# OUTLINE DIMENSIONS

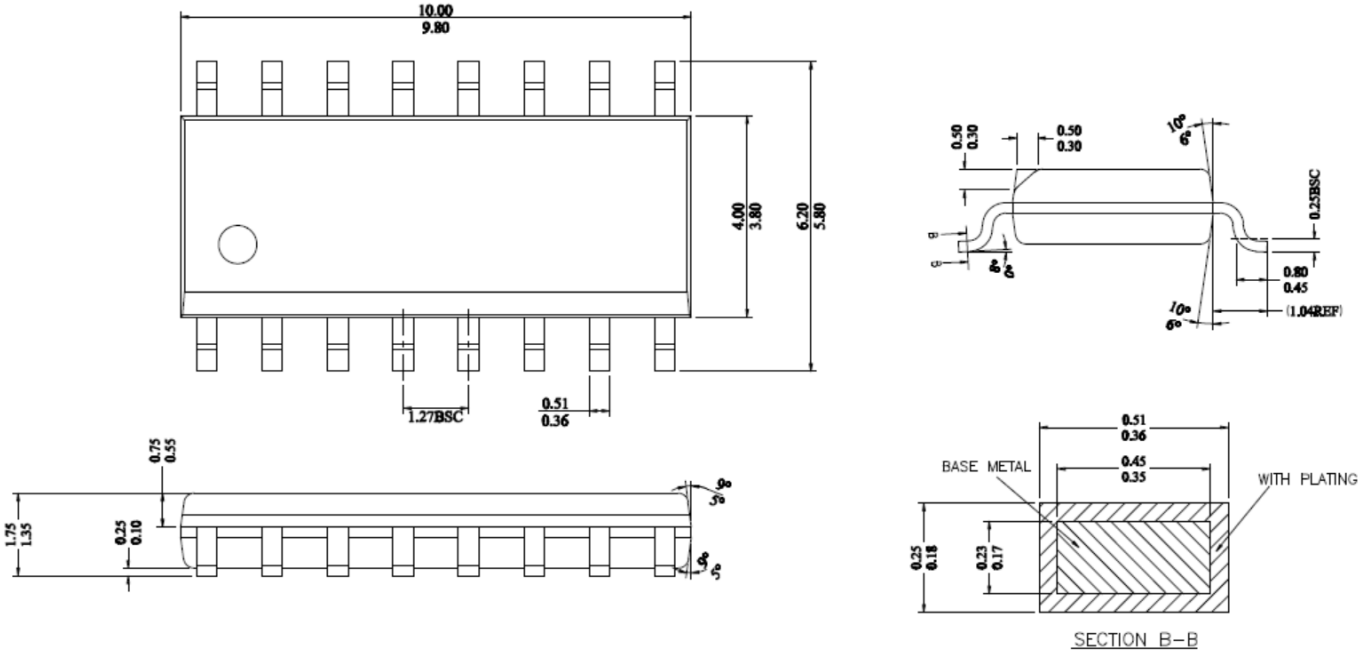



*Figure17. 16-Lead Standard Small Outline Package [16-Lead SOIC_N]*

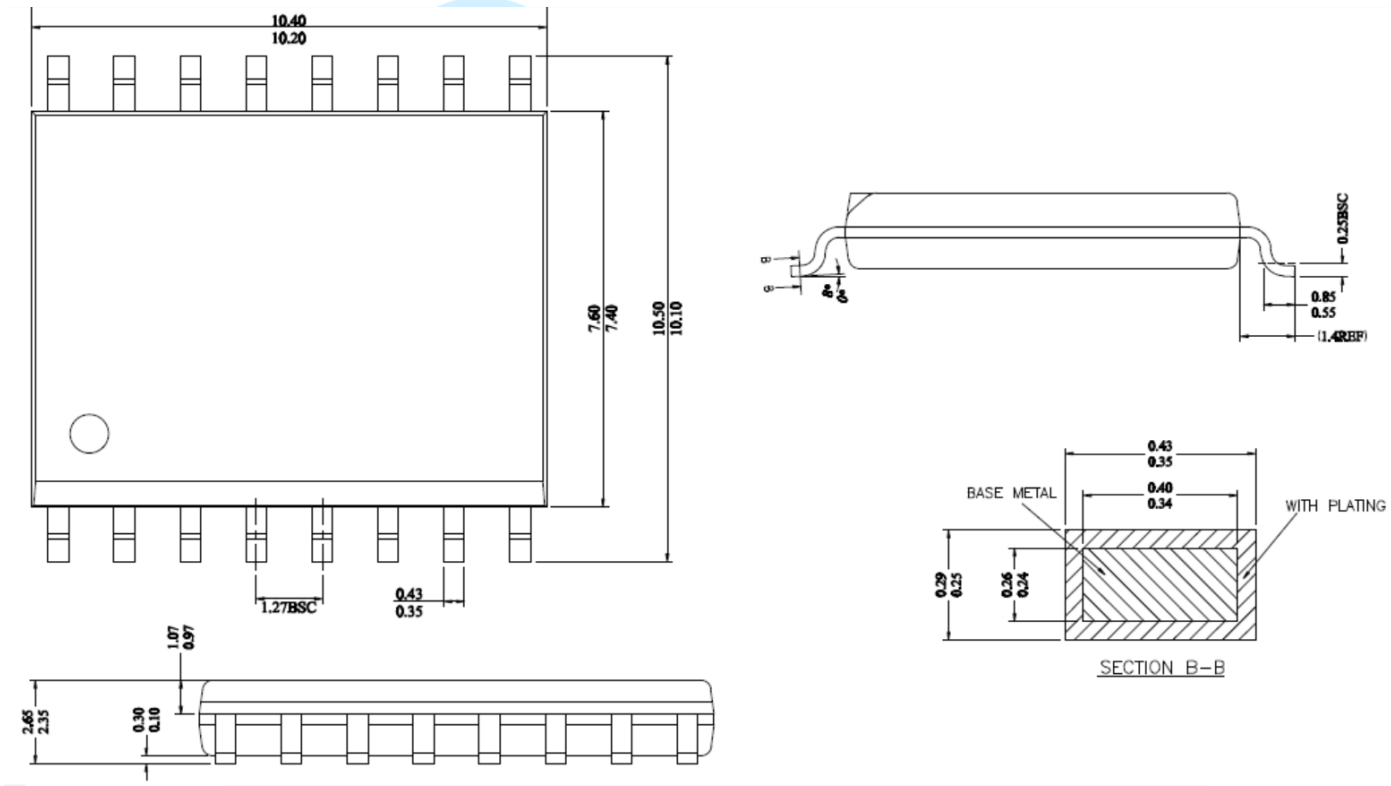
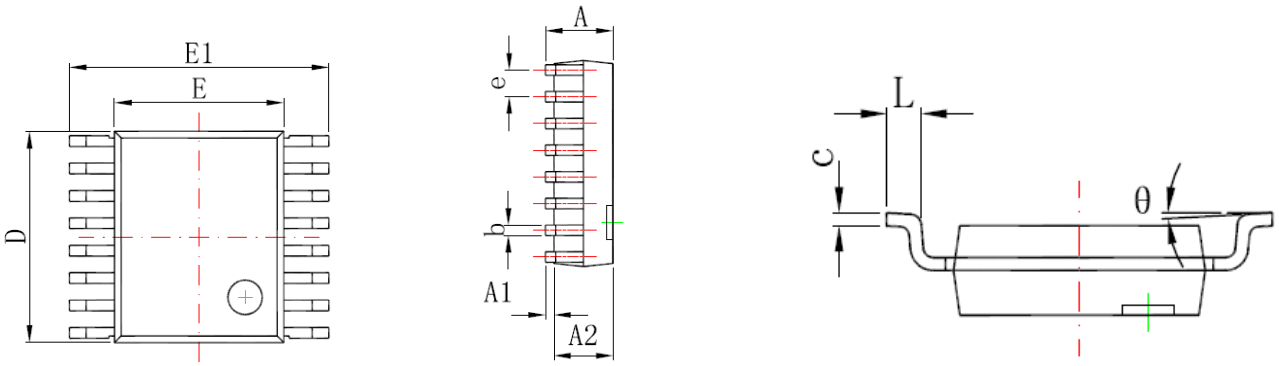



*Figure18. 16-Lead Wide Body Outline Package [16-Lead SOIC_W]*

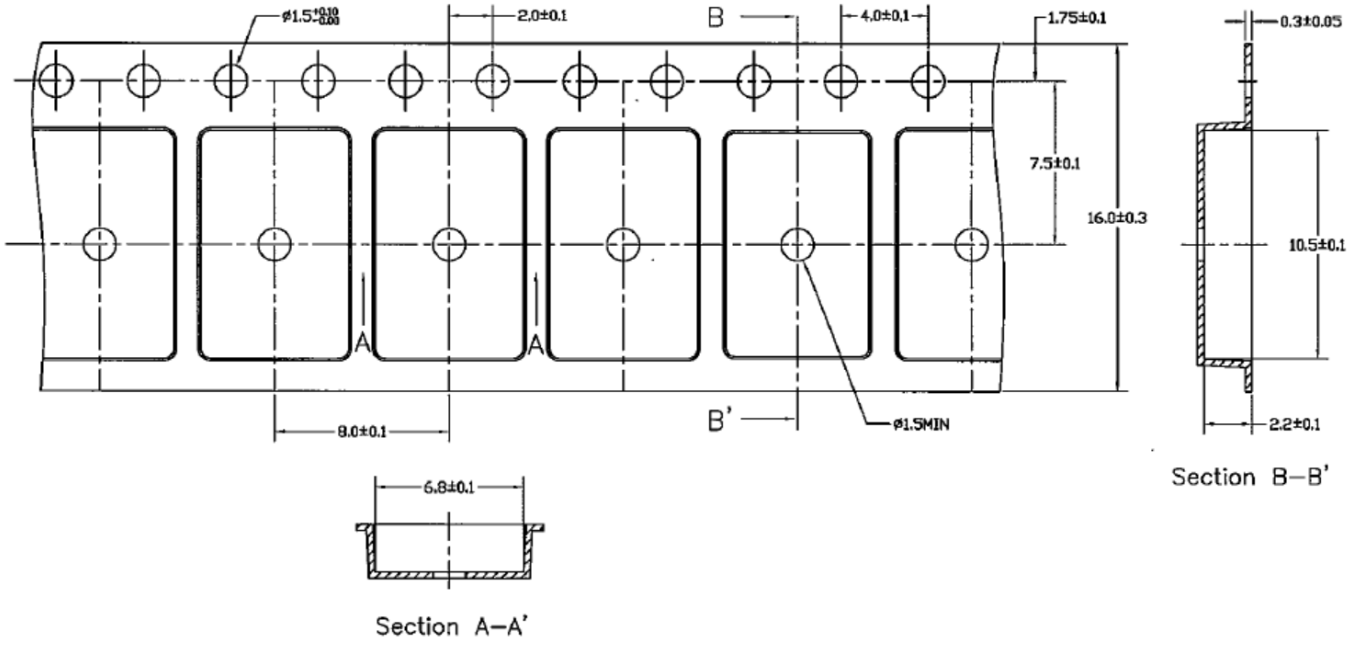



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.200 | 0.300 | 0.008 | 0.012 |
| c | 0.170 | 0.250 | 0.007 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.200 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 0.635(BSC) | | 0.025(BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

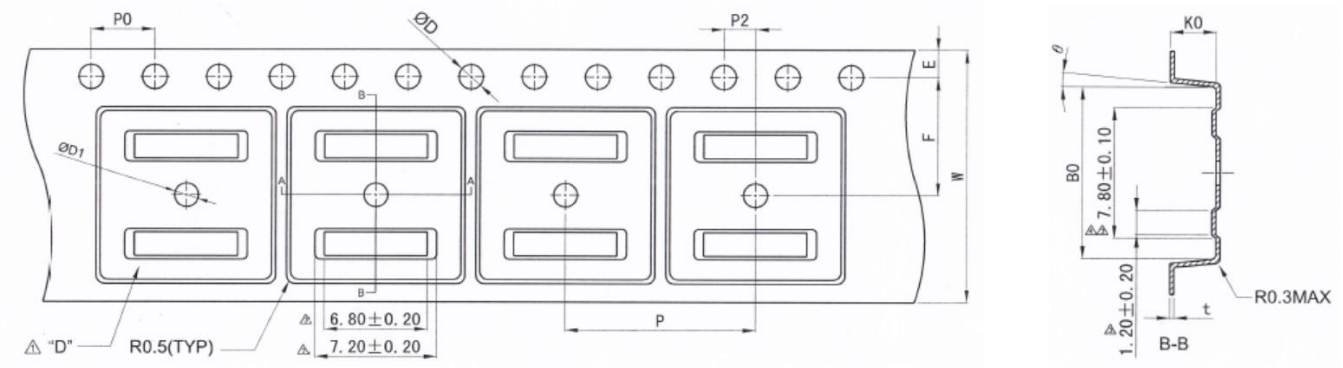
*Figure19. 16-Lead SSOP Outline Package [SSOP16]*

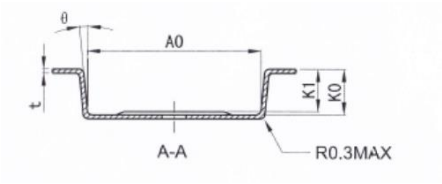
# REEL INFORMATION

16-Lead SOIC_N



16-Lead SOIC_W



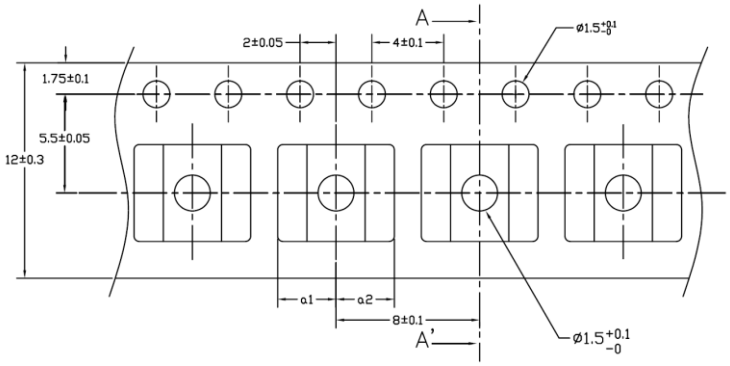



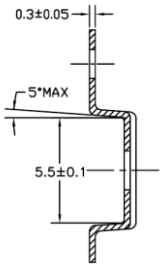

| Items | Size(mm) |
|---|---|
| E | 1.75±0.10 |
| F | 7.50±0.05 |
| P2 | 2.00±0.05 |
| D | 1.55±0.05 |
| D1 | 1.5±0.10 |
| P0 | 4.00±0.10 |
| 10P0 | 40.00±0.20 |

| Items | Size(mm) |
|---|---|
| W | 16.00±0.30 |
| P | 12.00±0.10 |
| A0 | 10.90±0.10 |
| B0 | 10.80±0.10 |
| K0 | 3.00±0.10 |
| t | 0.30±0.05 |
| K1 | 2.70±0.10 |
| θ | 5° TYP |

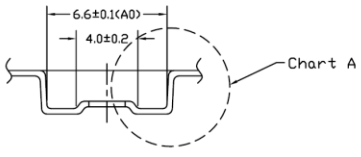


16-Lead SSOP




Section A-A'



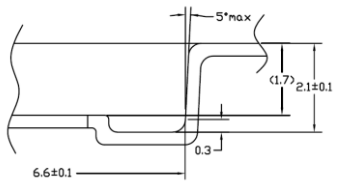




Chart A(3:1)

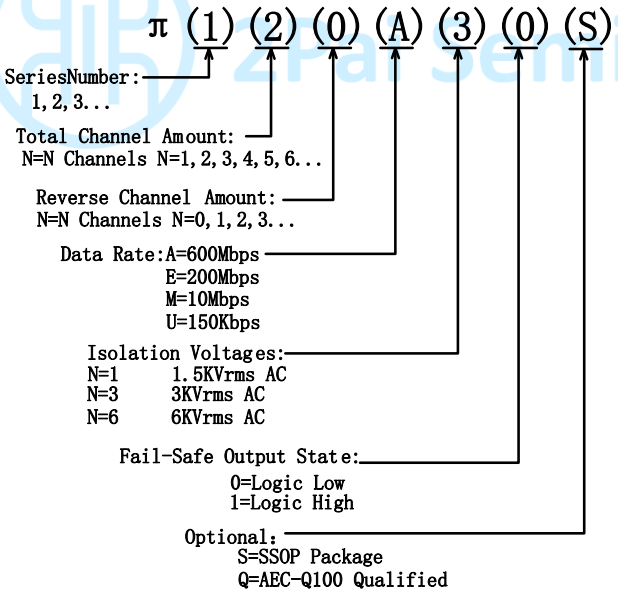
# ORDERING GUIDE

| Model Name | | Temperature Range | No. of Inputs, $V_{DD1}$ Side | No. of Inputs, $V_{DD2}$ Side | Withstand Voltage Rating (kV rms) | Fail-Safe Output State | Package Description | Package Option | Quantity |
|---|---|---|---|---|---|---|---|---|---|
| π130U31 | Pai130U31 | −40°C to +125°C | 3 | 0 | 3 | High | 16-Lead SOIC_N | S-16-N | 2500 per reel |
| π130U30 | Pai130U30 | −40°C to +125°C | 3 | 0 | 3 | Low | 16-Lead SOIC_N | S-16-N | 2500 per reel |
| π131U31 | Pai131U31 | −40°C to +125°C | 2 | 1 | 3 | High | 16-Lead SOIC_N | S-16-N | 2500 per reel |
| π131U30 | Pai131U30 | −40°C to +125°C | 2 | 1 | 3 | Low | 16-Lead SOIC_N | S-16-N | 2500 per reel |
| π130U61 | Pai130U61 | −40°C to +125°C | 3 | 0 | 6 | High | 16-Lead SOIC_W | S-16-W | 1500 per reel |
| π130U60 | Pai130U60 | −40°C to +125°C | 3 | 0 | 6 | Low | 16-Lead SOIC_W | S-16-W | 1500 per reel |
| π131U61 | Pai131U61 | −40°C to +125°C | 2 | 1 | 6 | High | 16-Lead SOIC_W | S-16-W | 1500 per reel |
| π131U60 | Pai131U60 | −40°C to +125°C | 2 | 1 | 6 | Low | 16-Lead SOIC_W | S-16-W | 1500 per reel |
| π130U31S | Pai130U31S | −40°C to +125°C | 3 | 0 | 3 | High | 16-Lead SSOP | SSOP16 | 4000 per reel |
| π130U30S | Pai130U30S | −40°C to +125°C | 3 | 0 | 3 | Low | 16-Lead SSOP | SSOP16 | 4000 per reel |
| π131U31S | Pai131U31S | −40°C to +125°C | 2 | 1 | 3 | High | 16-Lead SSOP | SSOP16 | 4000 per reel |
| π131U30S | Pai131U30S | −40°C to +125°C | 2 | 1 | 3 | Low | 16-Lead SSOP | SSOP16 | 4000 per reel |

Notes:

[1] π1xxxxxQ special for Auto, qualified for AEC-Q100

# PART NUMBER NAMED RULE




Notes:

Pai13xxxx is equals to π13xxxx in the customer BOM

# REVISION HISTORY

| Revision | Updated | Date | Page | Change Record |
|---|---|---|---|---|
| 1 | Victory | 2018/09/20 | All | Initial version |
| 2 | Victory | 2018/11/28 | P1,P11 | Changed $C_{IN}$, $C_{OUT}$ in Figure2 from 0.1uF to 1uF.<br>Changed the recommended bypass capacitor value from between 0.1 µF and 1 µF to between 0.1 µF and 10 µF. |
| 3 | Devin | 2019/09/08 | P1,P7,P11 ,P13,P14, P15 | P1: Changed the address from 'Room 19307, Building 8, No.498, GuoShouJing Road' to 'Room 308-309, No.22, Boxia Road'; Changed '(W)SOIC package' to 'SOIC_N, SOIC_W and SSOP package'; Add ***i*Divider** technology description in General Description.<br>Changed $C_{IN}$, $C_{OUT}$ in Figure2 from 1uF to 0.1uF.<br>P7: Add 'and SSOP16 Pin 1-Pin8' and 'and SSOP16 Pin 9-Pin16' in note 1.<br>P11: Add ***i*Divider** technology description in overview.<br>P13: Add Figure19. 16-Lead SSOP Outline Package drawing<br>P14: Add 16-Lead SSOP Reel drawing; Updated 16-Lead SOIC_W reel drawing.<br>P15: Add character 'S' and 'Q' in part number named rule; Changed the SOIC_W quantity from '1000 per reel' to '1500 per reel'; Add 'π130U31S、π130U30S、π131U31S、π131U30S' in ordering guide |