普 誠 科 技
Princeton Technology Corp.

# DESCRIPTION

The PT2467 provides an integrated motor driver for cameras, consumer products, toys and other application with low-voltage or battery-powered motion control.

The PT2467 can supply up to 1A of output DC current. It operates on a motor power supply(VM) from 0 to 12V and a device power supply voltage (VCC) of 1.8V to 6V.

The PT2467 has a PWM (IN1-IN2) input interface Full protections are integrated with over-current protection, under-voltage lockout and over-temperature shutdown.
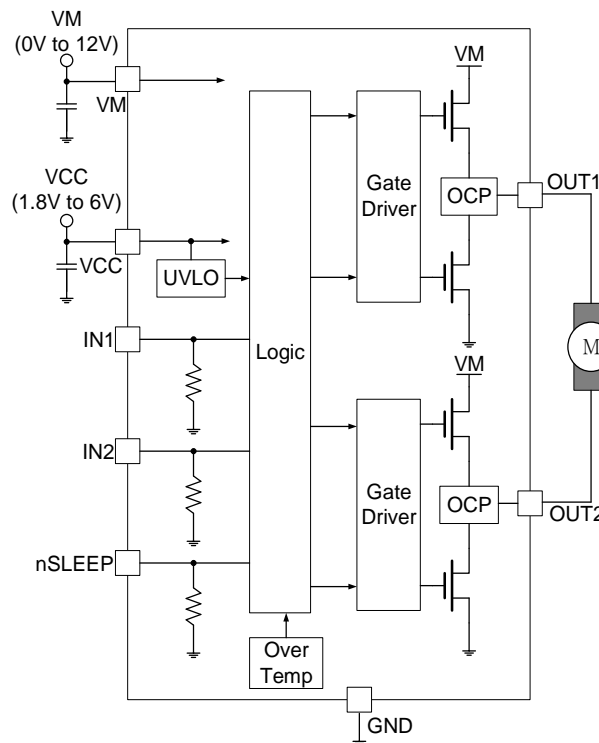
# APPLICATION

- Cameras
- DSLR Lenses
- Consumer Products
- Toys
- Robotics

# FEATURE

- H-Bridge Motor Driver
  - DC Motor or Other Loads
  - Low On-Resistance : HS+LS 1Ω
- 1-A Maximum DC Drive Current
- Separate Motor and Logic Supply
  - Motor VM : 0 to 12V
  - Logic VCC : 1.8V to 6V
- Low-Power Sleep Mode
  - 10nA with $I_{VM}$ and $I_{VCC}$
- Small Package and Footprint
  - 8-Pin DFN with Thermal PAD(2.0 X 2.0 mm)
  - 8-Pin SOP
- Protection Features
  - VCC Under-Voltage Lockout
  - Over-Current Protection
  - Thermal Shutdown

# BLOCK DIAGRAM
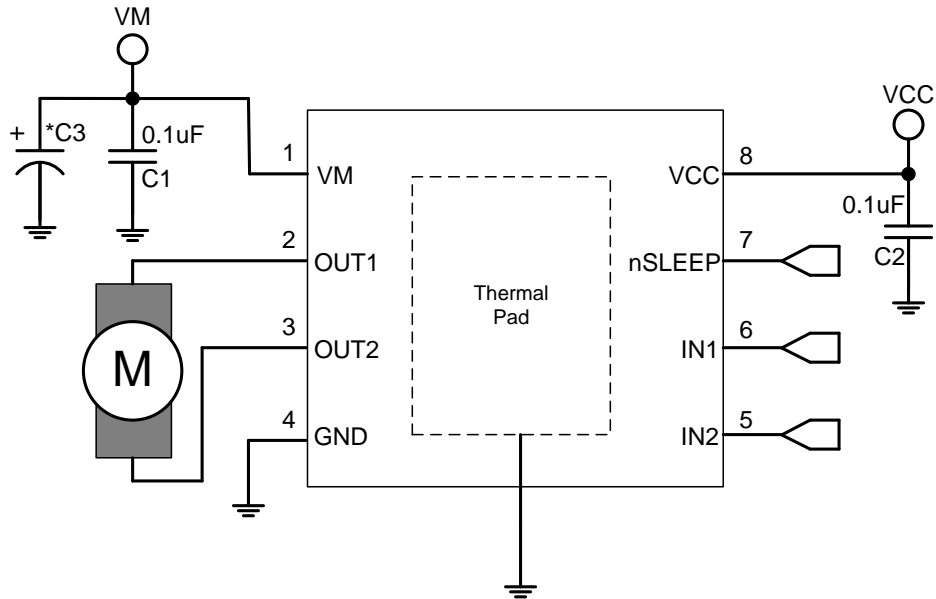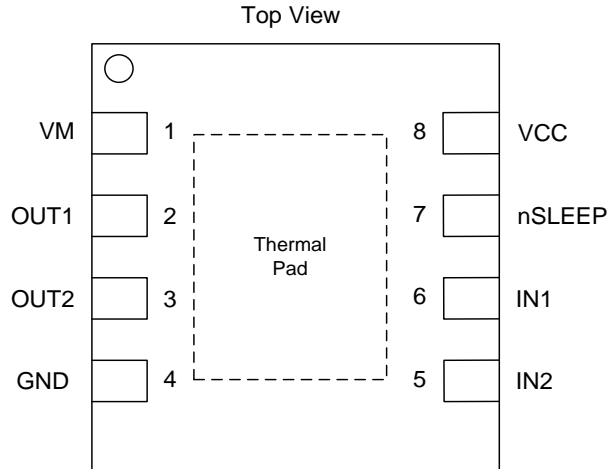


**Figure 1. Function Block Diagram**

# APPLICATION CIRCUIT



**Figure 2. Schematic of Application**

The recommended C3 is 10uF above. Details are referred to at the chapter *"Power Supply Recommendations"*.

# ORDER INFORMATION

| Valid Part Number | Package Type | Top Code |
|---|---|---|
| PT2467-S | SOP 8 | PT2467-S |
| PT2467 | DFN 8 | PT2467 |

# PIN DESCRIPTION

Top View

```
        ┌──────────────────────┐
        │ ○                    │
        │ ┌─┐                ┌─┐│
   VM ──┤ │ │ 1          8 │ │├── VCC
        │ └─┘  ┌ ─ ─ ─ ┐  └─┘│
        │ ┌─┐  ·        ·  ┌─┐│
 OUT1 ──┤ │ │ 2·        ·7 │ │├── nSLEEP
        │ └─┘  · Thermal ·  └─┘│
        │ ┌─┐  ·  Pad   ·  ┌─┐│
 OUT2 ──┤ │ │ 3·        ·6 │ │├── IN1
        │ └─┘  ·        ·  └─┘│
        │ ┌─┐  └ ─ ─ ─ ┘  ┌─┐│
  GND ──┤ │ │ 4          5 │ │├── IN2
        │ └─┘                └─┘│
        │                      │
        └──────────────────────┘
```

| Pin Name | I/O | Description | Pin No. |
|---|---|---|---|
| VM | Power | Motor power supply | 1 |
| OUT1 | Output | Motor output 1 | 2 |
| OUT2 | Output | Motor output 2 | 3 |
| GND | Power | Ground | 4 |
| IN2 | Input | Input 2 | 5 |
| IN1 | Input | Input 1 | 6 |
| nSLEEP | Input | Sleep mode input | 7 |
| VCC | Power | Logic power supply | 8 |

# FUNCTION DESCRIPTION

## *BRIDGE CONTROL*

The PT2467 is controlled using a PWM input interface, also called an IN-IN interface. Each output is controlled by a corresponding input pin.

| nsleep | IN1 | IN2 | Out1 | Out2 | Function (DC Motor) |
|--------|-----|-----|------|------|---------------------|
| 0 | X | X | Z | Z | Coast |
| 1 | 0 | 0 | Z | Z | Coast |
| 1 | 0 | 1 | L | H | Reverse |
| 1 | 1 | 0 | H | L | Forward |
| 1 | 1 | 1 | L | L | Brake |

**Table 1. Control Logic**

## *PROTECTION MANAGEMENT*

The PT2467 is fully protected against VCC under-voltage, overcurrent, and over-temperature events

| Fault | Condition | H-Bridge | Recovery |
|-------|-----------|----------|----------|
| VCC Under-Voltage | VCC < 1.6V | Disable | VCC>1.8V |
| Over-Current | IOUT > 1.9A (MIN) | Disable | tRETRY |
| Thermal Shutdown | TJ > 150℃ (MIN) | Disable | TJ < 150℃ |

**Table 2. Fault Behavior**

## *FUNCTIONAL MODES*

The PT2467 is active unless the nSLEEP pin is brought logic low. In sleep mode, the H-bridge FETs are disabled Hi-Z. The PT2467 is brought out of sleep mode automatically if nSLEEP is brought logic high.

| Mode | Condition | H-Bridge |
|------|-----------|----------|
| Operating | nSLEEP pin=1 | Operating |
| Sleep Mode | nSLEEP pin=0 | Disabled |
| Fault Encountered | Any fault condition met | Disabled |

**Table 3. Operation Modes**

# POWER SUPPLY RECOMMENDATIONS

Having appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance.

The amount of local bulk capacitor needed depends on the following factors,
- The highest current required by the motor system.
- The power-supply capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless dc, stepper)
- The motor braking method.

The inductance between the power supply and motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to supply. The recommended C3 is 10uF above.
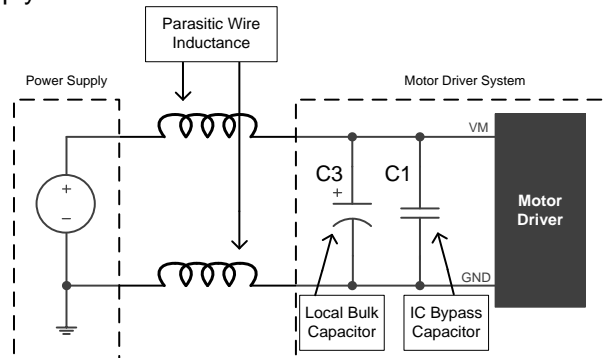


**Figure 3. Motor Driver System with External Power Supply**

# PCB LAYOUT

The VM and VCC should be bypassed to GND using low-ESR ceramic capacitors with recommended value of 0.1uF. These capacitors should be placed as close to the VM and VCC as possible with a thick trace or ground plane connection to GND.
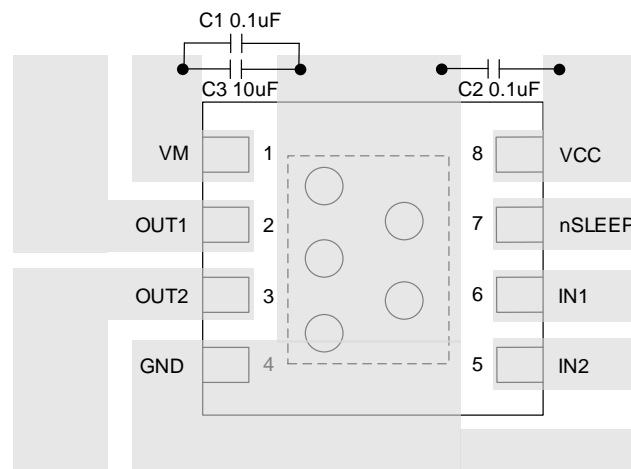


**Figure 4. Simplified Layout Example**

# ABSOLUTE MAXIMUM RATINGS

| Parameters | | | Min | Max | Unit |
|---|---|---|---|---|---|
| Motor Power Supply Voltage , VM | | | -0.3 | 13 | V |
| Logic Power Supply Voltage , VCC | | | -0.3 | 6.5 | V |
| Operating Temperature, Top | | | -40 | 150 | °C |
| Storage Temperature, Tstg | | | -40 | 150 | °C |
| Operation Humidity | | | 20 | 85 | % |
| Storage Humidity | | | 20 | 90 | % |
| ESD | All Pins | HBM | ±4 | | KV |
| | | MM | ±0.4 | | KV |
| | | CDM* | ±1.5 | | KV |

*CDM test is based on ANSI/ESDA/JECEC JS-002-2014

# RECOMMENDED OPERATING CONDITIONS

| | Parameters | Min | Max | Unit |
|---|---|---|---|---|
| VM | Motor Power Supply Voltage | 0 | 12 | V |
| VCC | Logic Power Supply Voltage | 1.8 | 6 | V |
| $I_{OUT}$ | Motor Peak Current | 0 | 1 | A |
| $f_{PWM}$ | Externally Applied PWM Frequency | 0 | 250 | KHz |
| $V_{LOGIC}$ | Logic Level Input Voltage | 0 | 6 | V |
| $T_A$ | Operating Ambient Temperature | -40 | 85 | °C |

# PACKAGE THERMAL CHARACTERISTICS

## *PACKAGE: DFN*

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| From chip conjunction dissipation to external environment | θJA | 75.6 | ℃/W |

## *PACKAGE: SOP, 150MIL*

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| From chip conjunction dissipation to external environment | θJA | 113.9 | ℃/W |

# ELECTRICAL CHARACTERISTICS

$T_A$=25℃ , over recommended operating conditions unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES(VM,VCC)** | | | | | | |
| VM Current | | | | | | |
| $I_{VM1}$ | VM coast current | VM=5V ; VCC=3V ; No PWM Coast Mode | | 70 | | µA |
| $I_{VM2}$ | VM F/R current | VM=5V ; VCC=3V ; No PWM Forward/Reverse Mode | | 350 | | µA |
| $I_{VM3}$ | VM brake current | VM=5V ; VCC=3V ; No PWM Brake Mode | | 70 | | µA |
| $I_{VM4}$ | VM PWM current | VM=5V ; VCC=3V PWM=50KHz | | 280 | | µA |
| $I_{VMQ}$ | VM sleep current | VM=5V ; VCC=3V nSLEEP=0 | | 5 | | nA |
| VCC Current | | | | | | |
| $I_{VCC1}$ | VCC coast current | VM=5V ; VCC=3V ; No PWM Coast Mode | | 380 | | µA |
| $I_{VCC2}$ | VCC F/R current | VM=5V ; VCC=3V ; No PWM Forward/Reverse Mode | | 500 | | µA |
| $I_{VCC3}$ | VCC brake current | VM=5V ; VCC=3V ; No PWM Brake Mode | | 550 | | µA |
| $I_{VCC4}$ | VCC PWM current | VM=5V ; VCC=3V PWM=50KHz | | 450 | | µA |
| $I_{VCCQ}$ | VCC sleep current | VM=5V ; VCC=3V nSLEEP=0 | | 2 | | nA |
| **CONTROL INPUTS (IN1, IN2, nSLEEP)** | | | | | | |
| $V_{IL}$ | Input logic low voltage | | | | 0.3*VCC | V |
| $V_{IH}$ | Input logic high voltage | | 0.5*VCC | | | V |
| $I_{IL}$ | Input logic low current | VIN=0V | | | 5 | µA |
| $I_{IH}$ | Input logic high current | VIN=3.3V | | | 50 | µA |
| $R_{PD}$ | Pulldown resistance | IN1 IN2 nSLEEP | | 100 | | KΩ |
| **MOTOR DRIVER OUTPUTS (OUT1, OUT2)** | | | | | | |
| $r_{DS(ON)}$ | HS + LS FETs on-resistance | VM=5V ; VCC=3V ; Io=800mA | | 700 | | mΩ |
| $I_{OFF}$ | Off-state leakage current | VOUT=0V | | 5 | | nA |
| **PROTECTION CIRCUITS** | | | | | | |
| $V_{UVLO}$ | VCC under-voltage lockout | VCC falling | | 1.6 | | V |
| | | VCC rising | | 1.8 | | V |
| $I_{OCP}$ | Over-current protection trip level | | 1.2 | | 2 | A |
| $t_{RETRY}$ | Over-current retry time | | | 1 | | mS |
| $T_{TSD}$ | Thermal shutdown temperature | Die temperature | | 160 | | ˚C |

# TIMING REQUIREMENTS

$T_A=25℃$ , VM=5V, VCC=3V, $R_L=20Ω$

| Time | Parameter | Max | Unit |
|---|---|---|---|
| t1 | Output enable time | 700 | nS |
| t2 | Output disable time | 700 | nS |
| t3 | Delay time, INx high to OUTx high | 380 | nS |
| t4 | Delay time, INx low to OUTx low | 380 | nS |
| t5 | Output rise time | 280 | nS |
| t6 | Output fall time | 280 | nS |
| twake | Wake time , nSLEEP rising edge to part active | 10 | µS |
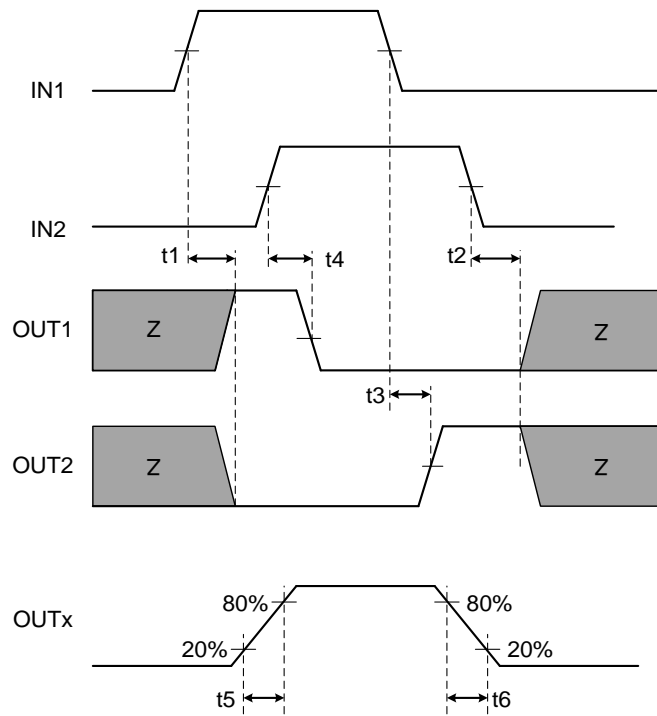
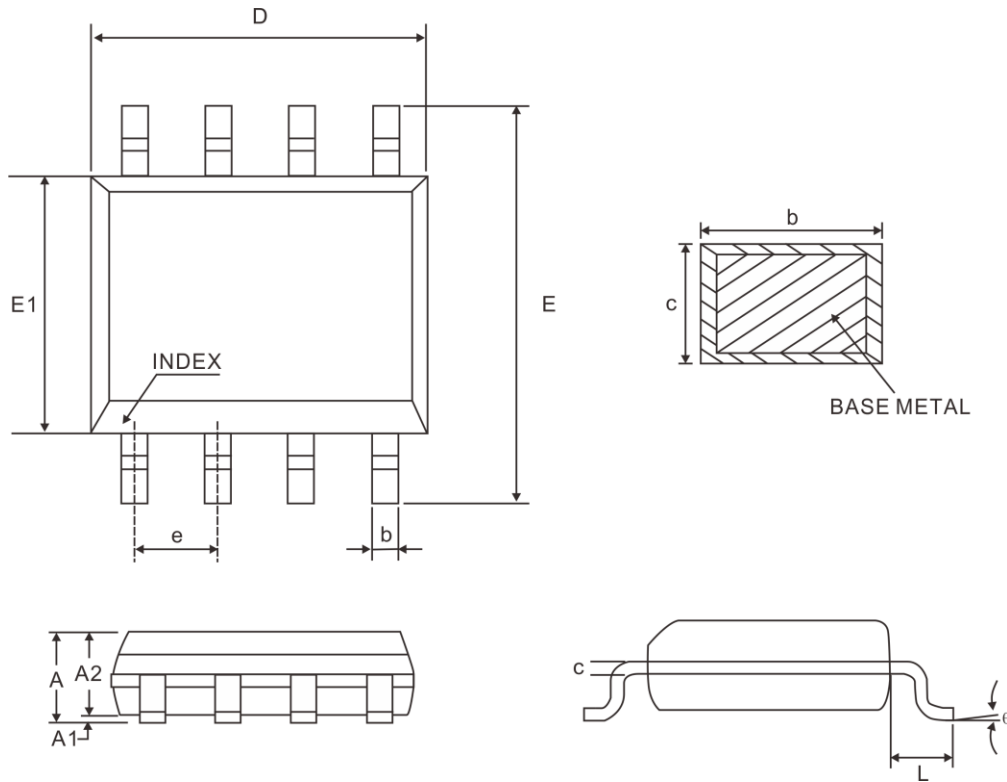**Figure 5. Input and Output Timing**

# PACKAGE INFORMATION

## *8-PIN, DFN*
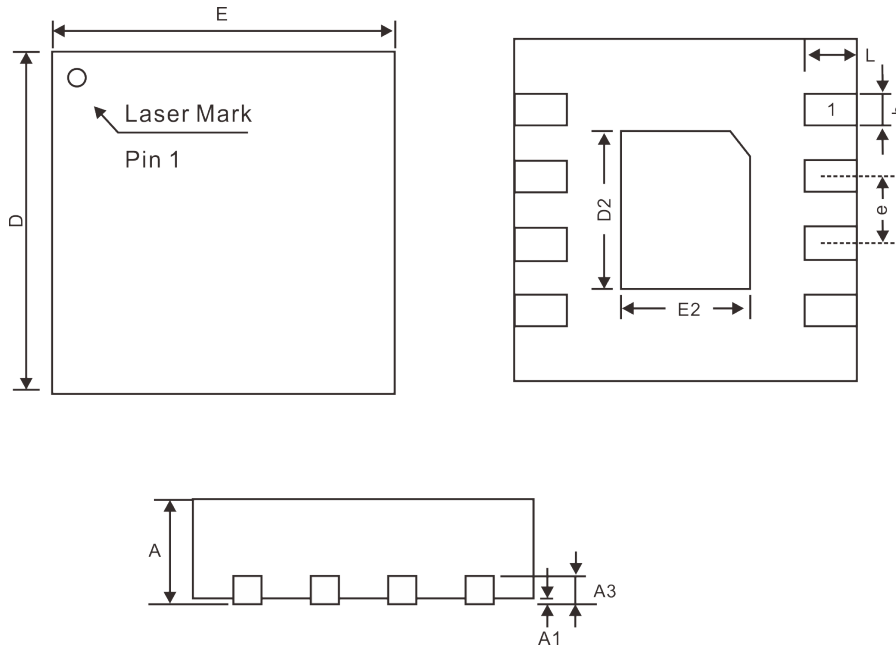


| Symbol | Dimensions(mm) | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.18 | 0.25 | 0.30 |
| D | 2.00 BSC | | |
| E | 2.00 BSC | | |
| e | 0.50 BSC | | |
| D2 | 1.50 | 1.60 | 1.65 |
| E2 | 0.80 | 0.90 | 0.95 |
| L | 0.25 | 0.30 | 0.35 |

Note: Refer to JEDEC MO-229

## *8 PINS, SOP, 150MIL*



| Symbol | Dimensions(mm) | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | - | - | 1.75 |
| A1 | 0.10 | - | 0.25 |
| A2 | 1.25 | - | - |
| b | 0.31 | - | 0.51 |
| c | 0.10 | - | 0.25 |
| D | 4.90 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| e | 1.27BSC | | |
| L | 0.40 | - | 1.27 |
| θ | 0° | - | 8° |

Notes:
1. Refer to JEDEC MS-012 AA
2. All dimensions are in millimeter

## IMPORTANT NOTICE

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