VS1000 - Ogg Vorbis Player IC with USB and NAND FLASH Interface

Hardware Features

- Low-power operation
- Single input voltage: Internal voltage regulation for analog, digital, and I/O power
- Operates with a single 12 MHz clock
- Internal PLL clock multiplier
- Power button pin, software-controlled power-off
- USB Full Speed hardware
- NAND FLASH interface with ECC
- I/O for user interface
- High-quality on-chip stereo DAC with no phase error between channels
- Stereo earphone driver capable of driving a 30 Ω load
- Lead-free RoHS-compliant package (Green)

Firmware Features

- Implements USB Mass Storage Device and Audio Device
- NAND FLASH handling with error correction, block remapping, and wear levelling
- Default player application in firmware
  - Decodes Ogg Vorbis, sound level normalization using Replay Gain
  - Pause / Play
  - Volume control
  - Next / Previous Song
  - Rewind and Fast Forward
  - Random Play
  - EarSpeaker Spatial Processing
- Bass and treble controls for customized player
- NAND FLASH boot for customized player
- SPI FLASH boot for special applications
- UART for debugging and special applications

Description

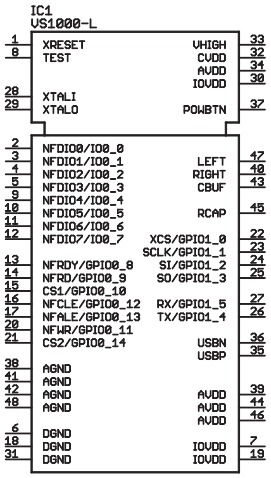
VS1000 is a single-chip Ogg Vorbis (license-free audio codec) player and a system-on-a-chip (SoC) for various control and audio applications. VS1000 contains a high-performance low-power DSP core VSDSP^4, NAND FLASH interface, Full Speed USB port, general purpose I/O pins, SPI, UART, as well as a high-quality variable-sample-rate stereo DAC, and an earphone amplifier and a common voltage buffer.

VS1000 firmware implements a default player that reads and plays files from NAND FLASH. The player can be customized or replaced by boot from NAND FLASH or SPI memory.

When connected to USB, the firmware implements USB Mass Storage Device protocol or acts as an Audio Device, providing a single-chip USB headphone application.

EarSpeaker spatial processing provides more natural sound in headphone listening conditions. It widens the stereo image and positions the sound sources outside the listener's head.

SPI EEPROM can be used to load code in applications that do not use NAND FLASH.



Contents

List of Figures

1 Disclaimer

All properties and figures are subject to change.

2 Definitions

B Byte, 8 bits.

b Bit.

Ki “Kibi” = 2^{10} = 1,024 (IEC 60027-2).

Mi “Mebi” = 2^{20} = 1,048,576 (IEC 60027-2).

Gi “Gibi” = 2^{30} = 1,073,741,824 (IEC 60027-2).

VS_DSP VLSI Solution’s DSP core.

W Word. In VS_DSP, instruction words are 32-bit and data words are 16-bit wide.

3 Characteristics & Specifications

3.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Regulator input voltage	VHIGH	-0.3	5.5	V
Analog Positive Supply	AVDD	-0.3	3.6	V
Digital Positive Supply	CVDD	-0.3	2.7	V
I/O Positive Supply	IOVDD	-0.3	3.6	V
Voltage at Any Digital Input		-0.3	IOVDD+0.3[1]	V
Total Injected Current on Pins			±200 [2]	mA
Operating Temperature		-40	+85	°C
Storage Temperature		-65	+150	°C

[1] Must not exceed 3.6 V
[2] Latch-up limit

3.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating temperature		-40		+85	°C
Analog and digital ground [1]	AGND DGND		0.0		V
Regulator input voltage[2]	VHIGH	AVDD+0.3	4.0	5.25	V
Analog positive supply[3]	AVDD	2.75	2.8	3.6	V
I/O positive supply[3]	IOVDD	1.8	2.8	3.6	V
Input clock frequency[4]	XTALI	12	12[5]	13	MHz
Master clock duty cycle		40	50	60	%
Digital positive supply [3], USB disconnected	CVDD	2.2	2.3	2.65	V
Internal clock frequency, USB disconnected	CLKI	12		42	MHz
Digital positive supply [3], USB connected	CVDD	2.5	2.5	2.65	V
Internal clock frequency, USB connected	CLKU	48		48	MHz

[1] Must be connected together as close the device as possible for latch-up immunity.
[2] At least 4.0 V is required for compliant USB level.
[3] Regulator output of the device.
[4] The maximum sample rate that can be played with correct speed is XTALI/256. With 12 MHz XTALI sample rates over 46875 Hz are played at 46875 Hz.
[5] To be able to use USB, XTALI must be 12 MHz.

3.3 Analog Characteristics of Audio Outputs

Unless otherwise noted: AVDD=2.8V, CVDD=2.4V, IOVDD=2.8V, TA=-40..+85°C, XTALI=12 MHz, Internal Clock Multiplier $3.0\times$. DAC tested with full-scale output sinewave, measurement bandwidth 20..20000 Hz, analog output load: LEFT to CBUF 30 Ω, RIGHT to CBUF 30 Ω.

Parameter	Symbol	Min	Typ	Max	Unit
DAC Resolution			18		bits
Dynamic range (DAC unmuted, A-weighted, min gain)	IDR		96		dB
S/N ratio (full scale signal, no load)	SNR		92		dB
S/N ratio (full scale signal, 30 ohm load)	SNRL	75	90		dB
Total harmonic distortion, max level, no load	THD		0.01		%
Total harmonic distortion, max level, 30 ohm load	THDL		0.1	0.3	%
Crosstalk (L/R to R/L), 30 ohm load, without CBUF [1]	XTALK1		75		dB
Crosstalk (L/R to R/L), 30 ohm load, with CBUF	XTALK2		54		dB
Gain mismatch (L/R to R/L)	GERR	-0.5		0.5	dB
Frequency response	AERR	-0.05		0.05	dB
Full scale output voltage	LEVEL	450	530	600	mVrms
Deviation from linear phase	PH		0	5	°
Analog output load resistance	AOLR		30[2]		Ω
Analog output load capacitance	AOLC			100[3]	pF
DC level (CBUF, LEFT, RIGHT)		1.1		1.3	V
CBUF disconnect current (short-circuit protection)			130	200	mA

[1] Loaded from Left/Right pin to analog ground via 100 µF capacitors.
[2] AOLR may be lower than *Typical*, but distortion performance may be compromised. Also, there is a maximum current that the internal regulators can provide.
[3] CBUF must have external 10 Ω + 47 nF load, LEFT and RIGHT must have external 20 Ω + 10 nF load for optimum stability and ESD tolerance.

3.4 Analog Characteristics of Regulators

Parameter	Symbol	Min	Typ	Max	Unit
IOVDD					
Recommended voltage setting range		1.7		3.6	V
Voltage setting step size		50	60	70	mV
Default setting, reset mode [1]			1.8		V
Default setting, active mode [2]			1.8 / 3.3[3]		V
Load regulation			4.0		mV/mA
Line regulation from VHIGH			2.0		mV/V
Continuous current			30[4]	40	mA
CVDD					
Recommended voltage setting range		1.8		2.6	V
Voltage setting step size		35	48	55	mV
Default setting, reset mode [1]			1.8		V
Default setting, active mode [2]			2.2		V
Continuous current			30[4]	35	mA
Load regulation			2.0		mV/mA
Line regulation from VHIGH			2.0		mV/V
AVDD					
Recommended voltage setting range		2.6		3.6	V
Voltage setting step size		35	46	55	mV
Default setting, reset mode [1]			2.5		V
Default setting, active mode [2]			2.7		V
Continuous current			30[4]	70	mA
Load regulation			1.5		mV/mA
Line regulation from VHIGH			2.0		mV/V

[1] Device enters reset mode when XRESET pin is pulled low.
[2] Device enters active mode when XRESET pin is pulled high after reset mode. Regulator settings can be modified when booted from external memory (see Section 7).
[3] Depends on GPIO0_7 pin status in boot (see Section 7). VS1000b/c used 1.8V / 3.6V.
[4] Device is tested with a 30 mA load.

3.5 Analog Characteristics of VHIGH Voltage Monitor

Parameter	Symbol	Min	Typ	Max	Unit
Trigger voltage	AMON		1.07×AVDD		V
Hysteresis			50		mV

3.6 Analog Characteristics of CVDD Voltage Monitor

Parameter	Symbol	Min	Typ	Max	Unit
Trigger voltage	CMON	1.40	1.53		V
Hysteresis			2		mV

3.7 Power Button Characteristics

When the PWRBTN input is high the internal regulators get start signal so that they activate and the vs1000 starts normal operation. Unless otherwise noted: VHIGH = 4.0..5.3 V

Parameter	Min	Typ	Max	Unit
PWRBTN pulse	10 ms, 2.5 V			

Note: PWRBTN is both an analog input pin and a digital input pin, so the voltage on the pin should not exceed 3.6 V.

Note: PWRBTN generates a RESET if it is continuously asserted for approximately 5.6 seconds.

If the application is intended to turn on automatically when power is applied instead of a press of a power button, a capacitor and a suitable resistor divider can generate a pulse to PWRBTN from the supply voltage. However, care must be taken that the voltage limit of 3.6 V is not exceeded.

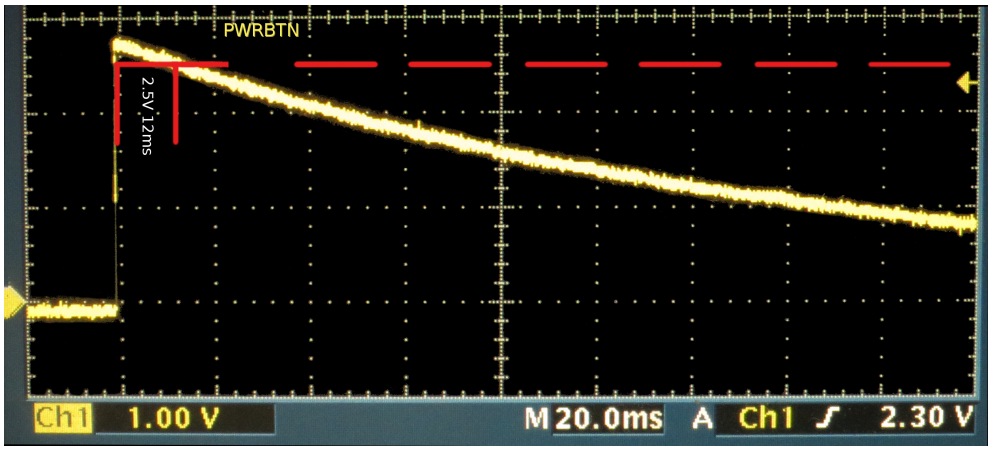


Figure 1: Typical PWRBTN pulse and minimum requirement

A PWRBTN pulse generated from a 5 V VHIGH using a 1μF capacitor and a 56kΩ/100kΩ resistor divider. PWRBTN is at or above 2.5V for a duration of about 12 ms, which is well over the guaranteed activation time.

3.8 Power-On Reset

Because the VS1000 contains its own regulators, special care must be taken to guarantee a good reset state during the power-up. The voltage on the xRESET pin has to remain sufficiently lower than the IOVDD voltage until the IOVDD and CVDD voltages have risen high enough to be able to reset and hold the reset state.

The suggested connection (schematics in Section 5) is to connect the xRESET signal with a 100kΩ resistor to IOVDD and a 10μF capacitor to ground. This should provide a sufficient delay in a full power-up situation.

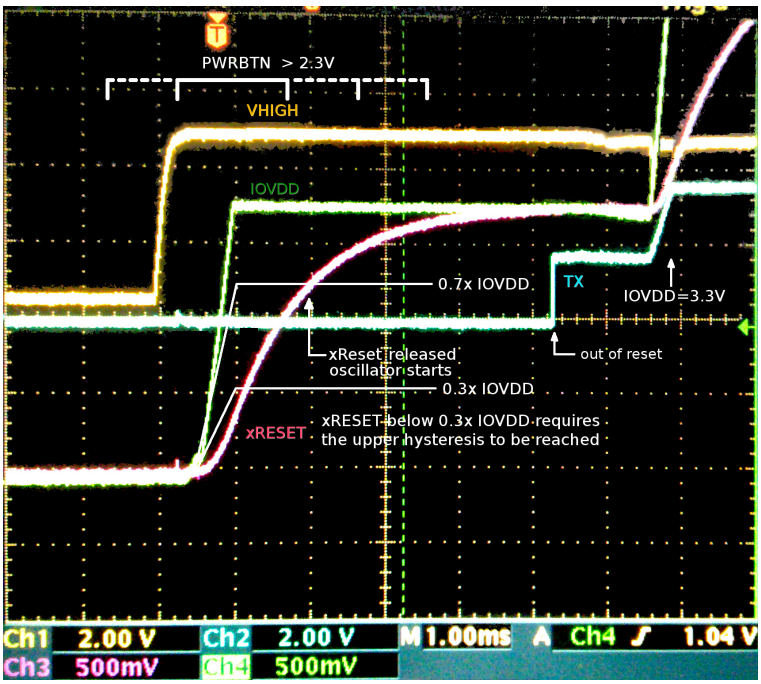


Figure 2: VS1000 Typical Power-up.

The above example picture shows a typical power-up sequence. A PWRBTN signal (not shown) is generated from VHIGH using a RC as discussed in Section 3.7. When both VHIGH and PWRBTN are active, the AVDD, IOVDD and CVDD regulators start (IOVDD shown). The IOVDD regulator starts in 1.8 V mode. Because xRESET stays below 0.3×IOVDD by the RC at the beginning of the power-up, xRESET needs to reach 0.7×IOVDD before RESET is de-asserted. After that happens, the oscillator amplifier leaves reset state, and the oscillator starts. When the amplitude of the oscillation is sufficient, the VS1000 leaves reset. At this moment, all peripheral pins that are normally outputs switch from high-impedance state to output mode in their default states. The TX pin is shown as an example. TX becomes an output and is driven high when VS1000 leaves the reset state. If GPIO0_7 contains a pull-up resistor, the IOVDD regulator is configured to 3.3V, which can also be seen.

Note that the passive RC circuit generates a reset only when power-up is performed from a total power-off state. If there are residual voltages in the system (such as during an intermittent supply voltage drop, or an external circuit driving any IO pin of VS1000), the relative levels of xRESET and IOVDD/CVDD may no longer fulfill the $<0.3\times$IOVDD condition to create a good reset. **You will need an external voltage monitor chip connected to xRESET or control xRESET using your microcontroller in any application where short power interruptions are possible.**

3.9 Power-Off

The power button pin (PWRBTN) turns the regulators on so that VS1000 can boot. When asserted for more than 5.6 seconds it generates a watchdog-type reset to reboot the system. Powering off, however, is performed by software. This prevents important data from being lost when the user requests power off while for example writing to external memory.

The ROM firmware detects a request to power off from a long press (2 seconds) of the power button. The power off function can also be called by user software. The default power off routine performs the following steps.

- Switch to 1.0x clock and disable PLL. This reduces power consumption.
- Disable interrupts.
- Power down USB and analog drivers.
- Turn off LEDs - switch IO1_1(SCLK), IO1_2(SI) and IO1_3(SO) low.
- Wait that the power button is released. Otherwise the power button being asserted would immediately force the regulators on again.
- Turn on watchdog with a 5-second interval if it isn't already active.
- Keep shutting down the regulators until vs1000 powers down or gets a watchdog reset.

Because the CVDD voltage monitor uses a reference that is derived from AVDD, the core voltage CVDD should drop sufficiently faster than AVDD so that the voltage monitor keeps the reset asserted long enough. Thus the capacitance on CVDD should be significantly smaller than in AVDD.

Note that when the CVDD monitor asserts reset, the current consumption of CVDD will drop near zero. If necessary, a large resistor (1MΩ) can be added to CVDD to drop the voltage faster.

If the supply voltage to VHIGH has a high internal impedance, such as batteries, the drop in current consumption may cause the voltages to rise enough for the CVDD monitor to deassert reset, causing a reboot of the system (which enables the regulators). With such a power source, smaller bypass capacitors for the IOVDD voltage would stop the oscillator sooner and thus prevent the vs1000 from leaving the reset state.

3.10 Analog Characteristics of USB

Parameter	Min	Max	Unit
Drive low level, 2.32 mA load	0.065	0.102	V
Drive low level, 6.1×AVDD mA load	0.171×AVDD	0.270×AVDD	V
Drive low level, 10.71×AVDD mA load	0.300×AVDD	AVDD	V
Drive high level, -2.32 mA load	AVDD-0.165	AVDD-0.065	V
Drive high level, -6.1×AVDD mA load	0.650×AVDD	0.829×AVDD	V
Drive high level, -10.71×AVDD mA load	0	0.700×AVDD	V
USBP level, with 15 kΩ pull-down	2.7	0.943×AVDD	V
High-Level input voltage (single-ended)	0.7×AVDD	AVDD+0.3	V
Low-Level input voltage (single-ended)	-0.2	0.3×AVDD	V
Differential input common voltage, AVDD≥3.3V	0.8	2.5	V
Differential input signal level, AVDD≥3.3V	200		mV
Input leakage current	-2.0	2.0	µA

3.11 Power Consumption

Parameter	Symbol	Min	Typ	Max	Unit
Current Consumption of AVDD, no signal			3.4		mA
Current Consumption of AVDD, sine test, CBUF + 30Ω load			33	55	mA
Current Consumption of CVDD, sine test 3.0× clock			13	25	mA
Current Consumption of USB suspend mode [1]			650		µA
Current Consumption, Reset @ 25 °C			24	48	µA
Example application (see Section 5) IOVDD=3.3V AVDD=2.8V CVDD=2.5V					
Total Power, play mode, CBUF + 30Ω load			120		mW
Example application (see Section 5) IOVDD=2.7V AVDD=2.6V CVDD=2.2V					
Total Power, pause mode			10		mW
Total Power, play mode, CBUF + 30Ω load			80		mW

[1] Requires user code support

3.12 Digital Characteristics

Parameter	Sym	Min	Typ	Max	Unit
High-Level Input Voltage		0.7×IOVDD		IOVDD+0.3	V
Low-Level Input Voltage		-0.2		0.3×IOVDD	V
High-Level Output Voltage, -1.0 mA load [1]		0.7×IOVDD			V
Low-Level Output Voltage, 1.0 mA load [1]				0.3×IOVDD	V
XTALO high-level output voltage, -0.1 mA load		0.7×IOVDD			V
XTALO low-level output voltage, 0.1 mA load				0.3×IOVDD	V
Input leakage current		-1.0		1.0	µA
Rise time of all output pins, load = 30 pF [1]				50	ns

[1] Pins GPIO0_[14:0], GPIO1_[5:0].

4 Packages and Pin Descriptions

4.1 Packages

LPQFP-48 is lead (Pb) free and RoHS-compliant package. RoHS is a short name of *Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment*.

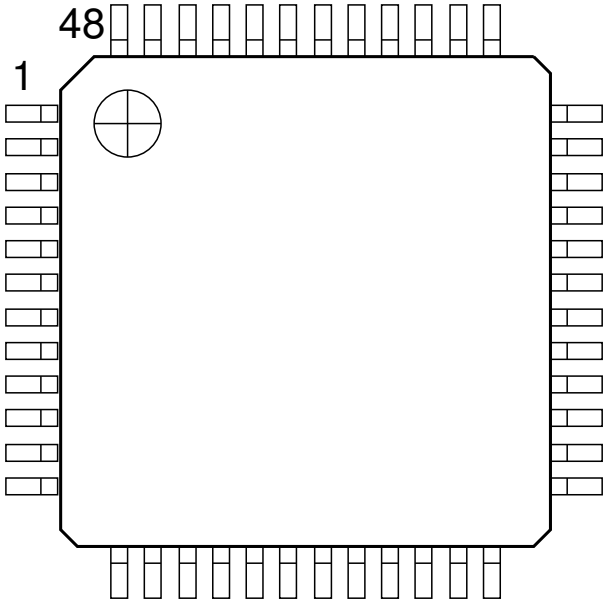


Figure 3: VS1000 pin configuration, LQFP-48.

LQFP-48 package dimensions are at *http://www.vlsi.fi/* .

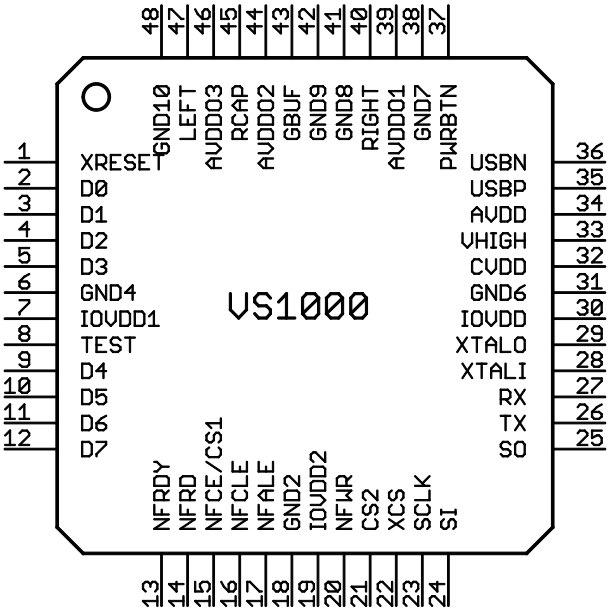


Figure 4: VS1000 pins, LQFP-48.

4.2 LQFP-48 Pin Descriptions

Pin Name	LQFP Pin	Pin Type	Function
XRESET	1	DI	Active low asynchronous reset, schmitt-trigger input
NFDIO0 / GPIO0_0	2	DIO	Nand-flash IO0 / General-purpose IO Port 0, bit 0
NFDIO1 / GPIO0_1	3	DIO	Nand-flash IO1 / General-purpose IO Port 0, bit 1
NFDIO2 / GPIO0_2	4	DIO	Nand-flash IO2 / General-purpose IO Port 0, bit 2
NFDIO3 / GPIO0_3	5	DIO	Nand-flash IO3 / General-purpose IO Port 0, bit 3
DGND0	6	DGND	Core & I/O ground
IOVDD1	7	IOPWR	I/O power supply
TEST	8	DI	Test mode input (active high), connect to DGND
NFDIO4 / GPIO0_4	9	DIO	Nand-flash IO4 / General-purpose IO Port 0, bit 4
NFDIO5 / GPIO0_5	10	DIO	Nand-flash IO5 / General-purpose IO Port 0, bit 5
NFDIO6 / GPIO0_6	11	DIO	Nand-flash IO6 / General-purpose IO Port 0, bit 6
NFDIO7 / GPIO0_7	12	DIO	Nand-flash IO7 / General-purpose IO Port 0, bit 7
NFRDY / GPIO0_8	13	DIO	Nand-flash READY / General-purpose IO Port 0, bit 8
NFRD / GPIO0_9	14	DIO	Nand-flash RD / General-purpose IO Port 0, bit 9
NFCE / GPIO0_10	15	DIO	Nand-flash CE / General-purpose IO Port 0, bit 10
NFCLE / GPIO0_12	16	DIO	Nand-flash CLE / General-purpose IO Port 0, bit 12
NFALE / GPIO0_13	17	DIO	Nand-flash ALE / General-purpose IO Port 0, bit 13
DGND1	18	DGND	Core & I/O ground
IOVDD2	19	IOPWR	I/O power supply
NFWR / GPIO0_11	20	DIO	Nand-flash WR / General-purpose IO Port 0, bit 11
CS2 / GPIO0_14	21	DIO	General-purpose IO Port 0, bit 14
XCS / GPIO1_0	22	DIO	SPI XCS / General-Purpose I/O Port 1, bit 0
SCLK / GPIO1_1	23	DIO	SPI CLK / General-Purpose I/O Port 1, bit 1
SI / GPIO1_2	24	DIO	SPI MISO / General-Purpose I/O Port 1, bit 2
SO / GPIO1_3	25	DIO	SPI MOSI / General-Purpose I/O Port 1, bit 3
TX / GPIO1_4	26	DIO	UART TX / General-Purpose I/O Port 1, bit 4
RX / GPIO1_5	27	DIO	UART RX / General-Purpose I/O Port 1, bit 5
XTALI	28	AI	Crystal input
XTALO	29	AO	Crystal output
IOVDD	30	IOPWR	I/O power supply, Regulator output
DGND2	31	DGND	Core & I/O ground
CVDD	32	CPWR	Core power supply, Regulator output
VHIGH	33	PWR	Power supply, Regulator input
AVDD	34	APWR	Analog power supply, Regulator output
USBP	35	AIO	USB differential + in / out, controllable 1.5kΩ pull-up
USBN	36	AIO	USB differential - in / out
PWRBTN	37	APB / DI	Power button for Regulator startup and Power Key
AGND0	38	APWR	Analog ground
AVDD1	39	APWR	Analog power supply
RIGHT	40	AO	Right channel output
AGND1	41	APWR	Analog ground
AGND2	42	APWR	Analog ground
CBUF	43	AO	Common voltage buffer for headphones (1.2V nominal)
AVDD2	44	APWR	Analog power supply
RCAP	45	AIO	Filtering capacitance for reference
AVDD3	46	APWR	Analog power supply
LEFT	47	AO	Left channel output
AGND3	48	APWR	Analog ground

Pin types:

Type	Description
DI	Digital input, CMOS input pad
DO	Digital output, CMOS input pad
DIO	Digital input/output
AI	Analog input
AO	Analog output
AIO	Analog input/output
APWR	Analog power supply pin
APB	Analog power button pin
GND	Core or I/O ground pin
CPWR	Core power supply pin
IOPWR	I/O power supply pin

5 Example Schematic

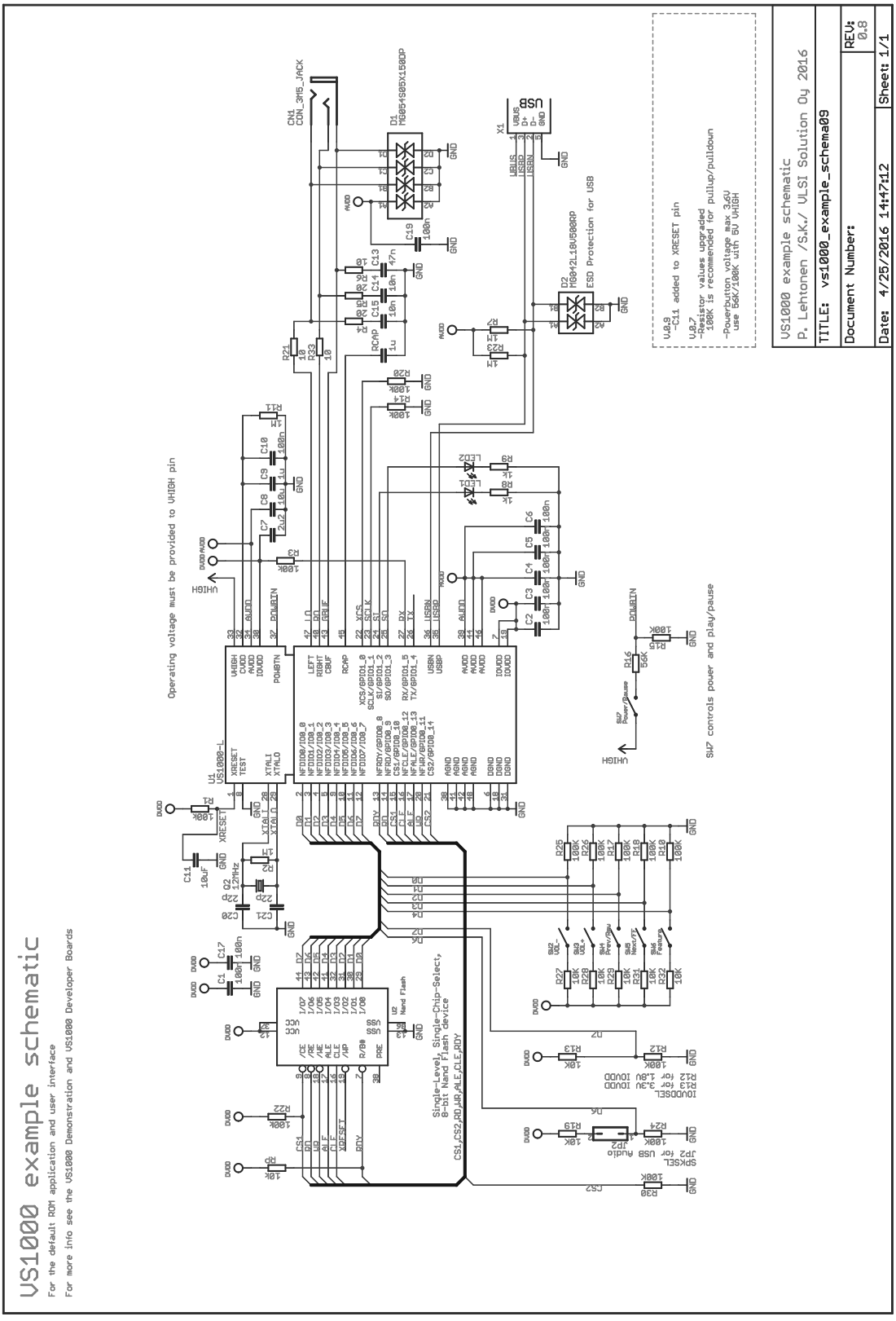


Figure 5: VS1000 example schematic. Populate only one of R12 and R13. Populate R11 if needed for your application.

6 VS1000 Functional Blocks

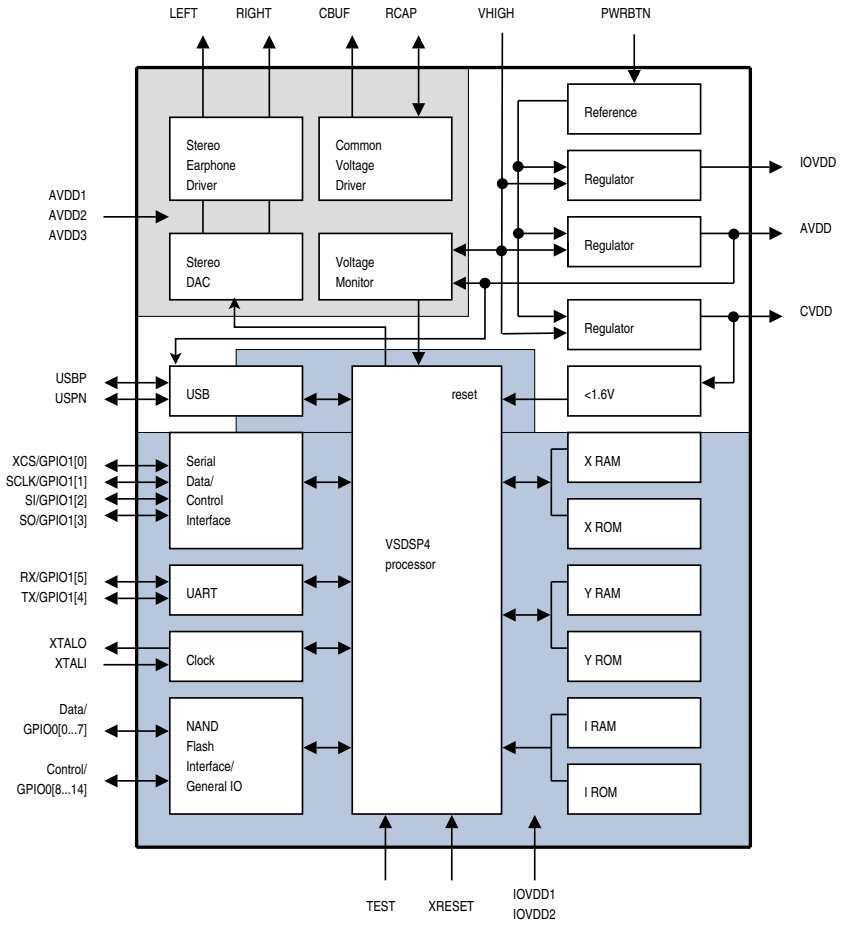


Figure 6: VS1000 block diagram.

6.1 Regulator Section

The VHIGH pin in the regulator section is used as a common main power supply for voltage regulation. This input is connected to three internal regulators, which are activated when the PWRBTN pin is set high (at least 2.3 V) for 1 to 10 milliseconds, so that AVDD starts to rise and reaches about 1.5 V. After the PWRBTN has given this initial start current, the regulators reach their default voltages even if the PWRBTN is released. VHIGH must be sufficiently (about 0.3 V) above the highest regulated power (normally AVDD) so that regulation can be properly performed.

The PWRBTN state can also be read by software, so it can be used as one of the user interface buttons.

A power-on reset monitors the core voltage and asserts reset if CVDD drops below the CMON level. It is also possible to force a reset by keeping PWRBTN pressed for longer than approximately 5.6 seconds. A watchdog counter and the XRESET pin can also generate a reset for the device.

Resets do not cause the regulators to shut down, but they restore the default regulator voltages. After boot the firmware and user software can change the voltages.

Return to power-off is possible only with active software control (VSDSP writes the regulator

shutdown bit), or when VHIGH voltage is removed for a sufficiently long time. In the default firmware player the power button has to be pressed for 2 seconds to make the software power-down the system and turn the regulators off.

6.2 Digital Section

Two of the regulators provide power supply for the digital section.

IOVDD is used for the level-shifters of the digital I/O and crystal oscillator. The IOVDD regulator output must be connected to IOVDD1 and IOVDD2 input pins, because they are not connected internally. Proper bypass capacitors should also be used.

The firmware uses GPIO0_7 to select I/O voltage level. After reset the I/O voltage is 1.8 V. If GPIO0_7 has a pull-down resistor, 1.8 V I/O voltage is used. If GPIO0_7 has a pull-up resistor, 3.3 V I/O voltage is used.

All other digital is powered from core voltage (CVDD). The core voltage is internally connected, and the CVDD pin should have a proper bypass capacitors.

Clock

The crystal amplifier uses a crystal connected to XTALI and XTALO. An external logic-level input clock can also be used. When VS1000 is used with USB, 12 MHz input clock must be used.

An internal phase-locked loop (PLL) generates the internal clock by multiplying the input clock by 1.0×, 1.5×, . . . , 4.0×. When USB is connected, the clock is 4.0×12 MHz = 48 MHz. When the player is active, the clock will be automatically changed according to the requirements of the song being played. The maximum clock in player mode is 3.5×12 MHz = 42 MHz. (Different voltage settings are used in player and USB modes.)

XRESET disables the clock buffer and puts the digital section into powerdown mode.

VSDSP^4

VSDSP^4 is VLSI Solution's proprietary digital signal processor with a 32-bit instruction word, two 16-bit data buses, and both 16-bit and 32/40-bit arithmetic.

IROM, XROM, and YROM contain the firmware, including the default player application. Most of the instruction RAM and some of the X and Y data RAM's can be used to customize and extend the functionality of the player.

UART

An asynchronous serial port is used for debugging and special applications. The default speed is 115200 bps. The UART operates in 8N1 mode (8 data bits, no parity, 1 stop bit). RX and TX pins can also be used for general-purpose I/O when the UART is not required.

SPI

A synchronous serial port peripheral is used for SPIEEPROM boot, and can be used to access other SPI peripherals (for example LCD or SED) by using another chip select. The SPI is only used for boot if the XCS pin has a high level after reset (pull-up resistor attached). These pins can also be used for general-purpose I/O when the SPI is not required.

The default player uses SI and SO for LED outputs.

NAND FLASH Interface

The NAND FLASH peripheral calculates a simple error-correcting code (ECC), and automates some of the communication with a NAND FLASH chip. The firmware uses the peripheral to access both small-page (512+16 B pages) and large-page (2048+64 B pages) NAND FLASH chips. The first sector in the FLASH tells the firmware how it should be accessed.

The NAND FLASH interface pins can also be used as general-purpose I/O. The default firmware uses GPIO0_[4:0] for keys, and GPIO0_[7:6] for other purposes. Pull-up and pull-down resistors must be used for these connections so that the data transfer to and from the NAND FLASH isn't disturbed when keys are pressed.

USB

The USB peripheral handles USB 1.1 Full Speed harware protocol. Low speed communication is not supported, but is correctly ignored. The USBP pin has a software-controllable 1.5kΩ pull-up.

A control endpoint (1 IN and 1 OUT) and up to 6 other endpoints (3 IN and 3 OUT) can be used simultaneously. Bulk, interrupt, and isochronous transfer modes are selectable for each endpoint. USB receive from USB host to device (OUT) uses a 2 KiB buffer, thus allowing very high transfer speeds. USB transmit from device to USB host (IN) also uses a 2 KiB buffer and allows all IN endpoints to be ready to transmit simultaneously. Double-buffering is also possible, but not usually required.

The firmware uses the USB peripheral to implement both USB Mass Storage Device and USB Audio Device. Which device is activated depends on the state of GPIO0_6 when the USB connection is detected. If GPIO0_6 has a pull-up resistor, VS1000 appears as an USB Audio Device. If GPIO0_6 has a pull-down resistor, VS1000 appears as an USB Mass Storage Device.

6.3 Analog Section

The third regulator provides power for the analog section.

The analog section consists of digital to analog converters and earphone driver. This includes a buffered common voltage generator (CBUF, around 1.2 V) that can be used as a virtual ground for headphones.

The AVDD regulator output pin must be connected to AVDD1..AVDD3 pins with proper bypass capacitors, because they are not connected internally.

The USB pins use the internal AVDD voltage, and the firmware configures AVDD to 3.6 V when USB is attached.

Low AVDD voltage can be monitored by software. Currently the firmware does not take advantage of this feature.

CBUF contains a short-circuit protection. It disconnects the CBUF driver if pin is shorted to ground. In practise this only happens with external power regulation, because there is a limit to how much power the internal regulators can provide.

6.3.1 Powering Up

In normal firmware operation the analog drivers are enabled only when the decoding of an audio file is started.

If the analog drivers are enabled without starting audio decoding, it is possible for the analog output to remain high or low until audio is output.

You can call the following function in your startup to force the outputs to the middle.

```
#include <vs1000.h>
#include <audio.h>
#include <string.h>
#include <player.h>
#include <codec.h>
#include <dev1000.h>

extern struct CodecServices cs;
void DACInit(void) {
    cs.sampleRate = 48000U;
    SetRate( (u_int16)cs.sampleRate );
    memset(tmpBuf, 24000, sizeof(tmpBuf));
    tmpBuf[7] = tmpBuf[6] = tmpBuf[3] = tmpBuf[2] = -24000;
    audioPtr.wr = (audioPtr.rd = audioBuffer) + 4;
    {
        int i;
        for (i=0;i<200;i++) {
            AudioOutputSamples(tmpBuf, 4);
        }
    }
}
```

7 Firmware Operation

The ROM firmware uses the following pins (see the example schematics in Section 5):

Pin	Description
PWRBTN	High level starts regulator, is also read as the Power button Key.
GPIO0_0	external 100 kΩ pull-down resistor, Key 1 connects a 10 kΩ pull-up resistor
GPIO0_1	external 100 kΩ pull-down resistor, Key 2 connects a 10 kΩ pull-up resistor
GPIO0_2	external 100 kΩ pull-down resistor, Key 3 connects a 10 kΩ pull-up resistor
GPIO0_3	external 100 kΩ pull-down resistor, Key 4 connects a 10 kΩ pull-up resistor
GPIO0_4	external 100 kΩ pull-down resistor, Key 5 connects a 10 kΩ pull-up resistor
GPIO0_6	external pull-down resistor for USB Mass Storage Device, pull-up for USB Audio Device
GPIO0_7	external pull-down resistor for 1.8 V I/O voltage, pull-up resistor for 3.3 V I/O voltage
NFCE	external pull-up resistor for normal operation, pull-down to use RAM disk for UMS Device
NFRDY	external 10 kΩ pull-up resistor
XCS	external pull-up to enable SPI EEPROM boot, pull-down to disable
SI	Power LED control during firmware operation
SO	Feature LED control during firmware operation
USBN	external 1 MΩ pull-up resistor
USBP	external 1 MΩ pull-up resistor

Boot order:

Stage	Description
Power on	Power button (PWRBTN) pressed when VHIGH has enough voltage
Reset	Power-on reset, XRESET, or watchdog reset causes software restart
UART Boot	Almost immediately after power-on UART can be used to enter emulator mode.
SPI EEPROM Boot	If XCS is high, SPI Boot is tried.
NAND FLASH probed	If NFCE is high, NAND FLASH is checked using 660 ns read/write low time.
Default firmware	The firmware in ROM takes control.

7.1 SPI Boot

The first boot method is SPI EEPROM. If GPIO1_0 is low after reset, SPI boot is skipped. If GPIO1_0 is high, it is assumed to have a pull-up resistor and SPI boot is tried.

First the first four bytes of the SPI EEPROM are read using 16-bit address. If the bytes are “VLSI”, a 16-bit EEPROM is assumed and the boot continues. If the last 3 bytes are read as “VLS”, a 24-bit EEPROM is assumed and boot continues in 24-bit mode. Both 16-bit and 24-bit EEPROM should have the “VLSI” string starting at address 0, and the rest of the boot data starting at address 4. If no identifier is found, SPI EEPROM boot is skipped.

Boot records are read from EEPROM until an execute record is reached. Unknown records are skipped using the data length field.

Byte	Description
0	type 0=I-mem 1=X-mem 2=Y-mem 3=execute
1,2	data len lo, hi – data length in bytes
3, 4	address lo, hi – record address
5..	data*

7.2 NAND FLASH Probe

If NAND FLASH chip select (NFCE) is high, a NAND FLASH is assumed to be present and the first sector is read. The access methods (nandTypes 0..5) are tried in order to find the "VLSI" identification. If the first bytes are "VLSI", a valid boot sector is assumed. This sector gives the necessary information about the NAND FLASH so that it can be accessed in the right way.

Byte	Value	Description
0,1,2,3	0x56 0x4c 0x53 0x49	'V' 'L' 'S' 'I' – Identification
4,5	0x00 0x03	nandType (0x0003 = large-page with 3-byte block address)
6	0x08	blockSizeBits ($2^8 * 512$ = 128 KiB per block)
7	0x13	flashSizeBits ($2^{19} * 512$ = 256 MiB flash)
8,9	0x00 0x46	nandWaitNs – NAND FLASH access time in ns
10,11	0x00 0x01	number of extra blocks for boot (example: 0x0001)
12,13,14,15	0x42 0x6f 0x4f 0x74	'B' 'o' 'O' 't' – Optional boot ident
16...511		code

NandType	Description
0	512+16 B small-page flash with 2-byte block address ($\leq$ 32 MiB)
1	2048+64 B large-page flash with 2-byte block address ($\leq$ 128 MiB)
2	512+16 B small-page flash with 3-byte block address ($>$ 32 MiB, $\leq$ 8 GiB)
3	2048+64 B large-page flash with 3-byte block address ($>$ 128 MiB, $\leq$ 32 GiB)
4	512+16 B small-page flash with 4-byte block address ($>$ 8 GiB)
5	2048+64 B large-page flash with 4-byte block address ($>$ 32 GiB)

If bytes 12-15 contain "BoOt", the value in bytes 10 and 11 determines how many sectors are read from NAND-flash. Value 1 means two 512-byte sectors are read, value 0 means only the first block is needed. After the data is read into memory, the boot records in this data are processed, transferring code and data sections into the right places in memory and possibly executed. If an unknown boot record is encountered, the booting is stopped and control returns to the firmware code.

Word	Description
0	type 0x8000=I-mem 0x8001=X-mem 0x8002=Y-mem 0x8003=execute
1	data length in words -1 – 0 = 1 word, 1 = 2 words, etc.
2	address – record address
3..	data

Note: In VS1000a you can not have Y-memory records.
Note: In VS1000b/c/d you need one filler word after each Y-memory record.

If NFCE is low during boot, or an uninitialized NAND FLASH is connected, the NAND FLASH type is set to 0xffff, and a RAM disk is initialized when USB is attached. In this mode you can drop a boot file named `VS1000_B.RUN` into the disk and it will be run when the USB is disconnected. This way you can easily program a player that has an uninitialized NAND FLASH or SPI EEPROM.

7.3 UART Boot/Monitor

When byte 0xef is sent to RX at 115200 bps, the firmware enters monitor mode and communicates with **vs3emu**. Memory contents can be displayed, executables can be loaded and run, or the firmware code can be restarted or continued.

The UART is also a convenient way to program the NAND FLASH boot sector(s) or the SPI EEPROM.

7.4 Default Firmware Features

The following lists the normal operation of the ROM firmware. In most applications you would have your own customized firmware which is loaded from SPI FLASH or NAND FLASH. For more information about firmware development refer to VS1000 Programmer's Guide and the VSDSP Forum at http://www.vsdsp-forum.com/ .

7.4.1 USB Mass Storage and Audio Device

When USB cable insertion is detected by the firmware, playing of the current file is stopped and USB handling code is started. The internal clock is configured to 4.0× 12 MHz = 48 MHz, the analog power is configured to 3.6 V, the USB peripheral is initialized, and the USB pull-up resistor is enabled.

If GPIO0_6 has a pull-up resistor, VS1000 appears as an USB Audio Device. If GPIO0_6 has a pull-down resistor, VS1000 appears as an USB Mass Storage Device.

If during power-on the NAND FLASH contained a valid boot sector, the NAND FLASH disk will be used with the mass storage device. The NAND FLASH disk requires a filesystem-level formatting before it can be used. If NFCE had a pull-down instead of pull-up, or if a valid boot sector was not found, a RAM disk is used instead.

The RAM disk is preformatted and can be used immediately, but it does not retain its contents between USB detachment and insertion. The RAM disk is only intended for loading software through USB. You can copy a file **VS1000_B.RUN** to RAM disk and it will be automatically run when you disconnect the USB cable. This mechanism can be used to program the NAND FLASH boot sector (perhaps containing custom boot code), and also for programming a SPI EEPROM in case NAND FLASH is not used in the application.

7.4.2 Default Player Application

When the USB cable is detached, the contents of the disk is checked. If the disk seems to contain a FAT16 or FAT32 filesystem, a cleanup of unused sectors is performed. The cleanup makes the disk perform faster the next time something is written on it. If a full disk has been formatted or emptied, this cleanup can take considerable time, even 30 seconds or more. After the cleanup is finished the player starts to play files.

Note: normally Windows formats smaller than about 16 MB disks as FAT12. The player has only partial support for FAT12 disks: no cleanup is performed, subdirectories are not allowed, and files are assumed not to be fragmented. If disks as small as or smaller than this are required, it is possible to format them as FAT16 with the following command. `format e: /A:512 /FS:FAT`

The default player application only decodes Ogg Vorbis files, but it can be extended to allow some simple codecs, like a WAV decoder.

In addition to the power button, 5 keys are connected to GPIO0_[4:0] so that they connect a 10 kΩ pull-up to the I/O when the button is pressed, and 100 kΩ pull-downs keep the lines low otherwise. The resistors are needed because these lines are also used for NAND FLASH communication. The keys are read approximately 16 times per second.

The key control can be changed by replacing the default key mapping table. The default user interface uses six buttons.

Button	Short Press $<$ 1 second	Long Press $\geq$ 1 second
POWER	Power On, Pause / Play	Power off (pressed for 2 seconds)
KEY1	Volume Down	Volume Down
KEY2	Volume Up	Volume Up
KEY3	Previous	Rewind
KEY4	Next	Fast Forward
KEY5	EarSpeaker	Random On / Off

Power Button

A press of the power button turns on the system. After boot the power LED (the LED connected to SI) is turned on. After the startup a short press of the power button toggles between pause and play modes. In pause mode the power LED flashes. After a few seconds of pause mode the system enters low-power pause mode automatically. When the power button is pressed for 2 seconds, the system powers down.

Volume Buttons

Volume can be turned up or down with 0.5 dB steps using the volume buttons. A short press changes the volume by 0.5 dB, a long press will change the volume by approximately 8 dB every second.

Previous / Next Buttons

A song can be changed using the previous and next buttons. A short press of the *previous* button will restart the song if it has been played for at least 5 seconds, and go to the previous song otherwise. A short press of the *next* button goes to the next song. A long press of *previous* or *next* will rewind and fast forward the song, respectively.

Feature Button

The sixth button controls two features: the EarSpeaker spatial processing and the random play function. A long press of the *feature* button toggles the random play function. When random play becomes activated, a new song is automatically randomly selected. When random play mode is active, the feature LED (the LED connected to SO) will light up. A short press of the *feature* button will select between four EarSpeaker modes: *off*, *minimal*, *normal*, and *extreme*.

7.5 Supported Audio Codecs

7.5.1 Supported Ogg Vorbis Formats

Parameter	Min	Max	Unit
Channels	1	2	
Window size	64	4096	samples
Sample rate		48000	Hz
Bit rate		500	kbit/s

Maximum window size for an Ogg Vorbis file is 8192, however only window sizes up to 4096 are in active use with sample rates not exceeding 48 kHz.

With USB (12 MHz clock) sample rates above 46875 Hz are played back at 46875 Hz. There are no sample rate restrictions for lower sample rates: non-standard sample rates can be played back without a performance penalty.

Only floor 1 is supported. No known current encoder uses floor 0.

All one- and two-channel Ogg Vorbis files within the restrictions above should be playable with this decoder.

Ogg Vorbis decoding supports Replay Gain technology. If the decoder finds a Replay Gain tag in the song header, the tag is parsed and the player software uses it to adjust the sound level. For a song without any Replay Gain tag, a default of -6 dB is used. For more details about Replay Gain, see http://en.wikipedia.org/wiki/Replay_Gain and *http://www.replaygain.org/*.

7.5.2 Additional Formats

VS1000 Developer library contains a simple WAV decoder, which can be easily included into your own applications. Currently the WAV decoder supports 8-bit ulaw, 8-bit linear PCM, and 16-bit linear PCM formats.

7.6 EarSpeaker Spatial Processing

While listening to headphones the sound has a tendency to be localized inside the head. The sound field becomes flat and lacking a sensation of dimensions. This is an unnatural, awkward and sometimes even disturbing situation. This phenomenon is often referred in literature as 'lateralization', meaning 'in-the-head' localization. Long-term listening to lateralized sound may lead to listening fatigue.

All real-life sound sources are external, leaving traces of the acoustic wavefront that arrives to the ear drums. From these traces, the auditory system in the brain is able to judge the distance and angle of each sound source. In loudspeaker listening the sound is external and these traces are available. In headphone listening these traces are missing or ambiguous.

The EarSpeaker processing makes listening via headphones more like listening to the same music from real loudspeakers or live. Once EarSpeaker processing is activated, the instruments are moved from inside to the outside of the head, making it easier to separate different instruments (see Figure 7). The listening experience becomes more natural and pleasant, and the stereo image is sharper as the instruments are widely in front of the listener instead of being inside the head.

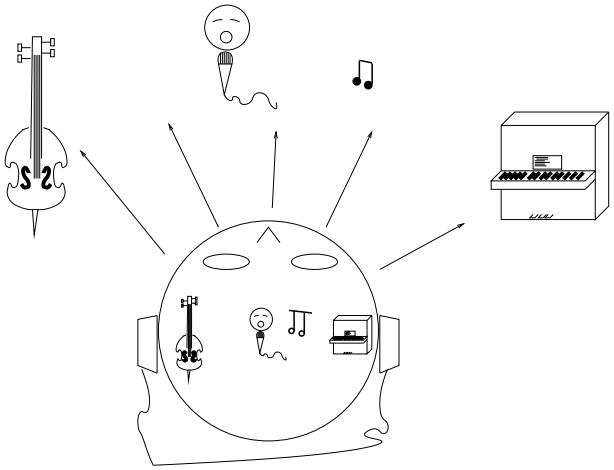


Figure 7: EarSpeaker externalized sound sources vs. normal inside-the-head sound.

Note that EarSpeaker differs from any common spatial processing effects, such as echo, reverb, or bass boost. EarSpeaker accurately simulates the human auditory model and real listening environment acoustics. Thus it does not change the tonal character of the music by introducing artificial effects.

EarSpeaker processing can be parameterized to a few different modes, each simulating a little different type of an acoustical situation and suiting different personal preferences as well as different types of recording.

- *Off*: Best option when listening through loudspeakers or if the audio to be played contains binaural preprocessing
- *Minimal*: Listening to normal musical scores with headphones, very subtle
- *Normal*: Listening to normal musical scores with headphones, moves sound source further than *minimal*
- *Extreme*: Old or 'dry' recordings, or if the audio to be played is artificial

8 VS1000 Errata

This chapter describes the known problems with different VS1000 revisions. Most of the problems are correctable with user code that is loaded to IRAM.

VS1000b Changes

- NAND FLASH and Ramdisk boot can have initialized Y data.
- EarSpeaker initialization fixed, EarSpeaker optimized from 12 MHz to 10 MHz (at 44.1 kHz).
- Small power-on click removed.
- User interface works even if there is no filesystem. (You can turn the power off.)
- NAND FLASH boot handles larger than 512-byte programs without a chain-loader routine (up to 8176 bytes). Ramdisk boot (VS1000_B.RUN) handles larger than 512-byte programs (up to 8192 bytes).
- When attached to USB, LED is flashed when there is read/write activity. LED is turned off when the file system has been flushed.
- Volume is always initialized, USB Audio Device can be powered on while attached to USB (powered from VBUS).
- USB Suspend + Resume are implemented (but need user tuning).
- Vorbis: Now uses adaptive accuracy for windowing, implements fast play mode, and has better synchronization after non-fatal errors. Replay gain has been fixed.
- Player: Fast play mode is used for better-sounding fast forward. Fast forward speeds up when the ff button is kept pressed. Player uses the suspend routine to implement low-power pause mode. Timeout turns the unit off after being 5 minutes in pause mode. The default maximum clock in player mode is 3.5×.
- Some new IRAM hooks: KeyEventHandler, MassStorage, USBSuspend, InitUSBDescriptors.

VS1000c Changes

- No changes. Has the same firmware as version B.

VS1000b/c Errata

- NAND FLASH and Ramdisk boot needs one filler word after every Y data record.
- BusyWait1() wait time equals BusyWait10() time.
- SCSI limited to 23-bit block address (4GB).
- File scan gets stuck if FAT12 disk has subdirectories. FAT12 is not used if disk is $>$ 16MB.

VS1000d Changes

- **Is backwards compatible with existing code, so can be used as a direct replacement for VS1000b/c.**
- **Code can be loaded and executed when in RAM disk mode without detaching the device.**
- Default 3 V IO voltage setting reduced from 3.6 V to 3.3 V (control value 31 to 27).
- SCSI supports the full 32-bit block address (2048GB).
- BusyWait1() now waits 1 ms at 12 MHz clock.
- Time to enter low-power pause mode doubled.
- Ignores subdirectories in FAT12 disks.
- RAMDISK label changed to VS1000D_RAM to make it possible to detect VS1000d.
- USB descriptors, including device ID is the same as with VS1000b.
- Fixed-width Latin-1 font (7x8 pixels) and 8-bit bit-reverse table added to YROM.

9 Document Version Changes

This chapter describes the latest and most important changes to this document.

Version 1.51, 2019-03-15

- Updated Chapter 2, *Definitions*.
- Increased the minimum required level for powerbutton pulse, section 3.7. No change to the suggested component values.

Version 1.5, 2016-06-09

- Added mention of 8N1 format to Chapter 6.2, *Digital Section*.
- Added Max limit to the Power Button activation threshold in Section 3.7.
- Added separate limits for voltages and clock in USB mode in Section 3.
- Added section about analog output startup in Section 6.3.1.
- Added a section 3.8 about power-on reset.
- Updated example schematics 5 to include capacitor in xRESET.

Version 1.44, 2014-12-19

- Updated telephone number in Chapter 10, *Contact Information*.

Version 1.43 for VS1000d, 2013-05-28

- Clarification to PWRBTN maximum voltage (IOVDD+0.3V).
- Updated the example schematics in Section 5, Figure 5.

Version 1.42 for VS1000d, 2013-05-15

- GPIO1_4 and GPIO1_5 fixed in the chip symbol on the front page.

Version 1.41 for VS1000d, 2012-04-04

- Added Section 3.7, Power Button Characteristics.

Version 1.4 for VS1000d, 2011-10-06

- Fixed VS1000 symbol in the first page (RX is GPIO1_5).
- Changed the suggested key pull-up and pull-down resistor values to 100 kΩ / 10 kΩ in Section 5.

Version 1.3 for VS1000d, 2008-05-14

- Added VS1000d changes and removed VS1000A errata.

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