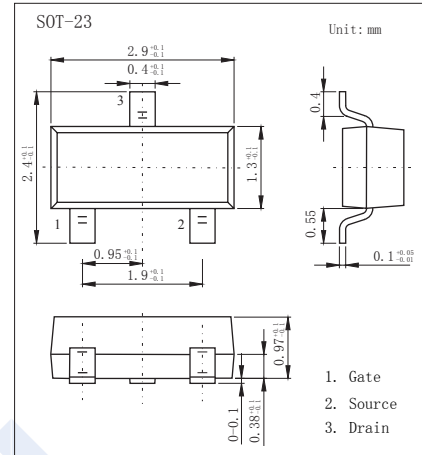
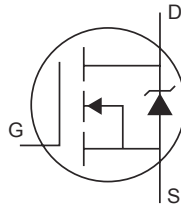


## N-Channel MOSFET

### IRLML2402 (KRIML2402)

#### ■ Features

- $V_{DS} (V) = 20V$
- $I_D = 1.2 A (V_{GS} = 4.5V)$
- $R_{DS(ON)} < 250m\Omega (V_{GS} = 4.5V)$
- $R_{DS(ON)} < 350m\Omega (V_{GS} = 2.7V)$



#### ■ Absolute Maximum Ratings $T_a = 25^\circ C$

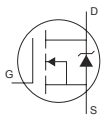
Parameter	Symbol	Rating	Unit	
Drain-Source Voltage	$V_{DS}$	20	V	
Gate-Source Voltage	$V_{GS}$	$\pm 12$		
Continuous Drain Current	$I_D$	$T_A=25^\circ C$	1.2	A
		$T_A=70^\circ C$	0.95	
Pulsed Drain Current	$I_{DM}$	7.4		
Power Dissipation	$P_D$	540	mW	
Linear Derating Factor		4.3	mW/ $^\circ C$	
Peak Diode Recovery $dv/dt$ (Note.1)	$dv/dt$	5	V/ns	
Thermal Resistance Junction- to-Ambient	$R_{thJA}$	230	$^\circ C/W$	
Junction Temperature	$T_J$	150	$^\circ C$	
Storage Temperature Range	$T_{stg}$	-55 to 150		

Note.1:  $I_{SD} \leq 0.93A$ ,  $di/dt \leq 90A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 150^\circ C$

## N-Channel MOSFET

### IRLML2402 (KRIML2402)

#### ■ Electrical Characteristics $T_a = 25^\circ\text{C}$

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{DS}$	$I_D=250\ \mu\text{A}$ , $V_{GS}=0\text{V}$	20			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=16\text{V}$ , $V_{GS}=0\text{V}$			1	$\mu\text{A}$
		$V_{DS}=16\text{V}$ , $V_{GS}=0\text{V}$ , $T_J=125^\circ\text{C}$			25	
Gate-Body Leakage Current	$I_{GSS}$	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 12\text{V}$			$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_D=250\ \mu\text{A}$	0.7		1.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{V}$ , $I_D=0.93\text{A}$ (Note.1)			250	m $\Omega$
		$V_{GS}=2.7\text{V}$ , $I_D=0.47\text{A}$ (Note.1)			350	
Forward Transconductance	$g_{FS}$	$V_{DS}=10\text{V}$ , $I_D=0.47\text{A}$	1.3			S
Input Capacitance	$C_{iss}$	$V_{GS}=0\text{V}$ , $V_{DS}=15\text{V}$ , $f=1\text{MHz}$		110		pF
Output Capacitance	$C_{oss}$			51		
Reverse Transfer Capacitance	$C_{rss}$			25		
Total Gate Charge	$Q_g$	$V_{GS}=16\text{V}$ , $V_{DS}=4.5\text{V}$ , $I_D=0.93\text{A}$ (Note.1)		2.6	3.9	nC
Gate Source Charge	$Q_{gs}$			0.41	0.62	
Gate Drain Charge	$Q_{gd}$			1.1	1.7	
Turn-On DelayTime	$t_{d(on)}$	$V_{DS}=10\text{V}$ , $I_D=0.93\text{A}$ , $R_D=11\ \Omega$ , $R_G=6.2\ \Omega$ (Note.1)		2.5		ns
Turn-On Rise Time	$t_r$			9.5		
Turn-Off DelayTime	$t_{d(off)}$			9.7		
Turn-Off Fall Time	$t_f$			4.8		
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F=0.93\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$ , $T_J=25^\circ\text{C}$ (Note.1)		25	38	nC
Body Diode Reverse Recovery Charge	$Q_{rr}$			16	24	
Maximum Body-Diode Continuous Current	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode. 			0.54	A
Pulse Source Current (Body Diode)	$I_{SM}$				7.4	
Diode Forward Voltage	$V_{SD}$	$I_S=0.93\text{A}$ , $V_{GS}=0\text{V}$ , $T_J=25^\circ\text{C}$ (Note.1)			1.2	V

Note.1: Pulse width  $\leq 300\ \mu\text{s}$ ; duty cycle  $\leq 2\%$ .

#### ■ Marking

Marking	1A**
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## N-Channel MOSFET IRLML2402 (KRIML2402)

■ Typical Characteristics

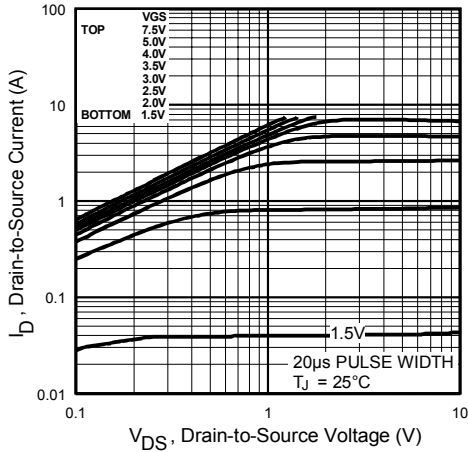


Fig 1. Typical Output Characteristics

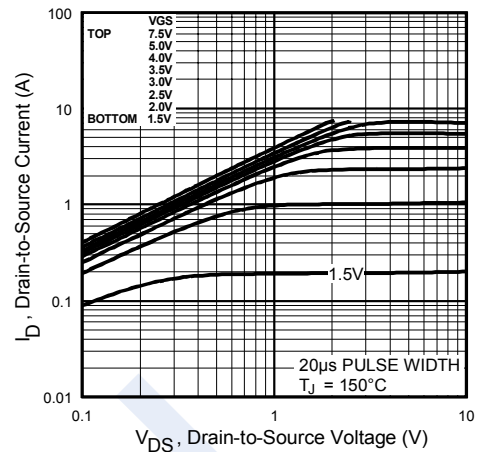


Fig 2. Typical Output Characteristics

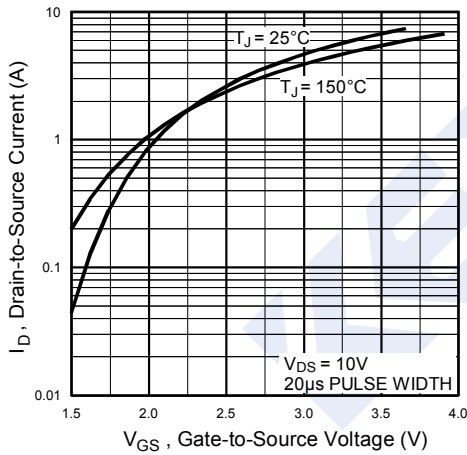


Fig 3. Typical Transfer Characteristics

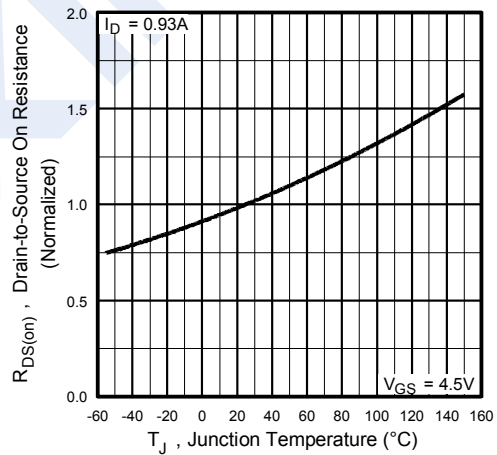


Fig 4. Normalized On-Resistance Vs. Temperature

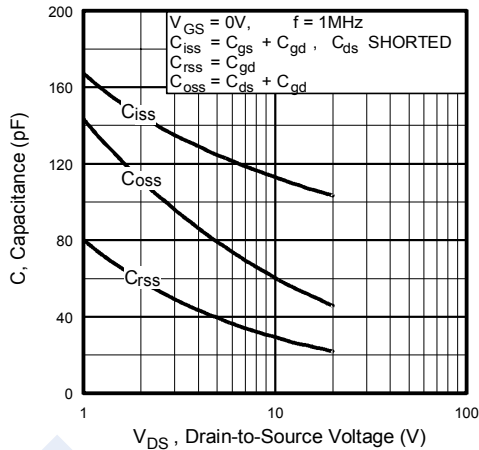


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

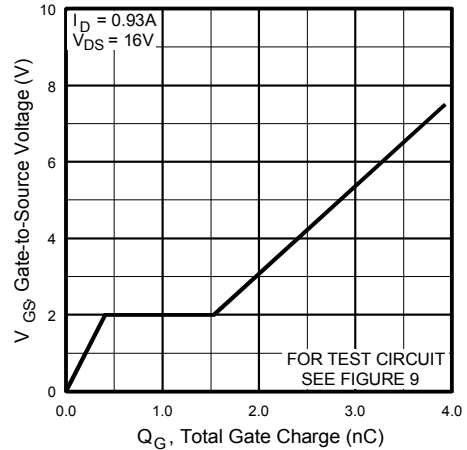


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

## N-Channel MOSFET IRLML2402 (KRIML2402)

■ Typical Characteristics

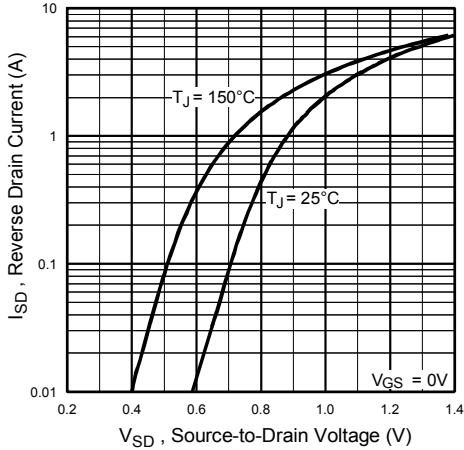


Fig 7. Typical Source-Drain Diode Forward Voltage

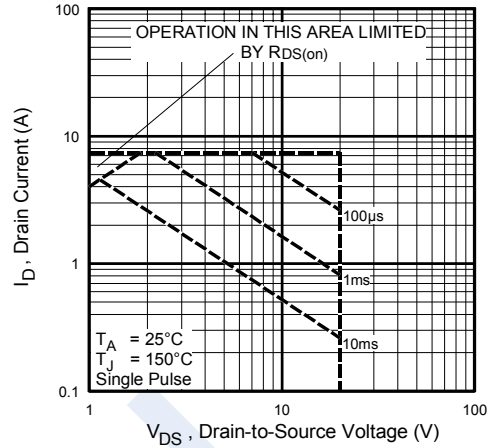


Fig 8. Maximum Safe Operating Area

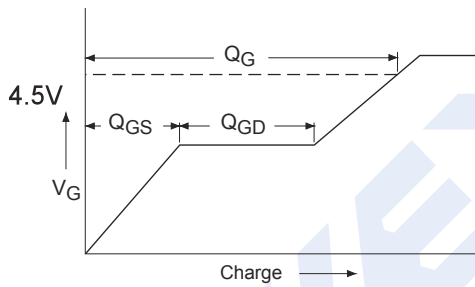


Fig 9a. Basic Gate Charge Waveform

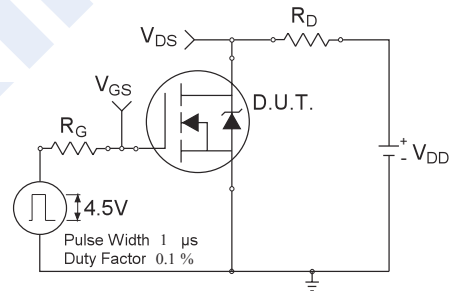


Fig 10a. Switching Time Test Circuit

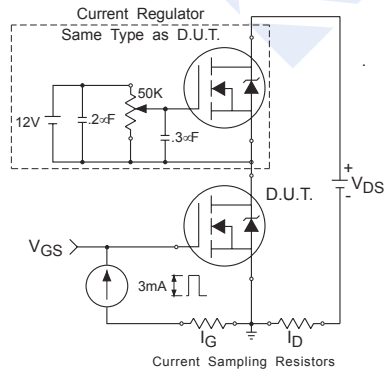


Fig 9b. Gate Charge Test Circuit

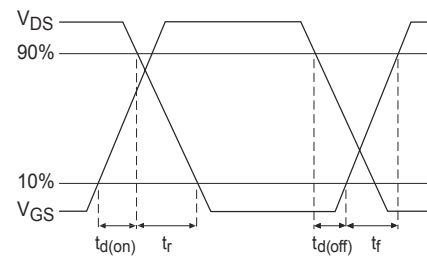


Fig 10b. Switching Time Waveforms

## N-Channel MOSFET IRLML2402 (KRIML2402)

■ Typical Characteristics

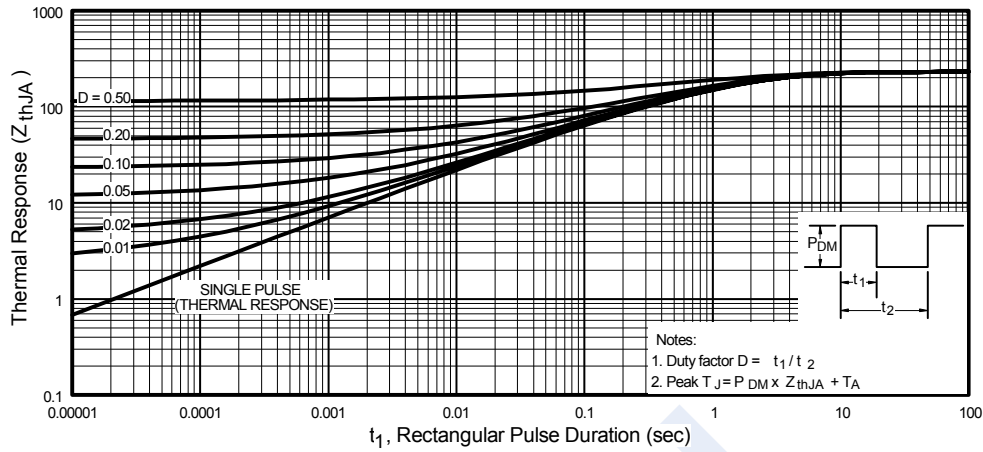
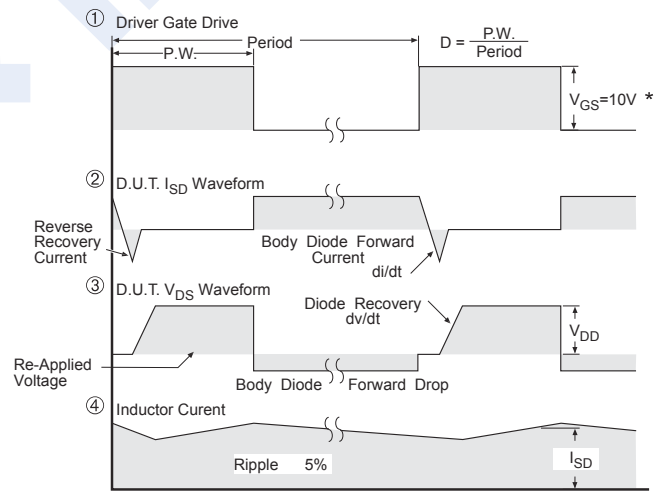
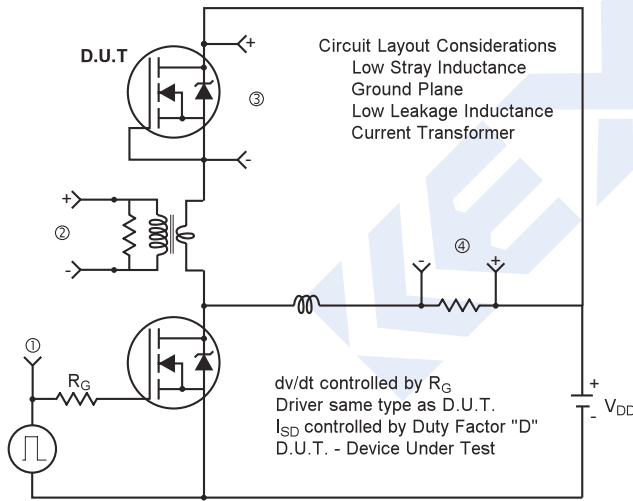


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

### Peak Diode Recovery $dv/dt$ Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

Fig 12. For N-Channel HEXFETS