TQL9066

50 – 1500 MHz Dual LNA

16-pin 4x4 mm QFN Package

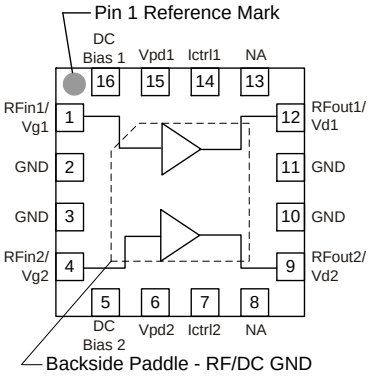
General Description

The TQL9066 is a high linearity, ultra-low noise figure dual device amplifier in a 4x4 mm package. At 830 MHz in a balanced configuration, the LNA provides 18.4 dB gain, 22 dBm IIP3 and 0.62 dB noise figure. The part does not require a negative supply for operation and is bias adjustable for both drain current and voltage. The device is housed in a green/RoHS-compliant industry standard QFN package.

The TQL9066 consists of a single monolithic GaAs E-pHEMT die and integrates bias circuitry as well as shut-down capability allowing the LNA to be useful for both FDD and TDD applications.

The TQL9066 is optimized for the 700−1000 MHz band, but can be used outside of the band. TriQuint offers pin-compatible dual LNAs for the 1.5−2.3 GHz band (TQP3M9040) and 2.3−4.0 GHz (TQP3M9041). The balanced amplifier is optimized for high performance receivers in wireless infrastructure and can be used for base-station transceivers or tower-mounted amplifiers.

Functional Block Diagram



Product Features

- 0.62 dB NF (Balanced configuration) at 830 MHz
- 50−1500 MHz Operational bandwidth
- 18.4 dB Gain at 830 MHz
- +22 dBm Input IP3
- -35 dB Reverse Isolation
- Integrated shut-down biasing feature
- Bias adjustable
- Does not require negative voltage supply
- 4x4 mm 16-pin QFN plastic package

Applications

- Base Station Receivers
- Tower Mount Amplifiers
- Balanced Amplifiers
- Defense Communications

Ordering Information

Part No.	Description
TQL9066	50−1500 MHz Dual LNA
TQL9066-PCB	700−1000 MHz Evaluation Board

Standard T/R size = 2500 pieces on a 13” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65 to 150°C
Drain Voltage (V_d)	+7 V
I_{dd} (V_d = 5V) per channel	300 mA
Input Power (CW)	+22 dBm
Input Power (CW, DC off condition)	+22 dBm
Input Power (DC off condition & 10% Duty Cycle)	+30 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{pd}	0		+5	V
V_g	0	+0.5	+1	V
V_d	+2		+5	V
I_d, single channel		57	85	mA
Operating Temp. Range	−40		+105	°C
T_{ch} (for>10^6 hrs MTTF)			190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_d = +4.35 V, Temp.=+25°C, tuned balanced configuration. NF is de-embedded to the input of the input hybrid coupler.

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		50		1500	MHz
Test Frequency			830		MHz
Gain		17.9	19	20.3	dB
Output P1dB			+21.4		dBm
Input IP3	Pin=−13 dBm/tone, Δf=1 MHz	+17	+22		dBm
Output IP3	Pout=+5 dBm/tone, Δf=1 MHz		+40		dBm
Noise Figure	Balanced configuration		0.62	0.95	dB
Reverse Isolation, S12			-35		dB
Drain Voltage, V_d			+4.35		V
Drain Current, I_d	Single Channel	40	55	85	mA
Power Down Control Voltage, V_{pd}[1]	On-State	0		+0.3	V
	Off-State	+2.1		V_d	V
Thermal Resistance, θ_{jc}	Channel to case - per channel		53.4		°C/W

Notes: This voltage is references to the turret labeled Vpd1, Vpd2 on the evaluation board turret as shown on page 3.

S-Parameters

Test Conditions: V_{DD}=+4.35 V, I_{DD}=55 mA (typ.), T=+25°C, unmatched 50 ohm system, calibrated to device leads

Freq (GHz)	S11 (mag)	S11 (ang)	S21 (mag)	S21 (ang)	S12 (mag)	S12 (ang)	S22 (mag)	S22 (ang)
0.63	0.79337	-12.900	8.26522	90.261	0.01148	75.844	0.92636	-12.494
0.68	0.79442	-13.874	7.74829	88.361	0.01248	75.711	0.92606	-13.755
0.73	0.79277	-14.172	7.26533	86.104	0.01339	75.404	0.92339	-15.078
0.78	0.78648	-15.172	6.84091	84.470	0.01432	75.284	0.92274	-16.327
0.83	0.79306	-15.631	6.49595	82.537	0.01531	74.926	0.92335	-17.625
0.88	0.78059	-16.375	6.14597	80.813	0.01622	74.516	0.92385	-18.774
0.93	0.78969	-17.284	5.88192	79.116	0.01727	74.219	0.92328	-20.130
0.98	0.78116	-17.695	5.59921	77.274	0.01820	73.540	0.92190	-21.322
1.03	0.78332	-18.899	5.36480	75.909	0.01920	73.430	0.91992	-22.552
1.08	0.78317	-19.210	5.15505	74.048	0.02024	72.645	0.92047	-23.861
1.13	0.77558	-20.396	4.95617	72.708	0.02126	72.415	0.92067	-24.977
1.18	0.78385	-20.946	4.79515	70.912	0.02239	71.594	0.91905	-26.433
1.23	0.77114	-21.773	4.61128	69.304	0.02335	71.051	0.91742	-27.760
1.28	0.78121	-22.803	4.47997	67.885	0.02451	70.482	0.91527	-29.220
1.33	0.77214	-23.231	4.32752	66.119	0.02555	69.734	0.91543	-30.654
1.38	0.77461	-24.510	4.20926	64.759	0.02670	69.193	0.91419	-32.037

Note: Single Ended Configuration.

Noise Parameters

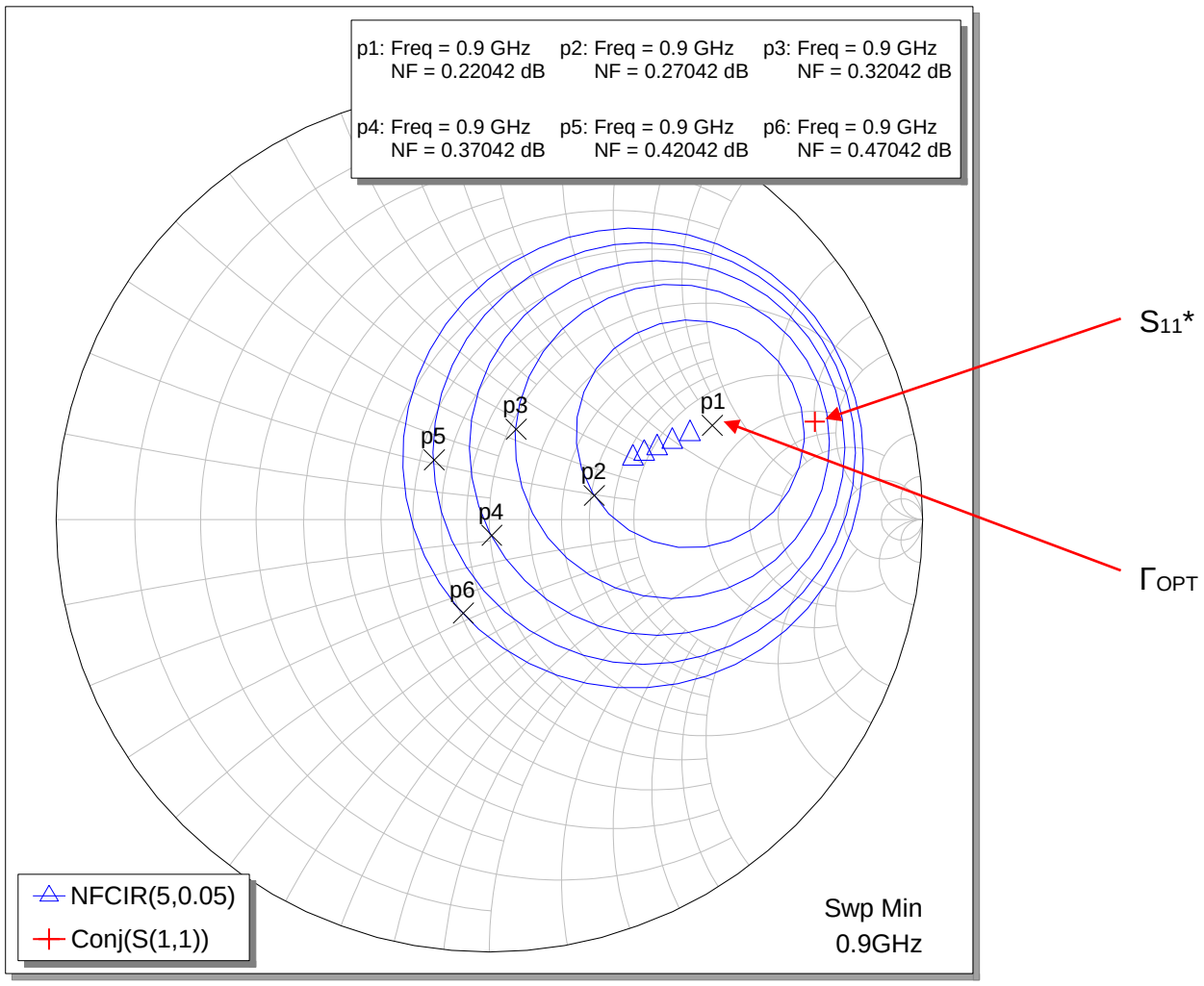
Test Conditions: V_{DD}=+4.35 V, I_{DD}=55 mA (typ.), T=+25°C, unmatched 50 ohm system, calibrated to device leads

Freq (GHz)	NF_{min} (dB)	MagOpt (mag)	AngOpt (deg)	Rn (Ω)
0.63	0.18904	0.68290	20.6785	0.06298
0.68	0.15268	0.60214	18.3406	0.06813
0.73	0.13607	0.59945	22.8778	0.06129
0.78	0.14421	0.61001	20.4961	0.06111
0.83	0.18132	0.56081	19.4236	0.06567
0.88	0.22549	0.58780	24.7523	0.06571
0.93	0.21280	0.51434	20.6518	0.06780
0.98	0.22103	0.55135	24.4779	0.05977
1.03	0.22786	0.51948	22.6357	0.06729
1.08	0.24764	0.49175	23.1648	0.06989
1.13	0.22524	0.48301	25.1937	0.06393
1.18	0.22329	0.44584	25.1826	0.06376
1.23	0.23666	0.46800	28.0534	0.06793
1.28	0.25239	0.44915	22.6713	0.06323
1.33	0.23498	0.40194	29.8884	0.06239
1.38	0.22454	0.42934	25.3527	0.07558

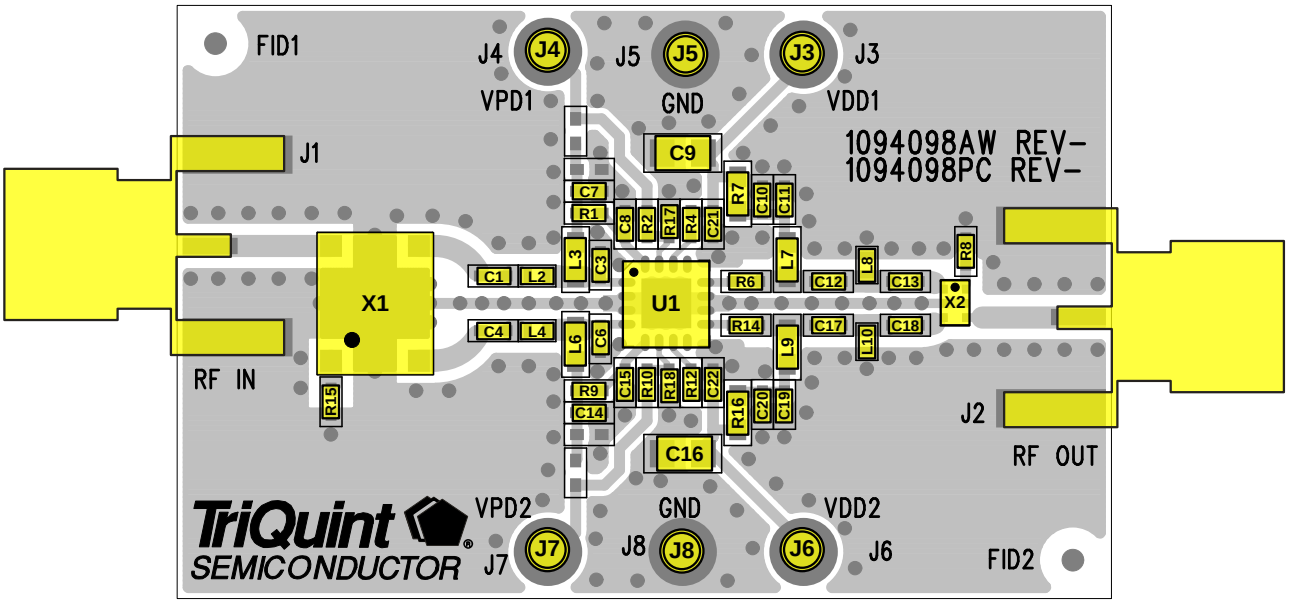
Note: Single Ended Configuration.

Noise Figure Circles at 900 MHz

Noise parameter measurements taken at the package pin reference plane. The gate and drain are biased externally through bias-tees. The achievable NFmin will worsen with on board non-ideal bias circuit.



TQL9066-PCB Evaluation Board Layout

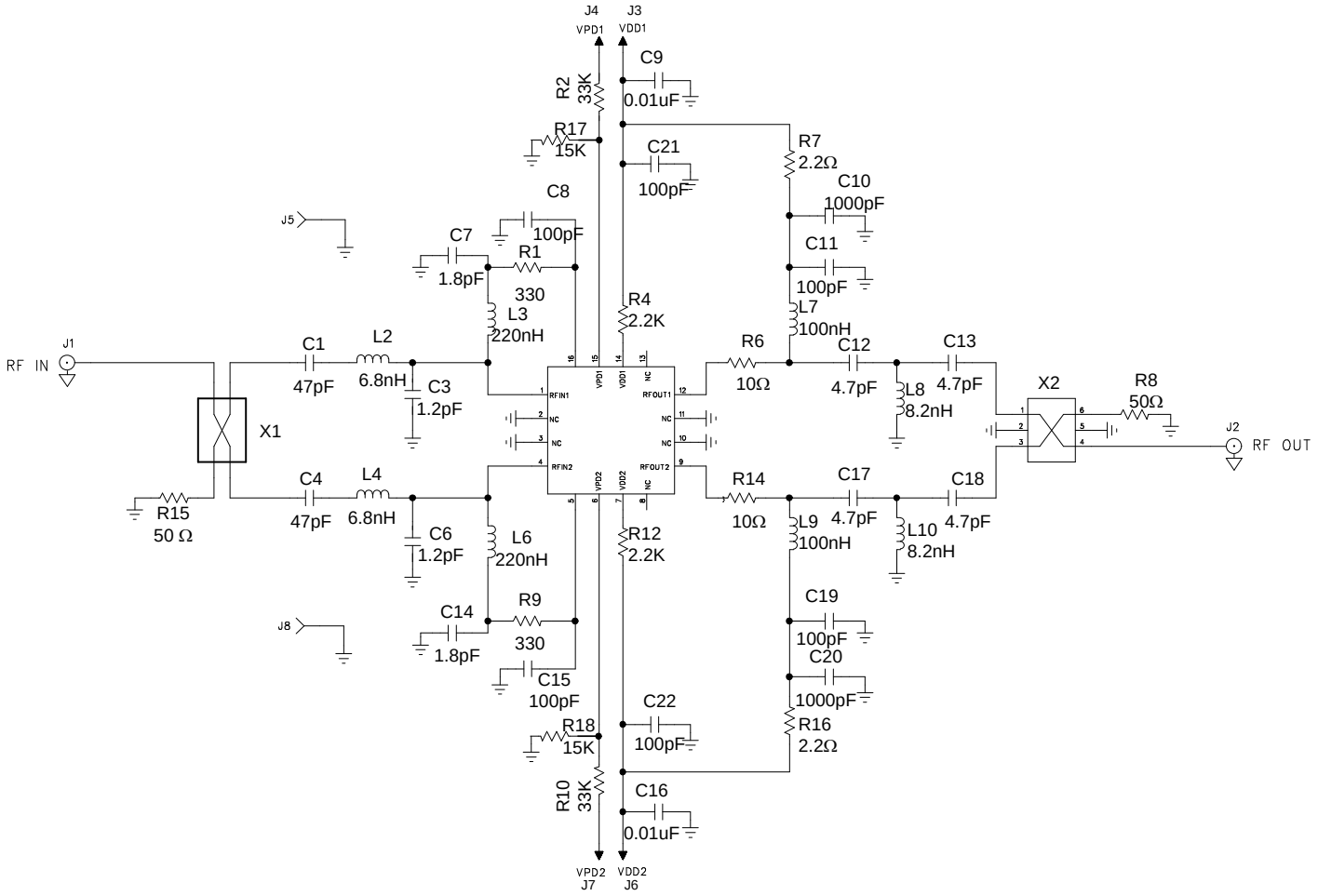


See Evaluation Board PCB Information section for PCB material and stack-up.

Bill of Material – TQL9066-PCB

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a	Dual LNA	TriQuint	TQL9066
X1	n/a	Hybrid coupler	Anaren	X3C09P1-03S
X2	n/a	Hybrid coupler	Anaren	C0810J5003AHF
R1, R9	330 Ω	RES, 0402, +/-5%, 1/16W	Various	
R8, R15	51 Ω	RES, 0402, +/-5%, 1/16W	Various	
R6, R14	10 Ω	RES, 0402, +/-5%, 1/16W	Various	
R4, R12	2.2K Ω	RES, 0402, +/-5%, 1/16W	Various	
R7, R16	2.2 Ω	RES, 0603, +/-5%, 1/8W	Various	
R17, R18	15K Ω	RES, 0402, +/-5%, 1/16W	Various	
R2, R10	33K Ω	RES, 0402, +/-5%, 1/10W	Various	
C1, C4	47 pF	CAP, 0402, +/-5%, 50V	Panasonic	ECJ-0EC1H470J
C3, C6	1.2 pF	CAP, 0402, +/-0.1pF, 25V	Panasonic	ECD-G0E1R2B
C7, C14	1.8 pF	CAP, 0402, +/-0.1pF, 50V	AVX	04025U1R8BAT2A
C8, C15, C21, C22, C11, C19	100 pF	CAP, 0402, +/-5%, 50V	Panasonic	ECJ-0EC1H101J
C9, C16	0.01 uF	CAP, 0805, +/-5%, 50V, X7R	Various	
C10, C20	1000 pF	CAP, 0402, +/-10%, 50V	Various	
C12, C13, C17, C18	4.7 pF	CAP, 0402, +/-0.1pF, 50V	AVX	04025U4R7BAT2A
L2, L4	6.8 nH	IND, 0402, +/-5%	Coilcraft	0402CS-6N8XJL
L3, L6	220 nH	IND, 0603, +/-5%	Coilcraft	0603CS-R22XJL
L7, L9	100 nH	IND, 0603, +/-5%, 600mA	Coilcraft	0603CS-R10XJL
L8, L10	8.2 nH	IND, 0402, +/-5%	Coilcraft	0402CS-8N2XJL

TQL9066-PCB Evaluation Board Schematic



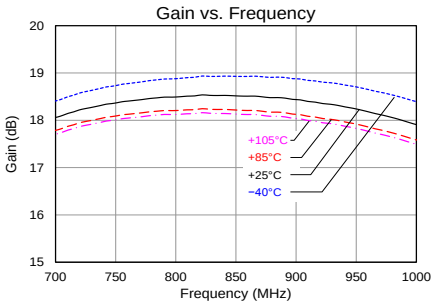
Typical Performance (Balanced Configuration)

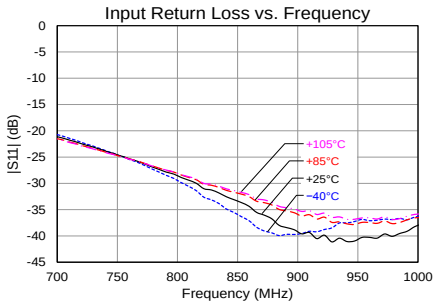
Test conditions unless otherwise noted: V_d = +4.35 V, I_d =115 mA, Temp.=+25°C. NF is de-embedded to the input of the input hybrid coupler.

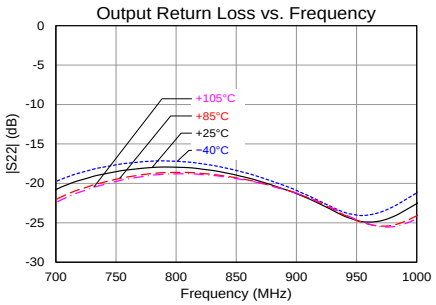
Parameter	Typical Value				Units
Frequency	700	830	900	1000	MHz
Gain	18	18.5	18.4	18.0	dB
Reverse Isolation, S12	-39	-38	-36	-35	dB
Noise Figure (Balanced Configuration)	0.57	0.62	0.6	0.69	dB
Output P1dB	+21.6	+21.5	+21.4	+21.3	dBm
IIP3 (Pin/tone=-13 dBm, Δf = 1 MHz)	+22.0	+24.8	+25.7	+25.0	dBm

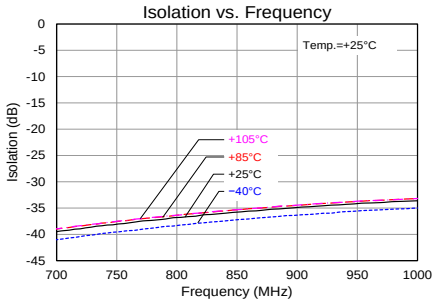
Performance Plots (Balanced Configuration)

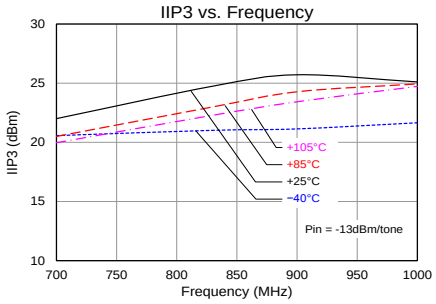
Test conditions unless otherwise noted: V_d = +4.35 V, I_d =115 mA, Temp.=+25°C

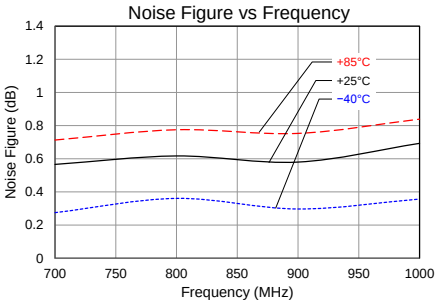


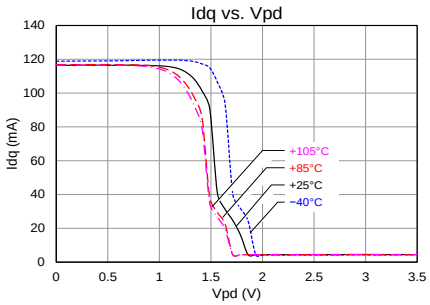




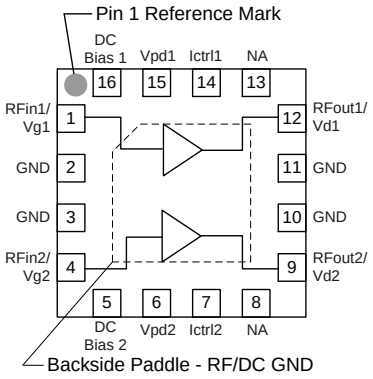








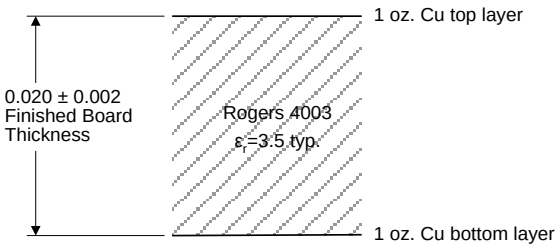
Pin Configuration and Description



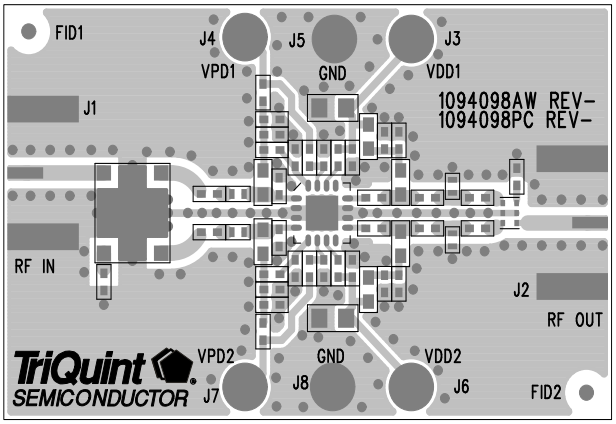
Pin No.	Label	Description
1	RFin1/Vg1	RF input pin for channel 1. Gate voltage bias pin for channel 1.
2, 3	GND	No internal connection but should be grounded to provide PCB mounting integrity and isolation between the two RF paths.
4	RFin2/Vg2	RF input pin for channel 2. Gate voltage bias pin for channel 2.
5	DC Bias 2	DC out bias for channel 2
6	Vpd2	Power down control voltage for channel 1
7	Ictrl2	Channel 2 drain current control
8, 13	NA	No internal connection. These pins can be left floating or grounded.
10, 11	GND	Internally connected. These pins must be externally grounded for functionality.
9	RFout2/Vd2	RF output pin for channel 2. Gate voltage bias pin for channel 2.
12	RFout1/Vd1	RF output pin for channel 1. Drain voltage bias pin for channel 1.
14	Ictrl1	Channel 1 drain current control
15	Vpd1	Power down control voltage for channel 1
16	DC Bias 1	DC out bias for channel 1
Backside Paddle	RF/DC GND	RF/DC Ground. Follow recommended via pattern and ensure good solder attach for best thermal and electrical performance.

Evaluation Board PCB Information

TriQuint PCB 1094098 Material and Stack-up



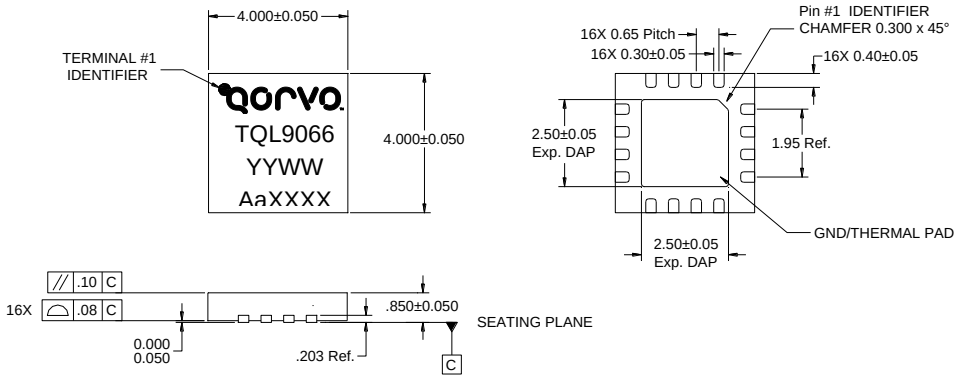
50 ohm line dimensions: width = .040”, spacing = .020”



Mechanical Information

Package Marking and Dimensions

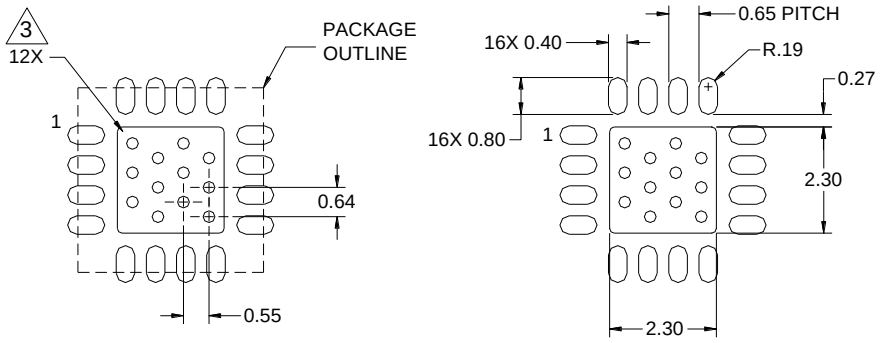
Marking: Part number – TQL9066
Year, week - YYWW
Assembly code - AaXXXX



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012

PCB Mounting Pattern



COMPONENT SIDE

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10”).
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ESDA / JEDEC JS-001-2014
ESD – Charged Device Model (CDM)	Class C3	ESDA / JEDEC JS-002-2014
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with lead-free (260°C max. reflow temp.) soldering process.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

For technical questions and application information: **Email:** appsupport@qorvo.com

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