

N-channel 600 V, 0.135 Ω typ., 20 A MDmesh™ II Power MOSFET in an I²PAKFP package

Datasheet - production data

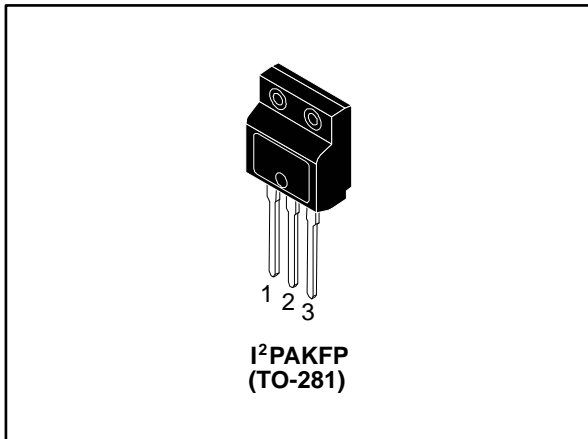
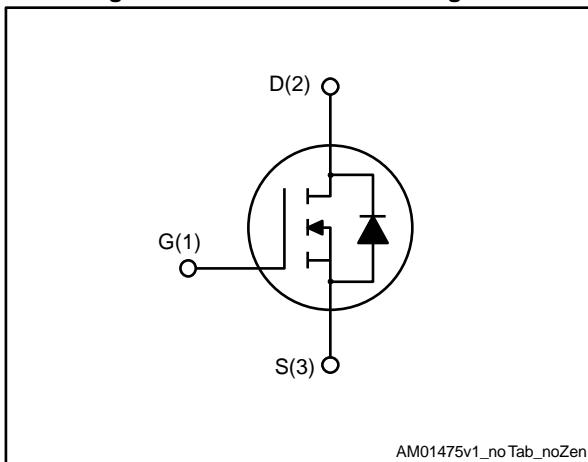


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STFI26NM60N	600 V	0.165 Ω	20 A

- Fully insulated and low profile package with increased creepage path from pin to heatsink plate
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STFI26NM60N	26NM60N	I ² PAKFP (TO-281)	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 30	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	20	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	12.6	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	80	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	35	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^\circ\text{C}$)	2500	V
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

Notes:

(1)Limited by package.

(2)Pulse width limited by safe operating area.

(3) $I_{SD} \leq 20\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS(\text{peak})} \leq V_{(BR)DSS}$, $V_{DD} \leq 80\% V_{(BR)DSS}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	3.6	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	$^\circ\text{C}/\text{W}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Single pulse avalanche current (pulse width limited by T_{jmax})	6	A
E_{AS}	Single pulse avalanche energy (starting $T_J=25\text{ }^\circ\text{C}$, $I_D=I_{AS}$, $V_{DD}=50\text{ V}$)	610	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	600			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 600 V			1	μA
		V _{GS} = 0 V, V _{DS} = 600 V, T _C = 125 °C ⁽¹⁾			100	
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±0.1	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 10 A		0.135	0.165	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0 V	-	1800	-	pF
C _{oss}	Output capacitance		-	115	-	pF
C _{rss}	Reverse transfer capacitance		-	6	-	pF
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{GS} = 0 V, V _{DS} = 0 to 480 V	-	310	-	pF
Q _g	Total gate charge	V _{DD} = 480 V, I _D = 20 A, V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	60	-	nC
Q _{gs}	Gate-source charge		-	8.5	-	nC
Q _{gd}	Gate-drain charge		-	30	-	nC
R _G	Gate input resistance	f = 1 MHz, I _D = 0 A	-	2.8	-	Ω

Notes:

⁽¹⁾C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 300 V, I _D = 10 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	13	-	ns
t _r	Rise time		-	25	-	ns
t _{d(off)}	Turn-off delay time		-	85	-	ns
t _f	Fall time		-	50	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		20	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		80	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 20\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	370		ns
Q_{rr}	Reverse recovery charge		-	5.8		μC
I_{RRM}	Reverse recovery current		-	31.6		A
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	450		ns
Q_{rr}	Reverse recovery charge		-	7.5		μC
I_{RRM}	Reverse recovery current		-	32.5		A

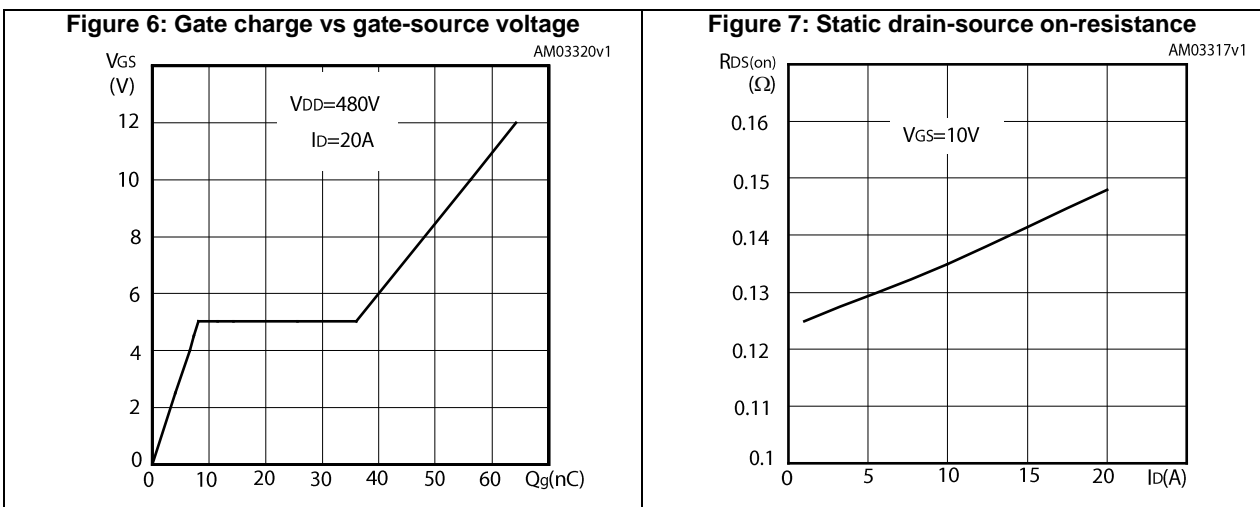
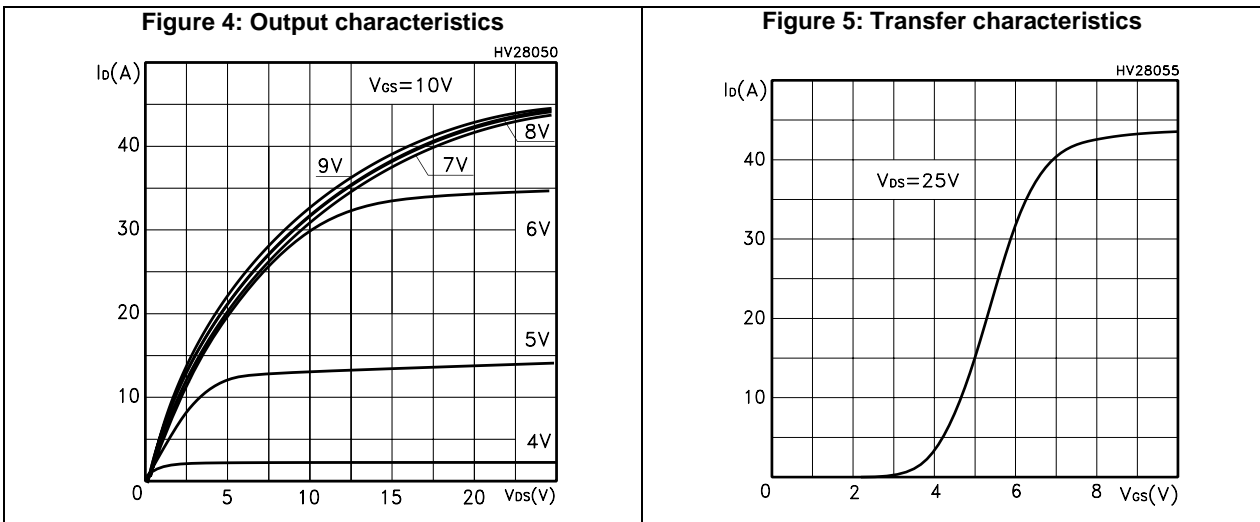
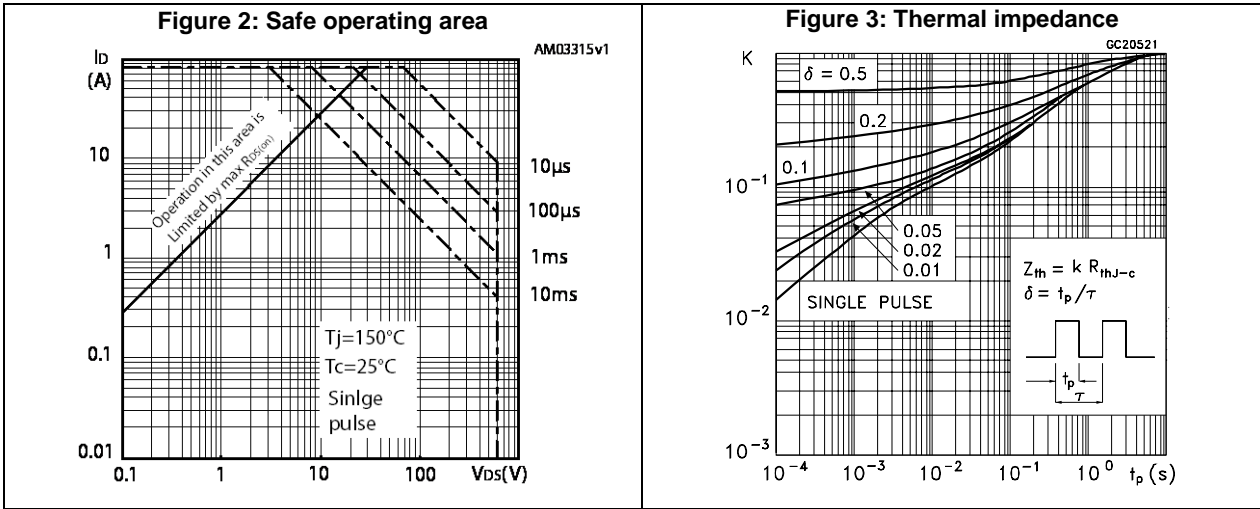
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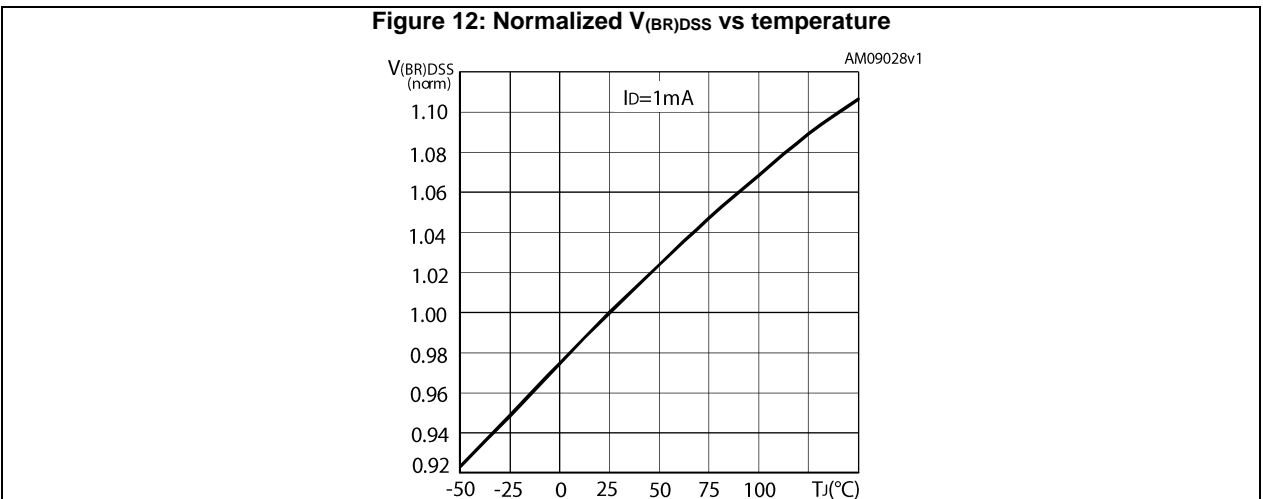
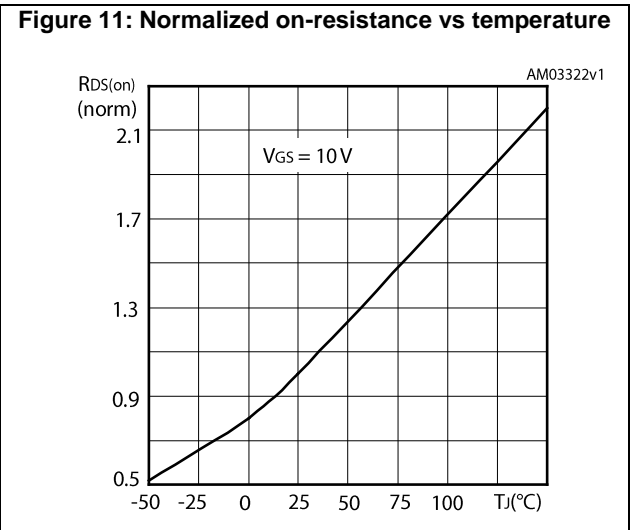
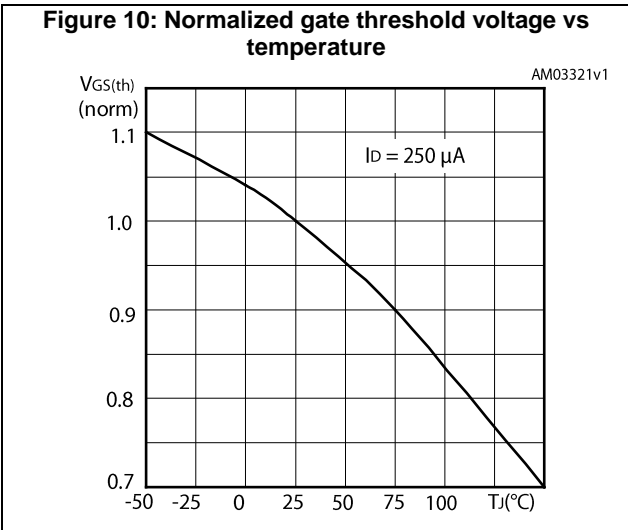
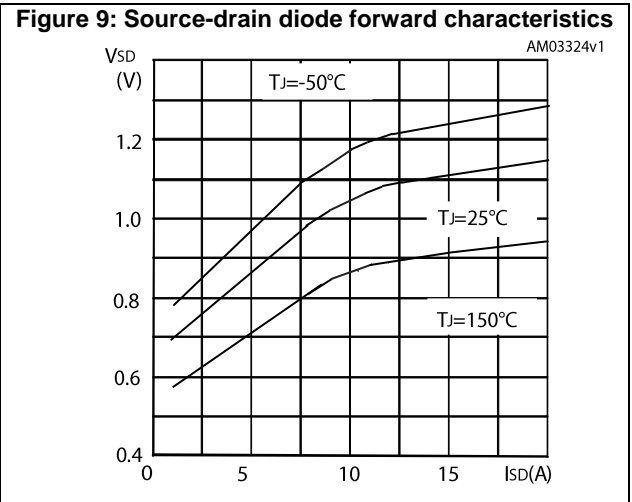
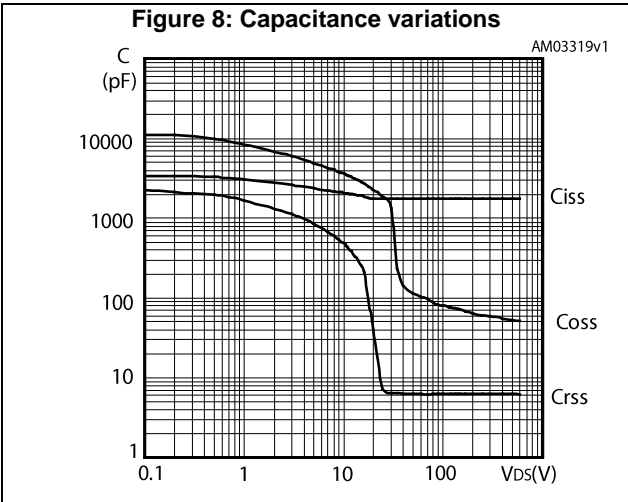
(1)Limited by package.

(2)Pulse width limited by safe operating area.

(3)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

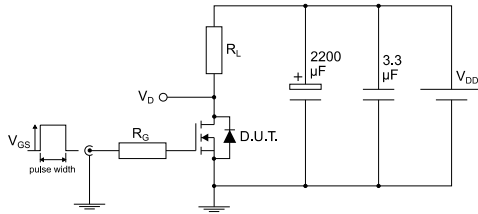
2.1 Electrical characteristics (curves)





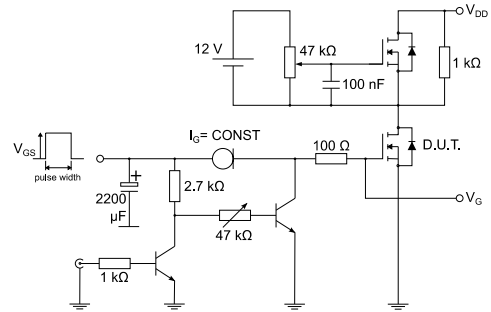
3 Test circuits

Figure 13: Test circuit for resistive load switching times



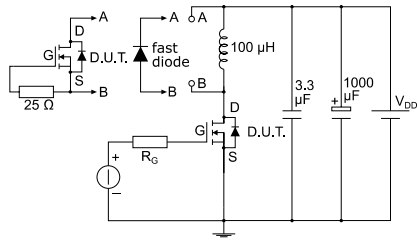
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Figure 14: Test circuit for gate charge behavior



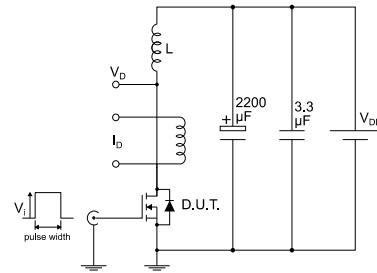
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Figure 15: Test circuit for inductive load switching and diode recovery times



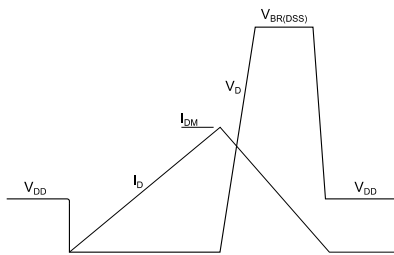
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Figure 16: Unclamped inductive load test circuit



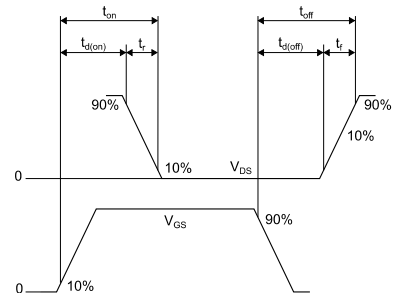
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 I²PAKFP package information

Figure 19: I²PAKFP (TO-281) package outline

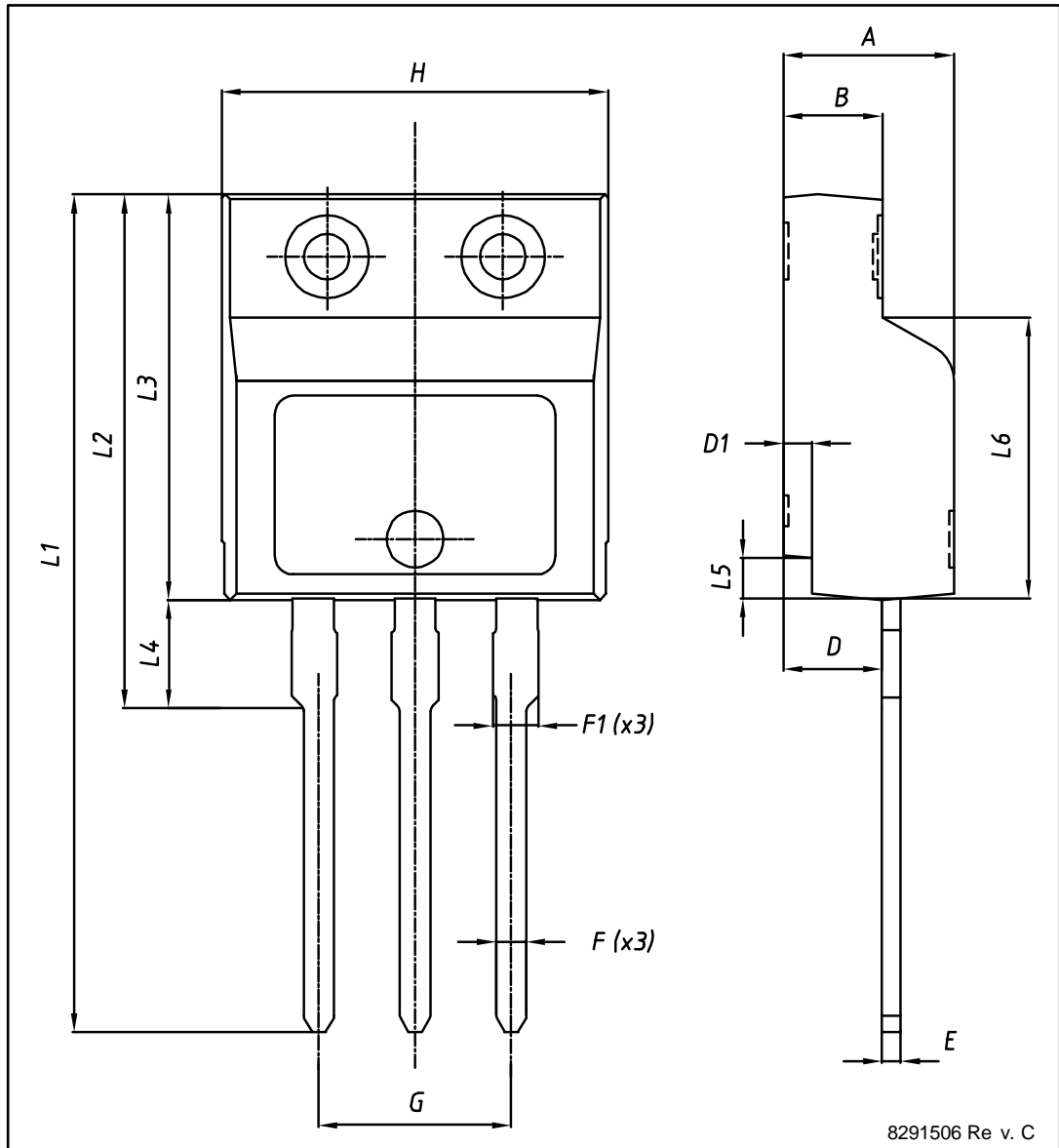


Table 9: I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.50	7.60	7.70

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
15-Nov-2011	1	First release.
04-Jun-2012	2	Document status promoted from preliminary data to production data. Updated P_{TOT} and Derating factor values in <i>Table 2: Absolute maximum ratings</i> , $R_{th-case}$ value in <i>Table 3: Thermal data</i> Package name has been updated.
10-Jun-2015	3	Updated <i>Section 4: Package information</i> . Minor text changes.
13-Dec-2016	4	Modified <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 5: "On/off states"</i> , <i>Table 6: "Dynamic"</i> and <i>Table 8: "Source-drain diode"</i> Modified <i>Section 2.1: "Electrical characteristics (curves)"</i> Minor text changes

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