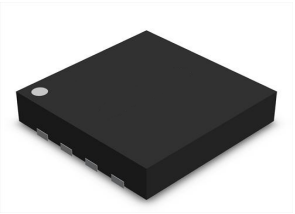
JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD

DFNWB3×3-8 L-J Plastic-Encapsulate MOSFETS

CJAE2002 Dual N-Channel MOSFET

DFNWB3×3-8L-J

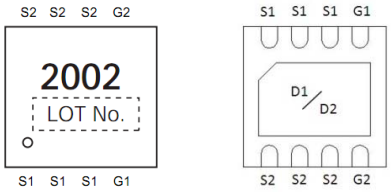


$V_{(BR)DSS}$	$R_{DS(on)}$TYP	I_D
18V	4.4 mΩ@4.5V	15A
	4.5 mΩ@4.0V	
	4.6 mΩ@3.8V	
	4.9 mΩ@3.1V	
	5.4 mΩ@2.5V	

DESCRIPTION

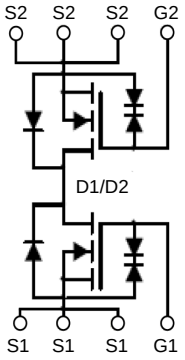
The CJAE2002 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch,facilitated by its common-drain configuration.

MARKING:



Top Back

Equivalent Circuit



MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	18	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A = 25 °C	I_D (1)	15	A
	T_A = 70 °C		13	
	T_C = 25 °C		55	
	T_C = 100 °C		35	
Pulsed Drain Current		I_{DM} (1),(2)	100	A
Thermal Resistance from Junction to Ambient		$R_{\theta JA}$	42	℃/W
Total Power Dissipation		P_D (3)	3	W
Junction Temperature		T_j	150	℃
Storage Temperature		T_{stg}	-55~+150	℃
Lead Temperature for Soldering Purposes(1/8'' from case for 10 s)		T_L	260	℃

MOSFET ELECTRICAL CHARACTERISTICS

T_a=25℃ unless otherwise specified

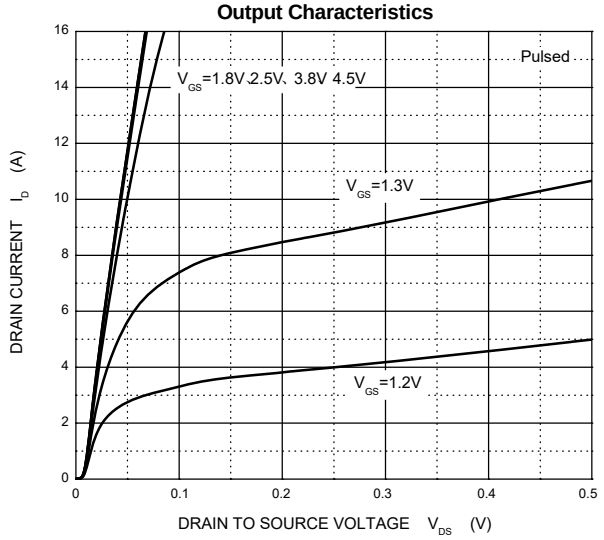
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	18			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =16V,V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±4.5V, V_{DS} = 0V			±1	μA
		V_{GS} =±8V, V_{DS} = 0V			±10	μA
Gate threshold voltage	$V_{GS(th)}$ (4)	V_{DS} =V_{GS}, I_D =250μA	0.4		1	V
Drain-source on-resistance	$R_{DS(on)}$ (4)	V_{GS} =4.5V, I_D =3A	4.0	4.4	5.5	mΩ
		V_{GS} =4.0V, I_D =3A	4.1	4.5	5.8	mΩ
		V_{GS} =3.8V, I_D =3A	4.2	4.6	6.0	mΩ
		V_{GS} =3.1V, I_D =3A	4.4	4.9	6.3	mΩ
		V_{GS} =2.5V, I_D =3A	4.8	5.4	6.5	mΩ
Forward tranconductance	g_{FS} (4)	V_{DS} =5V, I_D =3A	8	42		S
Diode forward voltage	V_{SD} (4)	I_S=1A, V_{GS} = 0V			1	V
DYNAMIC PARAMETERS (5)						
Input Capacitance	C_{iss}	V_{DS} =10V,V_{GS} =0V,f =1MHz		1970		pF
Output Capacitance	C_{oss}			315		pF
Reverse Transfer Capacitance	C_{rss}			285		pF
Total gate charge	Q_g	V_{DS} =10V,V_{GS} =4.5V,I_D =3A		26.5		nC
Gate-source charge	Q_{gs}			2.4		nC
Gate-drain charge	Q_{gd}			7.6		nC
SWITCHING PARAMETERS (5)						
Turn-on delay time	$t_{d(on)}$	V_{GS}=5V,V_{DD}=10V, I_D=3A R_L=1.35Ω,R_{GEN}=3Ω		4.5		ns
Turn-on rise time	t_r			8.9		ns
Turn-off delay time	$t_{d(off)}$			85		ns
Turn-off fall time	t_f			24		ns
Drain-Source Diode Characteristics						
Diode Forward Current	I_S (6)		-	-	15	A

Notes :

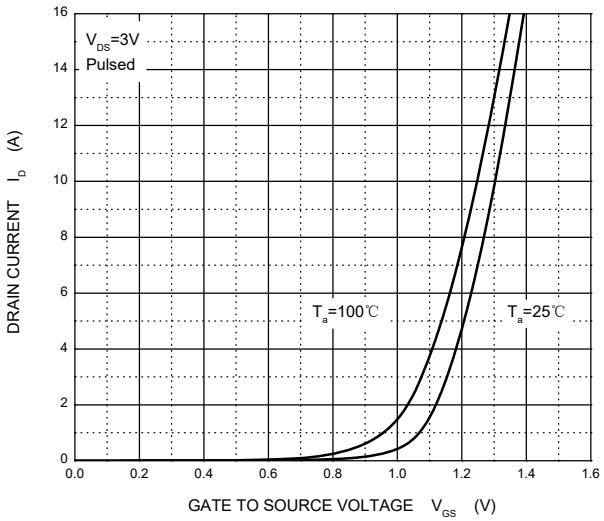
1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. Pulse Test:Pulse Width < 10us, Duty Cycle < 0.5%.
3. The power dissipation is limited by 150℃junction temperature
4. Pulse Test : Pulse width≤300μs, duty cycle≤0.5%.
5. Guaranteed by design, not subject to production testing.
6. The data is theoretically the same as I_D, in real applications , should be limited by total power dissipation.

Typical Characteristics

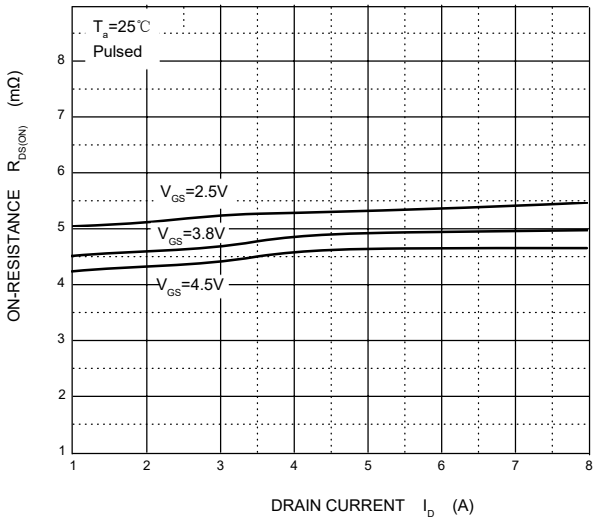
Output Characteristics



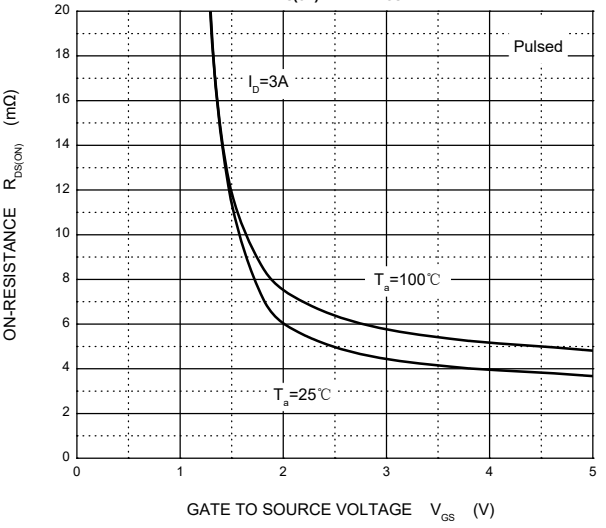
Transfer Characteristics



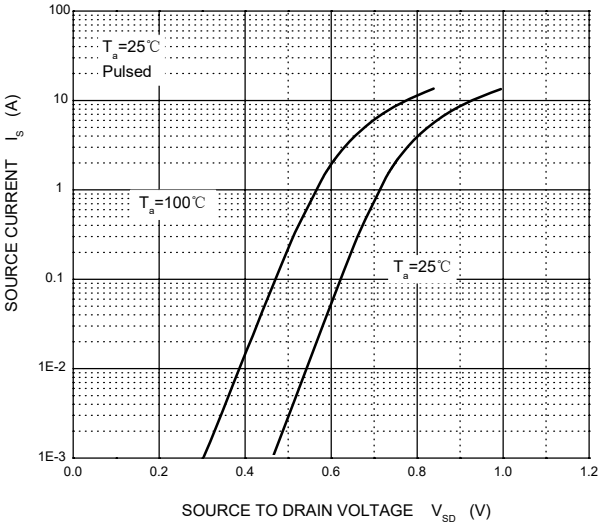
$R_{DS(ON)}$ —— I_D



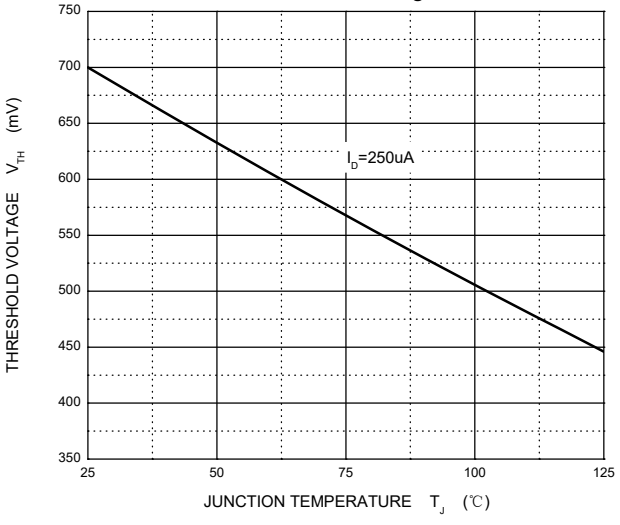
$R_{DS(ON)}$ —— V_{GS}



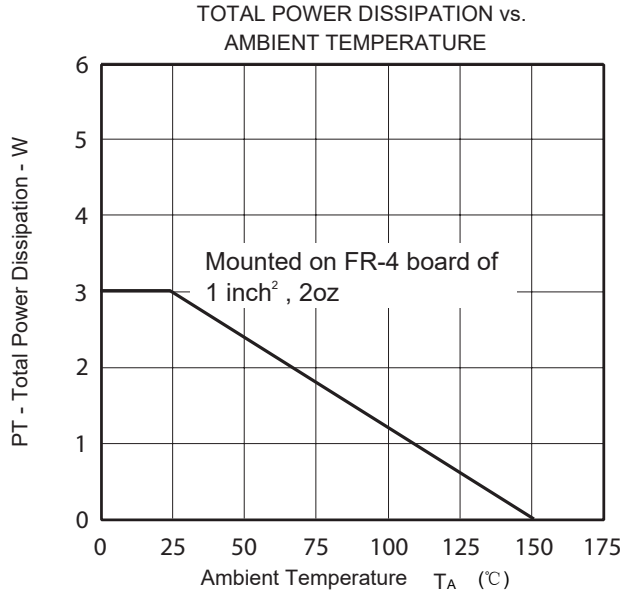
I_S —— V_{SD}

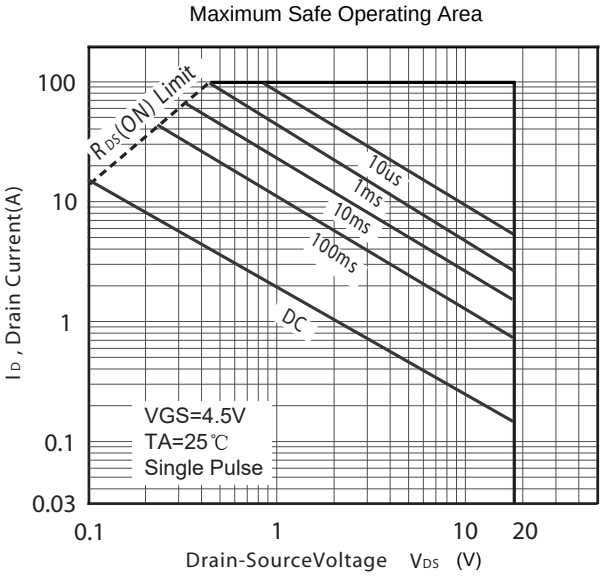


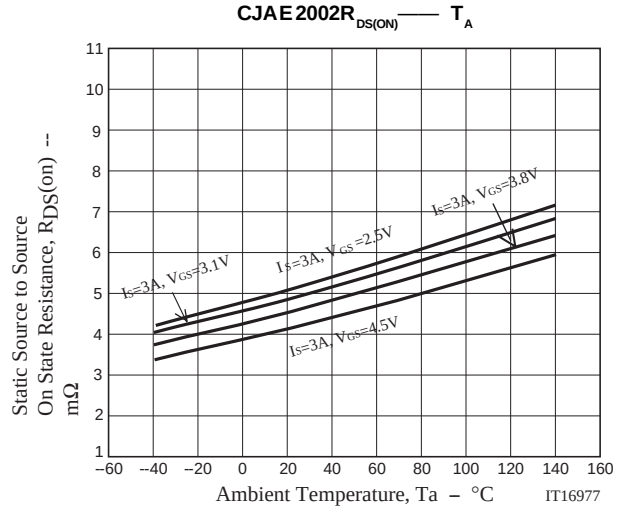
Threshold Voltage



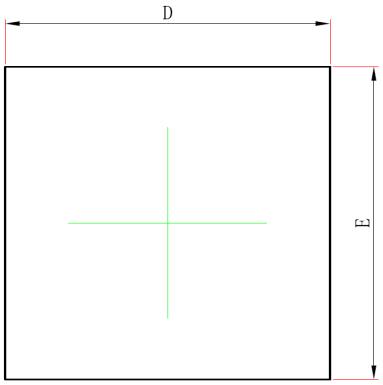
Typical Characteristics



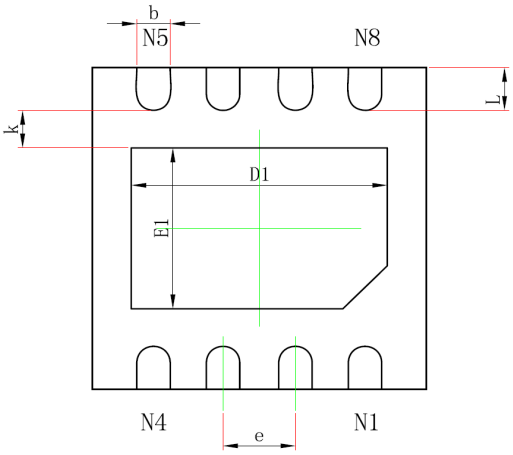




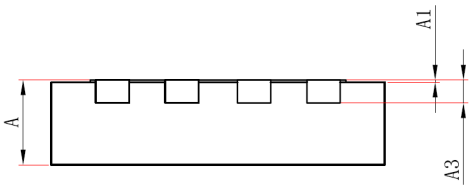
DFNWB3×3-8L-J Package Outline Dimensions(Unit:mm)



TOP VIEW



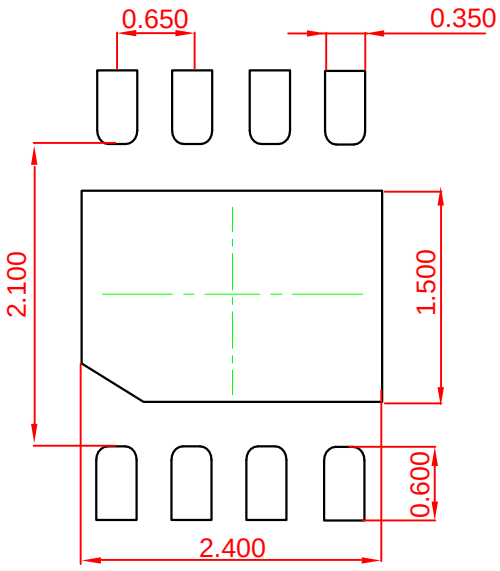
BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	2.200	2.400	0.087	0.094
E1	1.400	1.600	0.055	0.063
b	0.250	0.350	0.010	0.014
k	0.200MIN		0.008MIN	
e	0.650TYP.		0.026TYP.	
L	0.324	0.476	0.013	0.019

DFNWB3×3-8L-J Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.

NOTICE

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