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FDMC89521L

Dual N-Channel PowerTrench[®] MOSFET

60 V, 8.2 A, 17 mΩ

Features

- Max $r_{DS(on)}$ = 17 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 8.2\text{ A}$
- Max $r_{DS(on)}$ = 27 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 6.7\text{ A}$
- Termination is Lead-free
- RoHS Compliant

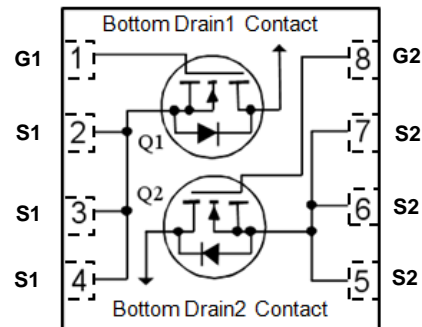
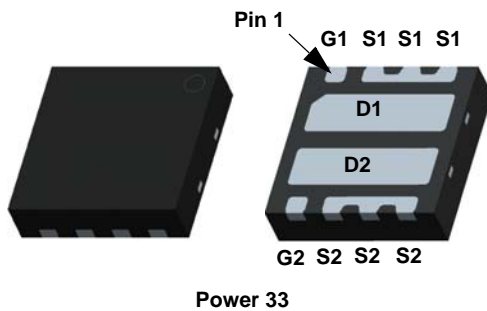


General Description

This device includes two 60 V N-Channel MOSFETs in a dual Power 33 (3 mm X 3 mm MLP) package. The package is enhanced for exceptional thermal performance.

Applications

- Battery Protection
- Load Switching
- Bridge Topologies



MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted.

| Symbol | Parameter | Ratings | Units |
|----------------|--|--------------------------------|-------|
| V_{DS} | Drain to Source Voltage | 60 | V |
| V_{GS} | Gate to Source Voltage | ±20 | V |
| I_D | Drain Current -Continuous | $T_A = 25\text{ °C}$ (Note 1a) | 8.2 |
| | -Pulsed | | 40 |
| E_{AS} | Single Pulse Avalanche Energy | (Note 3) | 32 |
| P_D | Power Dissipation | $T_C = 25\text{ °C}$ | 16 |
| | Power Dissipation | $T_A = 25\text{ °C}$ (Note 1a) | 1.9 |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | °C |

Thermal Characteristics

| | | | |
|-----------------|---|-----|------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 8.0 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 65 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1b) | 155 | |

Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|------------|----------|-----------|------------|------------|
| FDMC89521L | FDMC89521L | Power 33 | 13 " | 12 mm | 3000 units |

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|--------|-----------|-----------------|------|------|------|-------|
|--------|-----------|-----------------|------|------|------|-------|

Off Characteristics

| | | | | | | |
|--------------------------------------|---|---|----|----|-----------|----------------------|
| BV_{DSS} | Drain to Source Breakdown Voltage | $I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$ | 60 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ | | 30 | | mV/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$ | | | 1 | μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ | | | ± 100 | nA |

On Characteristics

| | | | | | | |
|--|--|---|---|-----|----|----------------------|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$ | 1 | 1.9 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ | | -6 | | mV/ $^\circ\text{C}$ |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS} = 10\text{ V}, I_D = 8.2\text{ A}$ | | 13 | 17 | m Ω |
| | | $V_{GS} = 4.5\text{ V}, I_D = 6.7\text{ A}$ | | 21 | 27 | |
| | | $V_{GS} = 10\text{ V}, I_D = 8.2\text{ A}, T_J = 125\text{ }^\circ\text{C}$ | | 20 | 26 | |
| g_{FS} | Forward Transconductance | $V_{DS} = 10\text{ V}, I_D = 8.2\text{ A}$ | | 28 | | S |

Dynamic Characteristics

| | | | | | | |
|-----------|------------------------------|---|--|------|------|----------|
| C_{iss} | Input Capacitance | $V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | | 1228 | 1635 | pF |
| C_{oss} | Output Capacitance | | | 243 | 325 | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 10 | 15 | pF |
| R_g | Gate Resistance | | | 0.7 | | Ω |

Switching Characteristics

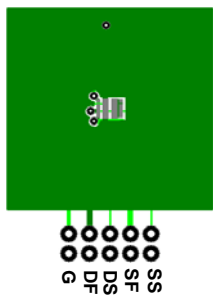
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|--------------|-------------------------------|---|--|-----|----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 30\text{ V}, I_D = 8.2\text{ A}, V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$ | | 7.9 | 16 | ns |
| t_r | Rise Time | | | 2.1 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 18 | 33 | ns |
| t_f | Fall Time | | | 1.7 | 10 | ns |
| Q_g | Total Gate Charge | $V_{GS} = 0\text{ V to } 10\text{ V}$ | | 17 | 24 | nC |
| Q_g | Total Gate Charge | $V_{GS} = 0\text{ V to } 4.5\text{ V}$ | $V_{DD} = 30\text{ V}, I_D = 8.2\text{ A}$ | 7.9 | 12 | nC |
| Q_{gs} | Gate to Source Charge | | | 3.8 | | nC |
| Q_{gd} | Gate to Drain "Miller" Charge | | | 1.9 | | nC |

Drain-Source Diode Characteristics

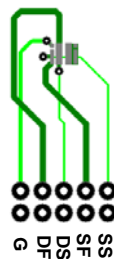
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|----------|------------------------------------|--|--|------|-----|----|
| V_{SD} | Source-Drain Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = 8.2\text{ A}$ (Note 2) | | 0.85 | 1.3 | V |
| | | $V_{GS} = 0\text{ V}, I_S = 1.6\text{ A}$ (Note 2) | | 0.75 | 1.2 | |
| t_{rr} | Reverse Recovery Time | $I_F = 8.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ | | 25 | 40 | ns |
| Q_{rr} | Reverse Recovery Charge | | | 11 | 20 | nC |

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad of 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $65\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper



b. $155\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty cycle < 2.0%.

3. E_{AS} of 32 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1\text{ mH}$, $I_{AS} = 8\text{ A}$, $V_{DD} = 54\text{ V}$, $V_{GS} = 10\text{ V}$. 100% tested at $L = 3\text{ mH}$, $I_{AS} = 5.4\text{ A}$.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

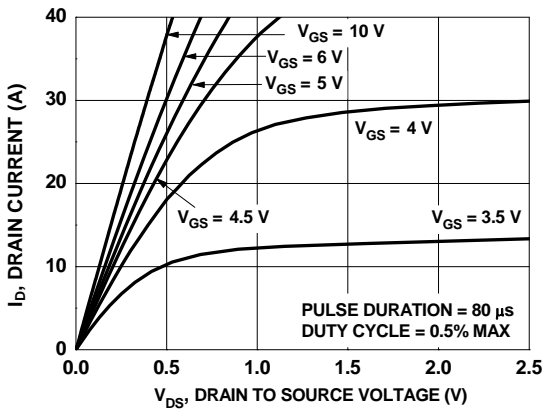


Figure 1. On Region Characteristics

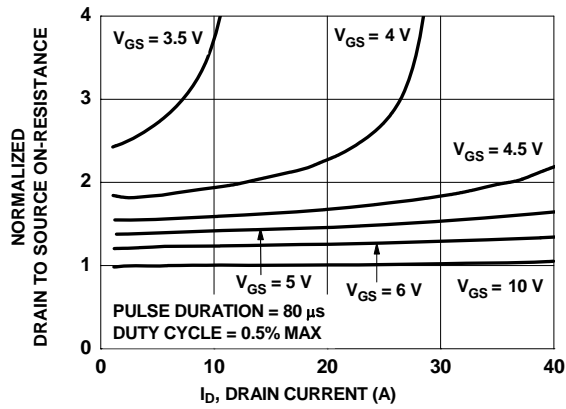


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

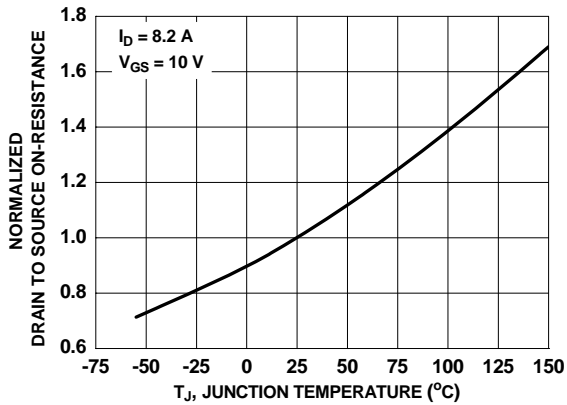


Figure 3. Normalized On Resistance vs. Junction Temperature

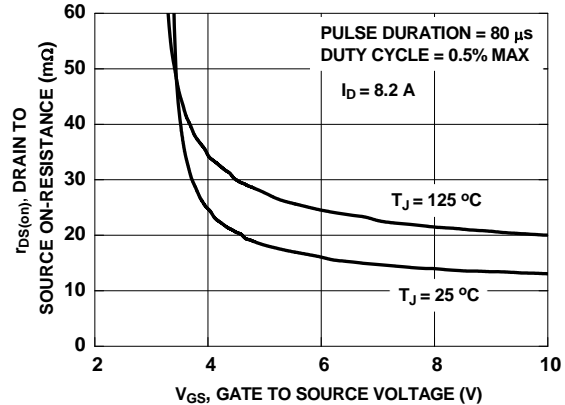


Figure 4. On-Resistance vs. Gate to Source Voltage

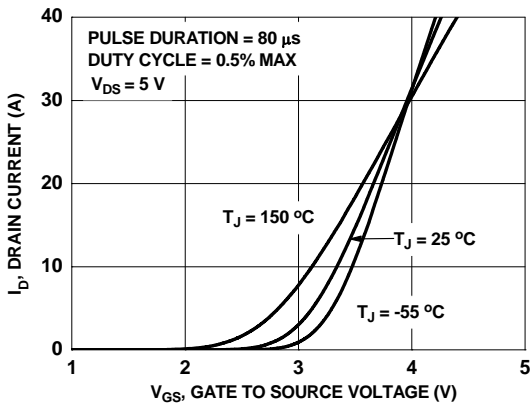


Figure 5. Transfer Characteristics

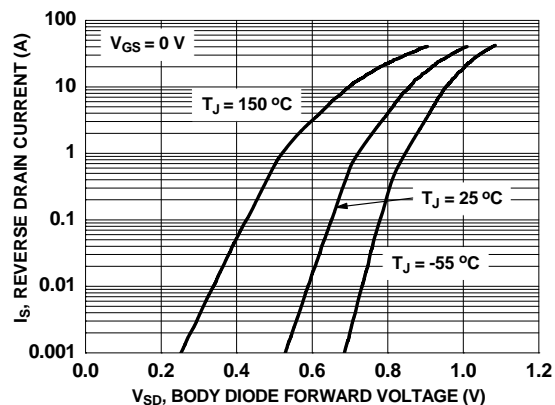


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

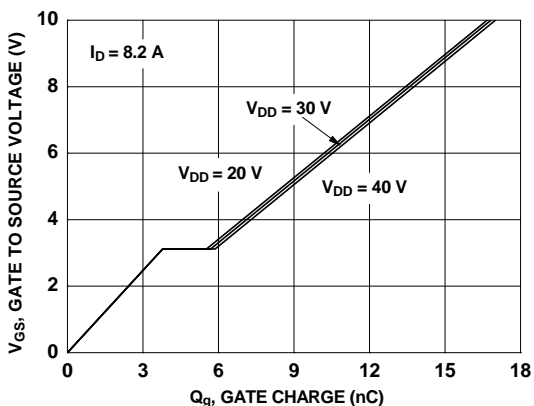


Figure 7. Gate Charge Characteristics

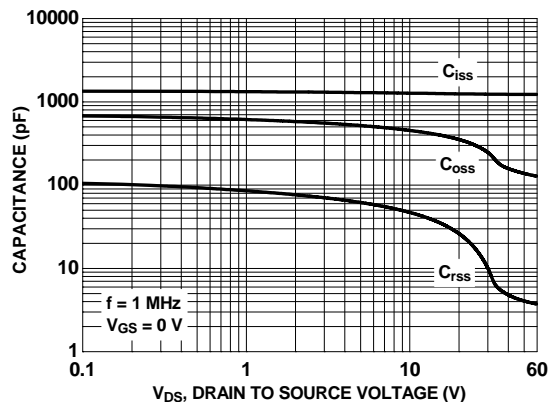


Figure 8. Capacitance vs. Drain to Source Voltage

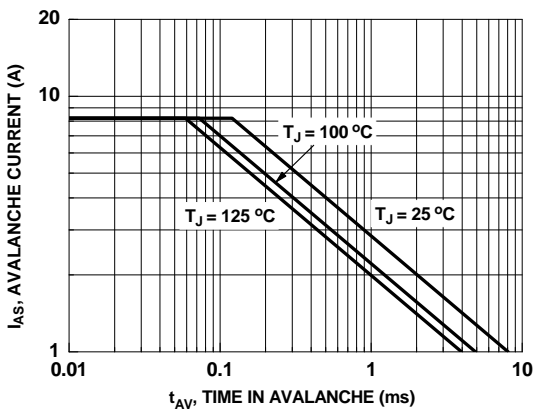


Figure 9. Unclamped Inductive Switching Capability

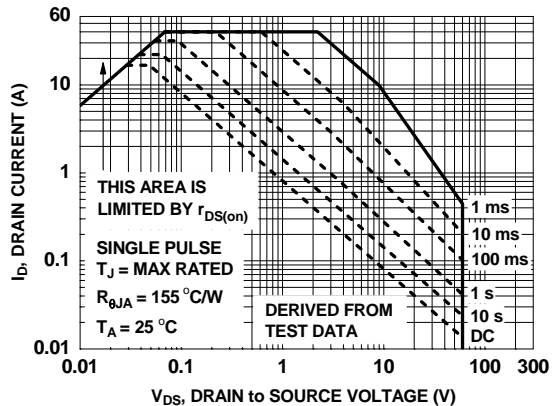


Figure 10. Forward Bias Safe Operating Area

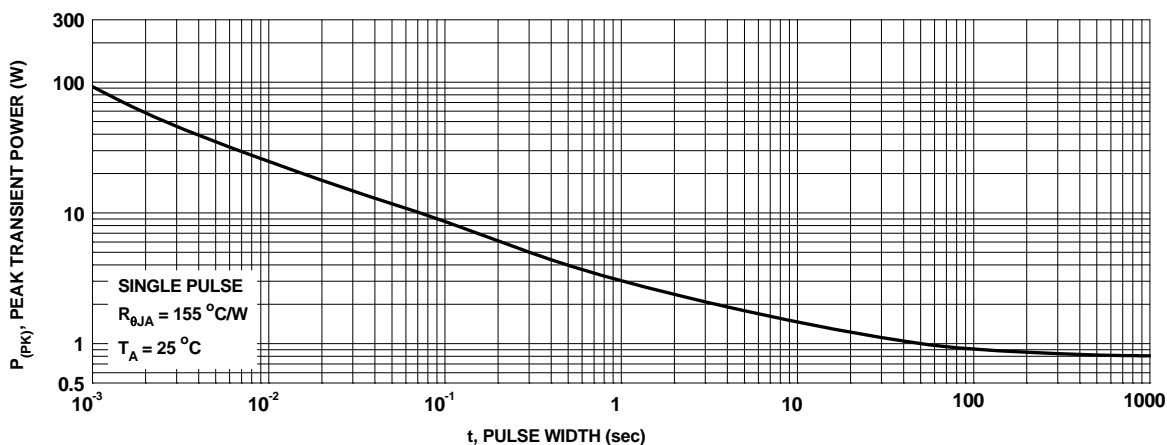


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

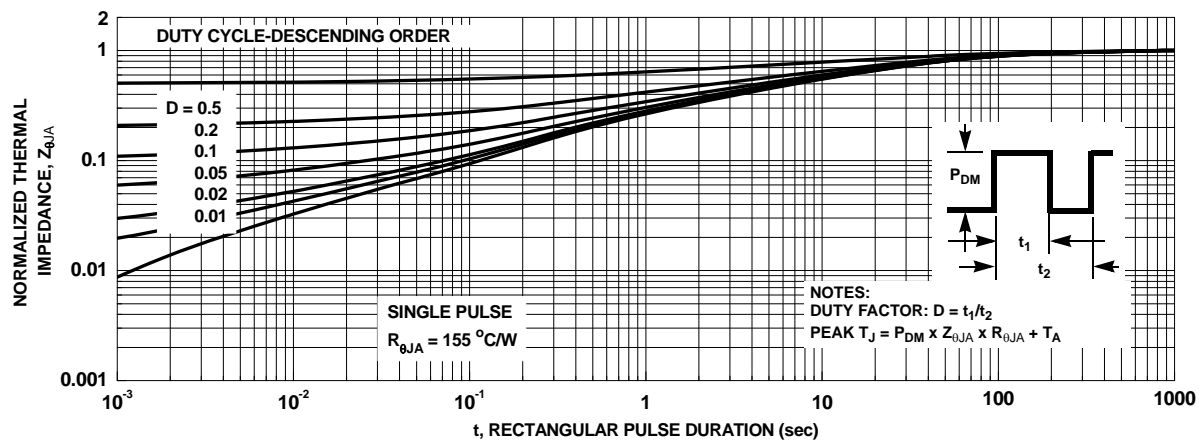
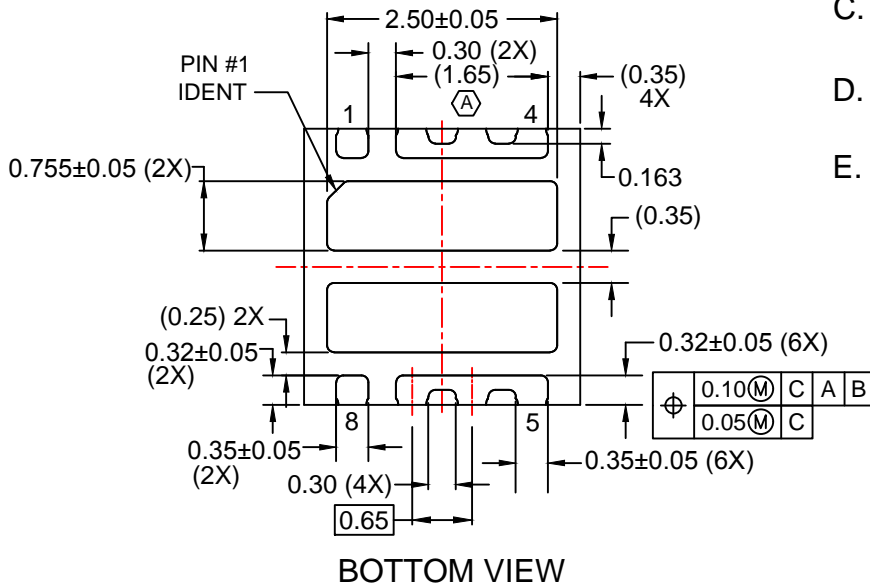
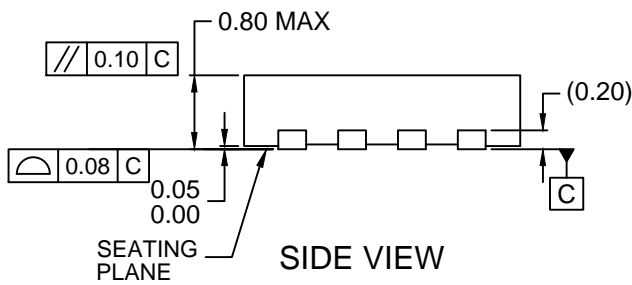
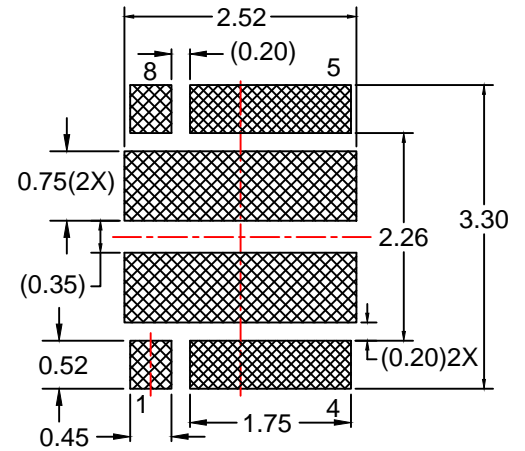
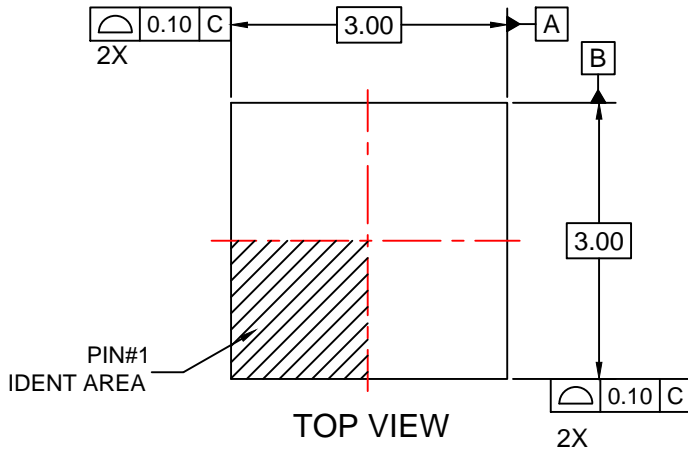


Figure 12. Junction-to-Ambient Transient Thermal Response Curve



RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
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