Description

The SD6022A is a compact, high efficiency, and low voltage step-up DC/DC converter with an Adaptive Current Mode PWM control loop, includes an error amplifier, ramp generator, comparator, switch pass element and driver in which providing a stable and high efficient operation over a wide range of load currents. It operates in stable waveforms without external compensation.

SD6022A can operate from an input voltage as low as 2.2V. SD6022A can generate 18V up to 700mA from a 5V supply.

The SD6022A is available in a low profile SOT-23-6L package.

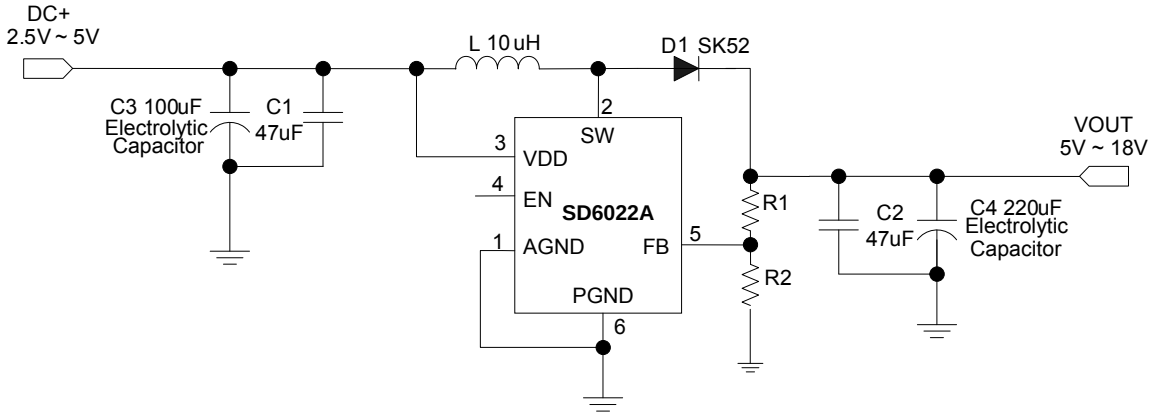
Features

- 2.2V Start-up Input Voltage
- 18V at 700mA from 5V Input
- Up to 88% Efficiency
- No External MOSFET Required
- Small SOT-23-6L Package

Applications

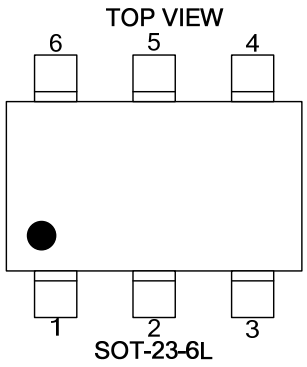
- PDA
- DSC
- LCD Panel
- RF-Tags
- MP3
- Portable Instrument
- Wireless Equipment

Typical Application Circuit



* The Output voltage is set by R1 and R2: V_{OUT} = 1.212V • [1 + (R1/R2)]

Pin Assignment and Function



PIN	NAME	FUNCTION
1	AGND	Analog Ground
2	SW	Switch Node For Output
3	VDD	Output Voltage Sense Input
4	EN	ON/OFF Control (High Enable)
5	FB	Feedback
6	PGND	Power Ground

Absolute Maximum Ratings (Note 1)

- Supply Voltage……..−0.3V ~ 6V
- SW Pin Switch Voltage……−0.3V ~ 22V
- Other I/O Pin Voltages……..−0.3V ~ (VDD + 0.3V)
- SW Pin Switch Current ……..……..4.5A
- Package Thermal Resistance (SOT-23-6L)
  θ_{JA}……+220°C/W
- Operating Temperature Range(Note 2)……-40°C ~ +85°C
- Junction Temperature……..+150°C
- Storage Temperature Range ……−65°C ~ +150°C
- Lead Temperature (Soldering 10sec)... ……....+265°C

Note 1: Stresses beyond those listed Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note2: The SD6022A is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Electrical Characteristics

Operating Conditions: T_A=25°C, V_{IN}=5V, V_{OUT}=18V, R1=430K, R2=30K, unless otherwise specified.

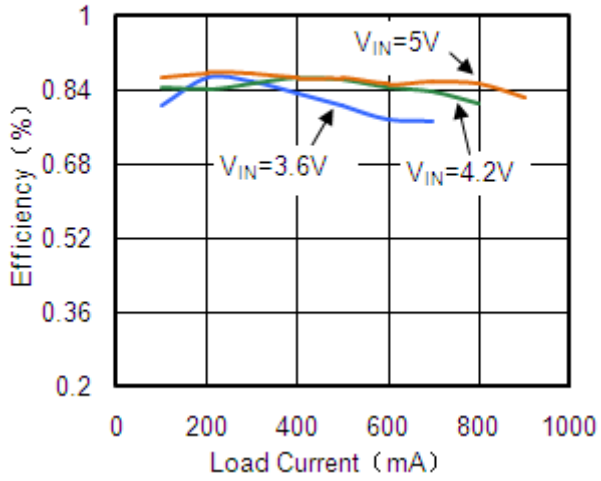
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{START}	Start-up Voltage	I_{OUT} = 1mA		2.2		V
V_{HOLD}	Hold-up Voltage	I_{OUT} = 1mA		1.7		V
V_{DD}	Operating VDD Range	VDD Pin Voltage	2.5		5	V
I_Q	Supply Current (Quiescent)	V_{IN}=2.5V		692		μA
		V_{IN}=3.6V		630		μA
I_{OFF}	Supply Current (Shutdown)	V_{EN}=0V		52		μA
V_{FB}	Feedback Reference Voltage		1.188	1.212	1.236	V
I_{FB}	FB Pin Bias Current			100		nA
V_{ENH}	EN High Threshold	V_{EN} Rising	1			V
V_{ENL}	EN Low Threshold				0.6	V
I_{EN}	EN Input Current	V_{EN}(H),V_{EN}=2V		8		μA
		V_{EN}(L),V_{EN}=0.5V		0.15		μA
F_{OSC}	Switching Frequency	I_{OUT} = 500mA		800		KHz
ΔF_{OSC}	Frequency Change	V_{DD}=3V→5V		20		KHz
DC	Maximum Duty			90		%
R_{SW}	SW ON Resistance			300		mΩ

Note: The EN pin shall be tied to VDD pin and inhibit to act the ON/OFF state whenever the VDD pin voltage may reach to 5.5V or above.

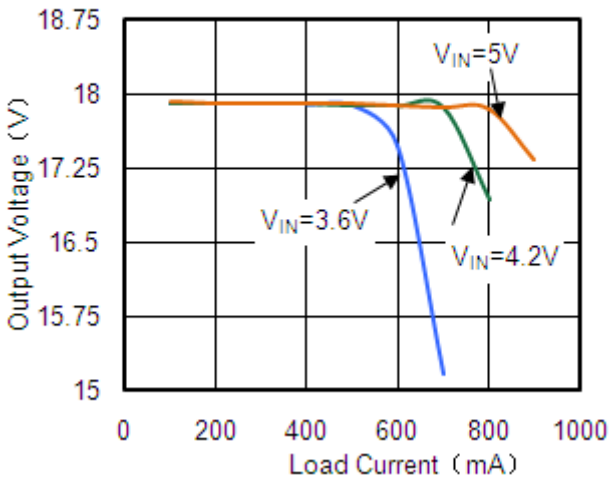
Typical Performance Characteristics

Operating Conditions: T_A=25°C, R1=430K, R2=30K, unless otherwise specified.

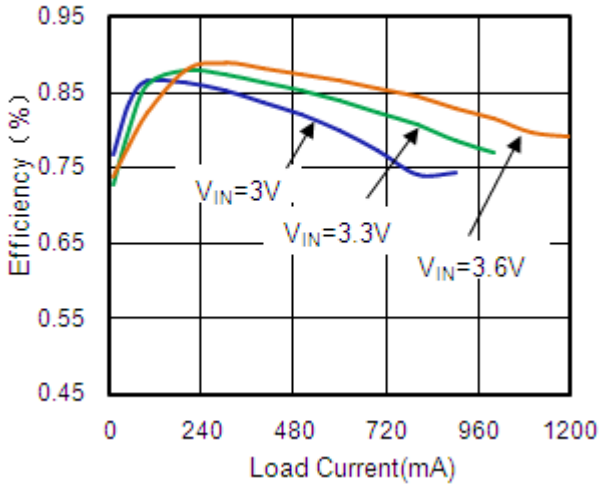
Efficiency vs. Load Current (V_{OUT}=18V)



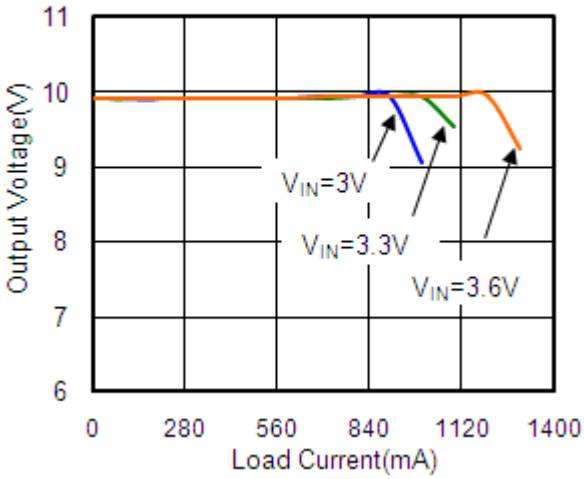
Output Voltage vs. Load Current (V_{OUT}=18V)



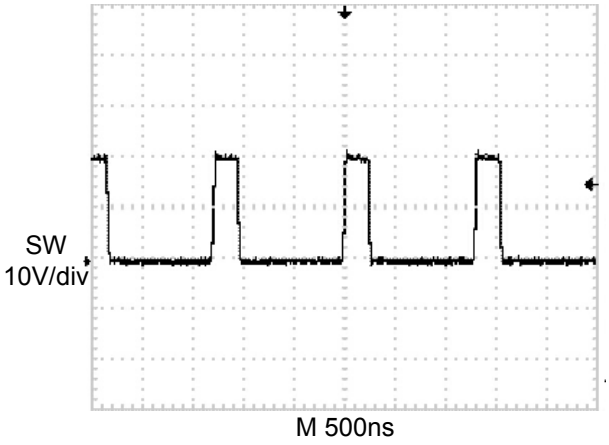
Efficiency vs. Load Current (V_{OUT}=10V)



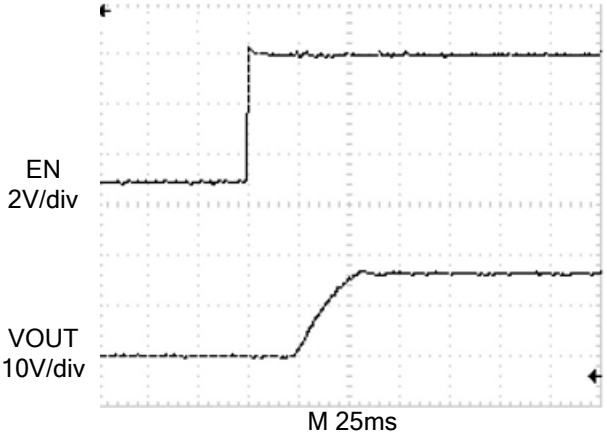
Output Voltage vs. Load Current (V_{OUT}=10V)



SW Waveform
(V_{IN}=5V, V_{OUT}=18V, I_{LOAD}=0.5A)



Start Up
(V_{IN}=5V, V_{OUT}=18V, I_{LOAD}=0.5A)



Pin Information

AGND (Pin 1): Analog Ground.

SW (Pin 2): Switch Pin. Connect inductor between SW and VIN. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.

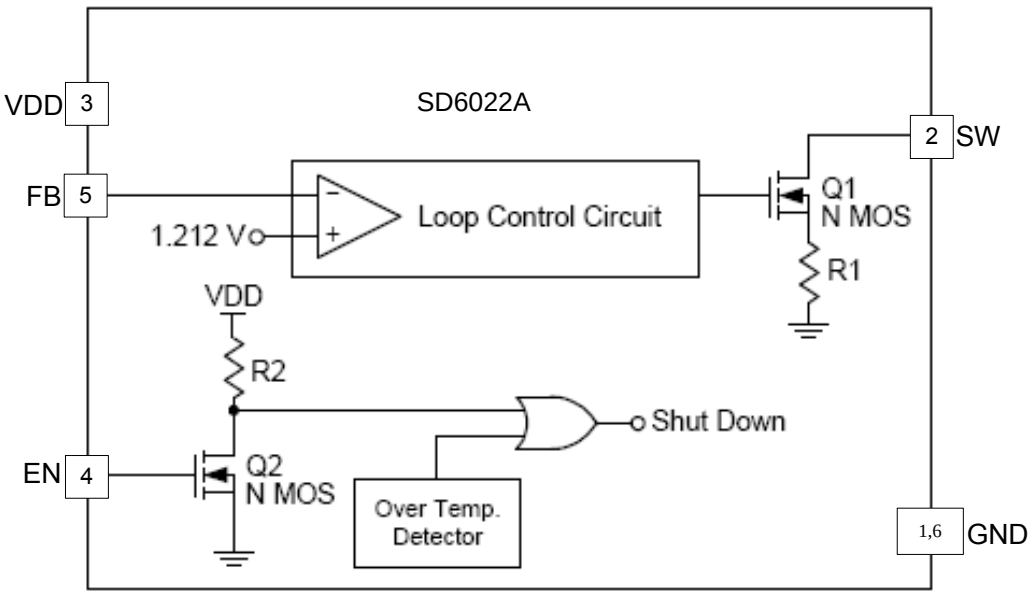
VDD (Pin 3): Output Voltage Sense Input. The NMOS switch gate drive is derived from the greater of V_{OUT} and V_{IN}.

EN (Pin 4): Logic Controlled Shutdown Input. EN=High: Normal free running operation. EN=Low: Shutdown.

FB (Pin 5): Feedback Input to the g_m Error Amplifier. Connect resistor divider tap to this pin.

PGND (Pin 6): Power Ground.

Block Diagram



Application Information

Inductor Selection

For most applications, the value of the inductor will fall in the range of 1μH to 4.7μH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation .A reasonable starting point for setting ripple current is ΔI_L = 0.72A (40% of 1.8A).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 2.16A rated inductor should be enough for most applications (1.8A + 0.36A). For better efficiency, choose a low DC-resistance inductor.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or perm alloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what VOUT requires to operate.

Output and Input Capacitor Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{OMAX} \frac{\left[V_{OUT}(V_{IN} - V_{OUT})\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR).Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}}\right)$$

Where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as: Efficiency = 100% - (L1+ L2+ L3+ ...) where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge ΔQ moves from V_{IN} to ground. The resulting ΔQ/Δt is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG}$ = f (QT+QB) where QT and QB are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW} and external inductor RL. In continuous mode the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows: R_{SW} = $R_{DS(ON)TOP}$ x DC + $R_{DS(ON)BOT}$ x (1-DC) The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current. Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

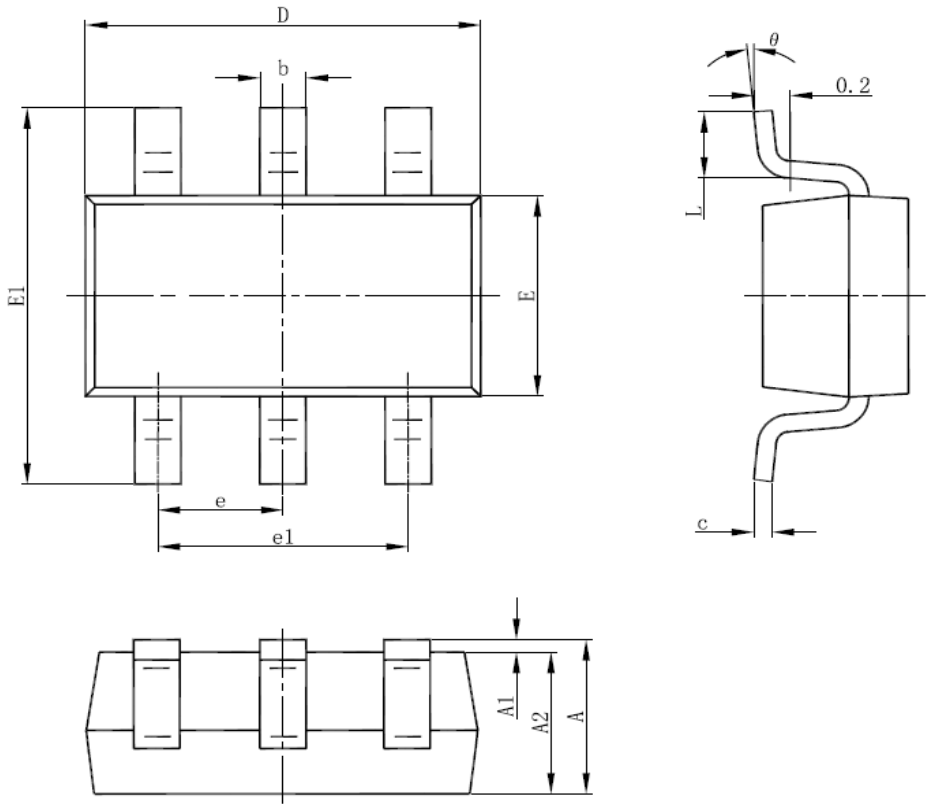
Board Layout Suggestions

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the SD6022A. Check the following in your layout:

1. The power traces, consisting of the GND trace, the SW trace and the VIN trace should be kept short, direct and wide.
2. Put the input capacitor as close as possible to the device pins (VIN and GND).
3. SW node is with high frequency voltage swing and should be kept small area. Keep analog components away from SW node to prevent stray capacitive noise pick-up.
4. Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.

Packaging Information

SOT-23-6L Package Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°