7+3 Channels PMIC

Features

- **3.0V ~ 5.5V Input Voltage Operation**
- **95% Efficient DC/DC Converter**
- **Built-in 7-ch synchronous buck converter, 3-ch LDOs**
- **Bucks and LDOs can be set to lower IQ at low load**
- **Buck2, Buck3, Buck5 and Buck6 Supports DVS Function**
- **Built-In Power ON/OFF Sequence for PMU**
- **Built-In Short Circuit Protection (SCP), Under Voltage Protection (UVP), and cycle-by cycle current limit for DC/DC Converters**
- **LDOs are Programmable to Voltage Options by I^2C**
- **Built-In Thermal Shutdown Function**
- **Built-In VCC OVP Function**
- **TQFN5X5-40 Package**

General Description

The G2249 provide a complete power supply solution for handsets or data card. It contains 7 dc/dc converters and 3 LDOs to power each critical blocks of mobile phone, and is optimized for maximum battery life, featuring a low ground current when in standby mode operation. All channels DC/DC converters operate at one fixed frequency of 3.0MHz or 1.5MHz to optimize size, cost, and efficiency. All Synchronous converters operate at pulse skipping mode at light load. The G2249 features a I^2C compatible interface.

The G2249 is available in TQFN5X5-40 package.

Applications

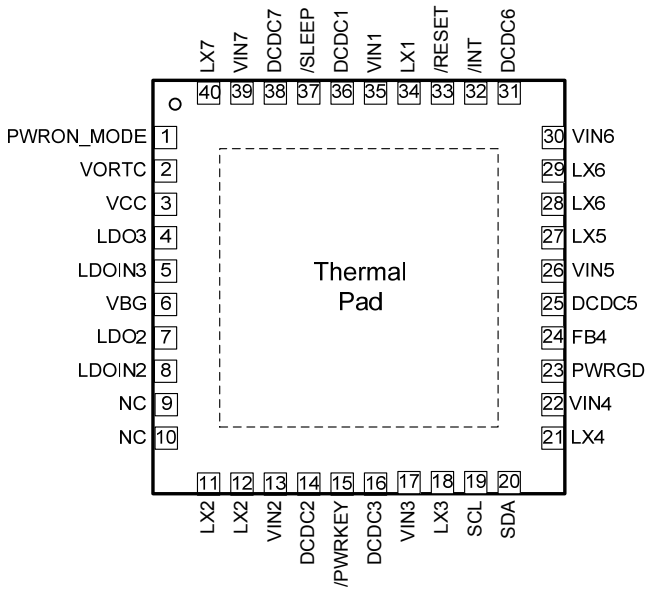
- **Mobile Handsets**
- **TV Dongle**
- **Smart Phone**
- **Set Top Box**

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2249RG1U	2249	-40°C~+85°C	TQFN5X5-40

Note: RG:TQFN5X5-40
1: Bonding code
U: Tape & Reel
Green : Lead Free / Halogen Free

Pin Configuration



G2249 TQFN5X5-40

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Absolute Maximum Ratings

VCC, VIN1, VIN2, VIN3, VIN4, VIN5, VIN6, VIN7, LDOIN2, LDOIN3 . . . . . -0.3V to +6.3V
DCDC1, DCDC2, DCDC3, FB4, DCDC5, DCDC6, DCDC7, VORTC, LDO2, LDO3 . . . . . -0.3V to +6.3V
LX1, LX2, LX3, LX4, LX5, LX6, LX7 . . . -0.3V to +6.3V
Other Pins . . . . . .-0.3V to +6.3V
Thermal Resistance Junction to Ambient, (θ_{JA})
TQFN5X5-40 . . . . . TBD
Continuous Power Dissipation (T_A=25°C)
TQFN5X5-40. . . . . TBD
Thermal Resistance Junction to Case, (θ_{JC})
TQFN5X5-40 . . . . . TBD
Operating Ambient Temperature .-35°C to 85°C
Storage Temperature Range. . . . . -55°C to +150°C
Reflow Temperature (soldering, 10 sec) . . . . . 260°C
ESD(HBM). 2KV
ESD(MM) 200V

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Device are ESD sensitive. Handling precaution recommended. The Human Body model is a 100pF capacitor discharged through a 1.5KΩ resistor into each pin.

Electrical characteristics

(**VCC=VINx=LDOINx=5V, T_A=25°C, unless otherwise specified)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
VCC Operating Voltage for PMU	V_{VCC_PMU}		2.8	---	5.5	V
VIN Operating Voltage for DCDCx	V_{VINX}		2.8	---	5.5	V
VCC Over Voltage threshold	V_{VCC_OVLO}	VCC rising	5.75	6.0	6.25	V
VCC Under Voltage threshold	V_{VCC_UVLO}	VCC rising	---	3.15	---	V
VCC Under Voltage Hysteresis	$V_{VCC\_UVLOHYS}$		---	200	---	mV
PMU Stand-by Supply Current	I_{VCC}	ALL converters enter ECO mode, and without loading current.	---	---	200	uA
OSCILLATOR						
Frequency	F_{OSC}	DCDC1, DCDC3~7	2.4	3.0	3.6	MHz
		DCDC2	1.2	1.5	1.8	MHz
DCDC1 Buck Converter						
Soft-Start Internal	SS_CH1		---	2	---	mS
VO1 regulation voltage accuracy	%VO1		-1.5	---	1.5	%
Load Regulation	$\Delta V_{O1,LOAD}$	FPWM	---	0.5	---	%
Maximum Duty Cycle	D_{max1}		---	100	---	%
VIN1 Leakage Current	I_{VIN1_LK}	V_{LX1}=0V, VIN1=5.0V	---	1	5	µA
LX1 Leakage Current	I_{LX1_LK}	V_{LX1}=5.0V	---	1	5	µA
Switch ON Resistance	Ron1-P		---	150	---	mΩ
	Ron1-N		---	120	---	
Peak Current Limit	I_{LIM_CH1}		2.5	2.8	---	A
Under Voltage Protection Threshold	$\%V_{UVP\_CH1}$	Ratio=V_{UVP}/V_{OUT}	---	75	---	%
DCDC2 Buck Converter						
Soft-Start Internal	SS_CH2		---	2	---	mS
VO2 regulation voltage accuracy	%VO2		-1.5	---	1.5	%
Load Regulation	$\Delta V_{O2,LOAD}$	FPWM	---	0.5	---	%
Maximum Duty Cycle	D_{max2}		---	100	---	%
VIN2 Leakage Current	I_{VIN2_LK}	V_{LX2}=0V, VIN2=5.0V	---	1	5	µA
LX2 Leakage Current	I_{LX2_LK}	V_{LX2}=5.0V	---	1	5	µA
Switch ON Resistance	Ron2-P		---	80	---	mΩ
	Ron2-N		---	35	---	
Peak Current Limit	I_{LIM_CH2}		3.6	4.0	---	A
Under Voltage Protection Threshold	ΔV_{UVP_CH2}	$\Delta V_{UVP\_CH2}=VOUT_{SET}-VOUT_{UVP}$	---	100	---	mV

Electrical characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
DCDC3 Buck Converter						
Soft-Start Internal	SS_CH3		---	2	---	mS
VO3 regulation voltage accuracy	%VO3		-1.5	---	1.5	%
Load Regulation	$\Delta V_{O3,LOAD}$	FPWM	---	0.5	---	%
Maximum Duty Cycle	D_{max3}		---	100	---	%
VIN3 Leakage Current	I_{VIN3_LK}	V_{LX3}=0V, VIN3=5.0V	---	1	5	µA
LX3 Leakage Current	I_{LX3_LK}	V_{LX3}=5.0V	---	1	5	µA
Switch ON Resistance	Ron3-P		---	150	---	mΩ
	Ron3-N		---	90	---	
Peak Current Limit	I_{LIM_CH3}		2.5	2.8	---	A
Under Voltage Protection Threshold	ΔV_{UVP_CH3}	ΔV_{UVP_CH3}=$VOUT_{SET}$-$VOUT_{UVP}$	---	100	---	mV
DCDC4 Buck Converter						
Soft-Start Internal	SS_CH4		---	2	---	mS
FB4 pin regulation voltage	V_{FB4}		0.788	0.80	0.812	V
Load Regulation	$\Delta V_{FB4,LOAD}$	FPWM	---	0.5	---	%
Maximum Duty Cycle	D_{max4}		---	100	---	%
VIN4 Leakage Current	I_{VIN4_LK}	V_{LX4}=0V, VIN4=5.0V	---	1	5	µA
LX4 Leakage Current	I_{LX4_LK}	V_{LX4}=5.0V	---	1	5	µA
Switch ON Resistance	Ron4-P		---	150	---	mΩ
	Ron4-N		---	120	---	
Peak Current Limit	I_{LIM_CH4}		2.5	2.8	---	A
Under Voltage Protection Threshold	$\%V_{UVP\_CH4}$	Ratio=V_{UVP}/V_{OUT}	---	87.5	---	%
DCDC5 Buck Converter						
Soft-Start Internal	SS_CH5		---	2	---	mS
VO5 regulation voltage accuracy	%VO5		-1.5	---	1.5	%
Load Regulation	$\Delta V_{O5,LOAD}$	FPWM	---	0.5	---	%
Maximum Duty Cycle	D_{max5}		---	100	---	%
VIN5 Leakage Current	I_{VIN5_LK}	V_{LX5}=0V, VIN5=5.0V	---	1	5	µA
LX5 Leakage Current	I_{LX5_LK}	V_{LX5}=5.0V	---	1	5	µA
Switch ON Resistance	Ron5-P		---	150	---	mΩ
	Ron5-N		---	120	---	
Peak Current Limit	I_{LIM_CH5}		2.5	2.8	---	A
Under Voltage Protection Threshold	ΔV_{UVP_CH5}	ΔV_{UVP_CH5}=$VOUT_{SET}$-$VOUT_{UVP}$	---	100	---	mV
DCDC6 Buck Converter						
Soft-Start Internal	SS_CH6		---	2	---	mS
VO6 regulation voltage accuracy	%VO6		-1.5	---	1.5	%
Load Regulation	$\Delta V_{O6,LOAD}$	FPWM	---	0.5	---	%
Maximum Duty Cycle	D_{max6}		---	100	---	%
VIN6 Leakage Current	I_{VIN6_LK}	V_{LX6}=0V, VIN6=5.0V	---	1	5	µA
LX6 Leakage Current	I_{LX6_LK}	V_{LX6}=5.0V	---	1	5	µA
Switch ON Resistance	Ron6-P		---	150	---	mΩ
	Ron6-N		---	60	---	
Peak Current Limit	I_{LIM_CH6}		2.5	2.8	---	A
Under Voltage Protection Threshold	ΔV_{UVP_CH6}	ΔV_{UVP_CH6}=$VOUT_{SET}$-$VOUT_{UVP}$	---	100	---	mV
DCDC7 Buck Converter						
Soft-Start Internal	SS_CH7		---	2	---	mS
VO7 regulation voltage accuracy	%VO7		-1.5	---	1.5	%
Load Regulation	$\Delta V_{O7,LOAD}$	FPWM	---	0.5	---	%
Maximum Duty Cycle	D_{max7}		---	100	---	%
VIN7 Leakage Current	I_{VIN7_LK}	V_{LX7}=0V, VIN7=5.0V	---	1	5	µA

Electrical characteristics (continued)

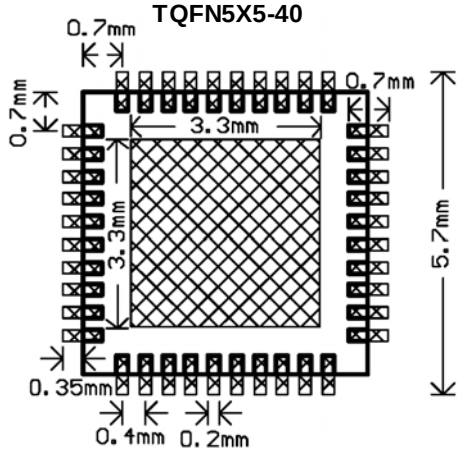
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
LX7 Leakage Current	I_{LX7_LK}	V_{LX7}=5.0V	---	1	5	μA
Switch ON Resistance	Ron7-P		---	150	---	mΩ
	Ron7-N		---	120	---	
Peak Current Limit	I_{LIM_CH1}		2.5	2.8	---	A
Under Voltage Protection Threshold	$\%V_{UVP\_CH1}$	Ratio=V_{UVP}/V_{OUT}	---	87.5	---	%
RTCLDO						
Input voltage range	V_{VINRTC}	VCC	3.0	---	5.5	V
Standby current	I_{Q_RTC}	V_{VCC}=3.7V	---	5	8	μA
Output voltage	V_{RTCO}	Io=0.1mA, VORTC=4'b0000	---	1.8	---	V
Dropout Voltage	V_{DO1_RTC}	Io=50mA, VORTC=4'b0000	---	---	800	mV
	V_{DO2_RTC}	Io=10mA, VORTC=4'b0000	---	---	150	mV
Maximum Output Current		V_{VCC}=4.2v, RTCOUT=95%*V_{SET}	60	---	200	mA
LDO2						
Input voltage range	V_{LDOIN2}	LDOIN2	2.8	---	5.5	V
Soft-Start Internal	SS_{LDO2}		---	2	---	mS
Output Voltage accuracy	$\%V_{LDO2}$	Io=100mA	-1.5	---	1.5	%
Continuous output current at ECO mode	I_{O2_ECO}		---	---	5	mA
LDO Input Current	I_{LDOIN2}	Io=0mA, Normal mode	---	---	32	μA
	I_{LDOIN2_ECO}	Io=0mA, ECO mode	---	---	8	μA
Dropout Voltage	V_{DOLDO2}	Io=300mA, Normal mode	---	200	400	mV
	$V_{DOLLDO2}$	Io=50mA, Normal mode		35	70	mV
Output current limit	$I_{LIMLDO2}$	LDOIN2>LDO2+1.0V, Normal mode	550	600	---	mA
LDO Load Regulation	$\%LD_2$	LDOIN2>LDO2+1.0V, Normal mode Io=1mA~200mA	---	---	1	%
Short Circuit Protection threshold	$\%V_{SCPLDO2}$	Ratio=V_{SCP}/V_{OUT}	---	12.5	---	%
Ripple Rejection	$PSRR_2$	f=10Hz~3kHz, Io=100mA, Normal mode	---	65	---	dB
Output Noise Voltage		f=10Hz~100kHz, Normal mode	---	45	---	uVrms
ECO exit time	t_{d2_ECO}	Minimum wait time to draw full current after leaving ECO mode	---	---	50	uS
LDO3						
Input voltage range	V_{LDOIN3}	LDOIN3	2.8	---	5.5	V
Soft-Start Internal	SS_{LDO3}		---	2	---	mS
Output Voltage accuracy	$\%V_{LDO3}$	Io=100mA	-1.5	---	1.5	%
Continuous output current at ECO mode	I_{O3_ECO}		---	---	5	mA
LDO Input Current	I_{LDOIN3}	Io=0mA, Normal mode	---	---	32	μA
	I_{LDOIN3_ECO}	Io=0mA, ECO mode	---	---	8	μA
Dropout Voltage	V_{DOLDO3}	Io=300mA, VCC=3.7V, Normal mode	---	200	400	mV
	$V_{DOLLDO3}$	Io=50mA, VCC=3.7V, Normal mode		35	70	mV
Output current limit	$I_{LIMLDO3}$	LDOIN3>LDO3+1.0V, Normal mode	550	600	---	mA
LDO Load Regulation	$\%LD_3$	LDOIN3>LDO3+1.0V, Normal mode Io=1mA~200mA	---	---	1	%
Short Circuit Protection threshold	$\%V_{SCPLDO3}$	Ratio=V_{SCP}/V_{OUT}	---	12.5	---	%
Ripple Rejection	$PSRR_3$	f=10Hz~3kHz, Io=100mA, Normal mode	---	70	---	dB
Output Noise Voltage		f=10Hz~100kHz, Normal mode	---	45	---	UVrms
ECO exit time	t_{d3_ECO}	Minimum wait time to draw full current after leaving ECO mode	---	---	50	uS

Electrical characteristics (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Protection						
UVP Protection Fault Delay	t_{D_Fault}	DCDC1~DCDC7	128	---	---	mS
Thermal Shutdown Detect	T_{SD}		---	150	---	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		---	20	---	°C
Control Signal						
Logic-Input Threshold (PWRON_MODE, /PWRKEY, /SLEEP and /RESET)	V_{TH}	High threshold	1.4	---	---	V
	V_{TL}	Low threshold	---	---	0.5	V
Pull High Resistance (PWRON_MODE, /PWRKEY, /SLEEP and /RESET)	R_{PH}		---	100	---	KΩ
Open-Drain Output Low Voltage (PWRGD,/INT,)	V_{ODLOW}	I_{SINK}=5mA, V_{VCC}=3.7V	---	---	100	mV
Open-Drain Output Leakage Current (PWRGD./INT)	I_{LK_OD}	V_{OD}=5V	---	---	1	µA
PWRGD Delay Time	t_{RDLY_PWRGD}		---	8	---	mS
Re-start up Delay Time	$t_{DLY\_REBOOST}$		---	1	---	Sec
SMBus Interface						
Logic Input High Voltage	V_{IH}	SCL, SDA	1.4	---	---	V
Logic Input Low Voltage	V_{IL}	SCL, SDA	---	---	0.5	V
Logic Input Current		Logic inputs forced to VCC or GND	-2	---	2	µA
SMBus Input Capacitance		SCL, SDA	---	5	---	pF
SMBus Clock Frequency	f_{SCL}	Fast mode	---	---	400	kHz
		High-speed mode, load 400pF max	---	---	1.7	MHz
		High-speed mode, load 100pF max	---	---	3.4	MHz
SCL Clock Low Time	t_{LOW}	Fast mode	1.3	---	---	µS
SCL Clock High Time	t_{HIGH}	Fast mode	0.6	---	---	µS
SDA Setup Time	$t_{SU:DAT}$	Fast mode	100	---	---	nS
SDA Hold Time	$t_{HD:DAT}$	Fast mode	0	---	0.9	uS
Bus-Free Time from START and STOP	t_{BUF}	Fast mode	1.3	---	---	µS
Hold Time Repeated START Condition	$t_{HD:STA}$	Fast mode	0.6	---	---	µS
Setup Time Repeated START Condition	$t_{SU:STA}$	Fast mode	0.6	---	---	µS
Setup Time for STOP Condition	$t_{SU;STO}$	Fast mode	0.6	---	---	µS
Rise Time of SCL/SDA signals	t_r	10% to 90% points	20	---	300	nS
Fall Time of SCL/SDA signals	t_f	90% to 10% points	20	---	300	nS

Minimum Footprint PCB Layout Section

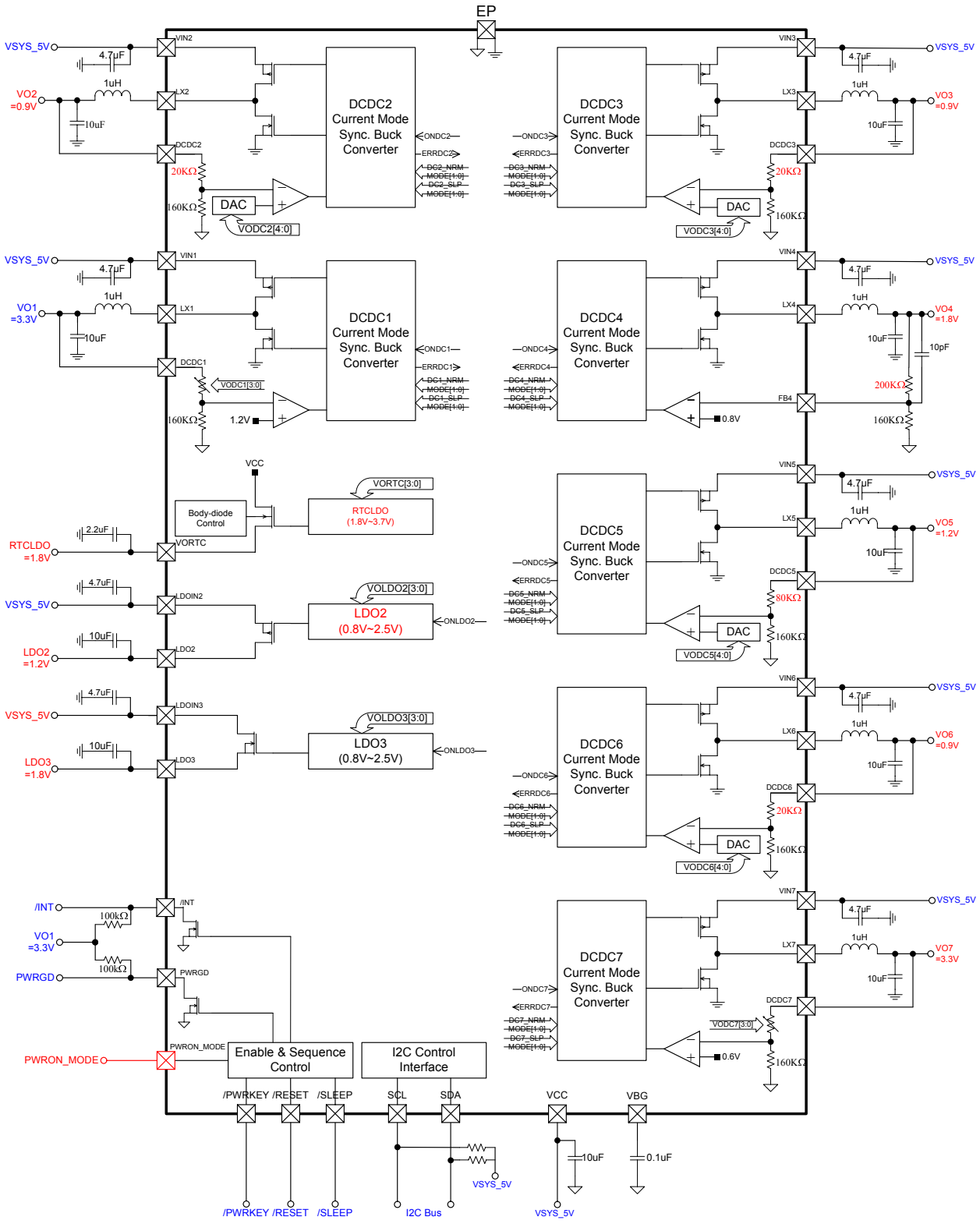
TQFN5X5-40



Pin Description

Pin No	Pin Name	Function
1	PWRON_MODE	Power ON/OFF Mode Select Pin. MODE=0: Mode1, MODE=Floating: Mode2.
2	VORTC	LDO Output of RTC LDO. Bypass this pin to ground with a 2.2uF ceramic capacitor.
3	VCC	IC Power Supply Input pin. Bypass with a 10uF or greater ceramic capacitor.
4	LDO3	LDO Output of LDO3.
5	LDOIN3	Power Input of LDO3.
6	VBG	1.23v Reference Voltage Output. Bypass this pin to ground with a 0.1µF ceramic capacitor.
7	LDO2	LDO Output of LDO2.
8	LDOIN2	Power Input of LDO2.
9,10	NC	No Connection
11,12	LX2	Inductor switch node of DCDC2 Buck Converter.
13	VIN2	Power Input of DCDC2 Buck Converter.
14	DCDC2	Sensing Input of DCDC2 Buck Converter's output voltage.
15	/PWRKEY	Power on/off key. Internal pull high to VCC.
16	DCDC3	Sensing Input of DCDC3 Buck Converter's output voltage.
17	VIN3	Power Input of DCDC3 Buck Converter.
18	LX3	Inductor switch node of DCDC3 Buck Converter.
19	SCL	Clock Input PIN of I^2C interface.
20	SDA	Data Input PIN of I^2C interface.
21	LX4	Inductor switch node of DCDC4 Buck Converter.
22	VIN4	Power Input of DCDC4 Buck Converter.
23	PWRGD	Indicator of PMU power on/off with open drain output.
24	FB4	Feedback Input of DCDC4 Buck Converter.
25	DCDC5	Sensing Input of DCDC5 Buck Converter's output voltage.
26	VIN5	Power Input of DCDC5 Buck Converter.
27	LX5	Inductor switch node of DCDC5 Buck Converter.
28,29	LX6	Inductor switch node of DCDC6 Buck Converter.
30	VIN6	Power Input of DCDC6 Buck Converter.
31	DCDC6	Sensing Input of DCDC6 Buck Converter's output voltage.
32	/INT	Interrupt Indicator with open drain output.
33	/RESET	RESET PIN of G2249. Internal pull high to VCC.
34	LX1	Inductor switch node of DCDC1 Buck Converter.
35	VIN1	Power Input of DCDC1 Buck Converter.
36	DCDC1	Sensing Input of DCDC1 Buck Converter's output voltage.
37	/SLEEP	SLEEP mode control pin. Internal pull high to VCC.
38	DCDC7	Sensing Input of DCDC7 Buck Converter's output voltage.
39	VIN7	Power Input of DCDC7 Buck Converter.
40	LX7	Inductor switch node of DCDC7 Buck Converter.
EP	VSSA, VSSD, PGNDX	All converters' power ground and chip analog ground. For good thermal dissipation, connect EP to the power and analog ground plane.

Block Diagram & Application Circuit



I2C Interface

G2249 I2C slave address=7'b0010010. The write or read bit stream (N≥1) is shown below:

Driven by Master

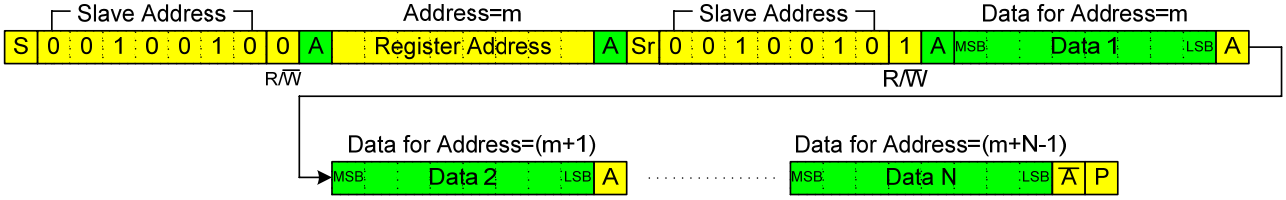
Driven by G2249

S Start

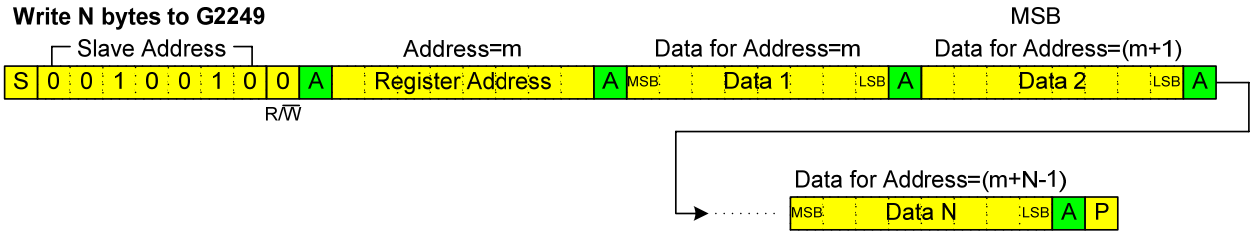
P Stop

Sr Repeat Start

Read N bytes from G2249



Write N bytes to G2249



I2C Register Map

ADDR	Byte Name		Data							
			b7	b6	b5	b4	b3	b2	b1	b0
0x00	INTR	Meaning	INT		PWRKEY	PWRKEY_LP	PWRKEY_IT			
		Default	0		0	0	0			
		Read/Write	R/W		R	R	R			
0x01	INTR _MASK	Meaning			MASK _PWRKEY	MASK_LP	MASK_IT			
		Default			0	0	0			
		Read/Write			R/W	R/W	R/W			
0x02	PWRKEY CONTROL	Meaning	LPOFF_TO_ DO	ENLPOFF	TIME_IT[1:0]		TIME_LP[1:0]		TIME_LPOFF[1:0]	
		Default	1	1	0	0	1	1	1	1
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x03	DCDC Fault Status	Meaning	ERRDC1	ERRDC2	ERRDC3	ERRDC4	ERRDC5	ERRDC6	ERRDC7	
		Default	0	0	0	0	0	0	0	
		Read/Write	R	R	R	R	R	R	R	
0x04	LDO Fault Status	Meaning							ERRLDO2	ERRLDO3
		Default							0	0
		Read/Write							R	R
0x05	SYS _Control	Meaning	SOFTOFF		RST_ERR	FSEL	VORTC[3:0]			
		Default	0		0	0	0	0	0	0
		Read/Write	R/W		R/W	R/W	R/W	R/W	R/W	R/W
0x06	DCDC _ONOFF CONTROL	Meaning	ONDC1	ONDC2	ONDC3	ONDC4	ONDC5	ONDC6	ONDC7	
		Default	1	1	1	1	1	1	0	
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0x07	LDO _ONOFF CONTROL	Meaning							ONLDO2	ONLDO3
		Default							1	1
		Read/Write							R/W	R/W
0x08	DCDC _DISCHG CONTROL	Meaning	ENDIS_DC1	ENDIS_DC2	ENDIS_DC3	ENDIS_DC4	ENDIS_DC5	ENDIS_DC6	ENDIS_DC7	
		Default	1	1	1	1	1	1	1	
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0x09	LDO _DISCHG CONTROL	Meaning							ENDIS_L2	ENDIS_L3
		Default							1	1
		Read/Write							R/W	R/W
0x0A	DC1DC2 _MODE CONTROL	Meaning	DC1_NRMMODE[1:0]		DC1_SLPMODE[1:0]		DC2_NRMMODE[1:0]		DC2_SLPMODE[1:0]	
		Default	0	0	1	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x0B	DC3DC4 _MODE CONTROL	Meaning	DC3_NRMMODE[1:0]		DC3_SLPMODE[1:0]		DC4_NRMMODE[1:0]		DC4_SLPMODE[1:0]	
		Default	0	0	1	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x0C	DC5DC6 _MODE CONTROL	Meaning	DC5_NRMMODE[1:0]		DC5_SLPMODE[1:0]		DC6_NRMMODE[1:0]		DC6_SLPMODE[1:0]	
		Default	0	0	1	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x0D	DC7 _MODE CONTROL	Meaning	DC7_NRMMODE[1:0]		DC7_SLPMODE[1:0]					
		Default	0	0	1	0				
		Read/Write	R/W	R/W	R/W	R/W				
0x0E	LDO2LDO3 _MODE CONTROL	Meaning	LDO2_NRMMODE[1:0]		LDO2_SLPMODE[1:0]		LDO3_NRMMODE[1:0]		LDO3_SLPMODE[1:0]	
		Default	0	0	1	0	0	0	1	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x0F	DCDC1 _NRMVOLT	Meaning					VODC1_NRM[3:0]			
		Default					1	0	1	1
		Read/Write					R/W	R/W	R/W	R/W
0x10	DCDC2 _NRMVOLT	Meaning				VODC2_NRM[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x11	DCDC3 _NRMVOLT	Meaning				VODC3_NRM[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x12	DCDC5 _NRMVOLT	Meaning				VODC5_NRM[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x13	DCDC6 _NRMVOLT	Meaning				VODC6_NRM[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x14	DCDC7 _NRMVOLT	Meaning					VODC7_NRM[3:0]			
		Default					1	1	1	1
		Read/Write					R/W	R/W	R/W	R/W
0x15	LDO _NRMVOLT	Meaning	VOLDO2_NRM[3:0]				VOLDO3_NRM[3:0]			
		Default	0	1	1	1	1	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

I2C Register Map (continued)

ADDR	Byte Name		Data							
			b7	b6	b5	b4	b3	b2	b1	b0
0x16	DCDC1 _SLPVOLT	Meaning					VODC1_SLP[3:0]			
		Default					1	0	1	1
		Read/Write					R/W	R/W	R/W	R/W
0x17	DCDC2 _SLPVOLT	Meaning				VODC2_SLP[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x18	DCDC3 _SLPVOLT	Meaning				VODC3_SLP[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x19	DCDC5 _SLPVOLT	Meaning				VODC5_SLP[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x1A	DCDC6 _SLPVOLT	Meaning				VODC6_SLP[4:0]				
		Default				1	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W
0x1B	DCDC7 _SLPVOLT	Meaning					VODC7_SLP[3:0]			
		Default					1	1	1	1
		Read/Write					R/W	R/W	R/W	R/W
0x1C	LDO _SLPVOLT	Meaning	VOLDO2_SLP[3:0]				VOLDO3_SLP[3:0]			
		Default	0	1	1	1	1	1	0	0
		Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x1D	CHIP_ID	Meaning			CHIP_ID[5:0]					
		Default			1	1	0	0	0	1
		Read/Write			R	R	R	R	R	R
0x1E	VERSION	Meaning					VERSION[3:0]			
		Default					0	0	0	0
		Read/Write					R	R	R	R
0xF1	GMT Testing	Meaning				TM[5:1]				
		Default				0	0	0	0	0
		Read/Write				R/W	R/W	R/W	R/W	R/W

I2C Register Reset Conditions

ADDR.	Register Function	Rest Condition
0x00	Interrupt Registers	VCC<3.0V, or the power-off reset pulse. Also reset by reading them
0x02	Power-key IT/LP/LPOFF Registers	VCC<3.0V, or the power-on leading pulse
0x03,0x04,0x05[5]	DCDC&LDO Fault Status	VCC<3.0V or 0x05[5] is written to 1
0x05[7]	SOFTOFF	VCC<3.0V, or the power-on leading pulse
0x08,0x09	DCDC and LDO enable discharge Registers	VCC<3.0V, or the power-on leading pulse
Other Registers		VCC<3.0V, or the power-off reset pulse.

I2C Register Function Table

Interrupt and Status

ADDR	Data Bit	Data Name	Function Description
0x00	b7	INT	INT is used to control the output status of /INT pin. When interrupt events happen, /INT pin goes low and this bit is set to 1'b1. After Micro-processor write the bit to be 1'b0, /INT pin goes to high-Z state. INT: 0 = Hi-Z, 1 = Low
0x00	b5	PWRKEY	PWRKEY is used to record the /PWRKEY pin status has changed since last read.
0x00	b4	PWRKEY_LP	PWRKEY_LP is used to record the /PWRKEY pin long press status. PWRKEY_LP is reset to 0 when this byte is read each time. This bit is also reset to 0 at each /PWRKEY pin falling edge or VCC plug-in/out. PWRKEY_LP: 0 = NO, 1 = YES ($T>T_{dPWRKEYLP}$)
0x00	b3	PWRKEY_IT	PWRKEY_IT is used to record the /PWRKEY pin falling status. PWRKEY_IT is reset to 0 when this byte is read each time. This bit is reset to 0 at each /PWRKEY pin falling edge or VCC plug-in/out. PWRKEY_IT: 0 = NO, 1 = YES ($T>T_{dbPWRKEYF}$)
0x01	b5	MASK _PWRKEY	By writing 1'b1 to MASK_PWRKEY to disable asserting /INT low when the event of /PWRKEY pin is toggled low occurs.
0x01	b4	MASK_LP	By writing 1'b1 to MASK_LP to disable asserting /INT low when the event of /PWRKEY pin is toggled low with duration longer than TdPWRKEYLP occurs.
0x01	b3	MASK_IT	By writing 1'b1 to MASK_IT to disable asserting /INT low when the event of /PWRKEY pin is toggled low duration longer than TdbPWRKEYF occurs.

Software PMIC ON/OFF Control

ADDR	Data Bit	Data Name	Function Description
0x05	b7	SOFTOFF	Write 1 to SOFTOFF to perform power-off sequence when PMIC is in operation mode.

Power-Key Function and Timing Control

ADDR	Data Bit	Data Name	Function Description
0x02	b7	LPOFF_TO_DO	Setting PMIC operating mode after it finishes power-off sequence caused by /PWRKEY pin long pressed with duration longer than $T_{dPWRKEYLPOFF}$. Default=1'b1 LPOFF_TO_DO: 0 = Remain in shutdown mode; ***1*** = ***Re-startup by sequence***
0x02	b6	ENLPOFF	Enable PMIC shutdown when /PWRKEY pin long pressed with duration longer than $T_{dPWRKEYLPOFF}$ defined by register TIME_LPOFF[1:0]. Default=1'b1 $T>T_{dPWRKEYLPOFF}$: 0 = NO; ***1*** = ***YES***
0x02	b5,b4	TIME_IT [1:0]	TIME_IT[1:0] is used to defined the /PWRKEY pin falling-edge de-bouncing delay time $T_{dbPWRKEYF}$. When /PWRKEY pin is toggled low with duration longer than $T_{dbPWRKEYF}$, PMIC enters power-on process and the register PWRKEY_IT is 1'b1. Default=2'b00 TIME_IT[1:0]: ***00*** = ***128mS***; 01 = 0.5S; 10 = 1.0S; 11 = 1.5S
0x02	b3,b2	TIME_LP [1:0]	TIME_LP[1:0] is used to defined the /PWRKEY pin long-press delay time $T_{dPWRKEYLP}$. When /PWRKEY pin is toggled low with duration longer than $T_{dPWRKEYLP}$, the register PWRKEY_LP is 1'b1. Default=2'b00 TIME_LP[1:0]: 00 = 0.5S; 01 = 1.0S; 10 = 1.5S; ***11*** = ***2.0S***
0x02	b1,b0	TIME_LPOFF [1:0]	TIME_LPOFF[1:0] is used to defined the /PWRKEY pin long-press delay time $T_{dPWRKEYLPOFF}$. When /PWRKEY pin is toggled low with duration longer than $T_{dPWRKEYLPOFF}$, PMIC enters power-off process. The function of /PWRKEY pin long-press delay to turn off PMIC can be inactive by writing 0 to the register ENLPOFF. Default=2'b00 TIME_LPOFF[1:0]: 00 = 1.0S; 01 = 2.0S; 10 = 3.0S; ***11*** = ***4.0S***

Fault Status of DCDC Converters and LDOs

ADDR	Data Bit	Data Name	Function Description
0x03	b7~b1	ERRDCX	Record whether the UVP protection of DCDC1~DCDC7 ever occurs respectively. ERRDCx: 0 = NO; 1 = YES
0x04	b1~b0	ERRLDOx	Record whether the UVP protection of LDO2~LDO3 ever occurs respectively. ERRLDOx: 0 = NO; 1 = YES
0x05	b5	RST_ERR	Write 1 to this bit to reset 0x03 and 0x04 to 0.

ON/OFF Control of DCDC Converters and LDOs

ADDR	Data Bit	Data Name	Function Description
0x06	b7~ b1	ONDCx	DCDC1~DCDC7 Enable Signal. ONDCx: 0 = Shutdown; ***1*** = ***Operation***
0x07	b1~ b0	ONLDOx	LDO2~LDO3 Enable Signal. ONLDOx: 0 = Shutdown; ***1*** = ***Operation***

Discharge Function of DCDC Converters and LDOs

ADDR	Data Bit	Data Name	Function Description
0x08	b7~ b1	ENDIS_DCx	Enable DCDC output discharge function during PMIC in shutdown mode. Default=1'b1 DCDC converter still has discharge function during power-off procedure even this bit is written to 0 ENDIS_DCx: 0 = Disable; ***1*** = ***Enable***
0x09	b1~ b0	ENDIS_Lx	Enable LDO output discharge function. Default=1'b1 ENDIS_Lx: 0 = Disable; ***1*** = ***Enable***

Mode Control of DCDC1~DCDC7

ADDR	Data Bit	Data Name	Function Description
0x0A 0x0B 0x0C 0x0D	b7,b6 b3,b2	DCx _NRMMODE [1:0]	Setting the operating mode of DCDC1~DCDC7 when /SLEEP pin is toggled high. Default=2'b00 DCx_NRMMODE[1:0]: ***00*** = ***Auto PWM/PSM with ECO***; 01 = ***Auto PWM/PSM with ECO***; 10 = Force PWM; 11 = Auto PWM/PSM w/o ECO
0x0A 0x0B 0x0C 0x0D	b5,b4 b1,b0	DC1~3, DC5~7 _SLPMODE [1:0]	Setting the DCDC1, DCDC2, DCDC3, DCDC5, DCDC6 and DCDC7s' operating mode, and output voltage configuration when /SLEEP pin is toggled low. Default=2'b10 DCx_SLPMODE[1:0]: 00 = Auto PWM/PSM w/o ECO, VODCx_NRM[x:0]; 01 = ***Auto PWM/PSM with ECO***, VODCx_NRM[x:0]; ***10*** = ***Auto PWM/PSM with ECO***, ***VODCx_SLP[x:0]***; 11 = shutdown, X
0x0B	b1,b0	DC4 _SLPMODE [1:0]	Setting the operating mode of DCDC4 when /SLEEP pin is toggled low. Default=2'b10 DC4_SLPMODE[1:0]: 00 = Auto PWM/PSM w/o ECO; 01 = ***Auto PWM/PSM with ECO***; ***10*** = ***Auto PWM/PSM with ECO***; 11 = shutdown

Mode Control of LDO2,LDO3

<table>
<tr><th>ADDR</th><th>Data Bit</th><th>Data Name</th><th>Function Description</th></tr>
<tr><td>0x0E</td><td>b7,b6
b3,b2</td><td>LDOx
_NRMMODE
[1:0]</td><td>Setting the LDOs' operating mode and output voltage when /SLEEP pin is toggled high.
Default=2'b00
<table>
<tr><th>LDOx_NRMMODE[1:0]</th><th>MODE</th><th>Output Voltage</th></tr>
<tr><td>00</td><td rowspan="2">Normal</td><td rowspan="2">VOLDOx_NRM [3:0]</td></tr>
<tr><td>01</td></tr>
<tr><td>10</td><td>ECO</td><td>VOLDOx_NRM[3:0]</td></tr>
<tr><td>11</td><td>Normal</td><td>VOLDOx_NRM [3:0]</td></tr>
</table></td></tr>
<tr><td>0x0E</td><td>b5,b4
b1,b0</td><td>LDOx
_SLPMODE
[1:0]</td><td>Setting the LDOs' operating mode and output voltage when /SLEEP pin is toggled low,
Default=2'b10
<table>
<tr><th>LDOx_SLPMODE[1:0]</th><th>MODE</th><th>Output Voltage</th></tr>
<tr><td>00</td><td>Normal</td><td>VOLDOx_NRM [3:0]</td></tr>
<tr><td>01</td><td>Normal</td><td>VOLDOx_SLP [3:0]</td></tr>
<tr><td>10</td><td>ECO</td><td>VOLDOx_SLP[3:0]</td></tr>
<tr><td>11</td><td>Shutdown</td><td>X</td></tr>
</table></td></tr>
</table>

Voltage Control of RTCLDO

<table>
<tr><th>ADDR</th><th>Data Bit</th><th>Data Name</th><th>Function Description</th></tr>
<tr><td>0x05</td><td>b3~b0</td><td>VORTC[3:0]</td><td>Setting the output voltage of RTCLDO, Default=4'b0000
<table>
<tr><th>VORTC [3:0]</th><th>VORTC</th><th>VORTC [3:0]</th><th>VORTC</th><th>VORTC [3:0]</th><th>VORTC</th><th>VORTC [3:0]</th><th>VORTC</th></tr>
<tr><td>1111</td><td>3.7V</td><td>1011</td><td>3.3V</td><td>0111</td><td>2.9V</td><td>0011</td><td>2.5V</td></tr>
<tr><td>1110</td><td>3.6V</td><td>1010</td><td>3.2V</td><td>0110</td><td>2.8V</td><td>0010</td><td>2.4V</td></tr>
<tr><td>1101</td><td>3.5V</td><td>1001</td><td>3.1V</td><td>0101</td><td>2.7V</td><td>0001</td><td>2.3V</td></tr>
<tr><td>1100</td><td>3.4V</td><td>1000</td><td>3.0V</td><td>0100</td><td>2.6V</td><td>0000</td><td>1.8V</td></tr>
</table></td></tr>
</table>

Voltage Control of LDO2, LDO3

<table>
<tr><th>ADDR</th><th>Data Bit</th><th>Data Name</th><th>Function Description</th></tr>
<tr><td>0x15
0x1C</td><td>b7~b4</td><td>VOLDO2
_NRM[3:0]
/VOLDO2
_SLP[3:0]</td><td>Setting the output voltage of LDO2,
VOLDO2_NRM/VOLDO2_SLP Default=4'b0111
<table>
<tr><th>VOLDO2_ [3:0]</th><th>LDO2</th><th>VOLDO2_ [3:0]</th><th>LDO2</th><th>VOLDO2_ [3:0]</th><th>LDO2</th><th>VOLDO2_ [3:0]</th><th>LDO2</th></tr>
<tr><td>1111</td><td>2.5V</td><td>1011</td><td>1.7V</td><td>0111</td><td>1.2V</td><td>0011</td><td>0.95V</td></tr>
<tr><td>1110</td><td>2.0V</td><td>1010</td><td>1.6V</td><td>0110</td><td>1.1V</td><td>0010</td><td>0.90V</td></tr>
<tr><td>1101</td><td>1.9V</td><td>1001</td><td>1.5V</td><td>0101</td><td>1.05V</td><td>0001</td><td>0.85V</td></tr>
<tr><td>1100</td><td>1.8V</td><td>1000</td><td>1.3V</td><td>0100</td><td>1.0V</td><td>0000</td><td>0.80V</td></tr>
</table></td></tr>
<tr><td>0x15
0x1C</td><td>b3~b0</td><td>VOLDO3
_NRM[3:0]
/VOLDO3
_SLP[3:0]</td><td>Setting the output voltage of LDO3,
VOLDO3_NRM/VOLDO3_SLP Default=4'b1100
<table>
<tr><th>VOLDO3_ [3:0]</th><th>LDO3</th><th>VOLDO3_ [3:0]</th><th>LDO3</th><th>VOLDO3_ [3:0]</th><th>LDO3</th><th>VOLDO3_ [3:0]</th><th>LDO3</th></tr>
<tr><td>1111</td><td>2.5V</td><td>1011</td><td>1.7V</td><td>0111</td><td>1.2V</td><td>0011</td><td>0.95V</td></tr>
<tr><td>1110</td><td>2.0V</td><td>1010</td><td>1.6V</td><td>0110</td><td>1.1V</td><td>0010</td><td>0.90V</td></tr>
<tr><td>1101</td><td>1.9V</td><td>1001</td><td>1.5V</td><td>0101</td><td>1.05V</td><td>0001</td><td>0.85V</td></tr>
<tr><td>1100</td><td>1.8V</td><td>1000</td><td>1.3V</td><td>0100</td><td>1.0V</td><td>0000</td><td>0.80V</td></tr>
</table></td></tr>
</table>

Voltage Control of DCDC1~DCDC7

<table>
<tr><th>ADDR</th><th>Data Bit</th><th>Data Name</th><th>Function Description</th></tr>
<tr><td>0x0F
0x16</td><td>b3~b0</td><td>VODC1
_NRM[3:0]
/VODC1
_SLP[3:0]</td><td>Setting the output voltage of DCDC1 in Normal/Sleep mode, Default=4’b1011
<table>
<tr><th>VODC1 [3:0]</th><th>VO1</th><th>VODC1 [3:0]</th><th>VO1</th><th>VODC1 [3:0]</th><th>VO1</th><th>VODC1 [3:0]</th><th>VO1</th></tr>
<tr><td>1111</td><td>3.7V</td><td>1011</td><td>3.3V</td><td>0111</td><td>2.9V</td><td>0011</td><td>2.5V</td></tr>
<tr><td>1110</td><td>3.6V</td><td>1010</td><td>3.2V</td><td>0110</td><td>2.8V</td><td>0010</td><td>2.4V</td></tr>
<tr><td>1101</td><td>3.5V</td><td>1001</td><td>3.1V</td><td>0101</td><td>2.7V</td><td>0001</td><td>2.3V</td></tr>
<tr><td>1100</td><td>3.4V</td><td>1000</td><td>3.0V</td><td>0100</td><td>2.6V</td><td>0000</td><td>2.2V</td></tr>
</table></td></tr>
<tr><td>0x10
0x11
0x13
0x17
0x18
0x1A</td><td>b4~b0</td><td>VODCx
_NRM[4:0]
/VODCx
_SLP[4:0]</td><td>Setting the feedback reference voltage of DCDC2, DCDC3 and DCDC6 in Normal/Sleep mode. VOx=VFBx x1.125, Default=5’b10000
VFBx=0.64V + 10mV x Value, VOx=0.72V + 11.25mV x Value, where Value is 5-bit binary code
<table>
<tr><th>FBDCX[4:0]</th><th>VFBX</th><th>VOX</th><th>FBDCX[4:0]</th><th>VFBX</th><th>VOX</th></tr>
<tr><td>11111</td><td>0.95V</td><td>1.06875V</td><td>01111</td><td>0.79V</td><td>0.88875V</td></tr>
<tr><td>11110</td><td>0.94V</td><td>1.0575V</td><td>01110</td><td>0.78V</td><td>0.8775V</td></tr>
<tr><td>11101</td><td>0.93V</td><td>1.04625V</td><td>01101</td><td>0.77V</td><td>0.86625V</td></tr>
<tr><td>11100</td><td>0.92V</td><td>1.035V</td><td>01100</td><td>0.76V</td><td>0.855V</td></tr>
<tr><td>11011</td><td>0.91V</td><td>1.02375V</td><td>01011</td><td>0.75V</td><td>0.84375V</td></tr>
<tr><td>11010</td><td>0.90V</td><td>1.0125V</td><td>01010</td><td>0.74V</td><td>0.8325V</td></tr>
<tr><td>11001</td><td>0.89V</td><td>1.00125V</td><td>01001</td><td>0.73V</td><td>0.82125V</td></tr>
<tr><td>11000</td><td>0.88V</td><td>0.99V</td><td>01000</td><td>0.72V</td><td>0.81V</td></tr>
<tr><td>10111</td><td>0.87V</td><td>0.97875V</td><td>00111</td><td>0.71V</td><td>0.79875V</td></tr>
<tr><td>10110</td><td>0.86V</td><td>0.9675V</td><td>00110</td><td>0.70V</td><td>0.7875V</td></tr>
<tr><td>10101</td><td>0.85V</td><td>0.95625V</td><td>00101</td><td>0.69V</td><td>0.77625V</td></tr>
<tr><td>10100</td><td>0.84V</td><td>0.945V</td><td>00100</td><td>0.68V</td><td>0.765V</td></tr>
<tr><td>10011</td><td>0.83V</td><td>0.93375V</td><td>00011</td><td>0.67V</td><td>0.75375V</td></tr>
<tr><td>10010</td><td>0.82V</td><td>0.9225V</td><td>00010</td><td>0.66V</td><td>0.7425V</td></tr>
<tr><td>10001</td><td>0.81V</td><td>0.91125V</td><td>00001</td><td>0.65V</td><td>0.73125V</td></tr>
<tr><td>10000</td><td>0.80V</td><td>0.9V</td><td>00000</td><td>0.64V</td><td>0.72V</td></tr>
</table></td></tr>
<tr><td>0x12
0x19</td><td>b4~b0</td><td>VODC5
_NRM[4:0]
/VODC5
_SLP[4:0]</td><td>Setting the feedback reference voltage of DCDC5 in Normal/Sleep mode. VOx=VFBx x1.5, Default=5’b10000
VFBx=0.64V + 10mV x Value, VOx=0.96V + 15mV x Value, where Value is 5-bit binary code
<table>
<tr><th>FBDCX[4:0]</th><th>VFBX</th><th>VOX</th><th>FBDCX[4:0]</th><th>VFBX</th><th>VOX</th></tr>
<tr><td>11111</td><td>0.95V</td><td>1.425V</td><td>01111</td><td>0.79V</td><td>1.185V</td></tr>
<tr><td>11110</td><td>0.94V</td><td>1.41V</td><td>01110</td><td>0.78V</td><td>1.17V</td></tr>
<tr><td>11101</td><td>0.93V</td><td>1.395V</td><td>01101</td><td>0.77V</td><td>1.155V</td></tr>
<tr><td>11100</td><td>0.92V</td><td>1.38V</td><td>01100</td><td>0.76V</td><td>1.14V</td></tr>
<tr><td>11011</td><td>0.91V</td><td>1.365V</td><td>01011</td><td>0.75V</td><td>1.125V</td></tr>
<tr><td>11010</td><td>0.90V</td><td>1.35V</td><td>01010</td><td>0.74V</td><td>1.11V</td></tr>
<tr><td>11001</td><td>0.89V</td><td>1.335V</td><td>01001</td><td>0.73V</td><td>1.095V</td></tr>
<tr><td>11000</td><td>0.88V</td><td>1.32V</td><td>01000</td><td>0.72V</td><td>1.08V</td></tr>
<tr><td>10111</td><td>0.87V</td><td>1.305V</td><td>00111</td><td>0.71V</td><td>1.065V</td></tr>
<tr><td>10110</td><td>0.86V</td><td>1.29V</td><td>00110</td><td>0.70V</td><td>1.05V</td></tr>
<tr><td>10101</td><td>0.85V</td><td>1.275V</td><td>00101</td><td>0.69V</td><td>1.035V</td></tr>
<tr><td>10100</td><td>0.84V</td><td>1.26V</td><td>00100</td><td>0.68V</td><td>1.02V</td></tr>
<tr><td>10011</td><td>0.83V</td><td>1.245V</td><td>00011</td><td>0.67V</td><td>1.005V</td></tr>
<tr><td>10010</td><td>0.82V</td><td>1.23V</td><td>00010</td><td>0.66V</td><td>0.99V</td></tr>
<tr><td>10001</td><td>0.81V</td><td>1.215V</td><td>00001</td><td>0.65V</td><td>0.975V</td></tr>
<tr><td>10000</td><td>0.80V</td><td>1.2V</td><td>00000</td><td>0.64V</td><td>0.96V</td></tr>
</table></td></tr>
</table>

<table>
<tr>
<td>0x14
0x1B</td>
<td>b3~b0</td>
<td>VODC7
_NRM[3:0]
/VODC7
_SLP[3:0]</td>
<td>Setting the output voltage of DCDC7 in Normal/Sleep mode, Default=4’b1111
<table>
<tr><td>VODC7
[3:0]</td><td>VO7</td><td>VODC7
[3:0]</td><td>VO7</td><td>VODC7
[3:0]</td><td>VO7</td><td>VODC7
[3:0]</td><td>VO7</td></tr>
<tr><td>1111</td><td>3.3V</td><td>1011</td><td>1.7V</td><td>0111</td><td>1.2V</td><td>0011</td><td>0.95V</td></tr>
<tr><td>1110</td><td>2.8V</td><td>1010</td><td>1.6V</td><td>0110</td><td>1.1V</td><td>0010</td><td>0.90V</td></tr>
<tr><td>1101</td><td>1.9V</td><td>1001</td><td>1.5V</td><td>0101</td><td>1.05V</td><td>0001</td><td>0.85V</td></tr>
<tr><td>1100</td><td>1.8V</td><td>1000</td><td>1.3V</td><td>0100</td><td>1.0V</td><td>0000</td><td>0.80V</td></tr>
</table>
</td>
</tr>
</table>

DCDC2 Operating Frequency Control

<table>
<tr><th>ADDR</th><th>Data Bit</th><th>Data Name</th><th>Function Description</th></tr>
<tr>
<td>0x05</td>
<td>b4</td>
<td>FSEL</td>
<td>DCDC2 Operating Frequency Control. Default=1’b0
<table>
<tr><td>FSEL</td><td>Frequency</td></tr>
<tr><td>0</td><td>1.5MHz</td></tr>
<tr><td>1</td><td>3.0MHz</td></tr>
</table>
</td>
</tr>
</table>

Version Code of G2249

ADDR	Data Bit	Data Name	Function Description
0x1D	b5~b0	CHIP_ID [5:0]	CHIP_ID[5:0] is the identification code of G2249, code=6’b110001
0x1E	b3~b0	VERSION [3:0]	VERSION[3:0] is the version code of G2249

FUNCTION DESCRIPTION

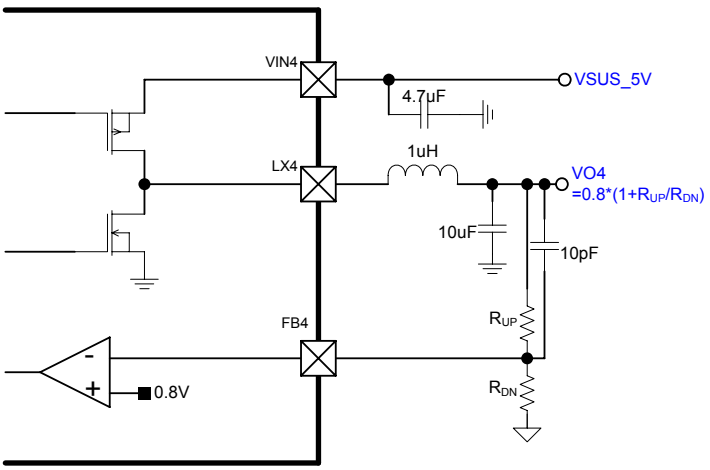
PMU

The G2249 includes 7 DC/DC Converter, and 3 LDO regulators to generate a multiple-output power-supply system.

	Topology	Default V_{OUT}	V_{OUT} range	Current rating	ON/OFF Control
DCDC1	3MHz Sync. Buck Converter	3.3V	16-steps voltages from 2.2v to 3.7v configured by I^2C	2.0A	Controlled by register bit ONDC1
DCDC2	1.5MHz Sync. Buck Converter	0.9V	32-steps DVS from 0.72v to 1.06875v configured by I^2C	3.0A	Controlled by register bit ONDC2
DCDC3	3MHz Sync. Buck Converter	0.9V	32-steps DVS from 0.72v to 1.06875v configured by I^2C	2.0A	Controlled by register bit ONDC3
DCDC4	3MHz Sync. Buck Converter	1.8V	Configured by FB4 pin resistors.	2.0A	Controlled by register bit ONDC4
DCDC5	3MHz Sync. Buck Converter	1.2V	32-steps DVS from 0.96v to 1.425v configured by I^2C	2.0A	Controlled by register bit ONDC5
DCDC6	3MHz Sync. Buck Converter	0.9V	32-steps DVS from 0.72v to 1.06875v configured by I^2C	2.0A	Controlled by register bit ONDC6
DCDC7	3MHz Sync. Buck Converter	3.3V	16-steps voltages from 0.8v to 3.3v configured by I^2C	2.0A	Controlled by register bit ONDC7
LDO1	RTC LDO	1.8V	16-steps voltages from 1.8v to 3.7v configured by I^2C	50mA	Always ON
LDO2	PMOS LDO	1.2V	16-steps voltages from 0.8v to 2.5v configured by I^2C	600mA	Controlled by register bit ONLDO2
LDO3	NMOS LDO	1.8V	16-steps voltages from 0.8v to 2.5v configured by I^2C	600mA	Controlled by register bit ONLDO3

DCDC4 Output Voltage Setting

The output voltage of DCDC4 is decided according to the resistor R_{UP} connecting between FB4 to converter's output voltage, and the resistor R_{DN} connecting between FB4 to ground. The suggesting resistance of R_{DN} is 160kΩ.



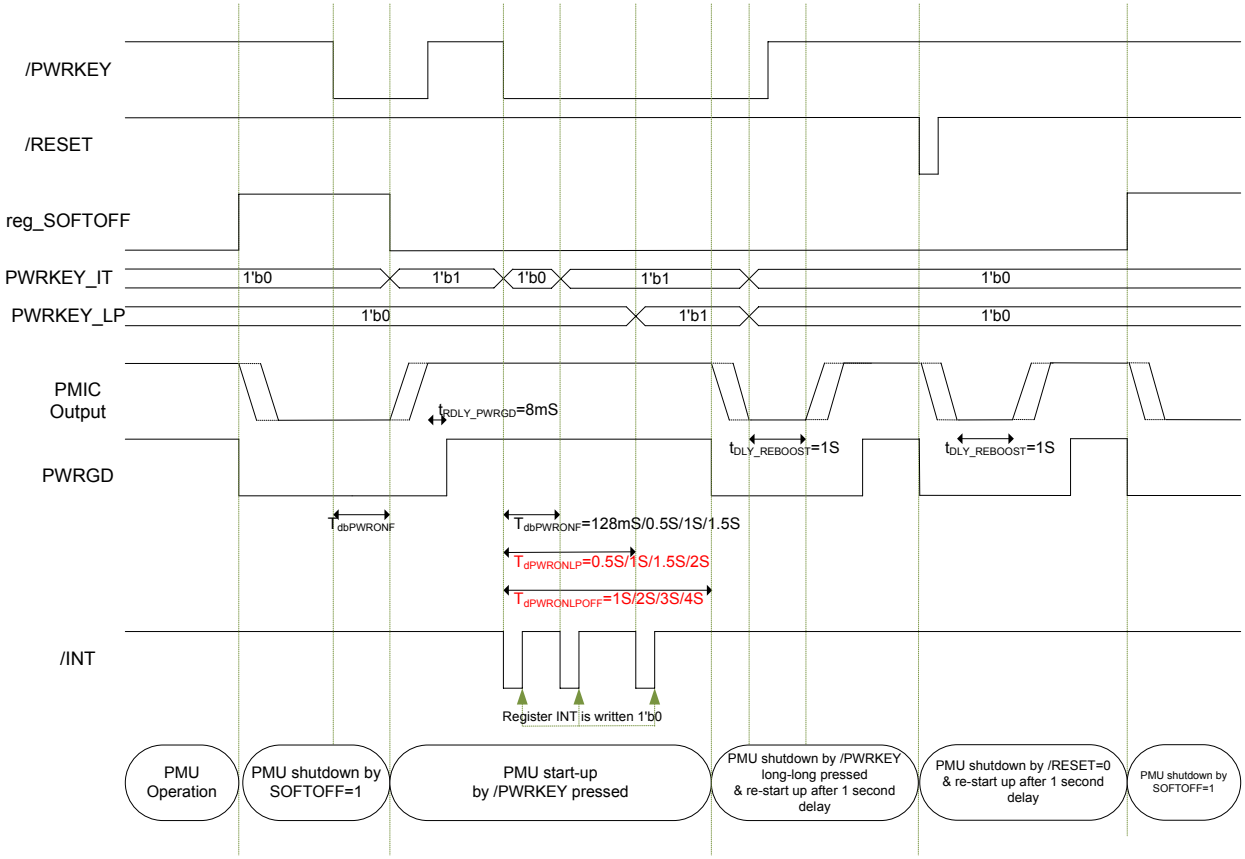
PMU Power ON/OFF Initiation (PWRON_MODE=0)

The following conditions are available to turn on the PMU of G2249:

- /PWRKEY pin is low-level pressed with duration longer than $T_{dbPWRKEYF}$
- After 1 second delay from shutdown of G2249 caused by /PWRKEY pin is long-long pressed with duration longer than $T_{dPWRKEYLPOFF,}$ and register ENLPOFF=1'b1, LPOFF_TO_DO=1'b1.
- After 1 second delay from shutdown of G2249 caused by toggling /RESET pin low.
- The voltage applied in VCC pin is higher than $V_{VCC\_UVLO}+V_{VCC\_UVLOHYS}$ (3.5V typ.)

The following conditions are available to turn off the PMU of G2249:

- /PWRKEY pin is low-level pressed with duration longer than $T_{dPWRKEYLPOFF}$ (if ENLPOFF=1'b1)
- Write 1 to register SOFTOFF after PWRGD is turned high.
- /RESET pin is toggle low.
- Output voltage UVP of DCDC converters occurs with duration longer than 128mS
- G2249 thermal shutdown occurs.



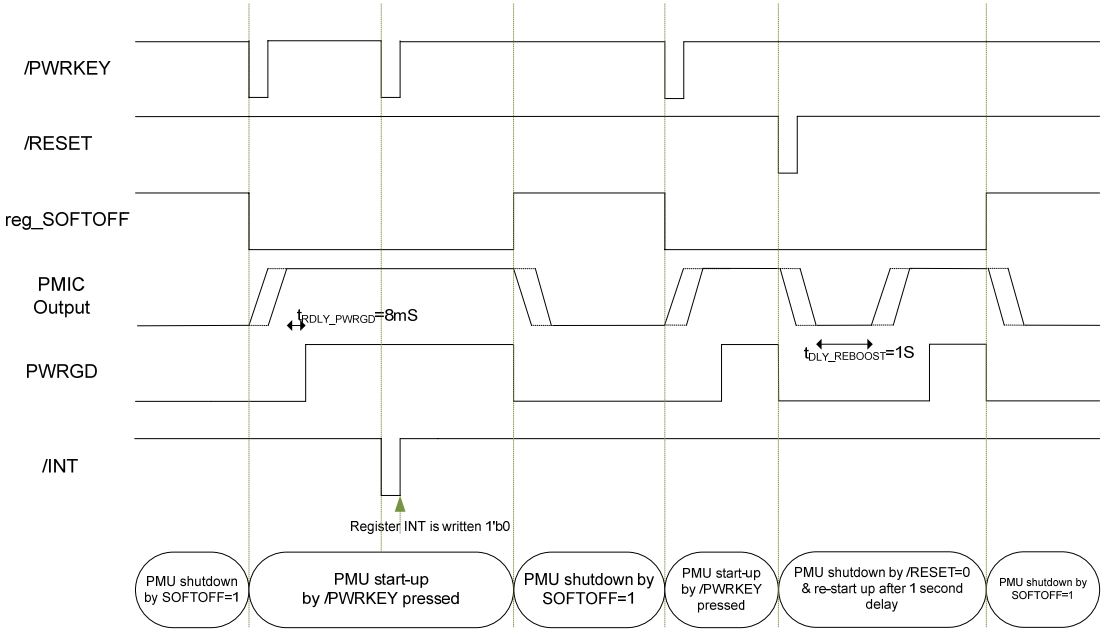
PMU Power ON/OFF Initiation (PWRON_MODE=Floating)

The following conditions are available to turn on the PMU of G2249:

- /PWRKEY pin is toggle low.
- After 1 second delay from shutdown of G2249 caused by toggling /RESET pin low.

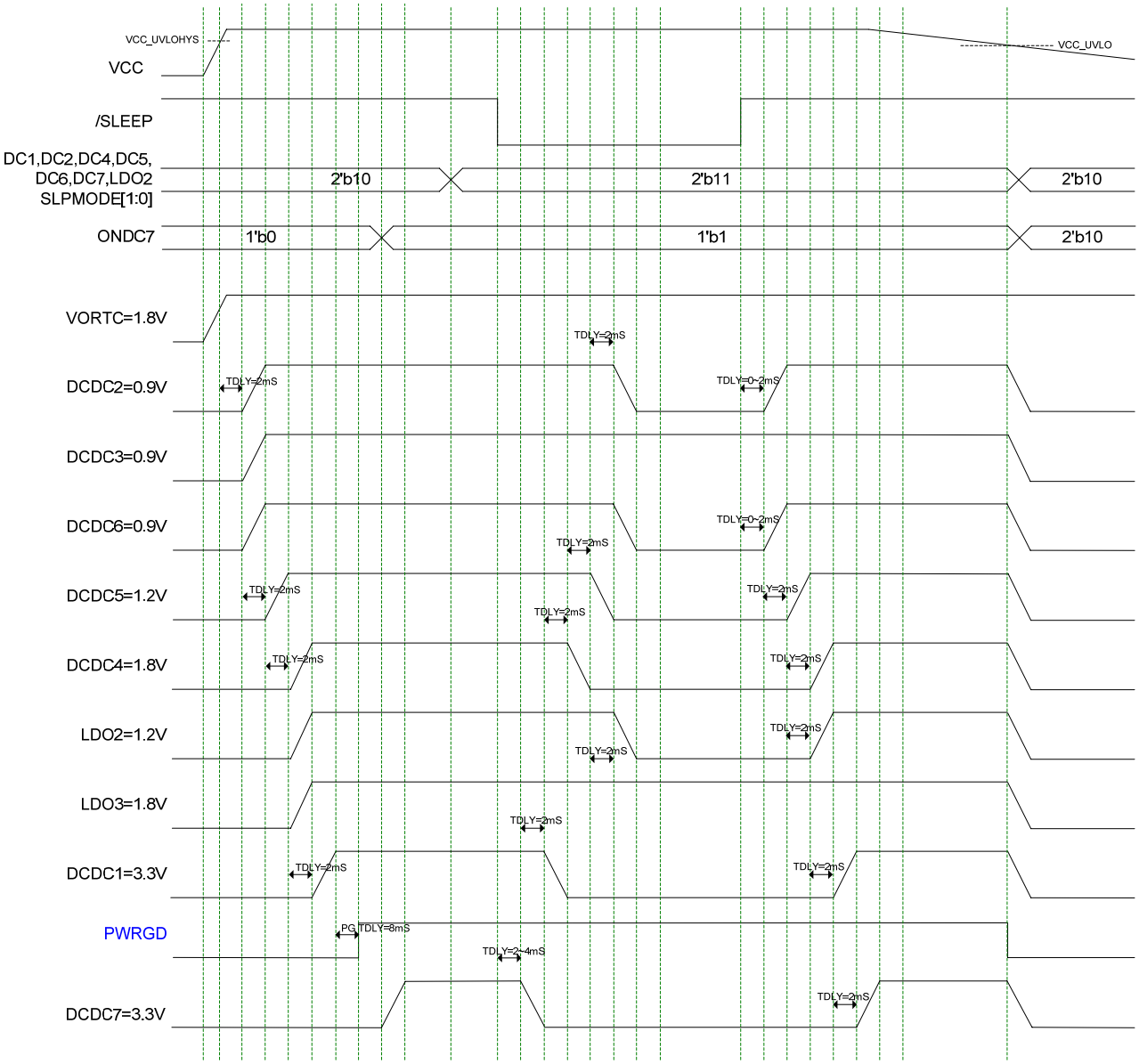
The following conditions are available to turn off the PMU of G2249:

- Write 1 to register SOFTOFF after PWRGD is turned high.
- /RESET pin is toggle low.
- Output voltage UVP of DCDC converters occurs with duration longer than 128mS
- G2249 thermal shutdown occurs.



PMU Power ON/OFF Sequence

When the power on condition is met, these DC/DC converters and LDOs start up in sequence. DCDC7 can start up by writing 1 to register bit ONDC7 after DCDC1 finishing startup process. After these converters finish power on sequence, the open-drain output PWRGD is high with 8ms time delay from DCDC1 are power ready. When G2249 enter sleep mode controlled by toggling /SLEEP pin low, PWRGD pin keeps high, and all converters' on/off mode is according to the setting of SLPMODE[1:0].



PMU Fault Protection

G2249 PMU provides VCC over voltage protection, over-current protection, under-voltage protection, short-circuit protection, and thermal shutdown protection to achieve complete protection.

	Protection type	Threshold	Protection methods	Reset Method
VCC	OVP	VCC>6.0V	IC shutdown	Reset by the power- on/off initiation conditions
DCDC1 Buck	Current Limit	pMOS current>2.8A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT1<75%*$VOUT_{SET}$	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC2 Buck	Current Limit	pMOS current>4.0A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT2< $VOUT_{SET}$-100mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC3 Buck	Current Limit	pMOS current>2.8A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT3< $VOUT_{SET}$-100mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC4 Buck	Current Limit	pMOS current>2.8A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT4<87.5%*$VOUT_{SET}$	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC5 Buck	Current Limit	pMOS current>2.8A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT5< $VOUT_{SET}$-100mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC6 Buck	Current Limit	pMOS current>2.8A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT6< $VOUT_{SET}$-100mV	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
DCDC7 Buck	Current Limit	pMOS current>2.8A	pMOS Off, nMOS on	Automatic Reset at next cycle
	UVP	VOUT7<87.5%*$VOUT_{SET}$	IC shutdown if period above 128ms	Reset by the power- on/off initiation conditions
LDO2 LDO	Current Limit	pMOS current>600mA		pMOS current<450mA
	UVP	LDOO2<12.5%*$LDOO2_{SET}$	pMOS Off	Reset by the power- on/off initiation conditions, or I^2C ONLDO2 control
LDO3 LDO	Current Limit	nMOS current>600mA		nMOS current<450mA
	UVP	LDOO3<12.5%*$LDOO3_{SET}$	nMOS Off	Reset by the power- on/off initiation conditions, or I^2C ONLDO3 control
Thermal	TSD	Junction Temp. >150°C	IC shutdown	Reset by the power- on/off initiation conditions

Application Information

Inductor Selection

The inductor value is chosen based on the desired ripple current. Large value inductors lower ripple current. The ΔIL is inductor peak-to-peak ripple current:

$$\Delta I_L = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

,where Fsw is switching frequency.

A good rule between physical size and efficiency is to allow the peak-to-peak ripple current equal to 30% of the maximum load current. The reasonable inductor current ripple is usually set as 20% to 50% of maximum output current. The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation.

$$I_{L,MAX} = I_{LOAD,MAX} + \frac{\Delta I_L}{2}$$

Input Capacitor Selection

Because the input current to the step-down converter is discontinuous, a capacitor is required to supply the AC current to the converter to maintain the DC input voltage. To prevent large voltage transients, a low ESR capacitor sized for maximum RMS current must be used. The input capacitor is given by:

$$C_{IN,MIN} = \frac{I_{LOAD}}{F_{SW} \times \Delta V_{IN\_RIPPLE,MAX}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor Selection

The selection of COUT is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for COUT has been met, the RMS current rating generally far exceeds the COUT requirement. The output ripple ΔVOUT is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right)$$

For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔIL increase with input voltage.

Load Step Regulation

The max positive and negative steps in output load current, ∆Iout, cause maximum output capacitor voltage undershoots, ∆Vsag, and overshoots, ∆Vsoar, repsectively. They are limited by rate at which the output inductor can supply or remove the new load current after the step. The change in current due to the step is initially removed from or supplied to the output capacitor, until the inductor can fully supply the new load current. This is expressed in the equations below:

$$V_{SAG} = \frac{L \times \left(\Delta I_{LOAD}\right)^2}{2 \times C_{OUT} \times \left(V_{IN,MIN} \times D_{MAX} - V_{OUT}\right)}$$

$$V_{SOAR} = \frac{L \times \left(\Delta I_{LOAD}\right)^2}{2 \times C_{OUT} \times V_{OUT}}$$

Setting the DCDC4 Output Voltage

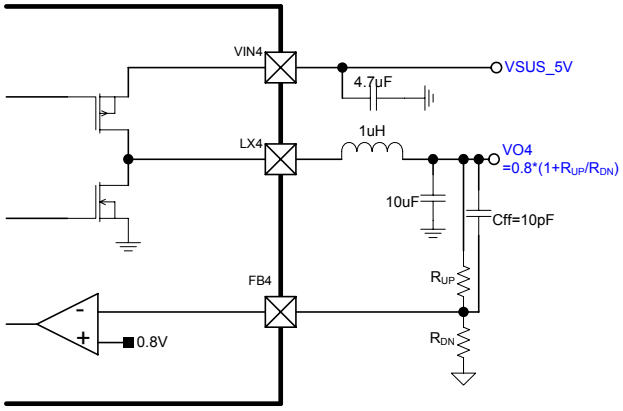
The output voltage of DCDC4 is set by a resistive divider according to the following formula:

$$V_{O4} = 0.8 \times \left(1 + \frac{R_{UP}}{R_{DN}}\right)$$

To optimize transient response, a Cff value is chosen such that the gain and phase boost of the feedback increases the bandwidth of the converter, while still maintaining an acceptable phase margin. Calculate the appropriate capacitor in parallel with the high-side feedback resistor (Rup) to achieve this:

$$C_{FF} = \frac{1}{2 \times \pi \times F_{Z,FF} \times R_{UP}}$$

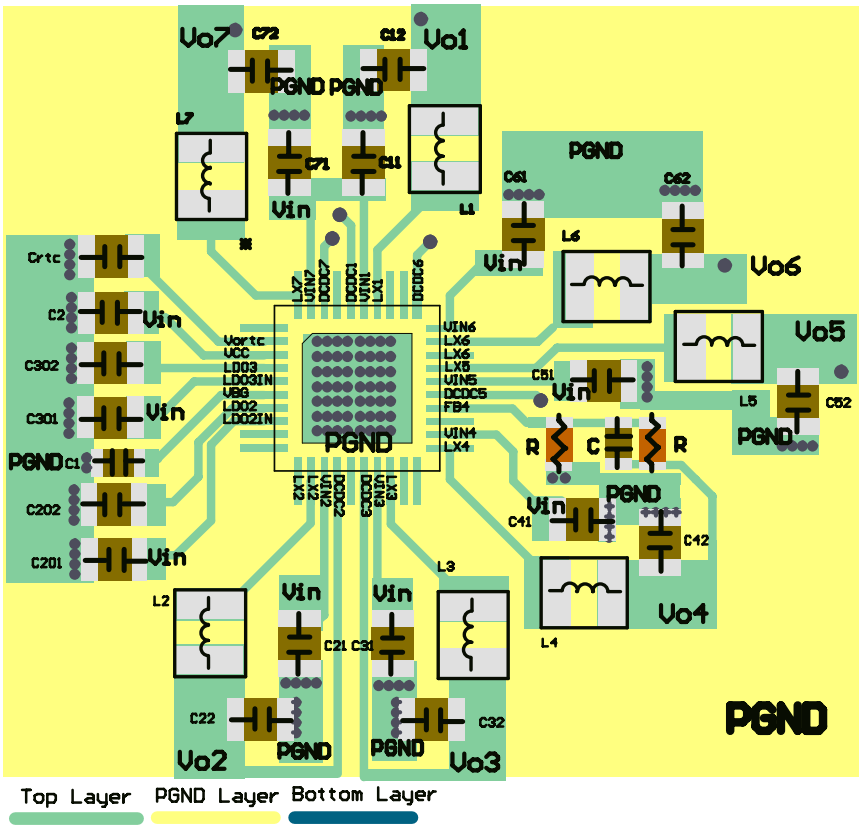
The feedforward capacitor Cff provides an ac coupling path between VOUT and the FB pin which reduces the output ripple. It is highly recommended to keep the Cff value in the range of 10pF.



Layout guidelines

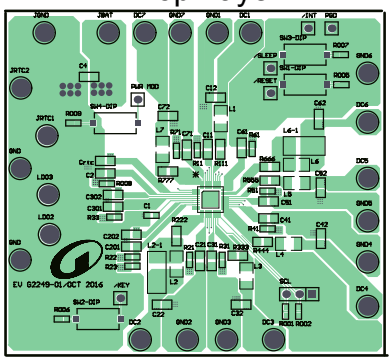
Careful printed circuit layout is extremely important to avoid causing parasitical capacitance and line inductance. The following layout guidelines are recommended to achieve optimum performance.

- Please the buck converter inductor close to the LX pin. Keep traces short, direct, and wide.
- Please ceramic bypass capacitors near the input/output pin.
- All feedback signal must first go through the regulator capacitors. Place feedback connection points near the output capacitors and minimize the control feedback loop as much as possible to achieve the best regulation performance.

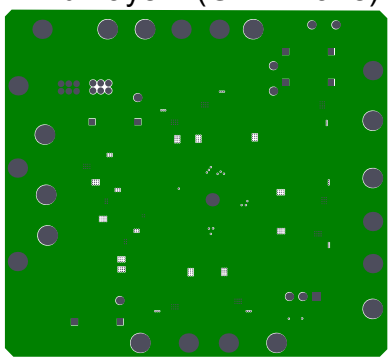


PCB layout EVB Information

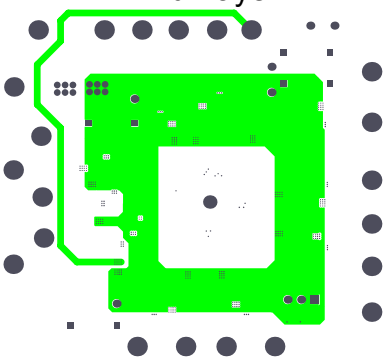
Top Layer



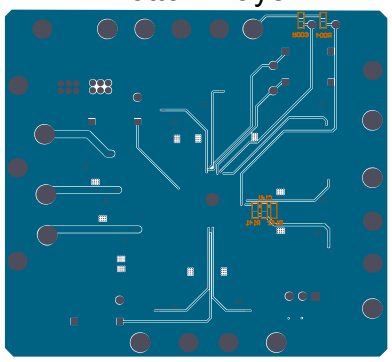
Mid-Layer 1(GND Plane)



Mid-Layer 2

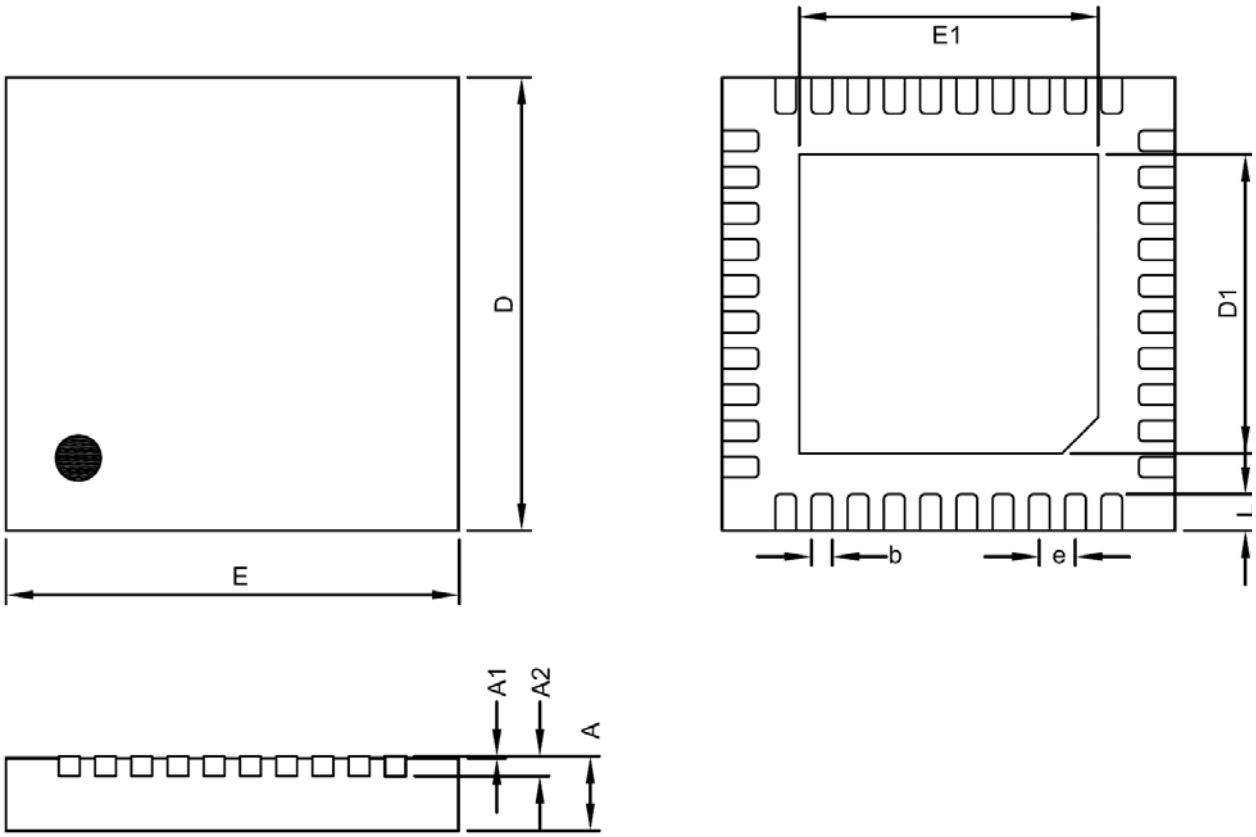


Bottom Layer



EV2249 PCB	Information
Board Material	FR4
Size	74mm×67mm
Board Thickness	1.6mm
Layers	4
Copper Thickness	2 oz.

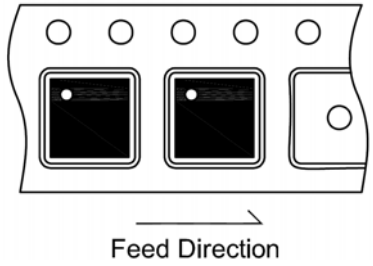
Package Information



TQFN5X5-40 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	4.95	5.00	5.05	0.1949	0.1969	0.1988
E	4.95	5.00	5.05	0.1949	0.1969	0.1988
D1	3.20	3.30	3.40	0.1260	0.1299	0.1339
E1	3.20	3.30	3.40	0.1260	0.1299	0.1339
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Taping Specification



PACKAGE	Q'TY/REEL
TQFN5X5-40	3,000 ea