SSD2831

Advance Information

MIPI D-PHY Rx and Tx Bridge Chip

Appendix: IC Revision history of SSD2831 Specification

Version	Change Items	Effective Date
0.10	1st Release	02-Sep-16
0.11	1. Delete unused data pin – Data0[43:30, 23:13] 2. Update command table	26-Sep-16
0.12	1. Update pin assignment in Table 6-1	14-Oct-16
1.0	Update to Advance Information	16-Feb-17
1.1	1. Change PLL configuration, from 5MHz<fIN=<100 to 5MHz<fIN=<40MHz 2. Modified DC characteristic 3. Change PEN range in 0xBA from “501 to 1000” to “501 to 1250” 4. Added power up/off sequence 5. Changed data buffer from 5120 to 4128 6. Remove DSI, lane and polarity swap features	17-Jul-17

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FIGURES

1 GENERAL DESCRIPTION

SSD2831 is a MIPI master bridge chip that supports MIPI DPHY DSI input and MIPI DPHY DSI output. It can support resolution up to WQHD (2560x1600) (native in) and UHD (4096x2160) (compressed in/out) format with 60Hz refresh rate in landscape or portrait.

2 FEATURES

- Support panel at refresh rate of 60Hz with resolution up to
  - WQHD (2560x1600) (native)
  - UHD (4096 x 2160) (compressed in/out)
- Support MIPI D-PHY standard version 1.1
- Support 2 MIPI D-option DSI engines with throughput up to 10.0Gbps using 8 D-PHY lanes for each DSI-RX (Each lane is up to 1.25Gbps)
- Support 2 MIPI D-option DSI engines with throughput up to 10.0Gbps using 8 D-PHY lanes for each DSI-TX (Each lane is up to 1.25Gbps)
- Support single or dual DSI mode at DSI-RX and DSI-TX output
- Support 16, 18, 24-bit per pixel color
- Support serial SPI interface (DBI version 2.0) up to 16-bits at the input
- Support both Video and Command mode
- Support Video BIST generation at the DSI-TX output with different colour patterns
- Support Burst or Non-burst video modes
- Each DSI-RX, DSI-TX port can control the number of lane independently
- On-chip PLL with variable output frequency
- Power supply: (V_{DDD} and V_{DDA}) 1.2V +/-5%, (VCIP) 3.3V +/-5%
- I IO Power supply: 1.8V +/-10% or 3.3V +/-10%

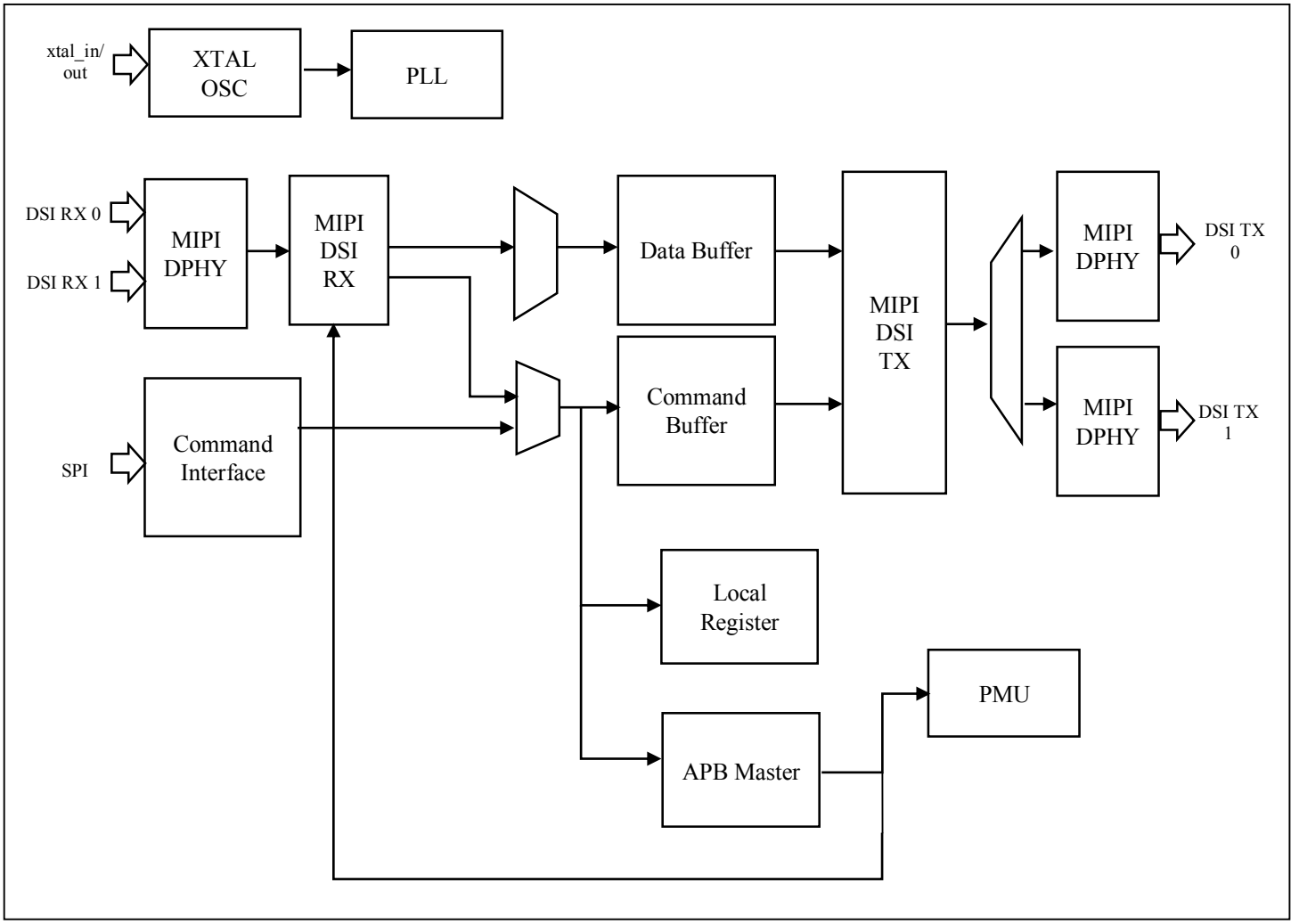
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	Package Form
SSD2831QL9	LQFP 128L, 14mm x 14mm

4 BLOCK DIAGRAM

Figure 4-1: SSD2831 Block Diagram



5 FUNCTIONAL DESCRIPTION

5.1 MIPI DSI RX

The main features of MIPI DSI-RX receiver pairs are:

- Internal APB interface for register programming
- Dual DSI ports up to 8-lanes
- 4 data lanes for each DSI port
- Up to 1.25Gbps per lane for each DSI or 10Gbps for 2 DSI ports
- Single or dual DSI mode
- Each DSI port can control the number of lane independently
- Left-right or odd-even split of the video in gang mode transfers
- Supports lane swap or polarity swap function which allow greater flexibility in the PCB footprint.
- Support 16, 18 and 24-bit per pixel
- Support burst or non-burst mode
- Support local registers access from DSI-0
- Support MIPI Alliance Standard for Display Serial Interface, version 1.01
- Support MIPI Alliance Standard for Display Command Set, version 1.02
- Support MIPI Alliance Standard for D-PHY, version 1.00

The DSI receiver pairs receive MIPI DSI packet data from external MIPI host and break down the packets to either commands or video. For command packets, it can be either directed to the internal local registers in SSD2831 or transmit out as a command at the output of MIPI DSI-TX.

The MIPI DSI receiver pairs can be configured as single DSI or dual DSI mode. Each DSI can support up to 4 lanes running up to 1Gbps per lane. The number of lanes for each DSI can be configured independently.

The MIPI packets that are supported by MIPI DSI-RX are listed in the table below.

Table 5-1: DSI-RX Support Format

Data Type (Hex)	Data Type (Bin)	Type	Description
0x01	00 0001	Short	Sync Event V Start
0x11	01 0001	Short	Sync Event V End
0x21	10 0001	Short	Sync Event H Start
0x31	11 0001	Short	Sync Event H End
0x08	00 1000	Short	End of Transmission (EoT)
0x02	00 0010	Short	Color Mode (CM) Off
0x12	01 0010	Short	Color mode (CM) On
0x22	10 0010	Short	Shut Down Peripheral
0x32	11 0010	Short	Turn On Peripheral
0x03	00 0011	Short	Generic Short Write, no parameter
0x13	01 0011	Short	Generic Short Write, 1 parameter
0x23	10 0011	Short	Generic Short Write, 2 parameters
0x04	00 0100	Short	Generic Read, no parameter
0x14	01 0100	Short	Generic Read, 1 parameter

Data Type (Hex)	Data Type (Bin)	Type	Description
0x24	10 0100	Short	Generic Read, 2 parameters
0x05	00 0101	Short	DCS Short Write, no parameter
0x15	01 0101	Short	DCS Short Write, 1 parameter
0x06	00 0110	Short	DCS Read, no parameter
0x37	11 0111	Short	Set Maximum Return Packet Size
0x09	00 1001	Long	Null Packet
0x19	01 1001	Long	Blanking Packet
0x29	10 1001	Long	Generic Long Write
0x39	11 1001	Long	DCS Long Write
0x0E	00 1110	Long	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format
0x1E	01 1110	Long	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
0x2E	10 1110	Long	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
0x3E	11 1110	Long	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format
0x02	00 0010	Short	Acknowledge and Error Report
0x11	01 0001	Short	Generic Short Read Response, 1 byte returned
0x12	01 0010	Short	Generic Short Read Response, 2 bytes returned
0x1A	01 1010	Long	Generic Long Read Response
0x1C	01 1100	Long	DCS Long Read Response
0x21	10 0001	Short	DCS Short Read Response, 1 byte returned
0x22	10 0010	Short	DCS Short Read Response, 2 bytes returned

5.2 Data Buffer

The data buffer consists of line buffers to store one line worth of video data before packetizing them for MIPI TX transmission. Each line buffer can support up to 2560 pixels each. Data for command 0x2C and 0x3C also make use of the data buffer for storage, instead of going to the command buffer.

There are one line buffer per MIPI DSI TX port. For DSI TX0, the line buffer size is 2560 pixels. For DSI TX1, the size is 2064 pixels. Dual DSI TX port can support up to 2 x 2064 = 4128 pixels..

5.3 Command Buffer

The command buffer consist of a 4096 bytes deep FIFO to store commands before packetizing them to command packets for MIPI TX transmission. Command 0x2C and 0x3C are excluded in this command buffer. They are routed to use data buffer instead.

There are one command FIFO per MIPI DSI TX port.

5.4 MIPI DSI-Tx

MIPI DSI-TX is a dual DSI TX module, supporting up to 2 clock lanes, 8 data lanes for D-option. Each DSI is 1.25Gbps per lane.

The main features of MIPI DSI-TX transmitter pairs are,

- Dual DSI-TX D-option up to 8-lanes
- 4 data lanes for each DSI-TX D-option
- Support up to 2560 pixel/line for 1 DSIt
- Up to 1.25Gbps per lane for each D-option lane or 10Gbps for 2 DSI DPHY
- Single or dual DSI mode
- Support 16, 18, 24-bit per pixel
- Support burst or non-burst mode
- Support new commands in DSI-2, such as Execute Queue, Scrambler On/Off, Compressed packets
- Support MIPI Alliance Standard for Display Serial Interface-2, version 1
- Support MIPI Alliance Standard for Display Command Set, version 1.02
- Support MIPI Alliance Standard for D-PHY, version 1.00

The MIPI packets that are supported by MIPI DSI-TX are listed in the table below.

Table 5-2: DSI-TX Support Format

Data Type (Hex)	Data Type (Bin)	Type	Description
0x01	00 0001	Short	Sync Event V Start
0x11	01 0001	Short	Sync Event V End
0x21	10 0001	Short	Sync Event H Start
0x31	11 0001	Short	Sync Event H End
0x08	00 1000	Short	End of Transmission (EoT)
0x02	00 0010	Short	Color Mode (CM) Off
0x12	01 0010	Short	Color mode (CM) On
0x22	10 0010	Short	Shut Down Peripheral
0x32	11 0010	Short	Turn On Peripheral
0x03	00 0011	Short	Generic Short Write, no parameter
0x13	01 0011	Short	Generic Short Write, 1 parameter
0x23	10 0011	Short	Generic Short Write, 2 parameters
0x04	00 0100	Short	Generic Read, no parameter
0x14	01 0100	Short	Generic Read, 1 parameter
0x24	10 0100	Short	Generic Read, 2 parameters
0x05	00 0101	Short	DCS Short Write, no parameter
0x15	01 0101	Short	DCS Short Write, 1 parameter
0x06	00 0110	Short	DCS Read, no parameter
0x16	01 0110	Short	Execute Queue
0x37	11 0111	Short	Set Maximum Return Packet Size

Data Type (Hex)	Data Type (Bin)	Type	Description
0x27	10 0111	Short	Scrambling Mode Command
0x09	00 1001	Long	Null Packet
0x19	01 1001	Long	Blanking Packet
0x29	10 1001	Long	Generic Long Write
0x39	11 1001	Long	DCS Long Write
0x0A	00 1010	Long	Picture Parameter Set
0x0B	00 1011	Long	Compressed Pixel Stream
0x0E	00 1110	Long	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format
0x1E	01 1110	Long	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
0x2E	10 1110	Long	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
0x3E	11 1110	Long	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format
0x02	00 0010	Short	Acknowledge and Error Report
0x11	01 0001	Short	Generic Short Read Response, 1 byte returned
0x12	01 0010	Short	Generic Short Read Response, 2 bytes returned
0x1A	01 1010	Long	Generic Long Read Response
0x1C	01 1100	Long	DCS Long Read Response
0x21	10 0001	Short	DCS Short Read Response, 1 byte returned
0x22	10 0010	Short	DCS Short Read Response, 2 bytes returned

MIPI DSI Link controller provides MIPI DSI packet assembly and disassembly. During transmission, it will form the DSI packet according to the instruction from the state machine. During reception, it will extract necessary information from the packet and pass to the higher level block. The MIPI DSI Link Controller is also responsible for generating the CRC and ECC for the out-going bit stream. During reception, it will check the correctness of the ECC and CRC field of the incoming stream.

When operated in 2-DSI mode, the MIPI DSI Link Controller is able to split the incoming video into 2 equal portions and send each half of the line to each of the MIPI DSI engines. Each MIPI DSI engine take the half video data and reformat it into RGB 16/18/24-bit packet and send out as 1 packet per line.

A line buffer is used to buffer a single video line from the upstream module and it will regenerate the Video timing with the video settings stored inside the local registers. The output rate from the buffer must be greater than the input rate to prevent data overflow.

MIPI DSI Link controller is also capable of sending DCS/Generic commands to external MIPI DSI drivers via multiple sources.

5.5 XTAL OSC

This is a crystal oscillator pad. From a circuit point of view, the crystal oscillator I/O cells are not real oscillators, but amplifiers used to generate high quality clock signals. Full range configurable output driving capability

5.6 PLL

This is a PLL to control the MIPI Tx frequency

5.7 PMU

The PMU (Power Management Unit) is responsible for putting SSD2831 into deep-sleep mode, cutting the power consumption to ultra-low level. Internally, it uses APB interface for register programming

6 PIN ARRANGEMENT

6.1 128 pins LQFP

Figure 6-1 : Pinout Diagram – 128 pins LQFP (Topview)

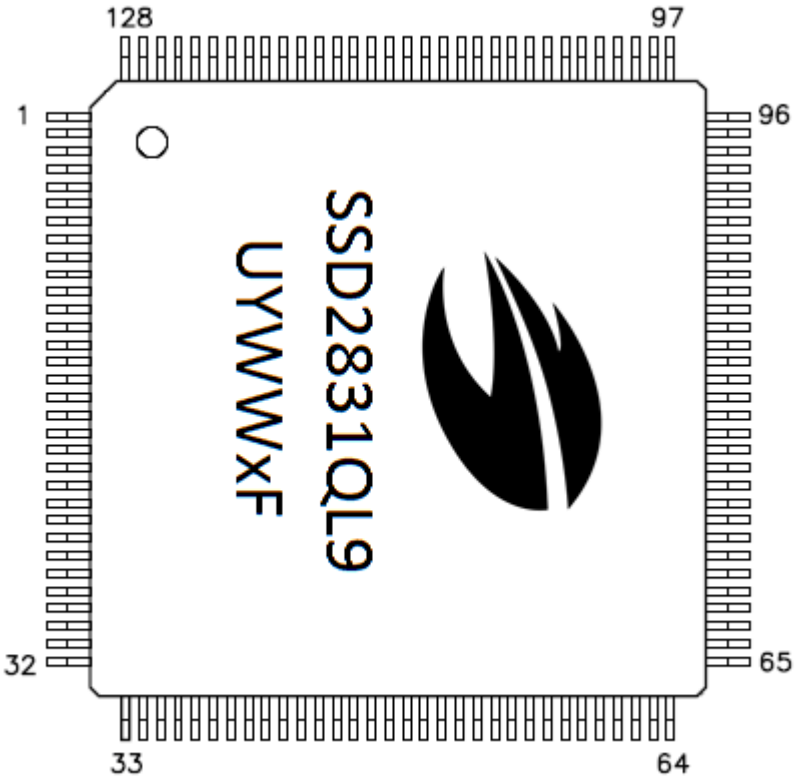


Table 6-1: LQFP Pin Assignment Table

Pin #	QFP Pin name	Pin #	QFP Pin name	Pin #	QFP Pin name	Pin #	QFP Pin name
1	AVDD	33	NC	65	SDI	97	AVDD_CDR
2	RX0_DP2	34	NC	66	SCK	98	TX1_DN3
3	RX0_DN2	35	NC	67	TE_IN_1	99	TX1_DP3
4	AVSS	36	NC	68	TE_IN_0	100	TX1_DN0
5	RX0_DP1	37	NC	69	VSS	101	TX1_DP0
6	RX0_DN1	38	NC	70	VDD_CORE	102	VDRV
7	VSS	39	NC	71	VDDIO	103	AVDD
8	RX0_CP	40	NC	72	SDC	104	AVDD
9	RX0_CN	41	NC	73	PS[4]	105	TX1_CN
10	AVDD	42	NC	74	PS[3]	106	TX1_CP
11	AVSS	43	TE_OUT_0	75	PS[2]	107	TX1_DN1
12	RX0_DP0	44	TE_OUT_1	76	PS[1]	108	VDRV
13	RX0_DN0	45	VDDIO	77	PS[0]	109	TX1_DP1
14	AVSS	46	XTAL_IN	78	INT_B	110	TX1_DN2
15	RX0_DP3	47	XTAL_OUT	79	VDD_CORE	111	TX1_DP2
16	RX0_DN3	48	VSS	80	VSS	112	AVDD
17	VSS	49	VDD_CORE	81	RX1_DN3	113	VCIP
18	IF_SEL[1]	50	NC	82	RX1_DP3	114	VDRV_REG
19	VDD_CORE	51	NC	83	VSS	115	VSS
20	IF_SEL[0]	52	NC	84	RX1_DN0	116	TX0_DN3
21	VDDIO	53	NC	85	RX1_DP0	117	TX0_DP3
22	VSS	54	NC	86	VSS	118	TX0_DN0
23	VSS	55	NC	87	AVDD	119	TX0_DP0
24	VSS	56	NC	88	RX1_CN	120	VDRV
25	RESET	57	NC	89	RX1_CP	121	AVDD
26	VDDIO	58	NC	90	AVSS	122	TX0_CN
27	VDD_CORE	59	NC	91	RX1_DN1	123	TX0_CP
28	VSS	60	NC	92	RX1_DP1	124	TX0_DN1
29	CSX	61	NC	93	VSS	125	VDRV
30	CLK_IN	62	NC	94	RX1_DN2	126	TX0_DP1
31	PD_N	63	NC	95	RX1_DP2	127	TX0_DN2
32	NC	64	SDO	96	AVDD	128	TX0_DP2

7 PIN DESCRIPTIONS

Key:

I = Input
O =Output
IO = Bi-directional (input/output)
P = Power pin

7.1 Power Supply Pin

Table 7-1: Power Supply Pin Description

Pin name	Type	Connect to	Description	When not in use
VDD_CORE	P	Power	Core Power Supply, 1.2V	-
VDDIO	P	Power	I/O Power Supply, 1.8V or 3.3V	-
VSS	P	GND	Ground	-
AVDD_CDR	P	Power	Analog Regulator Output for DPHY CDR, 1.2V	-
AVDD	P	Power	Analog Power Supply 1.2V	-
VCIP	P	Power	Power for Bandgap, 3.3V	-
VDRV_REG	P	Power	LV Regulator Output	-
VDRV	P	Power	Power for MIPI TX Driver (to be connected to VDRV_REG, 0.5V)	-

7.2 MIPI Pin

Table 7-2: MIPIRX Pin Description

Pin name	Type	Connect to	Description	When not in use
RX0_DP0	I/O	MIPI Tx	RX0 DSI Data Lane Positive 0	Open
RX0_DN0	I/O		RX0 DSI Data Lane Negative 0	
RX0_DP1	O		RX0 DSI Data Lane Positive 1	
RX0_DN1	O		RX0 DSI Data Lane Negative 1	
RX0_DP2	O		RX0 DSI Data Lane Positive 2	
RX0_DN2	O		RX0 DSI Data Lane Negative 2	
RX0_DP3	O		RX0 DSI Data Lane Positive 3	
RX0_DN3	O		RX0 DSI Data Lane Negative 3	
RX0_CP	O		RX0 DSI Clock Lane Positive	
RX0_CN	O		RX0 DSI Clock Lane Negative	
RX1_DP0	I/O		RX1 DSI Data Lane Positive 0	
RX1_DN0	I/O		RX1 DSI Data Lane Negative 0	
RX1_DP1	O		RX1 DSI Data Lane Positive 1	
RX1_DN1	O		RX1 DSI Data Lane Negative 1	
RX1_DP2	O		RX1 DSI Data Lane Positive 2	
RX1_DN2	O		RX1 DSI Data Lane Negative 2	
RX1_DP3	O		RX1 DSI Data Lane Positive 3	
RX1_DN3	O		RX1 DSI Data Lane Negative 3	
RX1_CP	O		RX1 DSI Clock Lane Positive	
RX1_CN	O		RX1 DSI Clock Lane Negative	

Table 7-3: MIPITX Pin Description

Pin name	Type	Connect to	Description	When not in use
TX0_DP0	I/O	MIPI Rx	TX0 DSI Data Lane Positive 0	Open
TX0_DN0	I/O		TX0 DSI Data Lane Negative 0	
TX0_DP1	O		TX0 DSI Data Lane Positive 1	
TX0_DN1	O		TX0 DSI Data Lane Negative 1	
TX0_DP2	O		TX0 DSI Data Lane Positive 2	
TX0_DN2	O		TX0 DSI Data Lane Negative 2	
TX0_DP3	O		TX0 DSI Data Lane Positive 3	
TX0_DN3	O		TX0 DSI Data Lane Negative 3	
TX0_CP	O		TX0 DSI Clock Lane Positive	
TX0_CN	O		TX0 DSI Clock Lane Negative	
TX1_DP0	I/O		TX1 DSI Data Lane Positive 0	
TX1_DN0	I/O		TX1 DSI Data Lane Negative 0	
TX1_DP1	O		TX1 DSI Data Lane Positive 1	
TX1_DN1	O		TX1 DSI Data Lane Negative 1	
TX1_DP2	O		TX1 DSI Data Lane Positive 2	
TX1_DN2	O		TX1 DSI Data Lane Negative 2	

TX1_DP3	O		TX1 DSI Data Lane Positive 3	
TX1_DN3	O		TX1 DSI Data Lane Negative 3	
TX1_CP	O		TX1 DSI Clock Lane Positive	
TX1_CN	O		TX1 DSI Clock Lane Negative	

7.3 Control Signal Pin

Table 7-4: Control Signal Pin Description

Pin name	Type	Connect to	Description	When not in use
RESET	I	VDDIO / GND	System Reset signal to the whole chip, active low	VDDIO
INT_B	O		Output Interrupt Signal	Open
PD_N	I	VDDIO / GND	Power Down, active low	VDDIO
IF_SEL[1:0]	I	VDDIO / GND	Interface selection signals IF_SEL[1] should be tied to VDDIO IF_SEL[0] should be tied to VSS	VDDIO / GND
PS[4:0]	I	VDDIO / GND	Interface selection signal PS[4:2] is reserved and should be tied to VDDIO PS[1:0] is for SPI interface - 2'b00: 3 wire 24-bit SPI interface - 2'b 01: 3 wire 8-Bit SPI interface - 2'b 10: 4 wire 8-Bit SPI interface - 2'b 11: Reserved	VDDIO / GND
CLK_IN	I	-	Reserved	Open
XTAL_OUT	I	-	Crystal inout for System PLL	Open
XTAL_IN	I	External CLK	Crystal in for System PLL Frequency range: 8MHz to 30MHz	VDDIO / GND
TE_IN_0	I	-	Input Tearing Effect Signal for DSI0	VDDIO / GND
TE_OUT_0	O	-	Output Tearing Effect Signal for DSI0	Open
TE_IN_1	I	-	Input Tearing Effect Signal for DSI1	VDDIO / GND
TE_OUT_1	O	-	Output Tearing Effect Signal for DSI1	Open

7.4 Interface Logic Pin

Table 7-5: SPI Interface Description

Pin name	Type	Connect to	Description	When not in use
CSX	I	SPI Signal	Chip Select for SPI interface	VDDIO / GND
SDC	I		Data or Command for SPI interface (for 8-bit 4 wire)	VDDIO / GND
SCK	I		Serial clock for SPI interface	VDDIO / GND
SDI	I		Serial data input for SPI interface	VDDIO / GND
SDO	O		Serial data output for SPI interface	Open

8 COMMAND TABLE

8.1 Local Registers (non-APB) Descriptions

8.1.1 RGB Interface Control Register 1

Offset Address

RICR1 **RGB Interface Control Register 1** **0xB1**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**VSA**							
TYPE	RW							
RESET	0x02							
BIT	7	6	5	4	3	2	1	0
NAME	**HSA**							
TYPE	RW							
RESET	0x0A							

Table 8-1: RGB Interface Control Register 1 Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
VSA Bit 15-8	**VSA** – Vertical Sync Active Period These bits specify the Vsync active period. The Hsync active period is from the Vsync falling edge to rising edge, in terms of Hsync lines. It is only used in non-burst mode with Sync pulses. (The minimum value is 1)	Per Application Condition
HSA Bit 7-0	**HSA** – Horizontal Sync Active Period These bits specify the Hsync active period. The Hsync active period is from the Hsync falling edge to rising edge, in terms of pclk. It is only used in non-burst mode with Sync pulses. (The minimum value is 1)	Per Application Condition

8.1.2 RGB Interface Control Register 2

Offset Address

RICR2 **RGB Interface Control Register 2** **0xB2**

BIT	31	30	29	28	27	26	25	24
NAME	**VBP[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	23	22	21	20	19	18	17	16
NAME	**HBP[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	15	14	13	12	11	10	9	8
NAME	**VBP[7:0]**							
TYPE	RW							
RESET	0x02							
BIT	7	6	5	4	3	2	1	0
NAME	**HBP[7:0]**							
TYPE	RW							
RESET	0x14							

Table 8-2: RGB Interface Control Register 2 Description

Name	Description	Setting
VBP[15:8] Bit 31-24	**VBP** – Vertical Back Porch Period High Byte Refer to VBP[7:0] for description	Per Application Condition
HBP[15:8] Bit 23-16	**HBP** – Horizontal Back Porch Period High Byte Refer to HBP[7:0] for description	Per Application Condition
VBP[7:0] Bit 15-8	**VBP** – Vertical Back Porch Period Low Byte These bits specify the vertical back porch period in terms of Hsync pulses. The vertical back porch period depends on the video mode setting. If the mode is non-burst mode with Sync pulses, it is from the Vsync rising edge to the Hsync of the first line of active display. If the mode is non-burst mode with Sync events or burst mode, it is from the Vsync falling edge to the Hsync of the first line of active display. (The minimum value is 1)	Per Application Condition
HBP[7:0] Bit 7-0	**HBP** – Horizontal Back Porch Period Low Byte These bits specify the horizontal back porch period in terms of pclk. The horizontal back porch period depends on the non-burst mode setting.	Per Application Condition

Name	Description	Setting
	If the mode is non-burst mode with Sync pulses, it is from the Hsync rising edge to the start of the valid display pixel. If the mode is non-burst mode with Sync events or burst mode, it is from the Hsync falling edge to the start of the valid display pixel. (The minimum value is 1)	

8.1.3 RGB Interface Control Register 3

Offset Address

RICR3 **RGB Interface Control Register 3** **0xB3**

BIT	31	30	29	28	27	26	25	24
NAME	**VFP[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	23	22	21	20	19	18	17	16
NAME	**HFP[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	15	14	13	12	11	10	9	8
NAME	**VFP[7:0]**							
TYPE	RW							
RESET	0x02							
BIT	7	6	5	4	3	2	1	0
NAME	**HFP[7:0]**							
TYPE	RW							
RESET	0x14							

Table 8-3: RGB Interface Control Register 3 Description

Name	Description	Setting
VFP[15:8] Bit 31-24	**VFP** – Vertical Front Porch Period High Byte Refer to VFP[7:0] for description	Per Application Condition
HFP[15:8] Bit 23-16	**HFP** – Horizontal Front Porch Period High Byte Refer to HFP[7:0] for description	Per Application Condition
VFP[7:0] Bit 15-8	**VFP** – Vertical Front Porch Period Low Byte These bits specify the vertical front porch period in terms of Hsync pulses. The vertical front porch period is from the first Hsync after the last line of active display to the next Vsync falling edge.	Per Application Condition
HFP[7:0] Bit 7-0	**HFP** – Horizontal Front Porch Period Low Byte These bits specify the horizontal front porch period in terms of pclk. The horizontal front porch period is from the end of the valid display pixel to the next Hsync falling edge.	Per Application Condition

8.1.4 RGB Interface Control Register 4

Offset Address

RICR4 **RGB Interface Control Register 4** **0xB4**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**HACT[15:8]**							
TYPE	RW							
RESET	0x07							
BIT	7	6	5	4	3	2	1	0
NAME	**HACT[7:0]**							
TYPE	RW							
RESET	0x80							

Table 8-4: RGB Interface Control Register 4 Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
HACT Bit 15-0	**HACT** – Horizontal Active Period These bits specify the horizontal active period in terms of pclk. During the horizontal active period, the den signal should always be high.	Per Application Condition

8.1.5 RGB Interface Control Register 5

Offset Address

RICR5 **RGB Interface Control Register 5** **0xB5**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**VACT[15:8]**							
TYPE	RW							
RESET	0x04							
BIT	7	6	5	4	3	2	1	0
NAME	**VACT[7:0]**							
TYPE	RW							
RESET	0x38							

Table 8-5: RGB Interface Control Register 5 Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
VACT Bit 15-0	**VACT** – Vertical Active Period These bits specify the vertical active period in terms of Hsync pulses.	Per Application Condition

8.1.6 RGB Interface Control Register 6

Offset Address

RICR6 **RGB Interface Control Register 6** **0xB6**

BIT	31	30	29	28	27	26	25	24
NAME	**VSD**							
TYPE	RW							
RESET	0x00							
BIT	23	22	21	20	19	18	17	16
NAME	**HSD**							
TYPE	RW							
RESET	0x02							
BIT	15	14	13	12	11	10	9	8
NAME	**VS_P**	**HS_P**	**PCLK_P**	**SDR**	**RGB_PACK_SEQ**		**VPF_EXT**	**CBM**
TYPE	RW	RW	RW	RW	RW		RW	RW
RESET	0x0	0x0	0x0	0x1	0x0		0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**NVB**	**NVD**	**BLLP**	**VCS**	**VM**		**VPF**	
TYPE	RW	RW	RW	RW	RW		RW	
RESET	0x0	0x0	0x1	0x0	0x1		0x0	

Table 8-6: RGB Interface Control Register 6 Description

Name	Description	Setting
VSD Bit 31-24	**VSD** – Vertical Sync Delay These bits control the internal pipeline delay of the Vsync input.	Per Application Condition
HSD Bit 23-16	**HSD** – Horizontal Sync Delay These bits control the internal pipeline delay of the Hsync input.	Per Application Condition
VS_P Bit 15	**VS_P** – Vertical Sync Polarity This bit control the polarity of the Vsync pulse input.	0 – Vsync Pulse is active low 1 – Vsync Pulse is active high
HS_P Bit 14	**HS_P** – Horizontal Sync Polarity This bit control the polarity of the Hsync pulse input.	0 – Hsync Pulse is active low 1 – Hsync Pulse is active high
PCLK_P Bit 13	**PCLK_P** – Pixel Clock Polarity This bit control the polarity of the PCLK input. This bit is valid when **SDR** is 1.	0 – Data is launch at falling edge, SSD2831 latch data at rising edge 1 – Data is launch at rising edge, SSD2831 latch data at falling edge
SDR Bit 12	**SDR** - Single Data Rate This bit control whether the RGB input is single data rate or dual data rate.	0 – Data is launch at both rising and falling edge 1 – Data is launch at either rising or falling edge, depends on the PCLK_P bit

Name	Description	Setting
RGB_PACK_SEQ Bit 11-10	**RGB_PACK_SEQ** - RGB Packing Sequence This is applicable for 2 DSI_RX to 1 DSI_TX output(2 to 1) configurations. This bit defines how 2 RGB sources concatenate the pixel data into 1 single RGB stream data{pixel[n], ..., pixel[4], pixel[3], pixel[2], pixel[1]} in dual RGB mode and how 1 RGB source split into 2 RGB stream data.	For dual DSI input and 1 DSI_TX output(2 to 1) 0 - RGB0 lower order pixel = pixel[0], RGB0 higher order pixel = pixel[2]. RGB1 lower order pixel = pixel[1], RGB1 higher order pixel = pixel[3]. (2 to 1) 1 - RGB0 lower order pixel = pixel[0], RGB0 higher order pixel = pixel[1]. RGB1 lower order pixel = pixel[2], RGB1 higher order pixel = pixel[3]. (2 to 1) 2 - RGB0 lower order pixel = pixel[0], RGB0 higher order pixel = pixel[1]. RGB1 lower order pixel = pixel[n/2], RGB1 higher order pixel = pixel[n-1]. (2 to 1) 3 - Reserved
VPF_EXT Bit 9	**VPF_EXT** - Video Pixel Format Extension This bit is used in conjunction with the **VPF[1:0]** bits to define the output pixel format.	[**VPF_EXT, VPF**] 000 - 16-bit 001 - 18-bit 010 - 18-bit loosely 011 - 24-bit 100 - Reserved 111 - Compressed pixel
CBM Bit 8	**CBM** – Compress Burst Mode Control If the video mode is burst(VM=0x2) and this bit is 1, MIPITX will send video packet in compressed burst mode (i.e. no blanking packet after horizontal sync packet)	0 – Video with blanking packet. 1 – Video with no blanking packet
NVB Bit 7	**NVB** – Non Video Data Burst Mode Control This bit specifies how non video data will be interleaved with video data transmission in burst mode.	0 - Non video data will be transmitted during any BLLP period 1 - Non video data will only be transmitted during vertical blanking period
NVD Bit 6	**NVD** – Non Video Data Transmission Control This bit specifies how non video data will be interleaved with video data transmission. The SSD2831 will send non video data (written from the SPI interface) during the vertical blanking period (non burst mode) or any BLLP period in burst mode (depends on NVB setting). The data can be sent either in high speed mode or low power mode. This bit selects which mode to use. If LP mode is selected, the data lane will enter LP mode for BLLP period, even if there is no non-video data to send. Please note that sending data in LP mode is much slower than HS mode. It is the responsibility of the host processor to make sure that the duration is long enough to finish the data transfer and the timing of Hsync and Vsync is not affected.	0 – Non video data will be transmitted using HS mode 1 – Non video data will be transmitted using LP mode

Name	Description	Setting
BLLP Bit 5	**BLLP** – Blanking and Low Power Control This bit specifies the SSD2831 operation during BLLP period. This bit takes effect only for non burst mode and **NVD** being 0. When the video mode is burst mode, the SSD2831 will not send any blanking packet during BLLP. It will enter LP mode. When **NVD** is 1 in non burst mode, the SSD2831 will stay in LP mode after sending the non video data (if there is any), until the BLLP period ends. When **NVD** is 0 in non burst mode, the SSD2831 will use this bit to decide whether to send blanking packet or enter LP mode after sending non video data (if there is any), until the BLLP period ends. Please note that entering and exiting from LP mode needs more time, as the speed of LP mode is slow. It is the responsibility of the host processor to make sure that the period is long enough to finish the data transfer and the timing of Hsync and Vsync is not affected.	0 – Blanking packet will be sent during BLLP period 1 – LP mode will be used during BLLP period
VCS Bit 4	**VCS** – Video Clock Suspend This bit specifies how non video data will be interleaved with video data transmission in burst mode. This bit specifies the clock lane behavior	0 – During burst mode, the clock lane remains in HS mode, when there is no data to transmit. During non burst mode, the clock lane will remain in HS mode all the time. 1 – During burst mode, the clock lane enters LP mode when there is no data to transmit. During non burst mode, the clock lane enters LP mode during vertical blanking period.
VM Bit 3-2	**VM** – Video Mode These bits specify the video mode when RGB interface is selected.	00 – Non burst mode with sync pulses 01 – Non burst mode with sync events 10 – Burst mode 11 – Reserved
VPF Bit 1-0	**VPF** – Video Pixel Format This bit is used in conjunction with the **VPF_EXT** bit to define the output pixel format.	[**VPF_EXT, VPF**] 000 - 16-bit 001 - 18-bit 010 - 18-bit loosely 011 - 24-bit 100 - Reserved 111 - Compressed pixel

Table 8-7: RGB data arrangement

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
24bpp	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
18bpp	X	X	X	X	X	X	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16bpp	X	X	X	X	X	X	X	X	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

8.1.7 Configuration Register

Offset Address

CFR **Configuration Register** **0xB7**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME		**VEN_CTR**	**SCR_EN**	**OTHER_ CMD**	**TXD**	**LPE**	**EOT**	**ECD**
TYPE	RO	RW	RW	RW	RW	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x1	0x1
BIT	7	6	5	4	3	2	1	0
NAME	**REN**	**DCS**	**CSS**	**HCLK**	**VEN**	**SLP**	**CKE**	**HS**
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-8: Configuration Register Description

Name	Description	Setting
Reserved Bit 31-15	**Reserved**	Not Applicable
VEN_CTR Bit 14	**VEN_CTR** – Video Enable Control This bit specifies whether the SSD2831 will extend the internal video enable bit until frame boundary.	0 – Internal video enable follows the **VEN** bit 1 – Internal video enable extends until the frame boundary
SCR_EN Bit 13	**SCR_EN** – Scrambler Mode Enable This bit specifies whether the SSD2831 will send the long packets with scrambled data. SSD2831 will send the Scrambling Mode Packet prior to the Long packet.	0 – Scrambling is disable 1 – Scrambling is enable
OTHER_C MD Bit 12	**OTHER_CMD** – Other Command This bit defines how DCS, Generic, PPS or Compression Mode packet is sent.	0 – **DCS** bit defines DCS or Generic command. 1 – **DCS** bit defines PPS or Compression mode packet.
TXD Bit 11	**TXD** –Transmit Disable This bit specifies whether the SSD2831 will disable the sending of MIPI Packets stored in the buffers. Software can enable TXD, fill out the buffers and then disable it to send all packets out in 1 burst.	0 – Transmit on 1 – Transmit halt
LPE Bit 10	**LPE** –Long Packet Enable	0 – Short Packet 1 – Long Packet

Name	Description	Setting
	This bit specifies whether the SSD2831 will send out a Generic Long Write Packet or Generic Short Write Packet when the payload is no more than 2 bytes. It also specifies whether the SSD2831 will send out a DCS Long Write Packet or DCS Short Write Packet when the payload is no more than 1 byte.	
EOT Bit 9	**EOT** – EOT Packet Enable This bit specifies whether the SSD2831 will send out the EOT packet at the end of HS transmission or not. This is only valid in DPHY mode.	0 – Do not send 1 – Send
ECD Bit 8	**ECD** – ECC CRC Check Disable This bit specifies whether SSD2831 will perform ECC and CRC checking for the packets received from the MIPI slave.	0 – Enable 1 – Disable
REN Bit 7	**REN** – Read Enable This bit specifies whether the next operation is a write or read operation.	0 – Write operation 1 – Read operation
REN Bit 6	**DCS** – DCS or Generic This bit specifies whether the packet to be sent is DCS packet or generic packet. This bit applies for both write and read operation. When **OTHER_CMD** bit is set, this bit specifies whether the packet to be sent is PPS or Compress Mode packet.	When **OTHER_CMD** is 0, 0 – Generic packet (The packet can be any one of Generic Long Write, Generic Short Write, Generic Read packet, depending on the configuration.) 1 – DCS packet (The packet can be any one of DCS Long Write, DCS Short Write, DCS Read packet, depending on the configuration.) When **OTHER_CMD** is 1, 0 – Picture Parameter Setting Packet 1 – Compress Mode Packet
CSS Bit 5	**CSS** – Clock Source Select This bit selects the clock source for the PLL. The **CSS** setting should be programmed only when **PEN** is 0. It has no effect when PEN is 1.	0 – The clock source is XTAL_IN 1 – The clock source is pclk
HCLK Bit 4	**HCLK** – High Speed Clock Disable This bit controls the clock lane behavior during the reverse direction communication. This bit takes effect only when **CKE** is 0 and **VEN** is 0.	0 – HS clock is enabled 1 – HS clock is disabled
VEN Bit 3	**VEN** – Video Mode Enable This bit controls the video mode operation. Only after this bit is set to 1, video mode is enabled.	0 – Video mode is disabled 1 – Video mode is enabled

Name	Description	Setting
SLP Bit 2	**SLP** – Sleep Mode Enable This bit controls the sleep mode operation. When this bit is set to 1, the HS bit will be cleared to 0 automatically.	0 – Sleep mode is disabled 1 – Sleep mode is enabled Only the register interface is active
CKE Bit 1	**CKE** – Clock Lane Enable This bit controls the clock lane mode when data lane enters LP mode.	0 – Clock lane will enter LP mode, if it is not in reverse direction communication. Clock lane will follow the setting of HCLK, if it is in reverse direction communication. 1 – Clock lane will enter HS mode for all the cases
HS Bit 0	**HS** – High Speed Mode This bit controls whether the SSD2831 is using HS or LP mode to send data. This bit can be affected by the SLP bit value.	0 – LP mode 1 – HS mode

8.1.8 Virtual Channel Control Register

Offset Address

VCCR **Virtual Channel Control Register** **0xB8**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**VCM**		**VCE**					
TYPE	RW		RW		RO		RO	
RESET	0x1		0x0		0x1		0x1	

Table 8-9: Virtual Channel Control Register Description

Name	Description	Setting
Reserved Bit 31-8	**Reserved**	Not Applicable
VCM Bit 7-6	**VCM** – Virtual Channel ID for Maximum Return Size Packet These bits specify the VC ID for the Maximum Return Size Packet sent by SSD2831. This register field is included as the VC ID for this packet might be different from the VC ID for the packets carrying the actual data.	Per Application Condition
VCE Bit 5-4	**VCE** – Virtual Channel ID for EOT Packet These bits specify the VC ID for the EOT Packet sent by SSD2831. This register field is included as the VC ID for this packet might be different from the VC ID for the packets carrying the actual data.	Per Application Condition
Reserved Bit 3-2	**Reserved**	Not Applicable
Reserved Bit 1-0	**Reserved**	Not Applicable

8.1.9 PLL Control Register

Offset Address

PCR **PLL Control Register** **0xB9**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME								**PEN**
TYPE	RO	RO	RO	RO	RO	RO	RO	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-10: PLL Control Register Description

Name	Description	Setting
Reserved Bit 31-1	**Reserved**	Not Applicable
PEN Bit 0	**PEN** – PLL Enable This bit controls the PLL operation.	0 – PLL power down 1 – PLL enable

Note: Frequency of PLL can only be changed during PEN=0

8.1.10 PLL Configuration Register

Offset Address

PCFR **PLL Configuration Register** **0xBA**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**FR**		**PLL_TEST**	**MS**				
TYPE	RW		RW	RW				
RESET	0x3		0x0	0x01				
BIT	7	6	5	4	3	2	1	0
NAME	**NS**							
TYPE	RW							
RESET	0x20							

Table 8-11: PLL Configuration Register Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
FR Bit 15-14	**PEN** – Frequency Range These bits select the range of the output clock.	00 – 62.5 to 125 01 – 126 to 250 10 – 251 to 500 11 – 501 to 1250
PLL_TEST Bit 13	**PLL_TEST** – PLL Test Mode This bit set the TEST_MODE pin of the PLL. It should be set to 0 in normal mode.	Per Application Condition
MS Bit 12-8	**MS** – PLL Divider These bits specify the PLL pre-divider value, **MS**.	0x00 - Reserved 0x01 - MS=1 0x02 - MS=2 … 0x1F - MS=31
NS Bit 7-0	**NS** – PLL Multiplier These bits specify the PLL output frequency multiplier value, **NS**.	0x00 - NS=1 0x01 - NS=1 0x02 - NS=2 … 0xFF - NS=255

e.g. XTAL_IN = 20MHz, 0xBAh = 0xC132h

PLL = 50 x 20 / 1 = 1Gbps

8.1.11 Clock Control Register

Offset Address

CCR **Clock Control Register** **0xBB**

BIT	31	30	29	28	27	26	25	24
NAME				**BYP_BIT_DIV**				
TYPE	RO	RO	RO	RW	RO			
RESET	0x0	0x0	0x0	0x1	0x6			
BIT	23	22	21	20	19	18	17	16
NAME	**RX_LPD**							
TYPE	RW							
RESET	0x07							
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**TX_LPD**							
TYPE	RW							
RESET	0x03							

Table 8-12: Clock Control Register Description

Name	Description	Setting
Reserved Bit 31-29	**Reserved**	Not Applicable
BYP_BIT_DIV Bit 28	**BYP_BIT_DIV** – Bypass bit clock divider for bit clock This bit when set will bypass the bit_div for the bit clock.	0 – bit_clk is divided by 2 from PLL clock 1 – bit_clk is directly from PLL clock
Reserved Bit 27-24	**Reserved**	Not Applicable
RX_LPD Bit 23-16	**RX_LPD** – LP Clock Divider for MIPIRX These bits give the divider value for generating the LP mode clock from the system clock.	0x0 – Divide by 2 0x1 – Divide by 2 0x2 – Divide by 4 … 0xFF – Divide by 256
Reserved Bit 15-8	**Reserved**	Not Applicable
TX_LPD Bit 7-0	**TX_LPD** – LP Clock Divider for MIPITX These bits give the divider value for generating the LP mode clock from the system clock.	0x0 – Divide by 1 0x1 – Divide by 2 0x2 – Divide by 3 … 0x3F – Divide by 64

Remark: e.g. LPD = 0x9

PLL = 1Gbps

LP clock = 1Gbps / LPD / 8 = 1000 / 10 / 8 = 12.5MHz

8.1.12 Operational Control Register

Offset Address

OCR **Operational Control Register** **0xC0**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME								**SWR**
TYPE	RO	RO	RO	RO	RO	RO	RO	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME								**COP**
TYPE	RO	RO	RO	RO	RO	RO	RO	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-13: Operational Control Register Description

Name	Description	Setting
Reserved Bit 31-9	**Reserved**	Not Applicable
SWR Bit 8	**SWR -** Software Reset Writing a '1' to this bit will reset the entire module. This bit will be cleared after the reset is completed. Wrting a '1' to this bit will cause the MIPI link enters TX stop state immediately and any outgoing MIPI packet will be terminated immediately.	Per Application Condition
Reserved Bit 7-1	**Reserved**	Not Applicable
COP Bit 0	**COP –** Cancel Operation This bit is to cancel the current operation. When this bit is set to 1, the SSD2831 will still finish transmitting the current packet. (Otherwise, the serial link operation will lose sync.) Afterwards, the SSD2831 will stop any further transmission. It will clear its internal buffer such that all the data being written in and not sent out yet will be cleared. It will also bring the state machine to its initial state. Once this process is finished, the **COP** bit will be automatically set to 0. At the same time, the **PO** bit of the status register will be	Per Application Condition

Name	Description	Setting
	set to 1 too. At this stage, there is no data in the internal buffer. The application processor can start a new operation. This operation is not valid in video mode(**VEN=1)**.	

8.1.13 Maximum Return Size Register

Offset Address

MRSR **Maximum Return Size Register** **0xC1**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**MRS[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**MRS[7:0]**							
TYPE	RW							
RESET	0x01							

Table 8-14: Maximum Return Size Register Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
MRS Bit 15-0	**MRS –** Maximum Return Size These bits set the maximum return size of the read response packet returned by the MIPI slave. The SSD2831 will automatically send out the Set Maximum Return Size packet using the value in this field, before every read operation. It informs the MIPI slave about the limit of the SSD2831. The application processor does not need to program the register before every read operation, if the maximum return size does not change. The Set Maximum Return Size packet will always be sent.	Per Application Condition

8.1.14

8.1.15 Line Control Register

Offset Address

LCR **Line Control Register** **0xC4**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME				**RT1**	**RTB1**	**FBC1**	**FBT1**	**FBW1**
TYPE	RO	RO	RO	RWAC	RWAC	RWAC	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME				**RT0**	**RTB0**	**FBC0**	**FBT0**	**FBW0**
TYPE	RO	RO	RO	RWAC	RWAC	RWAC	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-15: Line Control Register Description

Name	Description	Setting
Reserved Bit 31-21	**Reserved**	Not Applicable
RT1 Bit 20	**RT1 –** Reset Trigger for MIPITX1 This bit is to send a Reset Trigger Message. When this bit is set to 1, the SSD2831 will send a Reset Trigger Message. It is recommended to enter LP mode and send this trigger message. If this bit is programmed during vertical active data is being sent on MIPI link, the reset trigger will be delayed to next vertical blanking period so that the reset trigger message will not disturb the video timing on the MIPI link. Once the Reset Trigger Message is sent out, **RT1** bit will be automatically set to 0.	0 – Do not send 1 – Send Reset Trigger
RTB1 Bit 19	**RTB1 –** Register Triggered BTA for MIPITX1 This bit automatically perform Bus Turnaround(BTA) when link is not used. When bus is returned back from the slave, the link will remains in Low Power state until a new request come in where HS bit determination the transfer mode.	0 – Do not send 1 – Send BTA
FBC1 Bit 19	**FBC1 –** Force Bus Contention for MIPITX1	0 – Do not force 1 – Force Bus Contention

Name	Description	Setting
	This bit controls whether to force a bus contention on the data lane. This bit will be changed to 0, after the bus contention is not detected.	
FBT1 Bit 18	**FBT1 –** Force Bus Turnaround Tearing for MIPITX1 This bit controls whether to perform automatic BTA after previous BTA so as to get the TE response from MIPI slave.	0 – Do not force 1 – Force BTA for Tearing
FBW1 Bit 17	**FBW1 –** Force Bus Turnaround after write for MIPITX1 This bit controls whether to automatically generate a BTA after a write operation. It is only valid for write operation. After performing BTA, the bus authority has been passed to the MIPI slave. The SSD2831 is not able to send any data to the MIPI slave before the bus authority is passed back. It is the responsibility of the application processor to check the status of the bus before sending any data.	0 – Do not force 1 – Force BTA after write
Reserved Bit 16-5	**Reserved**	Not Applicable
RT0 Bit 4	**RT0 –** Reset Trigger for MIPITX0 This bit is to send a Reset Trigger Message. When this bit is set to 1, the SSD2831 will send a Reset Trigger Message. It is recommended to enter LP mode and send this trigger message. If this bit is programmed during vertical active data is being sent on MIPI link, the reset trigger will be delayed to next vertical blanking period so that the reset trigger message will not disturb the video timing on the MIPI link. Once the Reset Trigger Message is sent out, **RT1** bit will be automatically set to 0.	0 – Do not send 1 – Send Reset Trigger
RTB0 Bit 3	**RTB0 –** Register Triggered BTA for MIPITX0 This bit automatically perform Bus Turnaround(BTA) when link is not used. When bus is returned back from the slave, the link will remains in Low Power state until a new request come in where HS bit determination the transfer mode.	0 – Do not send 1 – Send BTA
FBC0 Bit 2	**FBC0 –** Force Bus Contention for MIPITX0 This bit controls whether to force a bus contention on the data lane. This bit will be changed to 0, after the bus contention is not detected.	0 – Do not force 1 – Force Bus Contention
FBT0 Bit 1	**FBT0 –** Force Bus Turnaround Tearing for MIPITX0	0 – Do not force 1 – Force BTA for Tearing

Name	Description	Setting
	This bit controls whether to perform automatic BTA after previous BTA so as to get the TE response from MIPI slave.	
FBW0 Bit 0	**FBW0 –** Force Bus Turnaround after write for MIPITX0 This bit controls whether to automatically generate a BTA after a write operation. It is only valid for write operation. After performing BTA, the bus authority has been passed to the MIPI slave. The SSD2831 is not able to send any data to the MIPI slave before the bus authority is passed back. It is the responsibility of the application processor to check the status of the bus before sending any data.	0 – Do not force 1 – Force BTA after write

8.1.16 Interrupt Control Register

Offset Address

ICR **Interrupt Control Register** **0xC5**

BIT	31	30	29	28	27	26	25	24
NAME	**CBEE1**	**CBAE1**					**MLEE1**	**MLAE1**
TYPE	RW	RW	RO	RO	RO	RO	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME		**LPTOE1**	**HSTOE1**		**ARRE1**	**BTARE1**		**RDRE1**
TYPE	RO	RW	RW	RO	RW	RW	RO	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**CBEE0**	**CBAE0**					**MLEE0**	**MLAE0**
TYPE	RW	RW	RO	RO	RO	RO	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**PLSE**	**LPTOE0**	**HSTOE0**		**ARRE0**	**BTARE0**		**RDRE0**
TYPE	RW	RW	RW	RO	RW	RW	RO	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-16: Interrupt Control Register Description

Name	Description	Setting
CBEE1 Bit 31	**CBEE1 –** Command Buffer Empty Enable for MIPITX1 This bit enables the mapping of **CBE1** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
CBAE1 Bit 30	**CBAE1 –** Command Buffer Available Enable for MIPITX1 This bit enables the mapping of **CBA1** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
Reserved Bit 29-26	**Reserved**	Not Applicable
MLEE1 Bit 25	**MLEE1 –** MCU Long Buffer Empty Enable for MIPITX1 This bit enables the mapping of **MLE1** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
MLAE1 Bit 24	**MLAE1 –** MCU Long Buffer Available Enable for MIPITX1 This bit enables the mapping of **MLA1** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
Reserved Bit 23	**Reserved**	Not Applicable
LPTOE1 Bit 22	**LPTOE1** – LP RX Time Out Enable for MIPITX1	0 – Do not enable 1 – Enable

Name	Description	Setting
	This bit enables the mapping of **LPTO1** interrupt to the interrupt pin, INT_B.	
HSTOE1 Bit 21	**HSTOE1** – HP TX Time Out Enable for MIPITX1 This bit enables the mapping of **HSTO1** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
Reserved Bit 20	**Reserved**	Not Applicable
ARRE1 Bit 19	**ARRE1** – ACK Response Ready Enable for MIPITX1 This bit enables the mapping of **ARR1** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
BTARE1 Bit 18	**BTARE1** – Bus Turnaround Response Enable for MIPITX1 This bit enables the mapping of **BTAR1** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
Reserved Bit 17	**Reserved**	Not Applicable
RDRE1 Bit 16	**RDRE1** – Read Data Ready Enable for MIPITX1 This bit enables the mapping of **RDR1** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
CBEE0 Bit 15	**CBEE0 –** Command Buffer Empty Enable for MIPITX0 This bit enables the mapping of **CBE0** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
CBAE0 Bit 14	**CBAE0 –** Command Buffer Available Enable for MIPITX0 This bit enables the mapping of **CBA0** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
Reserved Bit 13-10	**Reserved**	Not Applicable
MLEE0 Bit 9	**MLEE0 –** MCU Long Buffer Empty Enable for MIPITX0 This bit enables the mapping of **MLE0** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
MLAE0 Bit 8	**MLAE0 –** MCU Long Buffer Available Enable for MIPITX0 This bit enables the mapping of **MLA0** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
PLSE Bit 7	**PLSE** – PLL Lock Status Enable This bit enables the mapping of **PLS** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
LPTOE0 Bit 6	**LPTOE0** – LP RX Time Out Enable for MIPITX0	0 – Do not enable 1 – Enable

Name	Description	Setting
	This bit enables the mapping of **LPTO0** interrupt to the interrupt pin, INT_B.	
HSTOE0 Bit 5	**HSTOE0** – HP TX Time Out Enable for MIPITX0 This bit enables the mapping of **HSTO0** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
Reserved Bit 4	**Reserved**	Not Applicable
ARRE0 Bit 3	**ARRE0** – ACK Response Ready Enable for MIPITX0 This bit enables the mapping of **ARR0** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
BTARE0 Bit 2	**BTARE0** – Bus Turnaround Response Enable for MIPITX0 This bit enables the mapping of **BTAR0** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable
Reserved Bit 1	**Reserved**	Not Applicable
RDRE0 Bit 0	**RDRE0** – Read Data Ready Enable for MIPITX0 This bit enables the mapping of **RDR0** interrupt to the interrupt pin, INT_B.	0 – Do not enable 1 – Enable

8.1.17 Interrupt Status Register

Offset Address

ISR **Interrupt Status Register** **0xC6**

BIT	31	30	29	28	27	26	25	24
NAME	**CBE1**	**CBA1**			**CLS1**	**DLS1**	**MLE1**	**MLA1**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME		**LPTO1**	**HSTO1**	**ATR1**	**ARR1**	**BTAR1**		**RDRE1**
TYPE	RO	RESW1C	RESW1C	RESW1C	RESW1C	RESW1C	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**CBE0**	**CBA0**			**CLS0**	**DLS0**	**MLE0**	**MLA0**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**PLS**	**LPTO0**	**HSTO0**	**ATR0**	**ARR0**	**BTAR0**		**RDR0**
TYPE	RO	RESW1C	RESW1C	RESW1C	RESW1C	RESW1C	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-17: Interrupt Status Register Description

Name	Description	Setting
CBE1 Bit 31	**CBE1 –** Command Buffer Empty for MIPITX1 This bit reflects the status of the internal command buffer of the SPI/MCU interface. If the command buffer is empty, this bit will be set to 1. The application processor can write up to the maximum size of the command buffer.	0 – The command buffer is not empty 1 – The command buffer is empty
CBA1 Bit 30	**CBA1 –** Command Buffer Available for MIPITX1 This bit reflects the status of the internal command buffer of the SPI/MCU interface. If the command buffer is not full, this bit will be set to 1. The application processor can write at least 1 packet to the command buffer.	0 – The command buffer is not available 1 – The command buffer is available
Reserved Bit 29-28	**Reserved**	Not Applicable
CLS1 Bit 27	**CLS1 –** Clock Lane Status for MIPITX1 This bit reflects the status at the MIPI Clock lane in MIPITX1.	0 – Clock lane is not in LP-11 1 – Clock lane is in LP-11
DLS1 Bit 26	**DLS1 –** Data Lane Status for MIPITX1 This bit reflects the status at the MIPI Clock lane in MIPITX1.	0 – Data lanes are not in LP-11 1 – Data lanes are in LP-11
MLE1 Bit 25	**MLE1 –** MCU Long Buffer Empty for MIPITX1	0 – The long buffer is not empty 1 – The long buffer is empty

Name	Description	Setting
	This bit reflects the status of the internal long buffer of the MCU interface. If the long buffer is empty, this bit will be set to 1. The application processor can write up to the maximum size of the long buffer for DCS command 0x2C and 0x3C.	
MLA1 Bit 24	**MLA1 –** MCU Long Buffer Available for MIPITX1 This bit reflects the status of the internal long buffer of the MCU interface. If the long buffer is not full, this bit will be set to 1. The application processor can write at least 1 packet to the long buffer for DCS command 0x2C and 0x3C.	0 – The long buffer is not available 1 – The long buffer is available
Reserved Bit 23	**Reserved**	Not Applicable
LPTO1 Bit 22	**LPTO1** – LP RX Time Out for MIPITX1 This bit reflects the status of the LP RX timer. It will remain as 1 until the application processor writes 1 to clear it.	0 – The LP RX timer has expired 1 – The LP RX timer has not expired
HSTO1 Bit 21	**HSTO1** – HP TX Time Out for MIPITX1 This bit reflects the status of the HS TX timer. It will remain as 1 until the application processor writes 1 to clear it.	0 – The HS TX timer has expired 1 – The HS TX timer has not expired
ATR1 Bit 20	**ATR1** – ACK Trigger Response for MIPITX1 This bit reflects whether the ACK trigger message has been received or not. It will remain as 1 until the application processor writes 1 to clear it.	0 – ACK trigger message has not been received 1 – ACK trigger message has been received
ARR1 Bit 19	**ARR1** – ACK Response Ready for MIPITX1 This bit reflects whether the ACK response has been received or not. The ACK response can be an ACK trigger message or ACK with Error Report packet. It will remain as 1 until the application processor writes 1 to clear it.	0 – Response has not been received 1 – Response has been received
BTAR1 Bit 18	**BTAR1** – Bus Turnaround Response for MIPITX1 This bit reflects the data lane status after SSD2831 has made a BTA. It will remain as 1 until the application processor writes 1 to clear it.	0 – The MIPI slave has not passed the lane authority back 1 – The MIPI slave has passed the lane authority back
Reserved Bit 17	**Reserved**	Not Applicable
RDR1	**RDR1** – Read Data Ready for MIPITX1	0 – Not ready

Name	Description	Setting
Bit 16	This bit reflects whether the data from the MIPI slave is ready for read by the application processor. This bit is valid only during the read operation. This bit will be automatically cleared when all the received data are read out.	1 – Ready
CBE0 Bit 15	**CBE0 –** Command Buffer Empty for MIPITX0 This bit reflects the status of the internal command buffer of the SPI/MCU interface. If the command buffer is empty, this bit will be set to 1. The application processor can write up to the maximum size of the command buffer.	0 – The command buffer is not empty 1 – The command buffer is empty
CBA0 Bit 14	**CBA0 –** Command Buffer Available for MIPITX0 This bit reflects the status of the internal command buffer of the SPI/MCU interface. If the command buffer is not full, this bit will be set to 1. The application processor can write at least 1 packet to the command buffer.	0 – The command buffer is not available 1 – The command buffer is available
Reserved Bit 13-12	**Reserved**	Not Applicable
CLS0 Bit 11	**CLS0 –** Clock Lane Status for MIPITX0 This bit reflects the status at the MIPI Clock lane in MIPITX0.	0 – Clock lane is not in LP-11 1 – Clock lane is in LP-11
DLS0 Bit 10	**DLS0 –** Data Lane Status for MIPITX0 This bit reflects the status at the MIPI Clock lane in MIPITX0.	0 – Data lanes are not in LP-11 1 – Data lanes are in LP-11
MLE0 Bit 9	**MLE0 –** MCU Long Buffer Empty for MIPITX0 This bit reflects the status of the internal long buffer of the MCU interface. If the long buffer is empty, this bit will be set to 1. The application processor can write up to the maximum size of the long buffer for DCS command 0x2C and 0x3C.	0 – The long buffer is not empty 1 – The long buffer is empty
MLA0 Bit 8	**MLA0 –** MCU Long Buffer Available for MIPITX0 This bit reflects the status of the internal long buffer of the MCU interface. If the long buffer is not full, this bit will be set to 1. The application processor can write at least 1 packet to the long buffer for DCS command 0x2C and 0x3C.	0 – The long buffer is not available 1 – The long buffer is available
PLS Bit 7	**PLS** – PLL Lock Status This bit reflects the status of the PLL. Before the PLL is locked, the whole system is running at the reference clock input of the PLL, as the PLL	0 – PLL is not locked 1 – PLL is locked

Name	Description	Setting
	has no output before getting lock. Hence, the application processor must access the registers using slow speed.	
LPTO0 Bit 6	**LPTO0** – LP RX Time Out for MIPITX0 This bit reflects the status of the LP RX timer. It will remain as 1 until the application processor writes 1 to clear it.	0 – The LP RX timer has expired 1 – The LP RX timer has not expired
HSTO0 Bit 5	**HSTO0** – HP TX Time Out for MIPITX0 This bit reflects the status of the HS TX timer. It will remain as 1 until the application processor writes 1 to clear it.	0 – The HS TX timer has expired 1 – The HS TX timer has not expired
ATR0 Bit 4	**ATR0** – ACK Trigger Response for MIPITX0 This bit reflects whether the ACK trigger message has been received or not. It will remain as 1 until the application processor writes 1 to clear it.	0 – ACK trigger message has not been received 1 – ACK trigger message has been received
ARR0 Bit 3	**ARR0** – ACK Response Ready for MIPITX0 This bit reflects whether the ACK response has been received or not. The ACK response can be an ACK trigger message or ACK with Error Report packet. It will remain as 1 until the application processor writes 1 to clear it.	0 – Response has not been received 1 – Response has been received
BTAR0 Bit 2	**BTAR0** – Bus Turnaround Response for MIPITX0 This bit reflects the data lane status after SSD2831 has made a BTA. It will remain as 1 until the application processor writes 1 to clear it.	0 – The MIPI slave has not passed the lane authority back 1 – The MIPI slave has passed the lane authority back
Reserved Bit 1	**Reserved**	Not Applicable
RDR1 Bit 0	**RDR0** – Read Data Ready for MIPITX0 This bit reflects whether the data from the MIPI slave is ready for read by the application processor. This bit is valid only during the read operation. This bit will be automatically cleared when all the received data are read out.	0 – Not ready 1 – Ready

8.1.18 Error Status Register

Offset Address

ESR **Error Status Register** **0xC7**

BIT	31	30	29	28	27	26	25	24
NAME						**CRCE1**	**ECCE2_1**	**ECCE1_1**
TYPE	RO	RO	RO	RO	RO	RESW1C	RESW1C	RESW1C
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME	**CBO1**			**MLO1**		**CONT1**		**VMM1**
TYPE	RESW1C	RO	RO	RESW1C	RO	RO	RO	RESW1C
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME						**CRCE0**	**ECCE2_0**	**ECCE1_0**
TYPE	RO	RO	RO	RO	RO	RESW1C	RESW1C	RESW1C
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**CBO0**			**MLO0**		**CONT0**		**VMM0**
TYPE	RESW1C	RO	RO	RESW1C	RO	RO	RO	RESW1C
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-18: Error Status Register Description

Name	Description	Setting
Reserved Bit 31-27	**Reserved**	Not Applicable
CRCE1 Bit 26	**CRCE1 –** CRC Error for MIPITX1 This bit reflects the status of CRC checking for the packets received from the MIPI slave. The status is valid only when the **ECD** bit is set to 0. Once a CRC error occurs, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – No CRC error since this bit is cleared 1 – At least 1 CRC error since this bit is cleared
ECCE2_1 Bit 25	**ECCE2_1 –** ECC Multi Bit Error for MIPITX1 This bit reflects the status of ECC checking for the packets received from the MIPI slave. The status is valid only when the **ECD** bit is set to 0. Once an ECC multi-bit error occurs, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – No ECC multi-bit error since this bit is cleared 1 – At least 1 ECC multi-bit error since this bit is cleared
ECCE1_1 Bit 24	**ECCE1_1 –** ECC Single Bit Error for MIPITX1 This bit reflects the status of ECC checking for the packets received from the MIPI slave. The status is valid only when the **ECD** bit is set to 0.	0 – No ECC single bit error since this bit is cleared 1 – At least 1 ECC single bit error since this bit is cleared

Name	Description	Setting
	Once an ECC single-bit error occurs, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	
CBO1 Bit 23	**CBO1 –** Command Buffer Overflow for MIPITX1 This bit reflects the status of internal command buffer of the SPI/MCU interface. If the command buffer has overflowed, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – Overflow has not occurred 1 – Overflow has occurred
Reserved Bit 22-21	**Reserved**	Not Applicable
MLO1 Bit 20	**MLO1 –** MCU Long Buffer Overflow for MIPITX1 This bit reflects the status of internal long buffer of the MCU interface. If the long buffer has overflowed, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – Overflow has not occurred 1 – Overflow has occurred
Reserved Bit 19	**Reserved**	Not Applicable
CONT1 Bit 18	**CONT1** – Contention Detected for MIPITX1 This bit reflects the status of the data lane contention detector.	0 – No contention 1 – Contention has occurred
Reserved Bit 17	**Reserved**	
VMM1 Bit 16	**VMM1** – VC Mis-Match for MIPITX1 This bit reflects whether there is a mismatch between the VC ID transmitted by the SSD2831 and the VC ID received from the MIPI slave. It will remain as 1 until the application processor writes 1 to clear it.	0 – No mismatch 1 – Mismatch has occurred
Reserved Bit 15-11	**Reserved**	Not Applicable
CRCE0 Bit 10	**CRCE0 –** CRC Error for MIPITX0 This bit reflects the status of CRC checking for the packets received from the MIPI slave. The status is valid only when the **ECD** bit is set to 0. Once a CRC error occurs, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – No CRC error since this bit is cleared 1 – At least 1 CRC error since this bit is cleared
ECCE2_0 Bit 9	**ECCE2_0 –** ECC Multi Bit Error for MIPITX0	0 – No ECC multi-bit error since this bit is cleared

Name	Description	Setting
	This bit reflects the status of ECC checking for the packets received from the MIPI slave. The status is valid only when the **ECD** bit is set to 0. Once an ECC multi-bit error occurs, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	1 – At least 1 ECC multi-bit error since this bit is cleared
ECCE1_0 Bit 8	**ECCE1_0 –** ECC Single Bit Error for MIPITX0 This bit reflects the status of ECC checking for the packets received from the MIPI slave. The status is valid only when the **ECD** bit is set to 0. Once an ECC single-bit error occurs, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – No ECC single bit error since this bit is cleared 1 – At least 1 ECC single bit error since this bit is cleared
CBO0 Bit 7	**CBO0 –** Command Buffer Overflow for MIPITX0 This bit reflects the status of internal command buffer of the SPI/MCU interface. If the command buffer has overflowed, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – Overflow has not occurred 1 – Overflow has occurred
Reserved Bit 6-5	**Reserved**	Not Applicable
MLO0 Bit 4	**MLO0 –** MCU Long Buffer Overflow for MIPITX0 This bit reflects the status of internal long buffer of the MCU interface. If the long buffer has overflowed, this bit will be set to 1. It will remain as 1 until the application processor writes 1 to clear it.	0 – Overflow has not occurred 1 – Overflow has occurred
Reserved Bit 3	**Reserved**	Not Applicable
CONT0 Bit 2	**CONT0** – Contention Detected for MIPITX0 This bit reflects the status of the data lane contention detector.	0 – No contention 1 – Contention has occurred
Reserved Bit 1	**Reserved**	Not Applicable
VMM0 Bit 0	**VMM0** – VC Mis-Match for MIPITX0 This bit reflects whether there is a mismatch between the VC ID transmitted by the SSD2831 and the VC ID received from the MIPI slave. It will remain as 1 until the application processor writes 1 to clear it.	0 – No mismatch 1 – Mismatch has occurred

8.1.19 Compressed Register

Offset Address

CR **Compressed Register** **0xC8**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**VID_COMPRESSED_BYTE_COUNT[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**VID_COMPRESSED_BYTE_COUNT[7:0]**							
TYPE	RW							
RESET	0x00							

Table 8-19: Compressed Register Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
VID_COMPRESSED_BYTE_COUNT Bit 15-0	**VID_COMPRESSED_BYTE_COUNT –** Compressed slice byte count These bits indicate the number of bytes for each slide in the compressed pixel stream	Per Application Condition

8.1.20 Delay Adjustment Register 1

Offset Address

DAR1 **Delay Adjustment Register 1** **0xC9**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**HZD**							
TYPE	RW							
RESET	0x14							
BIT	7	6	5	4	3	2	1	0
NAME	**HPD**							
TYPE	RW							
RESET	0x02							

Table 8-20: Delay Adjustment Register 1 Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
HZD Bit 15-8	**HZD –** HS Zero Delay These bits specifies the number of system clock for HS zero delay period THS-ZERO. The minimum value is 1.	Per Application Condition
HPD Bit 7-0	**HPD –** HS Prepare Delay These bits specifies the number of system clock for HS prepare delay period THS-PREPARE. The minimum value is 1.	Per Application Condition

8.1.21 Delay Adjustment Register 2

Offset Address

DAR2 **Delay Adjustment Register 2** **0xCA**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**CZD**							
TYPE	RW							
RESET	0x28							
BIT	7	6	5	4	3	2	1	0
NAME	**CPD**							
TYPE	RW							
RESET	0x03							

Table 8-21: Delay Adjustment Register 2 Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
CZD Bit 15-8	**CZD** – Clock Zero Delay These bits specifies the number of system clock for HS zero delay period TCLK-ZERO. The minimum value is 1.	Per Application Condition
CPD Bit 7-0	**CPD –** Clock Prepare Delay These bits specifies the number of system clock for HS prepare delay period TCLK-PREPARE. The minimum value is 1.	Per Application Condition

8.1.22 Delay Adjustment Register 3

Offset Address

DAR3 **Delay Adjustment Register 3** **0xCB**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**CPED**							
TYPE	RW							
RESET	0x04							
BIT	7	6	5	4	3	2	1	0
NAME	**CPTD**							
TYPE	RW							
RESET	0x16							

Table 8-22: Delay Adjustment Register 3 Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
CPED Bit 15-8	**CPED** – Clock Pre Delay These bits specifies the number of system clock for CLK pre delay period TCLK-PRE. The minimum value is 1.	Per Application Condition
CPTD Bit 7-0	**CPTD –** Clock Prepare Delay These bits specifies the number of system clock for CLK post delay period TCLK-POST. The minimum value is 1.	Per Application Condition

8.1.23 Delay Adjustment Register 4

Offset Address

DAR4 **Delay Adjustment Register 4** **0xCC**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**CTD**							
TYPE	RW							
RESET	0x0A							
BIT	7	6	5	4	3	2	1	0
NAME	**HTD**							
TYPE	RW							
RESET	0x0A							

Table 8-23: Delay Adjustment Register 4 Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
CTD Bit 15-8	**CTD** – Clock Pre Delay These bits specifies the number of system clock for CLK trail delay period TCLK-TRAIL. The minimum value is 1.	Per Application Condition
HTD Bit 7-0	**HTD –** Clock Prepare Delay These bits specifies the number of system clock for HS trail delay period THS-TRAIL. The minimum value is 1.	Per Application Condition

8.1.24 Delay Adjustment Register 5

Offset Address

DAR5 **Delay Adjustment Register 5** **0xCD**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**WUD[15:8]**							
TYPE	RW							
RESET	0x10							
BIT	7	6	5	4	3	2	1	0
NAME	**WUD[7:0]**							
TYPE	RW							
RESET	0x00							

Table 8-24: Delay Adjustment Register 5 Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
WUD Bit 15-0	**WUD** – Wake Up Delay These bits specifies the number of clock cycles for wake up delay period TWAKEUP. The delay is used to wake up the MIPI slave from ULPS state. The clock is the low power clock.	Per Application Condition

8.1.25 Delay Adjustment Register 6

Offset Address

DAR6 **Delay Adjustment Register 6** **0xCE**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME					**TGO**			
TYPE	RO	RO	RO	RO	RW			
RESET	0x0	0x0	0x0	0x0	0x4			
BIT	7	6	5	4	3	2	1	0
NAME					**TGET**			
TYPE	RO	RO	RO	RO	RW			
RESET	0x0	0x0	0x0	0x0	0x5			

Table 8-25: Delay Adjustment Register 6 Description

Name	Description	Setting
Reserved Bit 31-12	**Reserved**	Not Applicable
TGO Bit 11-8	**TGO** – TA Go Delay These bits specifies the number of TLPX for TA go delay period TTA-GO.	Per Application Condition
Reserved Bit 7-4	**Reserved**	Not Applicable
TGET Bit 3-0	**TGET** – TA Get Delay These bits specifies the number of TLPX for TA get delay period TTA-GET.	Per Application Condition

8.1.26 HS TX Timer Register 1

Offset Address

HTTR1 **HS TX Timer Register 1** **0xCF**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**HTT_L[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**HTT_L[7:0]**							
TYPE	RW							
RESET	0x00							

Table 8-26: HS TX Timer Register 1 Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
HTT_L Bit 15-0	**HTT_L** – HS TX Timer Low These bits are the lower 16 bits of the HTT. These bits specify the HS TX timer timeout value. PLL reference clock is used to increment an internal timer. The timer starts when the SSD2831 enters HS transmit mode. When the SSD2831 exits from HS transmit mode, the timer will be reset. If the timer expires before the end of HS transmission, the SSD2831 will signal an error and switch to LP mode to continue the transmission. At the same time, the HS bit will be cleared to 0. Software intervention is required so that the SSD2831 can go back to proper HS transmission mode.	Per Application Condition

8.1.27 HS TX Timer Register 2

Offset Address

HTTR2 **HS TX Timer Register 2** **0xD0**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**HTT_H[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**HTT_H[7:0]**							
TYPE	RW							
RESET	0x00							

Table 8-27: HS TX Timer Register 2 Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
HTT_H Bit 15-0	**HTT_H** – HS TX Timer High These bits are the upper 16 bits of the HTT. These bits specify the HS TX timer timeout value. PLL reference clock is used to increment an internal timer. The timer starts when the SSD2831 enters HS transmit mode. When the SSD2831 exits from HS transmit mode, the timer will be reset. If the timer expires before the end of HS transmission, the SSD2831 will signal an error and switch to LP mode to continue the transmission. At the same time, the HS bit will be cleared to 0. Software intervention is required so that the SSD2831 can go back to proper HS transmission mode.	Per Application Condition

8.1.28 LP RX Timer Register 1

Offset Address

LRTR1 **LP RX Timer Register 1** **0xD1**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**LRT_L[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**LRT_L[7:0]**							
TYPE	RW							
RESET	0x00							

Table 8-28: LP RX Timer Register 1 Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
LRT_L Bit 15-0	**LRT_L** – LP RX Timer Low These bits are the lower 16 bits of the LRT. These bits specify the LP RX timer timeout value. PLL reference clock is used to increment an internal timer. The timer starts when the SSD2831 enters LP receive mode. When the SSD2831 exits from LP receive mode, the timer will be reset. If the timer expires before exiting from LP receive mode, the SSD2831 will signal an error and switch to LP transmit mode. The DPHY will drive the data lane to LP11 state. Software intervention is required so that any possible error could be cleared.	Per Application Condition

8.1.29 LP RX Timer Register 2

Offset Address

LRTR2 **LP RX Timer Register 2** **0xD2**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**LRT_H[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**LRT_H[7:0]**							
TYPE	RW							
RESET	0x00							

Table 8-29: LP RX Timer Register 2 Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
LRT_H Bit 15-0	**LRT_H** – LP RX Timer High These bits are the upper 16 bits of the LRT. These bits specify the LP RX timer timeout value. PLL reference clock is used to increment an internal timer. The timer starts when the SSD2831 enters LP receive mode. When the SSD2831 exits from LP receive mode, the timer will be reset. If the timer expires before exiting from LP receive mode, the SSD2831 will signal an error and switch to LP transmit mode. The DPHY will drive the data lane to LP11 state. Software intervention is required so that any possible error could be cleared.	Per Application Condition

8.1.30 TE Status Register

Offset Address

TESR **TE Status Register** **0xD3**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME		**CMD_BC**	**TE_OUT_SEL1**	**TE_OUT_SEL0**	**TE_IN_SEL1**	**TE_IN_SEL0**	**TER1**	**TER0**
TYPE	RO	RW	RW	RW	RW	RW	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-30: TE Status Register Description

Name	Description	Setting
Reserved Bit 31-7	**Reserved**	Not Applicable
CMD_BC Bit 6	**CMD_BC** – Command Broadcast This bit select whether to broadcast the 2C/3C content from MIPITX0 to MIPITX1 when the configuration is 1x2(**RX_DUAL**=0, **TX_DUAL**=1) for DSI input.	0 - No Broadcast 1 - Broadcast
TE_OUT_SEL1 Bit 5	**TE_OUT_SEL1** – TE output from MIPITX1 This bit select whether to send the TE output from MIPITX1 via the MIPIRX1 or TE_OUT1 pin.	0 - Internal TE is sent to TE_OUT_1 pin 1 - Internal TE is sent to MIPIRX1
TE_OUT_SEL0 Bit 4	**TE_OUT_SEL0** – TE output from MIPITX0 This bit select whether to send the TE output from MIPITX0 via the MIPIRX0 or TE_OUT0 pin.	0 - Internal TE is sent to TE_OUT_0 pin 1 - Internal TE is sent to MIPIRX0
TE_IN_SEL1 Bit 3	**TE_OUT_SEL1** – TE output from MIPITX1 This bit select which TE input to be used for pulse shaping.	0 - TE is taken from TE_IN_1 pin 1 - TE is taken from MIPITX1
TE_IN_SEL0 Bit 2	**TE_OUT_SEL0** – TE output from MIPITX0 This bit select which TE input to be used for pulse shaping.	0 - TE is taken from TE_IN_0 pin 1 - TE is taken from MIPITX0

Name	Description	Setting
TE_RESP1 Bit 1	**TE_RESP1** – TE Response from MIPITX1 This bit reflects whether a TE response has been received or not. Once a TE response is received, this bit will be set to 1. At the same time, the output TE signal will go high. The host processor can write 1 to clear this bit. Once the bit is cleared, the TE signal will go low.	0 –TE response has not been received 1 – TE response has been received
TE_RESP0 Bit 0	**TE_RESP0** – TE Response from MIPITX0 This bit reflects whether a TE response has been received or not. Once a TE response is received, this bit will be set to 1. At the same time, the output TE signal will go high. The host processor can write 1 to clear this bit. Once the bit is cleared, the TE signal will go low.	0 –TE response has not been received 1 – TE response has been received

8.1.31 SPI Read Register

Offset Address

SRR **SPI Read Register** **0xD4**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**RRA**							
TYPE	RW							
RESET	0xFA							

Table 8-31: SPI Read Register Description

Name	Description	Setting
Reserved Bit 31-8	**Reserved**	Not Applicable
RRA Bit 7-0	**RRA** – Register Read Address These bits specify the address of the register to be read through the SPI interface, when the interface is SPI 8-bit (either 3 wire or 4 wire).	Per Application Condition

8.1.32 PLL Lock Register

Offset Address

PLR **PLL Lock Register** **0xD5**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**LOCK[15:8]**							
TYPE	RW							
RESET	0x14							
BIT	7	6	5	4	3	2	1	0
NAME	**LOCK[7:0]**							
TYPE	RW							
RESET	0x50							

Table 8-32: PLL Lock Register Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
LOCK Bit 15-0	**LOCK** – Lock Counter These bits specify the PLL lock range in term of PLL reference frequency. The maximum PLL lock period is 500us and the default setting assumed the reference clock is 10Mhz.	Per Application Condition

8.1.33 Test Register

Offset Address

TR **Test Register** **0xD6**

BIT	31	30	29	28	27	26	25	24
NAME				**EHS**				
TYPE	RO	RO	RO	RW	RW			
RESET	0x0	0x0	0x0	0x1	0x0			
BIT	23	22	21	20	19	18	17	16
NAME	**VIDEO_3D[2:0]**				**COMP_SLICE**			
TYPE	RW			RO	RW			
RESET	0x0			0x0	0x0			
BIT	15	14	13	12	11	10	9	8
NAME	**TM**		**EIC**					**DIS_CONT**
TYPE	RW		RW					RW
RESET	0x0		0x00					0x1
BIT	7	6	5	4	3	2	1	0
NAME	**PNB**						**END**	**CO**
TYPE	RW						RW	RW
RESET	0x01						0x0	0x1

Table 8-33: Test Register Description

Name	Description	Setting
Reserved Bit 31-29	**Reserved**	Not Applicable
EHS Bit 28	**EHS** – Early High Speed clock This bit is used to allow MIPI output to enter HS 1 line earlier before the video data transmission.	0 - disable 1 - enable
Reserved Bit 27-21	**Reserved**	Not Applicable
Reserved Bit 20	**Reserved**	Not Applicable
COMP_SLICE Bit 19-16	**COMP_SLICE** – Number of Compressed Slice per Line These bits indicate the number of slice per line when the input DSI video stream is compressed data.	0 – 1 slice per line .. 15 –16 slices per line
TM Bit 15-14	**TM** – Test Mode These bits selects whether to inject CRC/ECC error for the outgoing streams. They are used for debugging purpose only. They should be set to 00 in normal mode.	00 – Normal mode 01 – Inject CRC error 10 – Inject 1 bit ECC error 11 – Inject 2 bit ECC error
EIC Bit 13-9	**EIC** – Error Injection Control	Per Application Condition

Name	Description	Setting
	These bits control the position of the error being injected for testing. It is only applicable when TM is 01.	
DIS_CONT Bit 8	**DIS_CONT** – Disable Contention input from Analog This bit selects whether to ignore the error contention signals output from the Phy.	0 – Enable 1 – Disable
PNB Bit 7-2	**PNB** – Packet Number during Blanking These bits control the number of packet to send during video mode blanking period.	Per Application Condition
END Bit 1	**END** – Endian-ness This bit specifies the endian-ness of the data transmitted over the serial link. During video mode transmission, this bit must be set to 0 so as to follow the MIPI DSI specification.	0 – Least significant byte sent first 1 – Most significant byte sent first
CO Bit 0	**CO** – Color Order This bit specifies the order of the color component in the pixel. During video mode transmission, this bit must be set to 1 so as to follow the MIPI DSI specification..	0 – RGB. R is in the higher portion of the pixel 1 – BGR. B is in the higher portion of the pixel

8.1.34 TE Count Register

Offset Address

TECR **TE Count Register** **0xD7**

BIT	31	30	29	28	27	26	25	24
NAME	**TEC1[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	23	22	21	20	19	18	17	16
NAME	**TEC1[7:0]**							
TYPE	RW							
RESET	0x01							
BIT	15	14	13	12	11	10	9	8
NAME	**TEC0[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**TEC0[7:0]**							
TYPE	RW							
RESET	0x01							

Table 8-34: TE Count Register Description

Name	Description	Setting
TEC1 Bit 31-16	**TEC1** – TE Counter for MIPITX1 These bits determines the pulse width of the output TE signal. A counter will be started after the TE signal goes to 1. When the counter reaches the value in **TEC1** field, the TE signal will be set to 0. The counter uses the PLL reference clock to do counting. The minimum value is 1.	Per Application Condition
TEC0 Bit 15-0	**TEC0** – TE Counter for MIPITX0 These bits determines the pulse width of the output TE signal. A counter will be started after the TE signal goes to 1. When the counter reaches the value in **TEC0** field, the TE signal will be set to 0. The counter uses the PLL reference clock to do counting. The minimum value is 1.	Per Application Condition

8.1.35 Analog Control Register 1

Offset Address

ACR1 **Analog Control Register 1** **0xD8**

BIT	31	30	29	28	27	26	25	24
NAME	**THFT_TLFT1**	**THFT_TLFT0**	**EN_REG**	**HSTX_RO_IN**				**LPTX_DS[2]**
TYPE	RW	RW	RW	RW				RW
RESET	0x0	0x0	0x1	0x5				0x0
BIT	23	22	21	20	19	18	17	16
NAME	**LPTX_DS[1:0]**		**BG_TRIM_V0P6**			**BG_IRX**		
TYPE	RW		RW			RW		
RESET	0x0		0x3			0x4		
BIT	15	14	13	12	11	10	9	8
NAME	**BG_TC**			**BG_TEN**	**BG_TRIM_0P5**			**BG_IDUTY[2]**
TYPE	RW			RW	RW			RW
RESET	0x4			0x0	0x3			0x1
BIT	7	6	5	4	3	2	1	0
NAME	**BG_IDUTY[1:0]**		**BG_IREG**		**BG_ISEL**			**EN_BG**
TYPE	RW		RW		RW			RW
RESET	0x0		0x1		0x4			0x1

Table 8-35: Analog Control Register 1 Description

Name	Description	Setting
THFT_TLFT1 Bit 31	**THFT_TLFT1** – Low Power Receiver Input Threshold High/Low Adjust Bit 1	Per Application Condition
THFT_TLFT0 Bit 30	**THFT_TLFT0** – Low Power Receiver Input Threshold High/Low Adjust Bit 0	Per Application Condition
EN_REG Bit 29	**EN_REG** – 0.5V LDO enable	Per Application Condition
HSTX_RO_IN Bit 28-25	**HSTX_RO_IN** – Driver output resistance control	Per Application Condition
LPTX_DS Bit 24-22	**LPTX_DS** – Low Power Transmitter Drive Strength	Per Application Condition
BG_TRIM_V0P6 Bit 21-19	**BG_TRIM_V0P6** – Voltage trimming bits	Per Application Condition
BG_IRX Bit 18-16	**BG_IRX** – Biasing current adjustment high speed receiver	Per Application Condition
BG_TC Bit 15-13	**BG_TC** – Temperature coefficient programming bits of bandgap	Per Application Condition
BG_TEN Bit 12	**BG_TEN** – Bandgap Test Enable	Per Application Condition
BG_TRIM_0P5 Bit 11-9	**BG_TRIM_0P5** – Voltage trimming bits of 0.5V LDO	Per Application Condition

Name	Description	Setting
BG_IDUTY Bit 8-6	**BG_IDUTY** – Biasing current adjustment of duty cycle regulation circuit	Per Application Condition
BG_IREG Bit 5-4	**BG_IREG** – Biasing current adjustment of 0.5V LDO	Per Application Condition
BG_ISEL Bit 3-1	**BG_ISEL** – Biasing current adjustment of contention detection	Per Application Condition
EN_BG Bit 0	**EN_BG** – Bandgap Enable	Per Application Condition

8.1.36 Analog Control Register 4

Offset Address

ACR4 **Analog Control Register 4** **0xDB**

BIT	31	30	29	28	27	26	25	24
NAME	**CLK_DUTY_REG_BYPASS**	**ROUT_EN**			**DPHY_HSRX_EQ_C3**			**DPHY_HSRX_EQ_C2[2]**
TYPE	RW	RW			RW			RW
RESET	0x1	0x0			0x7			0x1
BIT	23	22	21	20	19	18	17	16
NAME	**DPHY_HSRX_EQ_C2[1:0]**		**DPHY_HSRX_EQ_C1**			**DPHY_RX_LPTX_DS**		
TYPE	RW		RW			RW		
RESET	0x3		0x7			0x0		
BIT	15	14	13	12	11	10	9	8
NAME	**HSRXTI**				**DPHY_HSRX_EQ_R3**	**DPHY_HSRX_EQ_R2**	**DPHY_HSRX_EQ_R1**	**DPHY_RX_TM_EB1**
TYPE	RW				RW	RW	RW	RW
RESET	0x5				0x0	0x0	0x1	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**DPHY_RX_HS_BIAS_ENB1**	**DPHY_RX_TM_EB0**	**DPHY_RX_HS_BIAS_ENB0**					
TYPE	RW	RW	RW	RW			RW	RW
RESET	0x0	0x0	0x0	0x0			0x0	0x0

Table 8-36: Analog Control Register 4 Description

Name	Description	Setting
CLK_DUTY_REG_BYPASS Bit 31	**CLK_DUTY_REG_BYPASS** – Clock Duty Regulator Bypass	Per Application Condition
ROUT_EN Bit 30-28	**ROUT_EN** – High Speed Receiver Limiting Amplifier Output Impedance Adjust	Per Application Condition
DPHY_HSRX_EQ_C3 Bit 27-25	**DPHY_HSRX_EQ_C3** – High speed receiver equalizer for 3rd stage LA capacitor selection	Per Application Condition
DPHY_HSRX_EQ_C2 Bit 24-22	**DPHY_HSRX_EQ_C2** – High speed receiver equalizer for 2nd stage LA capacitor selection	Per Application Condition
DPHY_HSRX_EQ_C1 Bit 21-19	**DPHY_HSRX_EQ_C1** – High speed receiver equalizer for 1st stage LA capacitor selection	Per Application Condition
DPHY_RX_LPTX_DS Bit 18-16	**DPHY_RX_LPTX_DS** – Low Power Transmitter Driver Strength	Per Application Condition

Name	Description	Setting
HSRXTI Bit 15-12	**HSRXTI** – High speed receiver Termination setting	Per Application Condition
DPHY_HSRX_EQ_R3 Bit 11	**DPHY_HSRX_EQ_R3** – High speed receiver equalizer for 3rd stage LA resistor selection	Per Application Condition
DPHY_HSRX_EQ_R2 Bit 10	**DPHY_HSRX_EQ_R3** – High speed receiver equalizer for 2nd stage LA resistor selection	Per Application Condition
DPHY_HSRX_EQ_R1 Bit 9	**DPHY_HSRX_EQ_R1** – High speed receiver equalizer for 1st stage LA resistor selection	Per Application Condition
DPHY_RX_TM_EB1 Bit 8	**DPHY_RX_TM_EB1** – High speed termination enable for MIPIRX1	Per Application Condition
DPHY_RX_HS_BIAS_ENB1 Bit 7	**DPHY_RX_HS_BIAS_ENB1** – High Speed Bias current enable for MIPIRX1	Per Application Condition
DPHY_RX_TM_EB0 Bit 6	**DPHY_RX_TM_EB0** – High speed termination enable for MIPIRX0	Per Application Condition
DPHY_RX_HS_BIAS_ENB0 Bit 5	**DPHY_RX_HS_BIAS_ENB0** – High Speed Bias current enable for MIPIRX0	Per Application Condition
Reserved Bit 4-2	**Reserved**	Not Applicable
Reserved Bit 1	**Reserved**	Not Applicable
Reserved Bit 0	**Reserved**	Not Applicable

8.1.37 Interrupt Output Control Register

Offset Address

IOCR **Interrupt Output Control Register** **0xDC**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RW		RW	RW			RW	
RESET	0x0		0x0	0x3			0x1	
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RW					RW		
RESET	0x9					0x0		
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME						**IAS**		
TYPE	RO	RO	RO	RO	RO	RW	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-37: Interrupt Output Control Register Description

Name	Description	Setting
Reserved Bit 31-30	**Reserved**	Not Applicable
Reserved Bit 29	**Reserved**	Not Applicable
Reserved Bit 28-26	**Reserved**	Not Applicable
Reserved Bit 25-24	**Reserved**	Not Applicable
Reserved Bit 23-19	**Reserved**	Not Applicable
Reserved Bit 18-16	**Reserved**	Not Applicable
Reserved Bit 15-3	**Reserved**	Not Applicable
IAS Bit 2	**IAS** – Interrupt Active State This bit selects the polarity of the INT pin at the chip IO.	**0** – INT pin is active low, when there is no interrupt events, it is normally high 1 – INT pin is active high, when there is no interrupt events, it is normally low**.**
Reserved Bit 1-0	**Reserved**	Not Applicable

8.1.38 RGB Interface Control Register 7

Offset Address

RICR7 **RGB Interface Control Register 7** **0xDD**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME						**VEC**	**XEQ1**	**XEQ0**
TYPE	RO	RO	RO	RO	RO	RW	RWAC	RWAC
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**VBN**				**VFN**			
TYPE	RW				RW			
RESET	0x0				0x0			

Table 8-38: RGB Interface Control Register 7 Description

Name	Description	Setting
Reserved Bit 31-11	**Reserved**	Not Applicable
VEC Bit 10	**VEC –** Video Enable Control This bit controls how command is handled during video mode, **VEN**.	0 - Any command received will output immediately if there is no video packet to send. 1 - Any command received will only be output during the blanking period after first video packet is received. If there is no video packet to be sent, the command is held.
XEQ1 Bit 9	**XEQ1 –** Execute Queue for MIPITX1 This bit will cause SSD2831 to generate Execute Queue Packet(0x16) at the last line of the frame, after hsync packet. It will be cleared when Execute Queue Packet is sent out. This bit is auto cleared by hardware.	0 - Do nothing 1 - Send Execute Queue Packet(0x16) at the last line of the current frame, after hsync.
XEQ0 Bit 8	**XEQ –** Execute Queue for MIPITX0 This bit will cause SSD2831 to generate Execute Queue Packet(0x16) at the last line of the frame, after hsync packet. It will be cleared when Execute Queue Packet is sent out. This bit is auto cleared by hardware.	0 - Do nothing 1 - Send Execute Queue Packet(0x16) at the last line of the current frame, after hsync.

Name	Description	Setting
VBN Bit 7-4	**VBN –** Vertical Back Porch Non Video Data Window These fields specify the number of vertical back porch counting backward from the first vertical active line in which non-video data is not allowed to be sent via MIPI link. This field is only valid when **VEN** is 1 and if_sel[0] = 0. This field should not larger than VBP	Per Application Condition
VFN Bit 3-0	**VFN –** Vertical Front Porch Non Video Data Window These fields specify the number of vertical front porch counting forward from the last vertical active line in which non-video data is not allowed to be sent via MIPI link. This field is only valid when **VEN** is 1 and if_sel[0] = 0. This field should not larger than VFP.	Per Application Condition

8.1.39 INOUT Configuration Control Register

Offset Address

IOCR **INOUT Configuration Register** **0xDE**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME				**RX_DUAL**	**RX_LS1**		**RX_LS0**	
TYPE	RW	RW	RW	RW	RW		RW	
RESET	0x0	0x0	0x0	0x0	0x0		0x0	
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**TX_READ**	**TX_WRITE**		**TX_DUAL**	**TX_LS1**		**TX_LS0**	
TYPE	RW	RW		RW	RW		RW	
RESET	0x0	0x1		0x0	0x0		0x0	

Table 8-39: INOUT Configuration Register Description

Name	Description	Setting
Reserved Bit 31-27	**Reserved**	Not Applicable
Reserved Bit 26	**Reserved**	Not Applicable
Reserved Bit 25	**Reserved**	Not Applicable
Reserved Bit 24	**Reserved**	Not Applicable
Reserved Bit 23	**Reserved**	Not Applicable
Reserved Bit 22	**Reserved**	Not Applicable
Reserved Bit 21	**Reserved**	Not Applicable
RX_DUAL Bit 20	**RX_DUAL – M**IPIRX dual mode This bit defines the dual/single mode of MIPIRX.	0 – Single mode 1 – Dual mode
RX_LS1 Bit 19-18	**RX_LS1** – Lane Select for MIPIRX1 These bits define the number of lane to be used for MIPIRX1 in SSD2831.	00 – 1 lane mode 01 – 2 lane mode 10 – 3 lane mode 11 – 4 lane mode
RX_LS0 Bit 17-16	**RX_LS0** – Lane Select for MIPIRX0	00 – 1 lane mode 01 – 2 lane mode 10 – 3 lane mode

Name	Description	Setting
	These bits define the number of lane to be used for MIPIRX0 in SSD2831.	11 – 4 lane mode
Reserved Bit 15-8	**Reserved**	Not Applicable
TX_READ Bit 7	**TX_READ** – TX read This bit determines the destination of the read command when SSD2831 is configured as 1 input with 2 output(MIPITX).	0 - Read from MIPITX0 1 - Read from MIPITX1
TX_WRITE Bit 6-5	**TX_WRITE** – TX write This bit determines the destination of the write command when SSD2831 is configured as 1 input with 2 output(MIPITX).	00 - Discard 01 - Write to MIPITX0 10 - Write to MIPITX1 11 - Write to MIPITX0 and MIPITX1
TX_DUAL Bit 4	**TX_DUAL –** MIPITX dual mode This bit defines the dual/single mode of MIPITX.	0 – Single mode 1 – Dual mode
TX_LS1 Bit 3-2	**TX_LS1** – Lane Select for MIPITX1 These bits define the number of lane to be used for MIPITX1 in SSD2831.	00 – 1 lane mode 01 – 2 lane mode 10 – 3 lane mode 11 – 4 lane mode
TX_LS0 Bit 1-0	**TX_LS0** – Lane Select for MIPITX0 These bits define the number of lane to be used for MIPITX0 in SSD2831.	00 – 1 lane mode 01 – 2 lane mode 10 – 3 lane mode 11 – 4 lane mode

8.1.40 Delay Adjustment Register 7

Offset Address

DAR7 **Delay Adjustment Register 7** **0xDF**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME			**HED1**					
TYPE	RO	RO	RW					
RESET	0x0	0x0	0x0					
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME			**HED0**					
TYPE	RO	RO	RW					
RESET	0x0	0x0	0x0					

Table 8-40: Delay Adjustment Register 7 Description

Name	Description	Setting
Reserved Bit 31-22	**Reserved**	Not Applicable
HED1 Bit 21-16	**HED1 –** HS Exit Delay for MIPITX1 These bits specifies the number of system clock for HS exit delay period for data and clock lane.	Per Application Condition
Reserved Bit 15-6	**Reserved**	Not Applicable
HED0 Bit 5-0	**HED0 –** HS Exit Delay for MIPITX0 These bits specifies the number of system clock for HS exit delay period for data and clock lane.	Per Application Condition

8.1.41 APB Write Register

Offset Address

AWR **APB Write Register** **0xE0**

BIT	47	46	45	44	43	42	41	40
NAME	**DATA[31:24]**							
TYPE	W							
RESET	0x00							
BIT	39	38	37	36	35	34	33	32
NAME	**DATA[23:16]**							
TYPE	W							
RESET	0x00							
BIT	31	30	29	28	27	26	25	24
NAME	**DATA[15:8]**							
TYPE	W							
RESET	0x00							
BIT	23	22	21	20	19	18	17	16
NAME	**DATA[7:0]**							
TYPE	W							
RESET	0x00							
BIT	15	14	13	12	11	10	9	8
NAME	**ADDR[15:8]**							
TYPE	W							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**ADDR[7:0]**							
TYPE	W							
RESET	0x00							

Table 8-41: Delay Adjustment Register Description

Name	Description	Setting
DATA Bit 47-16	**DATA –** 32-bit write data for APB	Refer to APB write section
ADDR Bit 15-0	**ADDR –** 16-bit address for APB write/read	Refer to APB write section

8.1.42 APB Read Register

Offset Address

ARR **APB Read Register** **0xE1**

BIT	31	30	29	28	27	26	25	24
NAME	**DATA[31:24]**							
TYPE	R							
RESET	0x0							
BIT	23	22	21	20	19	18	17	16
NAME	**DATA[23:16]**							
TYPE	R							
RESET	0x0							
BIT	15	14	13	12	11	10	9	8
NAME	**DATA[15:8]**							
TYPE	R							
RESET	0x0							
BIT	7	6	5	4	3	2	1	0
NAME	**DATA[7:0]**							
TYPE	R							
RESET	0x0							

Table 8-42: APB Read Register Description

Name	Description	Setting
DATA Bit 31-0	**DATA** – 32 bits read data	Refer to APB read section

8.2 Local (APB) Registers Descriptions

The APB registers have 16 bit address, of which the most significant 4 bits represent the base address of the APB peripheral, and the least significant 16 bits represent the offset within the APB peripheral. The table below shows the APB peripherals and their respective base address & address range.

Address	Module
0x0000 – 0x0FFF	SCM
0x1000 – 0x1FFF	Reserved
0x2000 – 0x2FFF	Reserved
0x3000 – 0x3FFF	MIPI DSI RX
0x4000 – 0x4FFF	Reserved
0x5000 – 0x7FFF	Video BIST
0x6000 – 0x6FFF	Pixel Peek

8.2.1 SCM Registers Descriptions

8.2.1.1 SCM Miscellaneous Control Register

Offset Address

SCM_MISC **SCM Miscellaneous Control Register** **0x0010**

BIT	31	30	29	28	27	26	25	24
NAME			**ckmon**	lpstate				
TYPE	RO	RO	RW	RW	RW	RW	RW	
RESET	0x0	0x0	0x1	0x0	0x1	0x1	0x0	
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RW		RW		RW	RW	RW	RW
RESET	0x2		0x1		0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**clkout_sel**				**rx_ds1**		**rx_pns1**	
TYPE	RW				RW		RW	RW
RESET	0x0				0x3		0x1	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**flip1**	**flip0**						
TYPE	RW	RW	RW		RW	RW		RW
RESET	0x0	0x0	0x0		0x0	0x0		0x0

Table 8-43: SCM Miscellaneous Control Description

Name	Description	Setting
Reserved Bit31-30	**Reserved**	Not Applicable
clkmon Bit29	**Clock Monitor on TE_OUT0 –** This bit enable the TE_OUT0 to be used as clkout monitor signals	Per Application Condition
lpstate Bit28	**LP State –** This bit controls the state of the link when the chip is powered down	0=LP00 1=LP11
Reserved Bit 27-17	**Reserved**	Not Applicable
Reserved Bit 16	**Reserved**	Not Applicable
clkout_sel Bit 15-12	**Clock Out Select –** Select which internal clock is routed out for monitor	Per Application Condition
rx_ds1 Bit 11-10	**MIPI DSI_RX1 Data Lane Swap –** These bits configure the lane swapping feature of the MIPI DSI_RX1 pins	Per Application Condition
rx_pns1 Bit 9	**MIPI DSI_RX1 Polarity Swap –** This bit configures the polarity swap on the MIPI pins for DSI_RX1 pins	Per Application Condition
Reserved Bit 8	Reserved	Not Applicable
mtx_flip1 Bit 7	**MIPI Left/Right Flip for DSI1** – This bit configures the left and right image swap at the MIPI output.	0x0 = Data received from read from left to right (Default) 0x1 = Data received from read from right to left
mtx_flip0 Bit 6	**MIPI Left/Right Flip for DSI0** – This bit configures the left and right image swap at the MIPI output.	0x0 = Data received from read from left to right (Default) 0x1 = Data received from read from right to left
Reserved Bit 5-4	**Reserved**	Not Applicable
Reserved Bit 3	**Reserved**	Not Applicable
Reserved Bit 2-1	**Reserved**	Not Applicable
Reserved Bit 0	**Reserved**	Not Applicable

The table for the MIPI DSI_RX swap is as below. Note that MIPI DSI_RX0 is controlled by PS[4:2]

PS[4] = PNSW

PS[3:2] = LNSW[1:0]

Pin	<LNSW[1:0], PNSW>							
	111	110	101	100	011	010	001	000
DP2	d2_p	d2_n	d0_p	d0_n	d3_p	d3_n	d3_p	d3_n
DN2	d2_n	d2_p	d0_n	d0_p	d3_n	d3_p	d3_n	d3_p
DP1	d1_p	d1_n	d1_p	d1_n	d0_p	d0_n	d2_p	d2_n
DN1	d1_n	d1_p	d1_n	d1_p	d0_n	d0_p	d2_n	d2_p
CP	clk_p	clk_n	clk_p	clk_n	clk_p	clk_n	clk_p	clk_n
CN	clk_n	clk_p	clk_n	clk_p	clk_n	clk_p	clk_n	clk_p
DP0	d0_p	d0_n	d2_p	d2_n	d1_p	d1_n	d1_p	d1_n
DN0	d0_n	d0_p	d2_n	d2_p	d1_n	d1_p	d1_n	d1_p
DP3	d3_p	d3_n	d3_p	d3_n	d2_p	d2_n	d0_p	d0_n
DN3	d3_n	d3_p	d3_n	d3_p	d2_n	d2_p	d0_n	d0_p

8.2.1.2 SCM Scratch Register

Offset Address

SCM_SCRATCH **SCM Scratch Register** **0x0014**

BIT	31	30	29	28	27	26	25	24
NAME	**scratch[31:24]**							
TYPE	RW							
RESET	0x00							
BIT	23	22	21	20	19	18	17	16
NAME	**scratch[23:16]**							
TYPE	RW							
RESET	0x00							
BIT	15	14	13	12	11	10	9	8
NAME	**scratch[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**scratch0[7:0]**							
TYPE	RW							
RESET	0x00							

Table 8-44: SCM Scratch Register Description

Name	Description	Setting
scratch Bit 31-0	**Scratch Register –** User can use this register to store any value	Not Applicable

8.2.2 MIPI DSI RX Registers Description

8.2.2.1 MIPIRX Configuration 1 Register

Offset Address

MIPIRX _CFG1R **MIPIRX Configuration 1 Register** **0x0000**

BIT	31	30	29	28	27	26	25	24
NAME	**erm_h**							
TYPE	RW							
RESET	0x00							
BIT	23	22	21	20	19	18	17	16
NAME	**erm_l**							
TYPE	RW							
RESET	0x00							
BIT	15	14	13	12	11	10	9	8
NAME	**tm**		**te_en**	**te_pol**	**pclk_start**			**check_vc00**
TYPE	RW		RW	RW	RW	RO	RO	RW
RESET	0x0		0x1	0x0	0x1	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	tc_clr_err	**dsi_clr_err**	**pcu_timer_dis**	**hsclk_rst_en**	**byp_sfifo**	**crc_en**	**noeot_en**	**ecc_en**
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x1	0x1	0x1

Table 8-45: MIPIRX Configuration Register 1 Description

Name	Description	Setting
erm_h Bit 31:24	**Error Report Mask High** – Refer to erm_l for description.	Per Application Condition
erm_l Bit 23:16	**Error Report Mask Low** – These 16 bits control whether to enable the detection of MIPI DSI error. The bit position correspond to the Error Report defined in the DSI Specification.	Error Mask [15:0] = {erm_h, erm_l} 0 = Disable 1 = Enable Error Report defined in the DSI specification: Bit Error ---------- 0: SoT Error 1: SoT Sync Error 2: EoT Sync Error 3: Escape Mode Entry Command Error 4: Low-Power Transmit Sync Error 5: HS Receive Timeout Error 6: False Control Error 7: Reserved 8: ECC Error, single-bit (detected and corrected)

Name	Description	Setting
		9: ECC Error, multi-bit (detected, not corrected) 10: Checksum Error (Long packet only) 11: DSI Data Type Not Recognized 12: DSI VC ID Invalid 13: Invalid Transmission Length 14: Reserved 15: DSI Protocol Violation
tm Bit 15:14	**Test Mode** – These bits control whether to inject ECC/CRC error for outgoing streams. This is for tesing only. They should be set to 2'b00 during normal mode.	00 = Normal 01 = Inject CRC error 10 = Inject 1 bit ECC error 11 = Inject 2 bits ECC error
te_en Bit 13	**Tearing Effect Enable –** Enable the detection of TE input	Per Application Condition
te_pol Bit 12	**Tearing Effect Polarity –** Select the polarity of the TE input	0 = Rise 1 = Fall
pclk_start Bit 11	**Pixel Clock Start –** Enable the reception of RGB packets	Per Application Condition
Reserved Bit 10:9		Not Applicable
check_vc00 Bit 8	**Check Virtual Channel** 00 – When enabled, if the Virtual Channel ID of the packet is the same as 2'b00, the packet is for accessing this device. If it is not the same, the packet will be discarded and error flag is set.	0 = Enable 1 = Disable
tc_clr_err Bit 7	**Total Count Clear Error** – Clear the total count error accumulated on ECC/CRC errors.	0 = No Clear 1 = Clear Error
dsi_clr_err Bit 6	**DSI Clear Error** – Clear the DSI status errors on 0x0010.	0 = No Clear 1 = Clear Error
pcu_timer_dis Bit 5	**Disable HSRX/LPTX timer -** Disable internal timers for HS Receive and LP Transmit.	0 = Enable 1 = Disable
hsclk_rst_en Bit 4	**HS Clock Reset Enable -** Disable internal High speed clock when Data lanes goes LP-11.	0 = Enable 1 = Disable
byp_sfifo Bit 3	**Bypass Sync FIFO in 4-lane mode -** This bit enable the sync FIFO in Lane Merger block to be bypassed in 4-lane mode.	0 = The internal synchronous FIFO is not bypassed in 4-lane mode. 1 = The internal synchronous FIFO is bypassed in 4-lane mode for power saving. This bit should be set in LP mode.
crc_en Bit 2	**CRC Enable –** DSI CRC enable/disable	0 = CRC disable 1 = CRC enable
noeot_en Bit 1	**No EOT Enable –** This bit allows MIPIRX to support those MIPI masters that do not generate DSI EOT packet at the end of the HS transmission, and at the same time, will not generate MIPI DSI error when read.	0 = Used for newer version of mipi dsi where dsi eotp is supported. 1 = Used in older version of mipi dsi where dsi eotp is not supported.
ecc_en Bit 0	**ECC Enable –** DSI ECC enable/disable	0 = ECC detection disable 1 = ËCC detection enable

8.2.2.2 MIPIRX Configuration 2 Register

Offset Address

MIPIRX _CFG2R **MIPIRX Configuration 2 Register** **0x0004**

BIT	31	30	29	28	27	26	25	24
NAME							**endian**	**co**
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME	**tepw**							
TYPE	RW							
RESET	0x10							
BIT	15	14	13	12	11	10	9	8
NAME	**cext**							
TYPE	RW							
RESET	0x40							
BIT	7	6	5	4	3	2	1	0
NAME		**eot**				**sse**		**derc**
TYPE	RO	RW				RW		RW
RESET	0x0	0x0				0x0		0x0

Table 8-46: MIPIRX Configuration Register 2 Description

Name	Description	Setting
Reserved Bit 31-26		Not Applicable
endian Bit 25	**Endian –** This bit set the endianness at the word to pixel conversion at the output of DSI receiver.	0 = No Endian swap 1 = Endian swap to byte data
co Bit 24	**Color Order –** This bit set the color order at the word to pixel conversion at the output of DSI receiver.	0 = No Color order swap 1 = BGR swap to RGB
tepw Bit 23-16	**Tearing Effect Pulse Width -** These bits determine how the MIPI RX IP qualifies the pulse width of the TE input signal. A valid TE signal is considered when the TE input signal is greater than the TEPW count. The TE pulse is counted using the oscillator clock.	Per Application Condition
Cext Bit 15-8	**Clock Extender -** These bits extend the clocks after the end of a request transaction. The counter will be reset once another new request is received before current counter expire.	Per Application Condition
Reserved Bit 7		Not Applicable
eot Bit 6-3	**End Of Transmission –** These bits specify the number of bits in the $T_{HS\text{-}TRAIL}$ period that are used for DPHY EOT detection. Please see MIPI DPHY spec for the details.	Per Application Condition

Name	Description	Setting
sse Bit 2-1	**Select SOT edge –** These bits control whether the MIPIRX search the SOT sequnce in positive, negative edge or both edges.	00 = Search SOT sequence in both edges 01 = Search SOT sequence in positive edge 10 = Search SOT sequence in negative edge 11 = Search SOT sequence in both edges
derc Bit 0	**DERC** - Disable Error Contention Detection This bit controls the disabling of the detection of error contention detected by the PH	0 = Enable 1 = Disable

8.2.2.3 MIPIRX Timer Register

Offset Address

MIPIRX _TMR **MIPIRX Timer Register** **0x0008**

BIT	31	30	29	28	27	26	25	24
NAME	**sc**							
TYPE	RW							
RESET	0xFF							
BIT	23	22	21	20	19	18	17	16
NAME	**tat**							
TYPE	RW							
RESET	0x20							
BIT	15	14	13	12	11	10	9	8
NAME	**hst**							
TYPE	RW							
RESET	0x0A							
BIT	7	6	5	4	3	2	1	0
NAME	tget				**tgo**			
TYPE	RW				RW			
RESET	0x5				0x4			

Table 8-47: MIPIRX Timer Register Description

Name	Description	Setting
sc Bit 31:24	**SOT Counter –** These are the SOT count which determines when the MIPI RX IP will stop searching for the SoT sequence defined in MIPI D-PHY. The searching starts after the HS Settle Time has been passed. Once the searching starts, a counter will start counting from zero. The searching will stop, if a SoT sequence has been identified or the counter reaches the value specified in this register or the data lane enters LP mode. The counter uses byte_clk for counting. The HS byte clock frequency is one eighth of the data rate on the date lane. For example, if the serial link is running at 200Mbps, the nibble clock is 25MHz.	Per Application Condition
tat Bit 23:16	**Turnaround Acknowledge Timer** – These bits, specify the turnaround acknowledge timer timeout value. rx_sys_clk is used to increment an internal timer.	Per Application Condition
hst Bit 15:8	**HS Settle Time –** These bits specifies the duration of THS-SETTLE, when the data lane switch from LP to HS mode. The period is for the MIPI not to sample the incoming HS data, as the line is in transition stage. Refer to Chapter 12, Interfaces (under HS-Settle Time sub-section)	Per Application Condition
tget Bit 7:4	**Turnaround Get –** These bits define the turnaround timer for TA-GET	Per Application Condition

Name	Description	Setting
tgo Bit 3:0	**Turnaround Go –** These bits define the turnaround timer for TA-GO	Per Application Condition

8.2.2.4 MIPIRX HSRX Timer Register

Offset Address

MIPIRX _HSRXR **MIPIRX HSRX Timer Register** **0x000C**

BIT	31	30	29	28	27	26	25	24
NAME	**htt[31:24]**							
TYPE	RW							
RESET	0x10							
BIT	23	22	21	20	19	18	17	16
NAME	**htt[23:16]**							
TYPE	RW							
RESET	0x00							
BIT	15	14	13	12	11	10	9	8
NAME	**htt[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**htt[7:0]**							
TYPE	RW							
RESET	0x00							

Table 8-48: MIPIRX HSRX Timer Register Description

Name	Description	Setting
htt Bit 31:0	**High Speed Receive Timer –** These bits specify the HS RX timer timeout value. rx_sys_clk is used to increment an internal timer.	Per Application Condition

8.2.2.5 MIPIRX LPTX Timer Register

Offset Address

MIPIRX _LPTXR **MIPIRX LPTX Timer Register** **0x0010**

BIT	31	30	29	28	27	26	25	24
NAME	**ltt[31:24]**							
TYPE	RW							
RESET	0x10							
BIT	23	22	21	20	19	18	17	16
NAME	**ltt[23:16]**							
TYPE	RW							
RESET	0x00							
BIT	15	14	13	12	11	10	9	8
NAME	**ltt[15:8]**							
TYPE	RW							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**ltt[7:0]**							
TYPE	RW							
RESET	0x00							

Table 8-49: MIPIRX LPTX Timer Register Description

Name	Description	Setting
ltt Bit 31:0	**Low Power Transmit Timer –** These bits specify the LP TX timer timeout value. rx_sys_clk is used to increment an internal timer.	Per Application Condition

8.2.2.6 MIPIRX Data Trim 1 Register

Offset Address

MIPIRX_DT1R **MIPIRX Delay Trim 1 Register** **0x0014**

BIT	31	30	29	28	27	26	25	24
NAME	**d3_clk_dly0**				**d3_data_dly0**			
TYPE	RW				RW			
RESET	0x0				0x0			
BIT	23	22	21	20	19	18	17	16
NAME	**d2_clk_dly0**				**d2_data_dly0**			
TYPE	RW				RW			
RESET	0x0				0x0			
BIT	15	14	13	12	11	10	9	8
NAME	**d1_clk_dly0**				**d1_data_dly0**			
TYPE	RW				RW			
RESET	0x0				0x0			
BIT	7	6	5	4	3	2	1	0
NAME	**d0_clk_dly0**				**d0_data_dly0**			
TYPE	RW				RW			
RESET	0x0				0x0			

Table 8-50: MIPIRX Delay Trim 1 Register Description

Name	Description	Setting
d3_clk_dly0 Bit 31-28	**Data 3 Clock Delay for DSI 0**	These bits trim the clock delay of lane 3 in DSI 0
d3_data_dly0 Bit 27-24	**Data 3 Data Delay for DSI 0**	These bits trim the data delay of lane 3 in DSI 0
d2_clk_dly0 Bit 23-20	**Data 2 Clock Delay for DSI 0**	These bits trim the clock delay of lane 2 in DSI 0
d2_data_dly0 Bit 19-16	**Data 2 Data Delay for DSI 0**	These bits trim the data delay of lane 2 in DSI 0
d1_clk_dly Bit 15-120	**Data 1 Clock Delay for DSI 0**	These bits trim the clock delay of lane 1 in DSI 0
d1_data_dly0 Bit 11-8	**Data 1 Data Delay for DSI 0**	These bits trim the data delay of lane 1 in DSI 0
d0_clk_dly0 Bit 7-4	**Data 0 Clock Delay for DSI 0**	These bits trim the clock delay of lane 0 in DSI 0
d0_data_dly0 Bit 3-0	**Data 0 Data Delay for DSI 0**	These bits trim the data delay of lane 0 in DSI 0

8.2.2.7 MIPIRX Data Trim 2 Register

Offset Address

MIPIRX_DT2R **MIPIRX Delay Trim 2 Register** **0x0018**

BIT	31	30	29	28	27	26	25	24
NAME	**d3_clk_dly1**				**d3_data_dly1**			
TYPE	RW				RW			
RESET	0x0				0x0			
BIT	23	22	21	20	19	18	17	16
NAME	**d2_clk_dly1**				**d2_data_dly1**			
TYPE	RW				RW			
RESET	0x0				0x0			
BIT	15	14	13	12	11	10	9	8
NAME	**d1_clk_dly1**				**d1_data_dly1**			
TYPE	RW				RW			
RESET	0x0				0x0			
BIT	7	6	5	4	3	2	1	0
NAME	**d0_clk_dly1**				**d0_data_dly1**			
TYPE	RW				RW			
RESET	0x0				0x0			

Table 8-51: MIPIRX Delay Trim 2 Register Description

Name	Description	Setting
d3_clk_dly1 Bit 31-28	**Data 3 Clock Delay for DSI 1**	These bits trim the clock delay of lane 3 in DSI 1
d3_data_dly1 Bit 27-24	**Data 3 Data Delay for DSI 1**	These bits trim the data delay of lane 3 in DSI 1
d2_clk_dly1 Bit 23-20	**Data 2 Clock Delay for DSI 1**	These bits trim the clock delay of lane 2 in DSI 1
d2_data_dly1 Bit 19-16	**Data 2 Data Delay for DSI 1**	These bits trim the data delay of lane 2 in DSI 1
d1_clk_dly1 Bit 15-12	**Data 1 Clock Delay for DSI 1**	These bits trim the clock delay of lane 1 in DSI 1
d1_data_dly1 Bit 11-8	**Data 1 Data Delay for DSI 1**	These bits trim the data delay of lane 1 in DSI 1
d0_clk_dly1 Bit 7-4	**Data 0 Clock Delay for DSI 1**	These bits trim the clock delay of lane 0 in DSI 1
d0_data_dly1 Bit 3-0	**Data 0 Data Delay for DSI 1**	These bits trim the data delay of lane 0 in DSI 1

8.2.2.8 MIPIRX Phy Error Status 1 Register

Offset Address

MIPIRX_PES1R **MIPIRX Phy Error Status 1 Register** **0x001C**

BIT	31	30	29	28	27	26	25	24
NAME				**pv0_4**	**pv0_3**	**pv0_2**	**pv0_1**	**pv0_0**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME					**fce0_3**	**fce0_2**	**fce0_1**	**fce0_0**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**eme0_3**	**eme0_2**	**eme0_1**	**eme0_0**	**ese0_3**	**ese0_2**	**ese0_1**	**ese0_0**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**sse0_3**	**sse0_2**	**sse0_1**	**sse0_0**	**se0_3**	**se0_2**	**se0_1**	**se0_0**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-52: MIPIRX Phy Error Status 1 Register Description

Name	Description	Setting
Reserved Bit 31-29	**Reserved**	Not Applicable
pv0_4 Bit 28	**Protocol Violation Error Type 0 –** This bit reflects EOT packet is not detected DSI_RX0 at the end of the HS transmission.	0 = Not error 1 = Error has occurred
pv0_3 Bit 27	**Protocol Violation Error Type 1 –** This bit reflects BTA sequence is not detected by DSI_RX0 after receiving the read packet.	0 = Not error 1 = Error has occurred
pv0_2 Bit 26	**Protocol Violation Error Type 2 –** This bit reflects BTA timer out error.	0 = Not error 1 = Error has occurred
pv0_1 Bit 25	**Protocol Violation Error Type 3 –** This bit reflects video timing mismatched in Non-burst mode has error.	0 = Not error 1 = Error has occurred
pv0_0 Bit 24	**Protocol Violation Error Type 4 –** This bit reflects local MIPI bus transactor has encountered error.	0 = Not error 1 = Error has occurred
Reserved Bit 23-20	**Reserved**	Not Applicable
fce0_3 Bit 19	**False Control Error 3 –** This bit reflects the False Control Error detected by the DSI_RX0 at the lane 3.	0 = Not error 1 = Error has occurred
fce0_2 Bit 18	**False Control Error 2 –** This bit reflects the False Control Error detected by the DSI_RX0 at the lane 2.	0 = Not error 1 = Error has occurred

Name	Description	Setting
fce0_1 Bit 17	**False Control Error 1 –** This bit reflects the False Control Error detected by the DSI_RX0 at the lane 1.	0 = Not error 1 = Error has occurred
fce0_0 Bit 16	**False Control Error 0 –** This bit reflects the False Control Error detected by the DSI_RX0 at the lane 0.	0 = Not error 1 = Error has occurred
eme0_3 Bit 15	**Escape Mode Error 3 –** This bit reflects the Escape Mode Entry Command Error detected by the DSI_RX0 at the lane 3. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
eme0_2 Bit 14	**Escape Mode Error 2 –** This bit reflects the Escape Mode Entry Command Error detected by the DSI_RX0 at the lane 2. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
eme0_1 Bit 13	**Escape Mode Error 1 –** This bit reflects the Escape Mode Entry Command Error detected by the DSI_RX0 at the lane 1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
eme0_0 Bit 12	**Escape Mode Error 0 –** This bit reflects the Escape Mode Entry Command Error detected by the DSI_RX0 at the lane 0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ese0_3 Bit 11	**EOT Sync Error 3 –** This bit reflects the EoT Sync Error detected by the DSI_RX0 at the lane 3. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ese0_2 Bit 10	**EOT Sync Error 2 –** This bit reflects the EoT Sync Error detected by the DSI_RX0 at the lane 2. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ese0_1 Bit 9	**EOT Sync Error 1 –** This bit reflects the EoT Sync Error detected by the DSI_RX0 at the lane 1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ese0_0 Bit 8	**EOT Sync Error 0 –** This bit reflects the EoT Sync Error detected by the DSI_RX0 at the lane 0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
sse0_3 Bit 7	**SOT Sync Error 3 –** This bit reflects the SoT Sync Error detected by the DSI_RX0 at the lane 3. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
sse0_2 Bit 6	**SOT Sync Error 2 –** This bit reflects the SoT Sync Error detected by the DSI_RX0 at the lane 2. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
sse0_1 Bit 5	**SOT Sync Error 1 –** This bit reflects the SoT Sync Error detected by the DSI_RX0 at the lane 1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
sse0_0 Bit 4	**SOT Sync Error 0 –** This bit reflects the SoT Sync Error detected by the DSI_RX0 at the lane 0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
se0_3 Bit 3	**SOT Error 3 –** This bit reflects the SoT Error detected by the DSI_RX0 at the lane 3. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
se0_2 Bit 2	**SOT Error 2 –** This bit reflects the SoT Error detected by the DSI_RX0 at the lane 2. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred

Name	Description	Setting
se0_1 Bit 1	**SOT Error 1 –** This bit reflects the SoT Error detected by the DSI_RX0 at the lane 1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
se0_0 Bit 0	**SOT Error 0 –** This bit reflects the SoT Error detected by the DSI_RX0 at the lane 0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred

8.2.2.9 MIPIRX Phy Error Status 2 Register

Offset Address

MIPIRX_PES2R **MIPIRX Phy Error Status 2 Register** **0x0020**

BIT	31	30	29	28	27	26	25	24
NAME				**pv1_4**	**Pv1_3**	**pv1_2**	**pv1_1**	**pv1_0**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME					**fce1_3**	**fce1_2**	**fce1_1**	**fce1_0**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**eme1_3**	**eme1_2**	**eme1_1**	**eme1_0**	**ese1_3**	**ese1_2**	**ese1_1**	**ese1_0**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**sse1_3**	**sse1_2**	**sse1_1**	**sse1_0**	**se1_3**	**se1_2**	**se1_1**	**se1_0**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-53: MIPIRX Phy Error Status 2 Register Description

Name	Description	Setting
Reserved Bit 31-29	**Reserved**	Not Applicable
pv1_4 Bit 28	**Protocol Violation Error Type 0 –** This bit reflects EOT packet is not detected by DSI_RX1 at the end of the HS transmission.	0 = Not error 1 = Error has occurred
pv1_3 Bit 27	**Protocol Violation Error Type 1 –** This bit reflects BTA sequence is not detected by DSI_RX1 after receiving the read packet.	0 = Not error 1 = Error has occurred
pv1_2 Bit 26	**Protocol Violation Error Type 2 –** This bit reflects BTA timer out error.	0 = Not error 1 = Error has occurred
pv1_1 Bit 25	**Protocol Violation Error Type 3 –** This bit reflects video timing mismatched in Non-burst mode has error.	0 = Not error 1 = Error has occurred
pv1_0 Bit 24	**Protocol Violation Error Type 4 –** This bit reflects local MIPI bus transactor has encountered error.	0 = Not error 1 = Error has occurred
Reserved Bit 23-20	**Reserved**	Not Applicable
fce1_3 Bit 19	**False Control Error 3 –** This bit reflects the False Control Error detected by the DSI_RX1 at the lane 3.	0 = Not error 1 = Error has occurred
fce1_2 Bit 18	**False Control Error 2 –** This bit reflects the False Control Error detected by the DSI_RX1 at the lane 2.	0 = Not error 1 = Error has occurred

Name	Description	Setting
fce1_1 Bit 17	**False Control Error 1 –** This bit reflects the False Control Error detected by the DSI_RX1 at the lane 1.	0 = Not error 1 = Error has occurred
fce1_0 Bit 16	**False Control Error 0 –** This bit reflects the False Control Error detected by the DSI_RX1 at the lane 0.	0 = Not error 1 = Error has occurred
eme1_3 Bit 15	**Escape Mode Error 3 –** This bit reflects the Escape Mode Entry Command Error detected by the DSI_RX1 at the lane 3. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
eme1_2 Bit 14	**Escape Mode Error 2 –** This bit reflects the Escape Mode Entry Command Error detected by the DSI_RX1 at the lane 2. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
eme1_1 Bit 13	**Escape Mode Error 1 –** This bit reflects the Escape Mode Entry Command Error detected by the DSI_RX1 at the lane 1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
eme1_0 Bit 12	**Escape Mode Error 0 –** This bit reflects the Escape Mode Entry Command Error detected by the DSI_RX1 at the lane 0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ese1_3 Bit 11	**EOT Sync Error 3 –** This bit reflects the EoT Sync Error detected by the DSI_RX1 at the lane 3. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ese1_2 Bit 10	**EOT Sync Error 2 –** This bit reflects the EoT Sync Error detected by the DSI_RX1 at the lane 2. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ese1_1 Bit 9	**EOT Sync Error 1 –** This bit reflects the EoT Sync Error detected by the DSI_RX1 at the lane 1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ese1_0 Bit 8	**EOT Sync Error 0 –** This bit reflects the EoT Sync Error detected by the DSI_RX1 at the lane 0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
sse1_3 Bit 7	**SOT Sync Error 3 –** This bit reflects the SoT Sync Error detected by the DSI_RX1 at the lane 3. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
sse1_2 Bit 6	**SOT Sync Error 2 –** This bit reflects the SoT Sync Error detected by the DSI_RX1 at the lane 2. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
sse1_1 Bit 5	**SOT Sync Error 1 –** This bit reflects the SoT Sync Error detected by the DSI_RX1 at the lane 1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
sse1_0 Bit 4	**SOT Sync Error 0 –** This bit reflects the SoT Sync Error detected by the DSI_RX1 at the lane 0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
se1_3 Bit 3	**SOT Error 3 –** This bit reflects the SoT Error detected by the DSI_RX1 at the lane 3. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
se1_2 Bit 2	**SOT Error 2 –** This bit reflects the SoT Error detected by the DSI_RX1 at the lane 2. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred

Name	Description	Setting
se1_1 Bit 1	**SOT Error 1 –** This bit reflects the SoT Error detected by the DSI_RX1 at the lane 1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
se1_0 Bit 0	**SOT Error 0 –** This bit reflects the SoT Error detected by the DSI_RX1 at the lane 0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred

8.2.2.10 MIPIRX DSI Error Status 1 Register

Offset Address

MIPIRX_DES1R **MIPIRX DSI Error Status 1 Register** **0x0024**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**dpv0**	**Itte0**	**itle0**	**vce0**	**dte0**	**crc0**	**ecc2_0**	**ecc1_0**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**ce0**	**fce0**	**hrte0**	**ltse0**	**eme0**	**ese0**	**Sse0**	**se0**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-54: MIPIRX DSI Error Status 1 Register Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
dpv0 Bit 15	**DSI Protocol Violation 0 -** This bit reflects the DSI Protocol Violation error detected by the DSI_RX0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ltte0 Bit 14	**Low Power Transmit Timeout Error 0 -** This bit reflects the Low Power Transmit Timeout Error detected by the DSI_RX0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
vce0 Bit 12	**VC ID Error 0 -** This bit reflects the Invalid DSI VC ID detected by the DSI_RX0. Please see MIPI DSI spec for the details	0 = Not error 1 = Error has occurred
dte0 Bit 11	**Data Type Error 0 -** This bit reflects the DSI Data Type Not Recognized detected by the DSI_RX0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
crc0 Bit 10	**CRC Error 0 -** This bit reflects the Checksum Error detected by the DSI_RX0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ecc2_0 Bit 9	**ECC Error 2 0 -** This bit reflects the ECC Error, multiple bits, detected by the DSI_RX0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ecc1_0 Bit 8	**ECC Error 1 0 -** This bit reflects the ECC Error, single bit, detected by the DSI_RX0.	0 = Not error 1 = Error has occurred

Name	Description	Setting
	Please see MIPI DSI spec for the details.	
ce0 Bit 7	**Contention Error 0 –** This bit reflects the contention is detected by the DSI_RX0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
fce0 Bit 6	**False Control Error 0 –** This bit reflects the False Control Error detected by the DSI_RX0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
hrte0 Bit 5	**High speed Receive/Low Power Transmit Timeout Error 0 –** This bit reflects the High Speed Receive Timeout Error or Low Power Transmit Timeout Error detected by the DSI_RX0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ltse0 Bit 4	**Low power Transmit Sync Error 0** - This bit reflects the Low Power Transmit Sync Error detected by the DSI_RX0. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
eme0 Bit 3	**Escape Mode Error 0 –** This bit reflects the Escape Mode Entry Command Error detected by the DSI_RX0. Refer to **MIPIRX_PES1R** register for more information. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ese0 Bit 2	**EOT Sync Error 0 –** This bit reflects the EoT Sync Error detected by the DSI_RX0. Refer to **MIPIRX_PES1R** register for more information. Please see MIPI DSI spec for the details	0 = Not error 1 = Error has occurred
sse0 Bit 1	**SOT Sync Error 0 –** This bit reflects the SoT Sync Error detected by the DSI_RX0. Refer to **MIPIRX_PES1R** register for more information. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
se0 Bit 0	**SOT Error 0 –** This bit reflects the SoT Error detected by the DSI_RX0. Refer to **MIPIRX_PES1R** register for more information. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred

8.2.2.11 MIPIRX DSI Error Status 2 Register

Offset Address

MIPIRX_DES2R **MIPIRX DSI Error Status 2 Register** **0x0028**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**dpv1**	**Itte1**	**itle1**	**vce1**	**dte1**	**crc1**	**ecc2_1**	**ecc1_1**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	7	6	5	4	3	2	1	0
NAME	**ce1**	**fce1**	**hrte1**	**ltse1**	**eme1**	**ese1**	**sse1**	**se1**
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 8-55: MIPIRX DSI Error Status 2 Register Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
dpv1 Bit 15	**DSI Protocol Violation 1 -** This bit reflects the DSI Protocol Violation error detected by the DSI_RX1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ltte1 Bit 14	**Low Power Transmit Timeout Error 1 -** This bit reflects the Low Power Transmit Timeout Error detected by the DSI_RX1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
vce1 Bit 12	**VC ID Error 1 -** This bit reflects the Invalid DSI VC ID detected by the DSI_RX1. Please see MIPI DSI spec for the details	0 = Not error 1 = Error has occurred
dte1 Bit 11	**Data Type Error 1 -** This bit reflects the DSI Data Type Not Recognized detected by the DSI_RX1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
crc1 Bit 10	**CRC Error 1 -** This bit reflects the Checksum Error detected by the DSI_RX1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ecc2_1 Bit 9	**ECC Error 2 1 -** This bit reflects the ECC Error, multiple bits, detected by the DSI_RX1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ecc1_1 Bit 8	**ECC Error 1 1 -** This bit reflects the ECC Error, single bit, detected by the DSI_RX1.	0 = Not error 1 = Error has occurred

Name	Description	Setting
	Please see MIPI DSI spec for the details.	
ce1 Bit 7	**Contention Error 1 –** This bit reflects the contention is detected by the DSI_RX1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
fce1 Bit 6	**False Control Error 1 –** This bit reflects the False Control Error detected by the DSI_RX1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
hrte1 Bit 5	**High speed Receive/Low Power Transmit Timeout Error 1 –** This bit reflects the High Speed Receive Timeout Error or Low Power Transmit Timeout Error detected by the DSI_RX1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ltse1 Bit 4	**Low power Transmit Sync Error 1** - This bit reflects the Low Power Transmit Sync Error detected by the DSI_RX1. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
eme1 Bit 3	**Escape Mode Error 1 –** This bit reflects the Escape Mode Entry Command Error detected by the DSI_RX1. Refer to **MIPIRX_PES2R** register for more information. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
ese1 Bit 2	**EOT Sync Error 1 –** This bit reflects the EoT Sync Error detected by the DSI_RX1. Refer to **MIPIRX_PES2R** register for more information. Please see MIPI DSI spec for the details	0 = Not error 1 = Error has occurred
sse1 Bit 1	**SOT Sync Error 1 –** This bit reflects the SoT Sync Error detected by the DSI_RX1. Refer to **MIPIRX_PES2R** register for more information. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred
se1 Bit 0	**SOT Error 1 –** This bit reflects the SoT Error detected by the DSI_RX1. Refer to **MIPIRX_PES2R** register for more information. Please see MIPI DSI spec for the details.	0 = Not error 1 = Error has occurred

8.2.2.12 MIPIRX Error Count 1 Register

Offset Address

MIPIRX_EC1R **MIPIRX Error Count 1 Register** **0x002C**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**ec0[15:8]**							
TYPE	RO							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**ec0[7:0]**							
TYPE	RO							
RESET	0x00							

Table 8-56: MIPIRX Error Count 1 Register Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
ec0 Bit 15-0	**Error counter for ECC and CRC errors 0 -** These bits provide the accumulation of ECC and CRC errors collected by DSI_RX0. When Bit[15] is set, it will remains set.	Per Application Condition

8.2.2.13 MIPIRX Error Count 2 Register

Offset Address

MIPIRX_EC2R **MIPIRX Error Count 2 Register** **0x0030**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
BIT	15	14	13	12	11	10	9	8
NAME	**ec1[15:8]**							
TYPE	RO							
RESET	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**ec1[7:0]**							
TYPE	RO							
RESET	0x00							

Table 8-57: MIPIRX Error Count 2 Register Description

Name	Description	Setting
Reserved Bit 31-16	**Reserved**	Not Applicable
ec1 Bit 15-0	**Error counter for ECC and CRC errors 1 -** These bits provide the accumulation of ECC and CRC errors collected by DSI_RX1. When Bit[15] is set, it will remains set.	Per Application Condition

8.2.3 Video BIST Register Descriptions

8.2.3.1 Video BIST Register 0

Offset Address

VBISTR0 **Video BIST Register 0** **0x000**

BIT	31	30	29	28	27	26	25	24
NAME	**VB_REPEAT_CNT[15:8]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	23	22	21	20	19	18	17	16
NAME	**VB_REPEAT_CNT[7:0]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	7	6	5	4	3	2	1	0
NAME	**VB_MODE{3:0}**				**VB_CFG_MODE[1:0]**		**VB_CSPF**	**VB_EN**
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							

Table 8-58: Video BIST Register 0 Description

Name	Description	Setting
VB_REPEAT_CNT[15:0] Bit 31-16	**Video BIST Repeat Count –** These bits set the repeat count for video pattern generation. It will have different meaning for different **VB_MODE.**	Video BIST section for more information.
Reserved Bit15-8	**Reserved**	Not Applicable
VB_MODE[3:0] Bit 7-4	**Video BIST Mode –** These bits select the Video BIST image pattern.	Video BIST section for more information.
VB_CFG_MODE[1:0] Bit 3-2	**Video BIST Config Mode –** These bits select the mode that video bist generate the pattern	**0** – Single data buffer mode (Normal) **1** – Dual data buffer mode (Odd/Even) **2** – Dual data buffer mode (Left/Right) **3** – Dual data buffer mode (Broadcast)
VB_CSPF Bit 1	**Video BIST Color Swap per Frame –** This bit enable the color swap per frame	**0** – Disable **1** – Enable
VB_EN Bit 0	**Video BIST Enable –** This bit enable the Video BIST function	**0** – Disable **1** – Enable

8.2.3.2 Video BIST Register 1

Offset Address

VBISTR1 **Video BIST Register 1** **0x004**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	15	14	13	12	11	10	9	8
NAME							**VB_COLOR_X_R[9:8]**	
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	7	6	5	4	3	2	1	0
NAME	**VB_COLOR_X_R[7:0]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							

Table 8-59: Video BIST Register 1 Description

Name	Description	Setting
Reserved Bit 31-10	**Reserved**	Not Applicable
VB_COLOR_X_R[9:0] Bit 9-0	**Video BIST Color X Red Component** – These bits specify the Color X Red Component.	30bpp – [9:0] 24bpp – [7:0]

8.2.3.3 Video BIST Register 2

Offset Address

VBISTR2 **Video BIST Register 2** **0x008**

BIT	31	30	29	28	27	26	25	24
NAME							**VB_COLOR_X_G[9:8]**	
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	23	22	21	20	19	18	17	16
NAME	**VB_COLOR_X_G[7:0]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	15	14	13	12	11	10	9	8
NAME							**VB_COLOR_X_B[9:8]**	
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	7	6	5	4	3	2	1	0
NAME	**VB_COLOR_X_B[7:0]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							

Table 8-60: Video BIST Register 2 Description

Name	Description	Setting
Reserved Bit 31–26	**Reserved**	Not Applicable
VB_COLOR_X_G[9:0] Bit 25–16	**Video BIST Color X Green Component –** These bits specify the Color X Red Component.	30bpp – [9:0] 24bpp – [7:0]
Reserved Bit 15–10	**Reserved**	Not Applicable
VB_COLOR_X_B[9:0] Bit 9-0	**Video BIST Color X Blue Component –** These bits specify the Color X Red Component.	30bpp – [9:0] 24bpp – [7:0]

8.2.3.4 Video BIST Register 3

Offset Address

VBISTR3 **Video BIST Register 3** **0x00C**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	15	14	13	12	11	10	9	8
NAME							**VB_COLOR_Y_R[9:8]**	
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	7	6	5	4	3	2	1	0
NAME	**VB_COLOR_Y_R[7:0]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							

Table 8-61: Video BIST Register 3 Description

Name	Description	Setting
Reserved Bit 31–10	**Reserved**	Not Applicable
VB_COLOR_Y_R[9:0] Bit 9-0	**Video BIST Color X Red Component** – These bits specify the Color X Red Component.	30bpp – [9:0] 24bpp – [7:0]

8.2.3.5 Video BIST Register 4

Offset Address

VBISTR4 **Video BIST Register 4** **0x010**

BIT	31	30	29	28	27	26	25	24
NAME							**VB_COLOR_Y_G[9:8]**	
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	23	22	21	20	19	18	17	16
NAME	**VB_COLOR_Y_G[7:0]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	15	14	13	12	11	10	9	8
NAME							**VB_COLOR_Y_B[9:8]**	
TYPE	RO	RO	RO	RO	RO	RO	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	7	6	5	4	3	2	1	0
NAME	**VB_COLOR_Y_B[7:0]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							

Table 8-62: Video BIST Register 4 Description

Name	Description	Setting
Reserved Bit 31–26	**Reserved**	Not Applicable
VB_COLOR_Y_G[9:0] Bit 25–16	**Video BIST Color Y Green Component –** These bits specify the Color Y Red Component.	30bpp – [9:0] 24bpp – [7:0]
Reserved Bit 15–10	**Reserved**	Not Applicable
VB_COLOR_Y_B[9:0] Bit 9-0	**Video BIST Color Y Blue Component –** These bits specify the Color Y Red Component.	30bpp – [9:0] 24bpp – [7:0]

8.2.3.6 Video BIST Register 5

VBISTR5	Video BIST Register 5	Offset Address 0x014

BIT	31	30	29	28	27	26	25	24
NAME	**VB_X_START[15:8]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	23	22	21	20	19	18	17	16
NAME	**VB_X_START[7:0]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	15	14	13	12	11	10	9	8
NAME	**VB_X_END[15:8]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	7	6	5	4	3	2	1	0
NAME	**VB_X_END[7:0]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							

Table 8-63: Video BIST Register 5 Description

Name	Description	Setting
VB_X_START[15:0] Bit 31–16	**Video BIST X Start** – These bits define the X starting position.	Per Application Condition
VB_X_END[15:0] Bit 15–0	**Video BIST X End** – These bits define the X end position.	Per Application Condition

8.2.3.7 Video BIST Register 6

Offset Address

VBISTR6 **Video BIST Register 6** **0x018**

BIT	31	30	29	28	27	26	25	24
NAME	**VB_Y_START[15:8]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	23	22	21	20	19	18	17	16
NAME	**VB_Y_START[7:0]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	15	14	13	12	11	10	9	8
NAME	**VB_Y_END[15:8]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	7	6	5	4	3	2	1	0
NAME	**VB_Y_END[7:0]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							

Table 8-64: Video BIST Register 6 Description

Name	Description	Setting
VB_Y_START[15:0] Bit 31–16	**Video BIST Y Start** – These bits define the Y starting position.	Per Application Condition
VB_Y_END[15:0] Bit 15–0	**Video BIST Y End** – These bits define the Y end position.	Per Application Condition

8.2.4 Pixel Peek Registers Descriptions

8.2.4.1 Pixel Peek Register 0

Offset Address

PIXELPEEKR0 **Pixel Peek Register 0** **0x000**

BIT	31	30	29	28	27	26	25	24
NAME	**CURSOR_POSITION_Y[15:8]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	23	22	21	20	19	18	17	16
NAME	**CURSOR_POSITION_Y[7:0]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	15	14	13	12	11	10	9	8
NAME	**CURSOR_POSITION_X[15:8]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	7	6	5	4	3	2	1	0
NAME	**CURSOR_POSITION_X[7:0]**							
TYPE	RW	RW	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							

Table 8-65: Pixel Peek Register 0 Description

Name	Description	Setting
CURSOR_POSITION_Y [15:0] Bit 31–16	**Cursor Position Y –** These bits set the y-coordinate to measure	Per Application Condition
CURSOR_POSITION_X [15:0] Bit 15–0	**Cursor Position X –** These bits set the x-coordinate to measure	Per Application Condition

8.2.4.2 Pixel Peek Register 1

Offset Address

PIXELPEEKR1 **Pixel Peek Register 1** **0x004**

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	15	14	13	12	11	10	9	8
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	7	6	5	4	3	2	1	0
NAME			**PREVENT_UPDATE**	**CURSOR_VISIBLE**	**CURSOR_COLOR_DYNAMIC**	**CURSOR_COLOR_RGB[2:0]**		
TYPE	RO	RO	RW	RW	RW	RW	RW	RW
RESET	0	0	0	0	0	0	0	0
	0x0							

Table 8-66: Pixel Peek Register 1 Description

Name	Description	Setting
Reserved Bit 31–6	**Reserved**	Not Applicable
PREVENT_UPDATE Bit 5	**Prevent Update** – Set this bit before reading the values.	Per Application Condition
CURSOR_VISIBLE Bit 4	**Cursor Visible** – This bit enable cursor display.	0 = disable 1 = enable
CURSOR_COLOR_DYNAMIC Bit 3	**Cursor Color Dynamic** – This bit enable dynamic color for cursor	0 = disable 1 = enable
CURSOR_COLOR_BGR[2:0] Bit 2–0	**Cursor Color BGR** – These bits set the color for cursor (BGR, B on MSB).	Per Application Condition

8.2.4.3 Pixel Peek Register 2

PIXELPEEKR2	Pixel Peek Register 2	Offset Address 0x008

BIT	31	30	29	28	27	26	25	24
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x00							
BIT	23	22	21	20	19	18	17	16
NAME								
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x00							
BIT	15	14	13	12	11	10	9	8
NAME	**MEAS_VALUE_B[15:8]**							
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x00							
BIT	7	6	5	4	3	2	1	0
NAME	**MEAS_VALUE_B[7:0]**							
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x00							

Table 8-67: Pixel Peek Register 2 Description

Name	Description	Setting
Reserved Bit 31–16	**Reserved**	Not Applicable
MEAS_VALUE_B[15:0] Bit 15–0	**Measure Value B** – Measured value for Blue.	Per Application Condition

8.2.4.4 Pixel Peek Register 3

Offset Address

PIXELPEEKR3 **Pixel Peek Register 3** **0x00C**

BIT	31	30	29	28	27	26	25	24
NAME	**MEAS_VALUE_G[15:8]**							
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	23	22	21	20	19	18	17	16
NAME	**MEAS_VALUE_G[7:0]**							
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	15	14	13	12	11	10	9	8
NAME	**MEAS_VALUE_R[15:8]**							
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x0							
BIT	7	6	5	4	3	2	1	0
NAME	**MEAS_VALUE_R[7:0]**							
TYPE	RO	RO	RO	RO	RO	RO	RO	RO
RESET	0	0	0	0	0	0	0	0
	0x0							

Table 8-68: Pixel Peek Register 3 Description

Name	Description	Setting
MEAS_VALUE_G[15:0] Bit 31–16	**Measure Value G** – Measured value for Green.	Per Application Condition
MEAS_VALUE_R[15:0] Bit 15–0	**Measure Value R** – Measured value for Red.	Per Application Condition

9 MAXIMUM RATINGS

Table 9-1: Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Min	Typ	Max	Unit
AVDD	Analog Power Supply	-0.3	-	1.44	V
AVDD_RC	Analog Power Supply	-0.3	-	1.44	V
VCIP	Analog Power for Bandgap, 3.3V	-0.3	-	3.96	V
VDRV	Analog Power for MIPI TX Driver	-0.3	-	1.44	V
VDD_CORE	Digital Core Power Supply	-0.3	-	1.44	V
VDDIO	I/O Power Supply	-0.3	-	3.96	V
T_{STG}	Storage Temperature	-40	-	150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{CI} and V_{OUT} be constrained to the range $V_{SS} < V_{DD} \leq V_{CI} < V_{OUT}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

10 DC OPERATING CONDITIONS

Table 10-1 : Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
AVDD	Analog Power Supply	1.08	1.2	1.32	V
AVDD_RC	Analog Power Supply	1.08	1.2	1.32	V
VDD_CORE	Digital Core Power Supply	1.08	1.2	1.32	V
VDDIO	I/O Power Supply	1.62	1.8	1.98	V
	I/O Power Supply	2.7	3.3	3.6	V
T_A	Operating Temperature	-40	25	85	°C

10.1 DC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$I_{DD\_1.2V\_active}$	Current for all 1.2V supplies for active mode	Active Mode (Video Mode) 2560x1600@60Hz, MIPITX-D@1.25Gbps X 8 lanes	-	200	350	mA
$I_{DD\_1.8V\_active}$	Current for all 1.8V supplies for active mode		-	7	15	mA
$I_{DD\_1.2V\_powerdown}$	Current for all 1.2V supplies for power down mode	Power Down mode MIPIRX off MIPITX off	-	110	250	µA
$I_{DD\_1.8V\_powerdown}$	Current for all 1.8V supplies for power down mode		-	300	600	µA
$V_{OH\ (CMOS)}$	Output High Voltage (CMOS)	I_{OH} = -2 ~ -16 mA	VDDIO*80%	-	-	V
$V_{OL\ (CMOS)}$	Output Low Voltage (CMOS)	I_{OL}= 2 ~ 16 mA	-	-	VDDIO*15%	V
$V_{IH\ (CMOS)}$	Input High Voltage (CMOS)	-	VDDIO*70%	-	-	V
$V_{IL\ (CMOS)}$	Input Low Voltage (CMOS)	-	-	-	VDDIO*20%	V
I_{OZ}	Tri-state Output Leakage Current	-	-1	-	+1	µA
I_{IN}	Input Leakage Current	-	-1	-	+1	µA

11 AC CHARACTERISTICS

11.1 Power Up Timing

Symbol	Parameters	Min	Typ	Max	Units
T_{VDD12_RISE}	Rise time for all 1.2V VDD supplies (10% to 90%)	1	-	10	ms
T_{VDD18_RISE}	Rise time for all 1.8V VDD supplies (10% to 90%)	1	-	10	ms
T_{VDD18_ON}	Time from 1.2V supplies on to 1.8V and 3.3V supplies on. Note: If VDD18 is applied before VDD12 is applied, there could be up to 1mA of additional leakage during the period when VDD12 is still not available.	-5	-	30	ms

11.2 RESET Timing

Symbol	Parameters	Min	Typ	Max	Units
T_{RESET}	RESET_IN “Low” Pulse Width	10	-	-	us

11.3 Interface Timing

11.3.1 SPI Interface Timing

Symbol	Parameters	Min	Typ	Max	Units
T_{MC}	SPI Clock Frequency	-	-	50	Mhz
t_{CYCLE_WR}	Clock Cycle Time(Write)	1	-	-	T_{MC}
t_{CYCLE_RD}	Clock Cycle Time(Read)	4	-	-	T_{MC}
t_{CSS}	Chip Select Setup Time	2	-	-	ns
t_{CSH}	Chip Select Hold Time	4	-	-	ns
t_{DCS}	Chip Select Setup Time(for 4 wire 8 bit mode)	2	-	-	ns
t_{DCH}	Chip Select Hold Time(for 4 wire 8 bit mode)	4	-	-	ns
t_{DSW}	Write Data Setup Time	2	-	-	ns
t_{OHW}	Write Data Hold Time	4	-	-	ns
t_{ACC}	Read Data Access Time	8	-	-	ns
t_{DHR}	Read Data Hold Time	t_{CYCLE_RD} /2	-	-	ns
t_{CSWD}	Chip Select Write Delay Time	1	-	-	T_{BC}
t_{CSRD}	Chip Select Read Delay Time	1	-	-	T_{BC}
t_R	Rise time	1	-	-	ns
t_F	Fall time	1	-	-	ns

Figure 11-1 SPI Interface Timing Characteristics

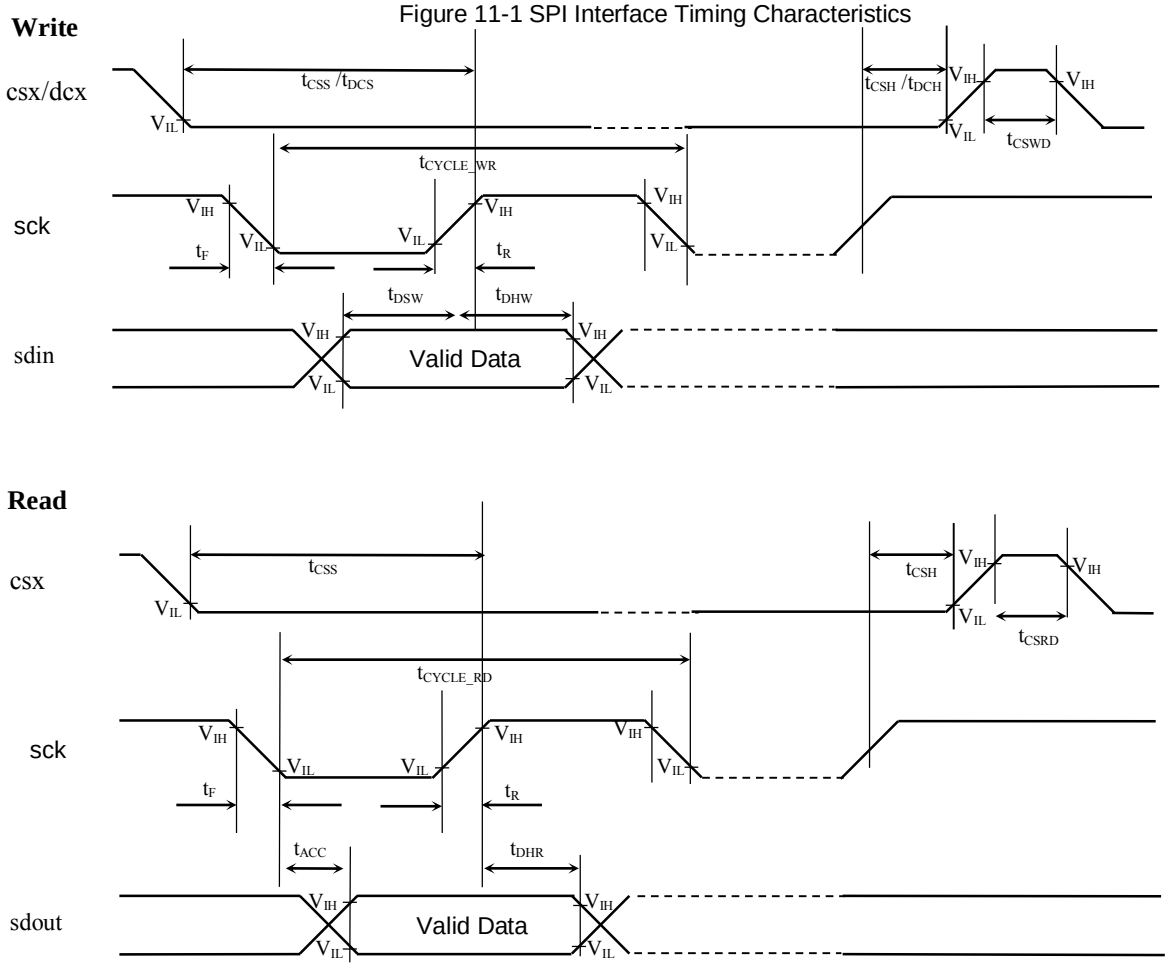
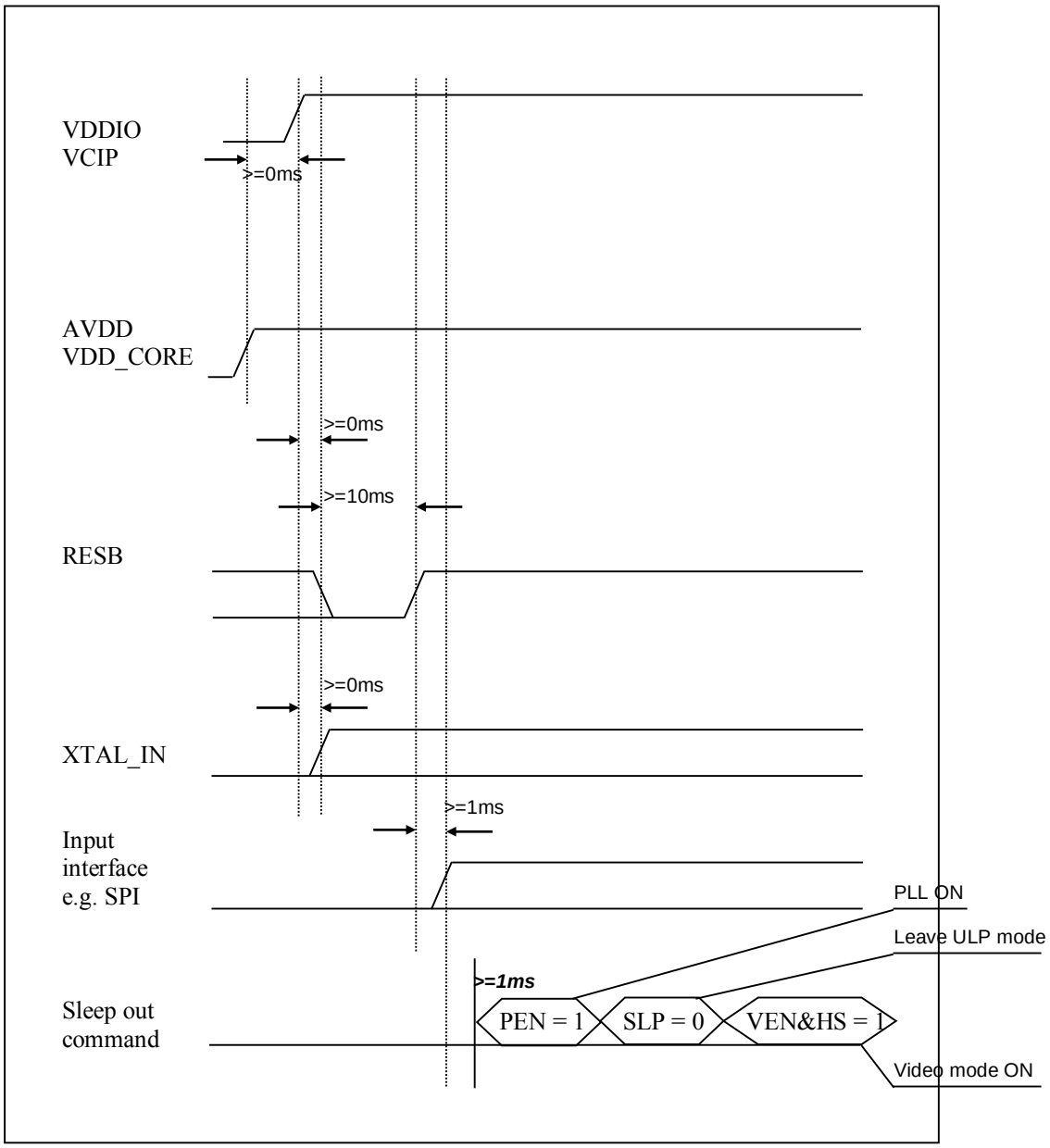


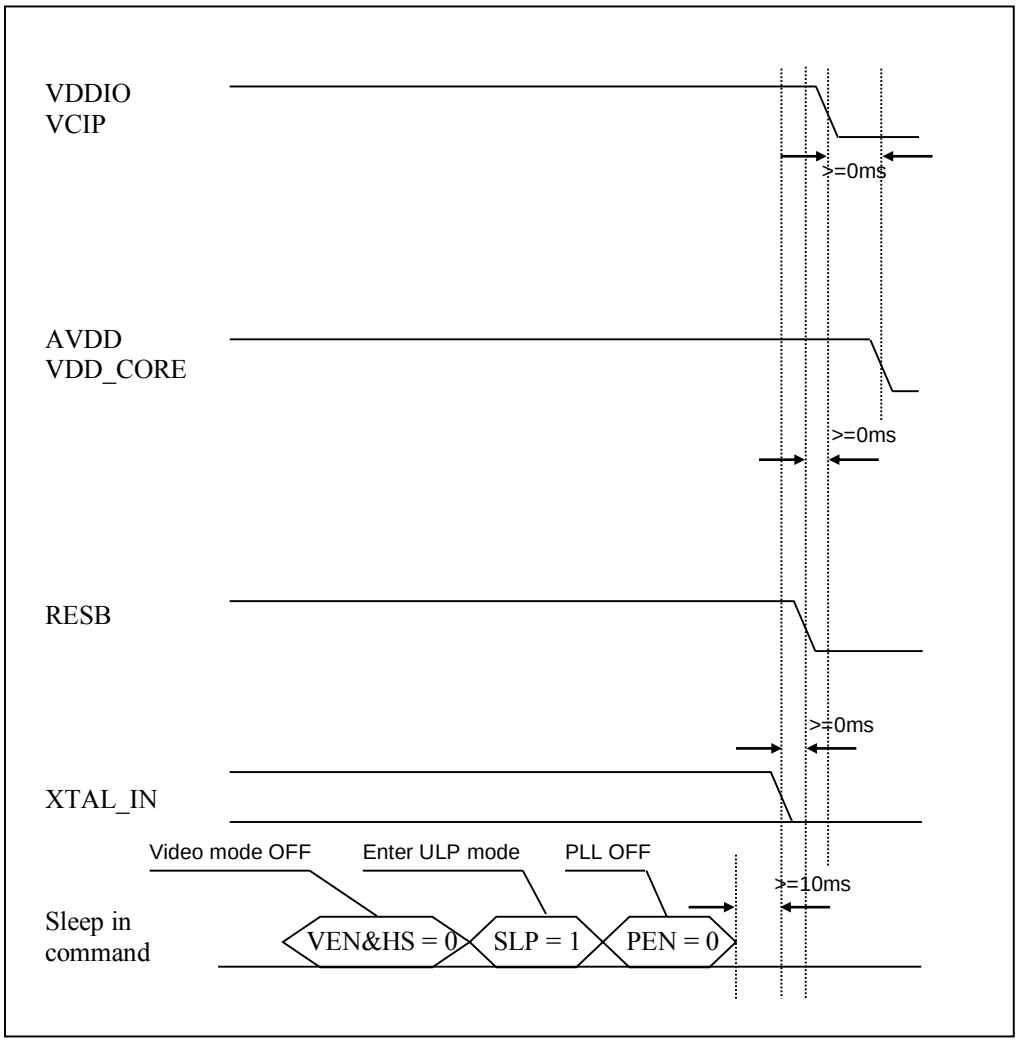
Figure 11-2: SPI Interface Timing Diagram

Note: V_{IL} and V_{IH} refers to DC CHARACTERISTICS

12 POWER UP SEQUENCE



13 POWER OFF SEQUENCE



14 MIPI DPHY CHARACTERISTICS

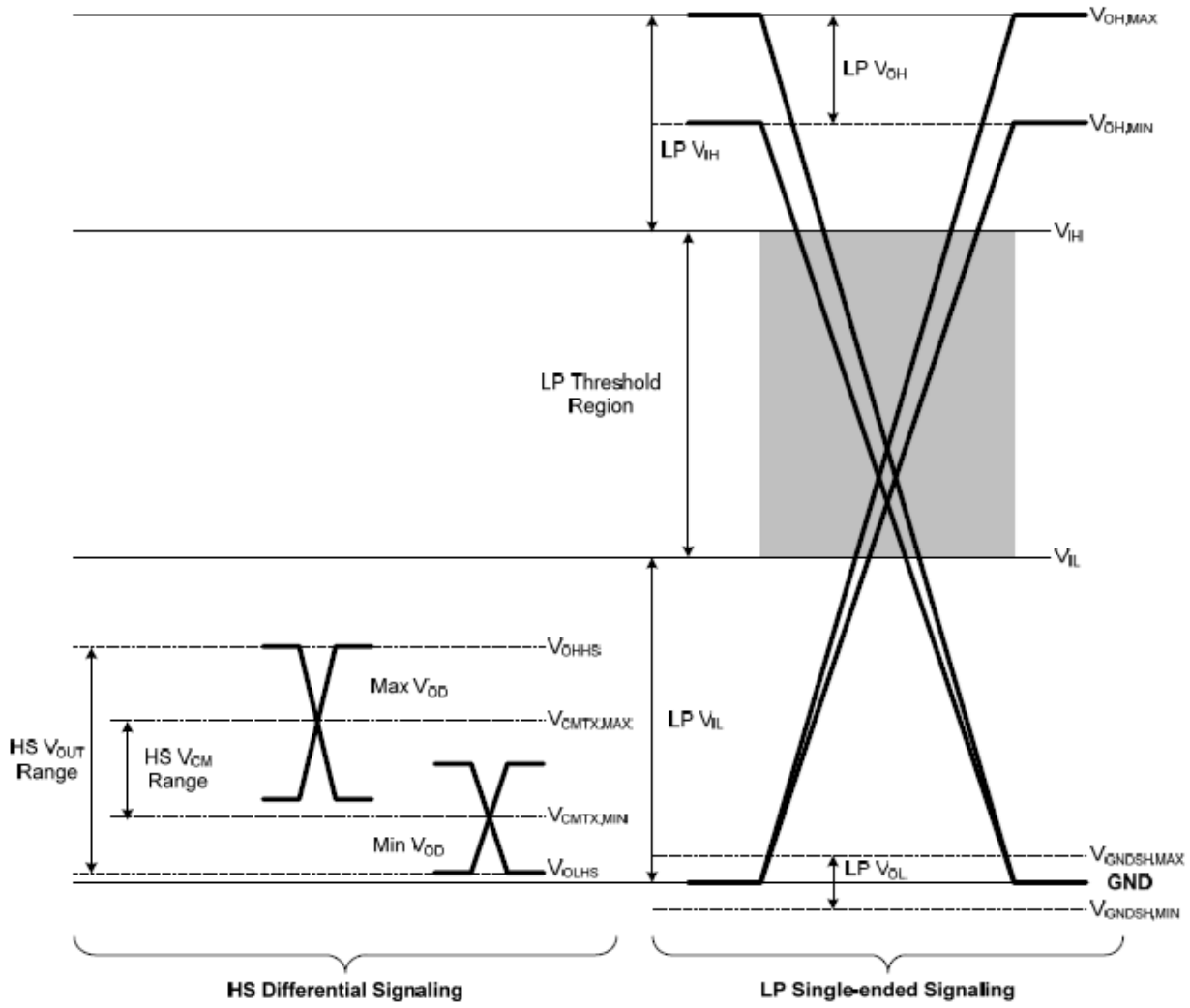


Figure 14-1 DPHY Signaling Levels

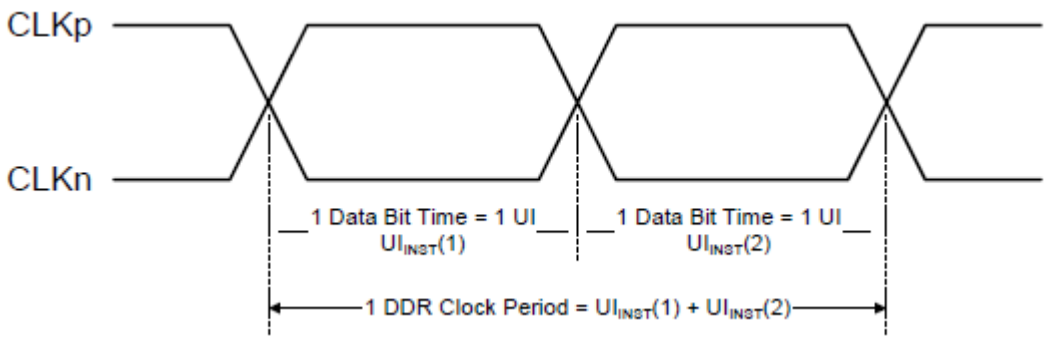


Figure 14-2 DDR Clock Definition

Table 14-1 : Clock Signal Specification

Clock Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}			12.5	ns	1,2
UI variation	ΔUI	-10%		10%	UI	3
		-5%		5%	UI	4

Notes:

1. *This value corresponds to a minimum 80 Mbps data rate.*
2. *The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst. The allowed instantaneous UI variation can cause instantaneous data rate variations. Therefore, devices should either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.*
3. *When UI ≥ 1ns, within a single burst.*
4. *When UI < 1ns, within a single burst.*

14.1 MIPI DPHY RX CHARACTERISTICS

Table 14-2 : HS Receiver DC Specifications

Parameter	Description	Min	Nom	Max	Units	Note
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70		330	mV	1,2
V_{IDTH}	Differential input high threshold			70	mV	
V_{IDTL}	Differential input low threshold	-70			mV	
V_{IHHS}	Single-ended input high voltage			460	mV	1
V_{ILHS}	Single-ended input low voltage	-40			mV	1
$V_{TERM-EN}$	Single-ended threshold for HS termination enable			450	mV	
Z_{ID}	Differential input impedance	80	100	125	Ω	

Notes:

1. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
2. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 14-3 : HS Receiver AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450 MHz			100	mV	2
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz – 450MHz	-50		50	mV	1, 4
C_{CM}	Common-mode termination			60	pF	3

Notes:

1. Excluding 'static' ground shift of 50mV
2. $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.
3. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.
4. Voltage difference compared to the DC average common-mode potential.

Table 14-4 : LP Receiver DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{IH}	Logic 1 input voltage	880			mV	
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV	
V_{HYST}	Input hysteresis	25			mV	

Table 14-5 : LP Receiver AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
e_{SPIKE}	Input pulse rejection			300	V·ps	1, 2, 3
T_{MIN-RX}	Minimum pulse width response	20			ns	4
V_{INT}	Peak interference amplitude			200	mV	
f_{INT}	Interference frequency	450			MHz	

Notes:

1. Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
4. An input pulse greater than this shall toggle the output.

14.2 MIPI DPHY TX CHARACTERISTICS

Table 14-6 HS Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{CMTX}	HS transmit static common-mode voltage	150	200	250	mV	1
$\|\Delta V_{CMTX(1,0)}\|$	V_{CMTX} mismatch when output is Differential-1 or Differential-0			5	mV	2
$\|V_{OD}\|$	HS transmit differential voltage	140	200	270	mV	1
$\|\Delta V_{OD}\|$	V_{OD} mismatch when output is Differential-1 or Differential-0			14	mV	2
V_{OHHS}	HS output high voltage			360	mV	1
Z_{OS}	Single ended output impedance	40	50	62.5	Ω	
ΔZ_{OS}	Single ended output impedance mismatch			10	%	

Notes:

1. *Value when driving into load impedance anywhere in the Z_{ID} range.*
2. *A transmitter should minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ in order to minimize radiation, and optimize signal integrity.*

Table 14-7 HS Transmitter AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMTX(HF)}$	Common-level variations above 450MHz			15	mV_{RMS}	
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450MHz			25	mV_{PEAK}	
t_R and t_F	20%-80% rise time and fall time			0.3	UI	1, 2
				0.35	UI	1, 3
		100			ps	4

Notes:

1. *UI is equal to 1/(2*fh). See Section 8.3 for the definition of fh.*
2. *Applicable when operating at HS bit rates ≤ 1 Gbps (UI ≥ 1 ns).*
3. *Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).*
4. *Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps.*

Table 14-8 LP Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	
V_{OL}	Thevenin output low level	-50		50	mV	
Z_{OLP}	Output impedance of LP transmitter	110			Ω	1, 2

Notes:

1. *See Figure 42 and Figure 43.*
2. *Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the T_{RLP}/T_{FLP} specification is met.*

Table 14-9 LP Transmitter AC Specifications

Parameter	Description		Min	Nom	Max	Units	Notes
T_{RLP}/T_{FLP}	15%-85% rise time and fall time				25	ns	1
T_{REOT}	30%-85% rise time and fall time				35	ns	1, 5, 6
$T_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40			ns	4
		All other pulses	20			ns	4
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock		90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ C_{LOAD} = 0pF				500	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 5pF				300	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 20pF				250	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 70pF				150	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 0 to 70pF (Falling Edge Only)		30			mV/ns	1, 2, 3
	Slew rate @ C_{LOAD} = 0 to 70pF (Rising Edge Only)		30			mV/ns	1, 3, 9
	Slew rate @ C_{LOAD} = 0 to 70pF (Rising Edge Only)		30 – 0.075 * ($V_{O,INST}$ – 700)			mV/ns	1, 3, 10, 11
C_{LOAD}	Load capacitance		0		70	pF	1

Notes:

1. *C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.*
2. *When the output voltage is between 400 mV and 930 mV.*
3. *Measured as average across any 50 mV segment of the output signal transition.*
4. *This parameter value can be lower than T_{LPX} due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior as described in Section 9.2.2.*
5. *The rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.*
6. *With an additional load capacitance C_{CM} between 0 and 60 pF on the termination center tap at RX side of the Lane*

15 OPERATING MODE

15.1 Programming Model

The table below shows the local register map summary in SSD2831.

Table 15-1: SSD2831 Local Register Map

<table>
<tr><th>Command</th><th>Description</th></tr>
<tr><td>0xB0 – 0xDF</td><td>Same register definition as in SSD2828. Some of the commands would have additional data parameters added to support extension of certain register fields. For example VBP (Vertical back porch) is an 8-bit field. With the extension of the number of data parameters, VBP can now become a 16-bit field. The original register fields' location would be maintained in the first 2 data parameters for back-ward compatibility purpose. Only 2 data parameters would be added.</td></tr>
<tr><td>0xE0</td><td>This is the command for APB peripheral access (e.g. MIPIRX, PMU, GPIO)

If all 6 data parameters are given, SSD2831 would issue APB write access with the APB_ADDR and APB_DATA.

If only 2 data parameters are given, SSD2831 would store the APB_ADDR for read operation. Host can do a data read to read back the APB_DATA. If DSI (RX) interface is used for the read, Generic Read of 0 parameter should be used.

<table>
<tr><th>Data Parameter</th><th>Description</th></tr>
<tr><td>1</td><td>APB_ADDR[7:0]</td></tr>
<tr><td>2</td><td>APB_ADDR[15:8]</td></tr>
<tr><td>3</td><td>APB_DATA[7:0]</td></tr>
<tr><td>4</td><td>APB_DATA[15:8]</td></tr>
<tr><td>5</td><td>APB_DATA[23:16]</td></tr>
<tr><td>6</td><td>APB_DATA[31:24]</td></tr>
</table>
</td></tr>
<tr><td>0xE1 – 0xFE</td><td>Reserved register ranges for new features in SSD2831</td></tr>
<tr><td>0xFF</td><td>This is a special command which has 2 different usages depending on the interface through which the command is received.

<u>SPI Interface</u>
This is the command to read back data returned by the external MIPI slave.
The application processor can treat this register as an FIFO and continuously read data from it.</td></tr>
</table>

The read of this register is only valid when the **RDR** bit is 1. In other words, only when the data returned by the MIPI slave is received, the application processor can read this register to get return data.

MIPI DSI RX Interface

This is the command indicate to internal arbiter that the subsequent streams of MIPI command packets are addressed to internal register. The usage is as follows:

Data Parameter	Description
1	0x0: means subsequent command packets are meant for SSD2831 internal registers 0x1: means subsequent commands are meant for retransmission via MIPITX 0xFF: means this particular command will be reconstructed as a generic (long/short) packet for retransmission via MIPITX with parameter0=0xFF
2 and beyond	If Parameter 0 and Parameter 1 are both 0xFF, then parameter N will become the (N-1)th parameter of the packets reconstructed for retransmission via MIPITX. E.g. If incoming generic packet has the following parameters (in ascending order): 0xFF, 0xFF, 0xA1, 0xA2, then the outgoing generic packet at MIPITX would be 0xFF, 0xA1, 0xA2

15.2 MIPI DSI RX Interface

15.2.1 Local Register or External Access in MIPI DSI RX

There is a need to distinguish between local registers and external MIPI access via DSI-TX output. This is done by a special MIPI Generic command sent by the host. The host writes Generic Short Write with 2 parameters packet with the 0xFF as the first parameter to switch between local registers access or external access via DSI-TX output. The second parameter determine whether SSD2831 should go to local mode (internal registers access) or external mode(DSI-TX access).

0xFF, 0x00 => Internal Mode
0xFF, 0x01 => External Mode
0xFF, other data => Not allowed

The default power-up state of SSD2831 is set to local mode. To set to external mode, host sends the following packets.

Bytes Sequence	Definition
0x23	Generic Short Write with 2 Parameters Packet ID
0xFF	Switch Mode Command
0x01	0x01 : External Mode
0xXX	ECC

Once the mode is set to external mode, all DSI commands will be re-transmitted.

To switch back to internal mode, host sends the Generic Short Write with 2 Parameters Packets.

Bytes Sequence	Definition
0x23	Generic Short Write with 2 Parameters Packet
0xFF	Switch Mode Command
0x00	0x00 : Internal Mode
0xXX	ECC

15.2.2 Sending Generic Packet with 0xFF as payload to External MIPI Devices

In the event that the host want to send external command with 0xFF as part of the payload, the host needs to send Generic Long Write.

The example below shows how Generic Long Write Packet is sent with payload as 0xFF, 0x01, 0x02.

Bytes Sequence	Definition
0x39	Generic Long Write Packet ID
0x03	Word Length Low
0x00	Word Length High
0xXX	ECC
0xFF	0xFF
0x01	Parameter 1
0x02	Parameter 2
0xXX	CRC Low Byte
0xXX	CRC High Byte

15.2.3 Access Local Registers in MIPI DSI-Rx for Write

For write access, the DSI-RX shall be in internal mode.

The packet to be sent should be a Generic long packet, with the first byte in the payload as the address of the local register. The sub-sequence bytes defined the data byte of the local registers. The data bytes to be written should be sent in unit of 2 bytes.

The order of the MIPI Generic Long packet is as follow,

{0x39, word length low, word Length high, ECC, Address, data 0, data 1, CRC, CRC} – For 16-bit registers

Or

{0x39, word length low, word length high, ECC, Address, data 0, data 1, data 2, data 3, CRC, CRC} – For 32-bit registers

If only 2 bytes are written (data 0 and data 1) for a 32-bit registers, data 2 and data 3 will preserve the previous value.

For example, if host want to write to 0xB1 register with the data 32'h0123_4567, host should send a Generic Long Write packet as shown below.

Bytes Sequence	Definition
0x39	Generic Long Write Packet
0x05	Word Length Low byte
0x00	Word Length High byte
0xXX	ECC
0xB1	Address of SSD2831
0x67	Data Byte 0
0x45	Data Byte 1
0x23	Data Byte 2
0x01	Data Byte 3
0xXX	CRC Low byte
0xXX	CRC High byte

15.2.4 Access Local Registers in MIPI DSI-Rx for Read

For read access, the packet should be Generic read packets, with the address of the local register in the short packet.

The order of the MIPI Generic short packet read is as follow,

{0x14, Address, 0x00, ECC} – Generic Short Read with 1 parameter Or

{0x24, Address, 0x00, ECC} – Generic Short Read with 2 parameters

When Generic Short Read with 2 parameters is used, the DSI-RX ignored the second parameter. The number of byte returned to host depends on the maximum return size register located inside DSI-RX. The default value is 2.

For example, if host want to read to 0xB1 register with the 32-bit data, host will send Maximum Return Size Packet of 4 bytes, follows by Generic Read packets as shown below.

Bytes Sequence	Definition
0x37	Maximum Return Size Packet
0x04	Length of bytes to return(4 bytes)
0x00	Don't Care
0xXX	ECC
0x14	Generic Short Read Packet with 1 parameter
0xB1	Address of SSD2831
0x00	Don't Care
0xXX	ECC

The response of DSI-RX will be Generic long response packet with 4 returned bytes in the payload.

Bytes Sequence	Definition
0x1A	Generic Long Read Response Packet
0x04	Length of bytes to return
0x00	Don't Care
0xXX	ECC
0x67	Data Byte 0
0x45	Data Byte 1
0x23	Data Byte 2
0x01	Data Byte 3
0xXX	CRC Low byte
0xXX	CRC High byte

15.2.5 Access Local (APB) Registers in MIPI DSI-Rx for Write

For write to the Extended Register (0xE0), host will send the following packet.

1. {0x39, word length low, word length high, ECC, 0xE0, address low, address high, data0, data1, data2, data3, CRC, CRC} – To program the content of the Extended register

For example, if host want to write to 0x4014 register with the 32-bit data(32'h0102_0304), host will send Generic Long Write packet as shown below.

Bytes Sequence	Definition
0x39	Generic Long Write Packet
0x07	Word Length Low byte
0x00	Word Length High byte
0xXX	ECC
0xE0	Entry to Extended Registers of SSD2831
0x14	Extended Register Low byte
0x40	Extended Register High byte
0x04	Data Byte 0
0x03	Data Byte 1
0x02	Data Byte 2
0x01	Data Byte 3
0xXX	CRC Low byte
0xXX	CRC High byte

15.2.6 Access Local (APB) Registers in MIPI DSI-Rx for Read

For read from the extended register (0xE0), host will send the following 2 packets.

1. {0x39, word length low, word length high, ECC, 0xE0, address low, address high, CRC, CRC} – To set the address of the Extended register

2. {0x04, Address, 0x00, ECC} – Generic Read with 0 parameter

The number of bytes returned depends the max return size register (MRS) stored in the DSI-RX register. The register is updated when host send the max return size packet to SSD2831.

For example, if host want to read to 0x4014 register with the 32-bit data, host will send Maximum Return Size Packet of 4 bytes, follows by Generic Read packets as shown below.

Bytes Sequence	Definition
0x37	**Maximum Return Size Packet**
0x04	Length of bytes to return
0x00	Don't Care
0xXX	ECC
0x39	Generic Long Write Packet
0x03	Word Length Low byte

Bytes Sequence	Definition
0x00	Word Length High byte
0xXX	ECC
0xE0	Entry to Extended Registers of SSD2831
0x14	Extended Register Low byte
0x40	Extended Register High byte
0xXX	CRC Low byte
0xXX	CRC High byte
0x04	Generic Short Read Packet with no parameter
0xXX	Don't Care
0xXX	Don't Care
0xXX	ECC

The response of DSI-RX will be Generic long response packet with 4 returned bytes in the payload.

Bytes Sequence	Definition
0x1A	Generic Long Read Response Packet
0x04	Length of bytes to return
0x00	Don't Care
0xXX	ECC
0x67	Data Byte 0
0x45	Data Byte 1
0x23	Data Byte 2
0x01	Data Byte 3
0xXX	CRC Low byte
0xXX	CRC High byte

15.2.7 Back-to-back HS Transmission Limitation

When using MIPI DSI RX to send HS transmission back-to-back, there is a limitation of the length of the packet to be transmitted. The minimum length of the preceding HS packet (the data payload) needs to be at least 16 bytes. If the length is less than 16bytes (e.g. short packet, or long packet with word count less than 16 bytes), the user needs to insert a NULL packet of at least 16 bytes of word count before sending the next HS packet.

15.3 SPI Interface

SSD2831 supports three types of SPI interface,

8-Bit 3 wire (type C option 1, DBI 2.0)
8-Bit 4 wire (type C option 3, DBI 2.0)
24-bit 3 wire

The selection is controlled by PS[1:0] pins. The least significant byte should be written first

15.3.1 SPI Interface 8-Bit 4 Wire

This interface consists of sdc, sck, sdin, sdout and csx. It only supports 8-Bit data. Each cycle contains 8-Bit data. The first cycle should be a command write cycle to specify the register address for access. The subsequent cycles are read or write cycles for read or write operations.

The csx should be driven from 1 to 0 to start an operation and from 0 to 1 to end an operation. During 1 operation, the application processor can write or read multiple bytes.

sdcx indicates whether the operation is for data or command. When sdcx is 1, the operation is for data. When sdcx is 0, the operation is for command. sdcx is sampled at every 8th rising edge of sck during 1 operation.

During write operation, sdin will be sampled by SSD2831 at the rising edge of sck. The first rising edge of sck after the falling edge of csx samples the bit 7 of the 8-Bit data. The second rising edge of sck samples the bit 6 of the 8-Bit data, and so on. The value of sdcx is sampled at the 8th rising edge of sck, together with bit 0 of the 8-Bit data. Please see the diagram below for illustration. Optionally, the csx can be driven to 1 in between cycles.

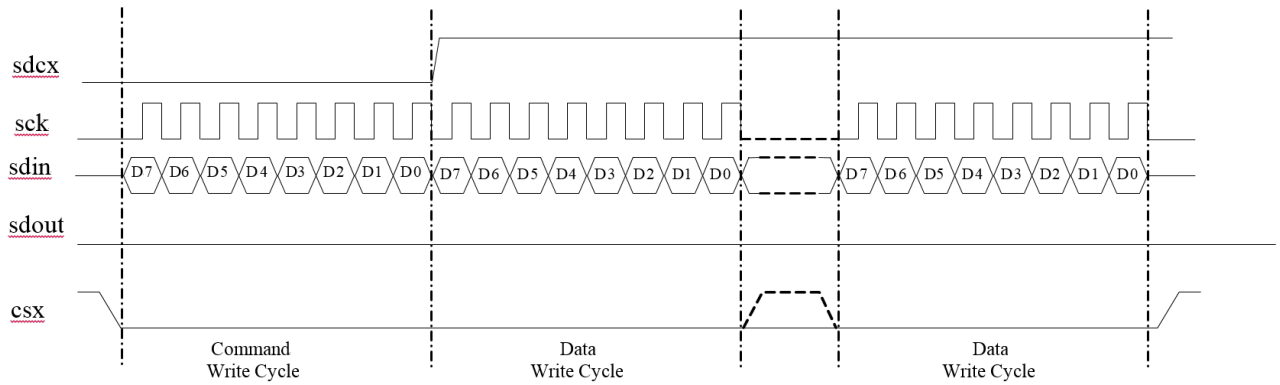


Figure 15-1: SPI Interface 8-bit 4 wire for write

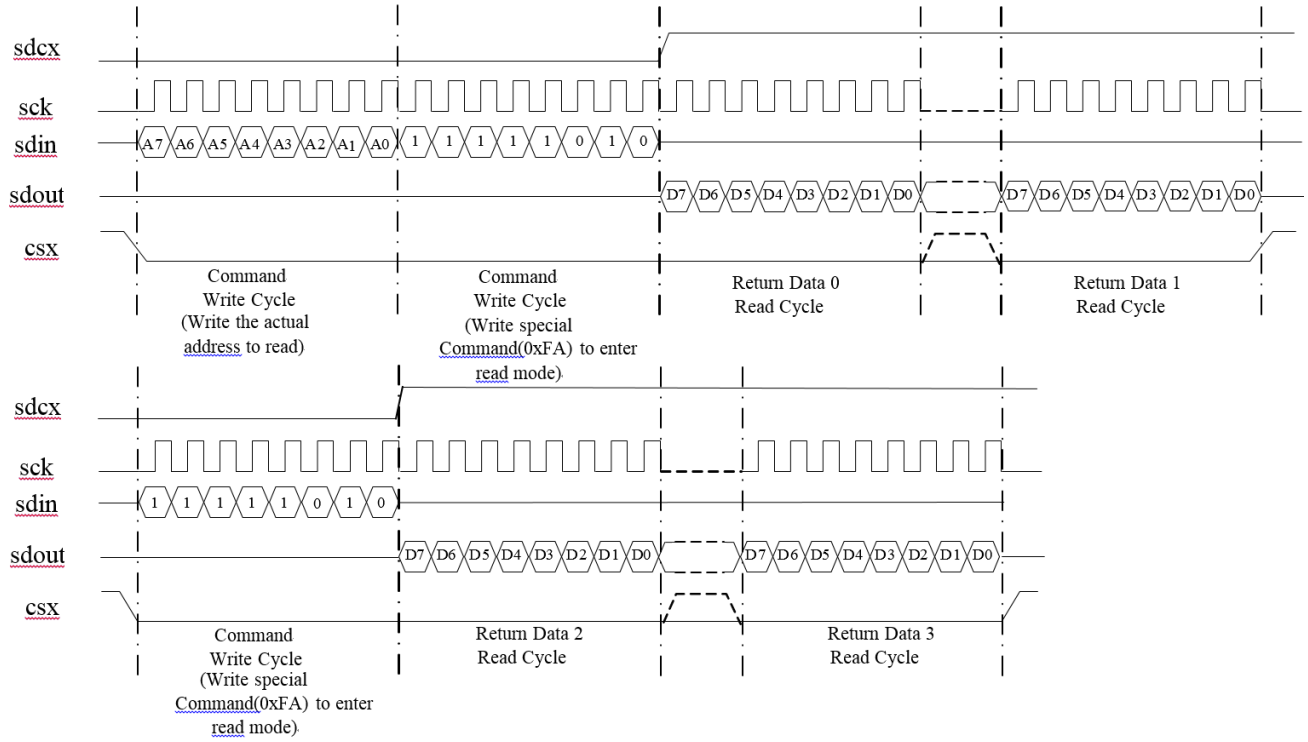


Figure 15-2: SPI Interface 8-bit 4 wire for read

SPI Interface 8-Bit 3 Wire

This interface consists of sck, sdin, sdout and csx. It only supports 8-Bit data. Each cycle contains 8-Bit data. The first cycle should be a write cycle to specify the register address for access. The subsequent cycles are read or write cycles for read or write operations.

The csx should be driven from 1 to 0 to start an operation and from 0 to 1 to end an operation. During 1 operation, the application processor can write or read multiple bytes.

Instead of sdcx, an sdcx bit is used to indicate whether the operation is for data or command. Each byte is associated with an sdcx bit. When sdcx is 1, the operation is for display data. When sdcx is 0, the operation is for command. The sdcx bit is sent priori to each byte. In other words, the sdcx bit is the first bit of every 9 bits during 1 operation.

During write operation, sdin will be sampled by SSD2831 at the rising edge of sck. The first rising edge of sck after the falling edge of csx samples the sdcx bit. The second rising edge samples bit 7 of the 8-Bit data. The third rising edge of sck samples the bit 6 of the 8-Bit data, and so on. Please see the diagram below for illustration. Optionally, the csx can be driven to 1 in between cycles.

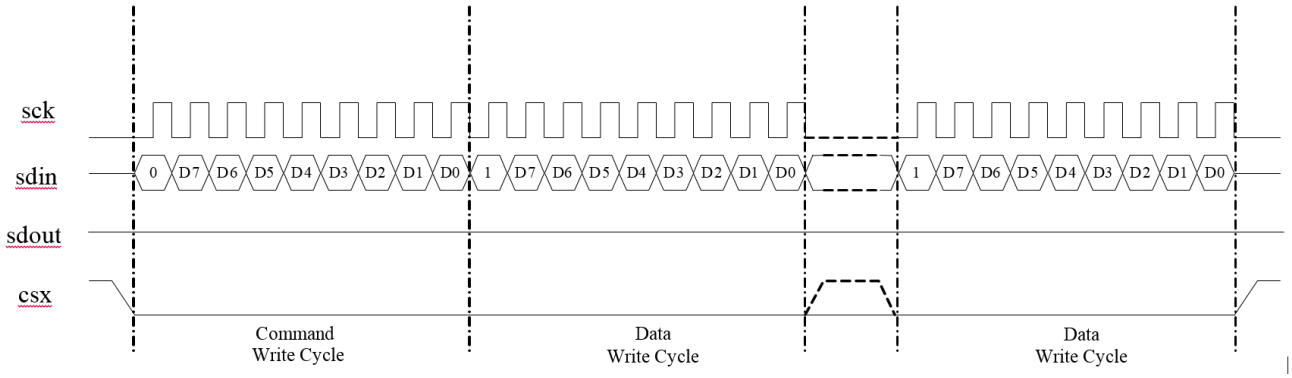


Figure 15-3: SPI Interface 8-bit 3 wire for write

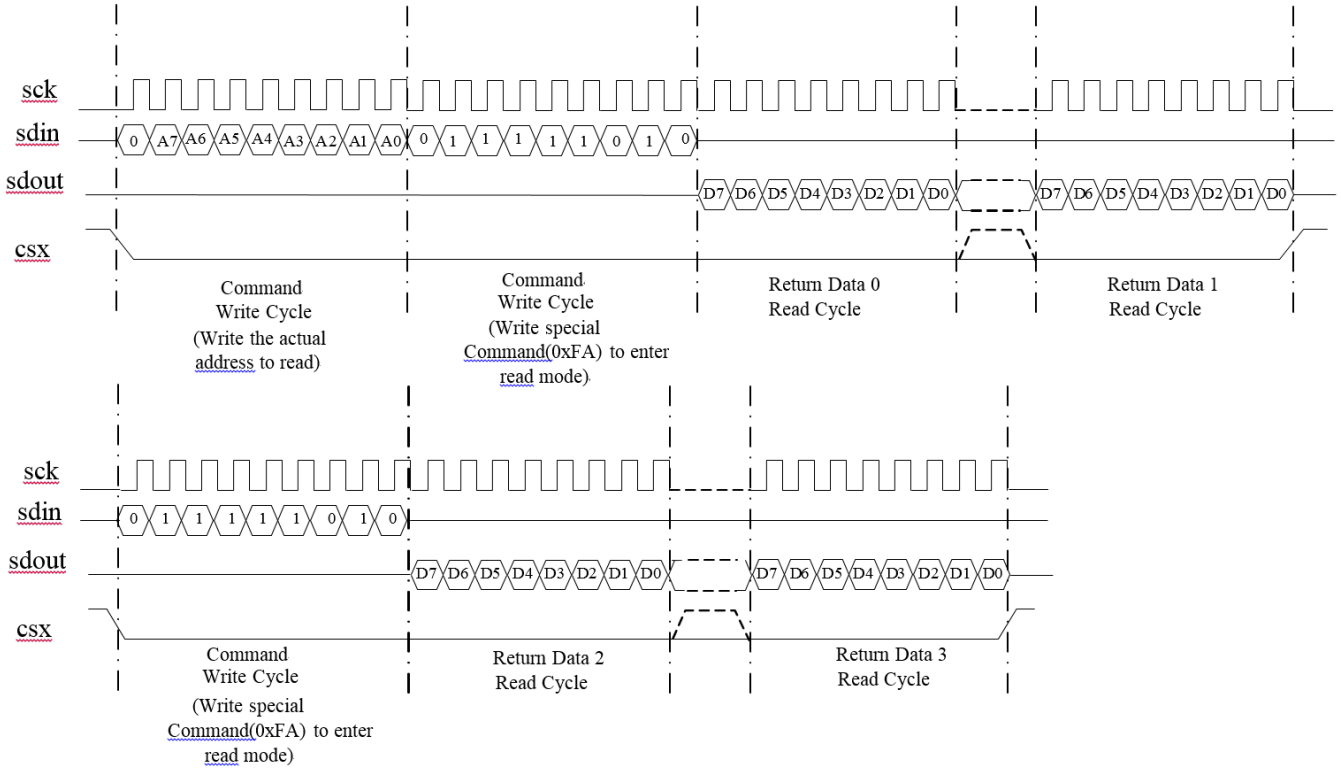


Figure 15-4: SPI Interface 8-bit 3 wire for read

15.3.2 SPI Interface 24-Bit 3 Wire

This interface consists of sck, sdin, sdout and csx. It only supports 16-bit data. Each cycle contains 16-bit data. The first cycle should be a write cycle to specify the register address for access. The subsequent cycles are read or write cycles for read or write operations.

The csx should be driven from 1 to 0 to start cycle and from 0 to 1 to end a cycle. During 1 operation, the application processor can have multiple write or read cycles. However, the csx must go from 0 to 1 at the end of each cycle.

Each cycle contains 24-bit data. Among the 24-bit data, the first 8-Bit are for control purpose and the next 16-bit are the actual data. The first 6 bits are the ID bit for SSD2831, which must be 011100. If this field does not match, the cycle will not be taken in. The 7th bit is the sdcx bit which is the same as the 8-Bit 3 wire interface. The 8th bit is the RW bit which indicates whether the current cycle is a read or write cycle. When RW is 1, the cycle is a read cycle. When RW is 0, the cycle is a write cycle.

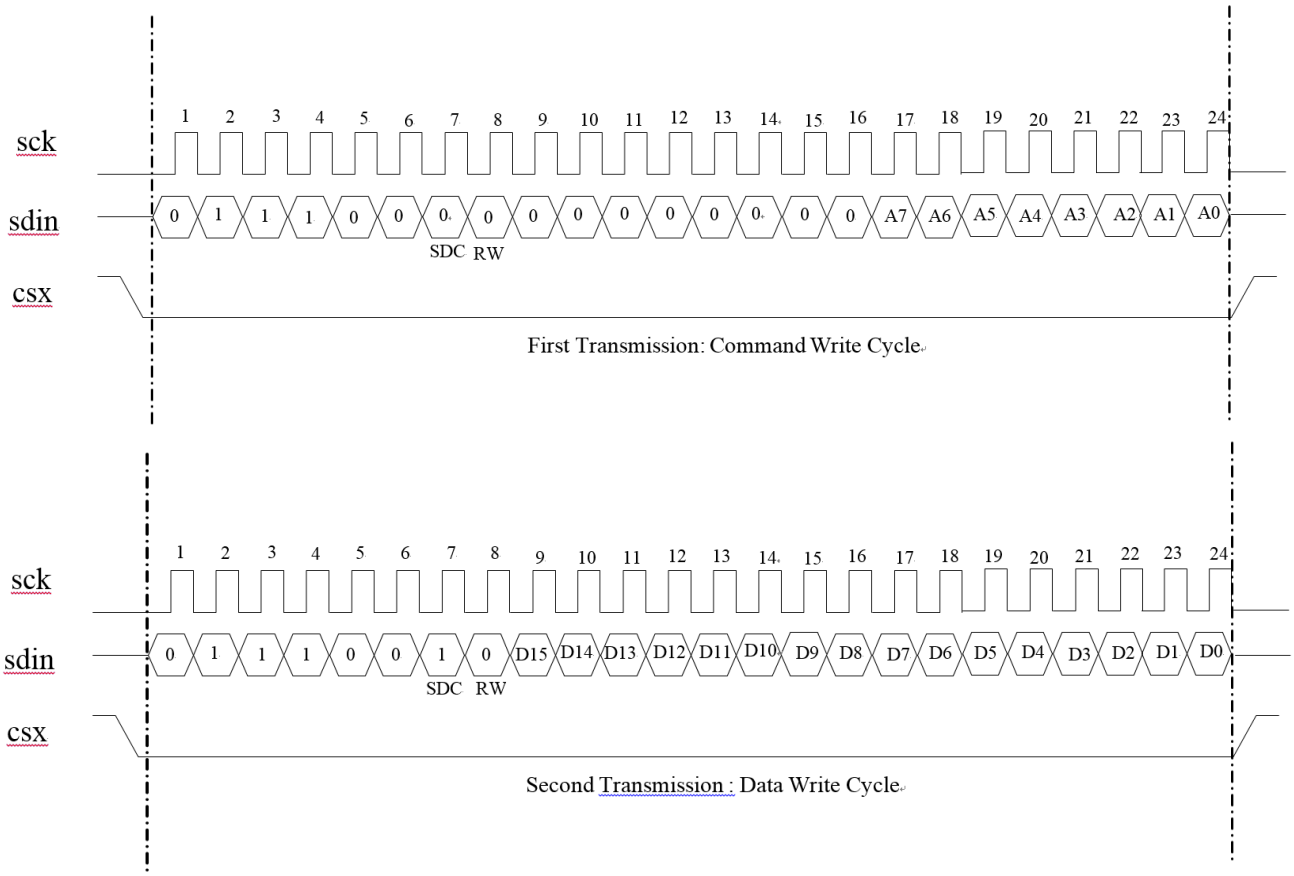


Figure 15-5: SPI Interface 24it 3wire for write

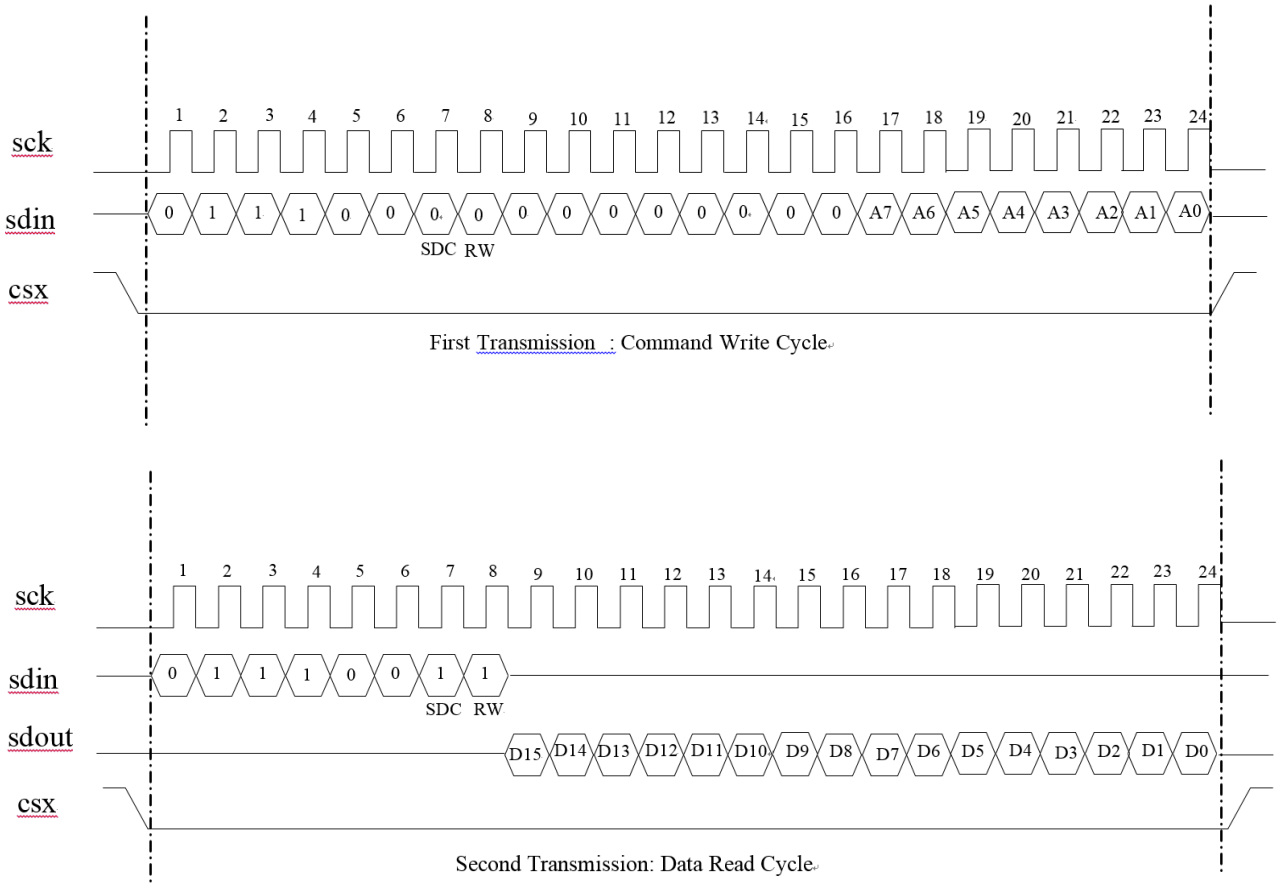


Figure 15-6: SPI Interface 24it 3wire for read

15.3.3 MIPI DSI RX

For this mode, the user must set if_sel[1:0] to "10" to select the interface as a combination of MIPI DSI RX and SPI interface. The video data come from the MIPI DSI RX and the configuration is done through SPI interface. (Note: configuration can be done through the MIPI DSI RX interface itself also)

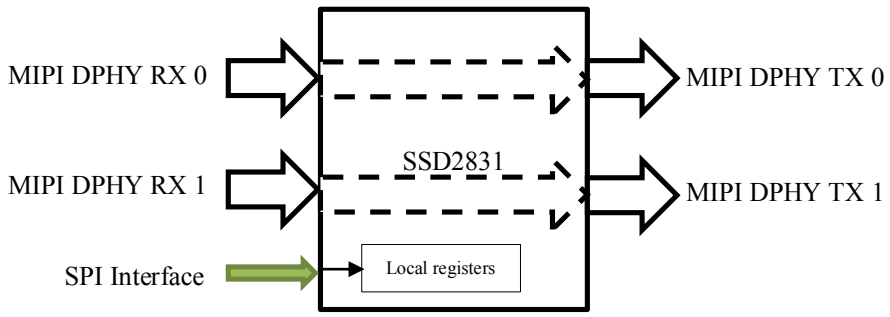
The table below shows the minimum requirements for MIPI DSI inputs, with respect to the video timing parameter for MIPI DSI output. The units are in pixels for horizontal parameters, and in lines for vertical parameters.

	MIPI DSI Input Video Timing Parameter (per input DSI)	Output Video Timing Parameter (per output DSI) - Programmed at 0xB1 to 0xB6 commands
Horizontal Back Porch (HBP)	Single DSI input AND Dual DSI output: Minimum of 64, and Multiple of 2 Other cases: Minimum of 32, and Multiple of 2	Single DSI output: Equal to input HBP Dual DSI output: Half of input HBP
Horizontal Sync Width (HSW)	Single DSI input AND Dual DSI output: Minimum of 64, and Multiple of 2 Other cases: Minimum of 32, and Multiple of 2	Single DSI output: Equal to input HSW Dual DSI output: Half of input HSW
Horizontal Actual (HACT)	Multiple of 4 for the following cases: - Single DSI input AND Dual DSI output - 18bpp or 30bpp pixel format Otherwise, multiple of 2	Single DSI output: Equal to input HACT Maximum of 2640 Dual DSI output: Half of input HACT Maximum of 2064 (per DSI)

Horizontal Front Porch (HFP)	Single DSI input AND Dual DSI output: Minimum of 128, and Multiple of 2 Other cases: Minimum of 64, and Multiple of 2	Single DSI output: 16 less than input HFP Dual DSI output: 16 less than half of input HFP E.g. if input HFP is 128, then output HFP should be 128/2 – 16 = 48
Vertical Back Porch	Minimum of 2	
Vertical Sync Width	Minimum of 1	
Vertical Actual	Minimum of 2	
Vertical Front Porch	Minimum of 2	

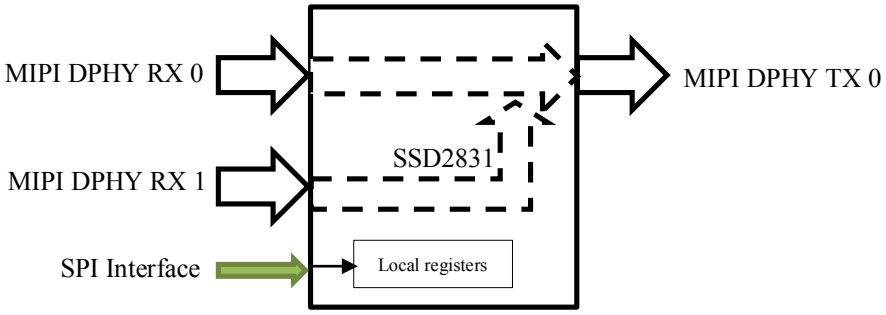
The possible video paths supported in this mode are shown below. The SPI interface can only be used to program local registers.

Dual MIPI DPHY Input, Dual MIPI Video Output

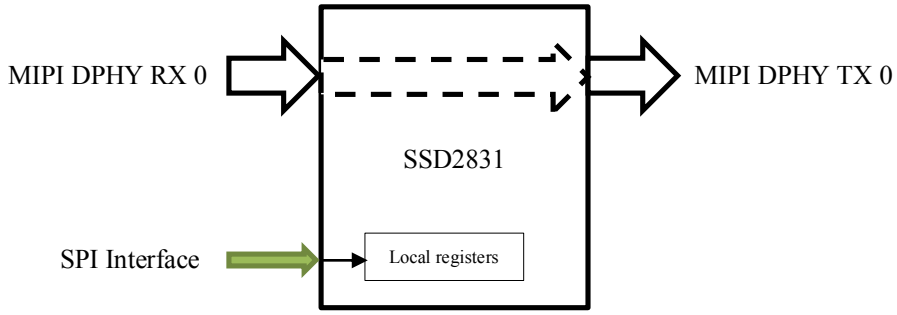


Dual MIPI DPHY Input, Single MIPI Video Output

This is a merge use case. MIPI DPHY RX 0/1 can be the odd/even pixels of the merged image or can be left/right side of the merged image.

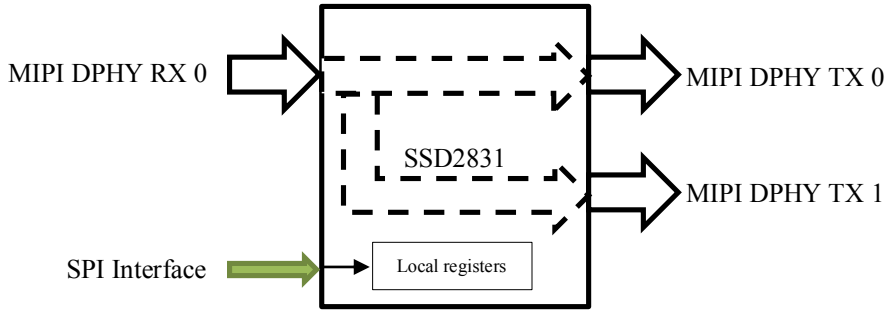


Single MIPI DPHY Input, Single MIPI Video Output



Single MIPI DPHY Input, Dual MIPI Video Output

This is either a split use case or a broadcast use case. For split use case, it can be either odd/even pixel split, or left/right image split



15.4 Interrupt Operation

An interrupt signal int has been provided to interrupt the application processor so that it does not need to poll the status all the time. This will save the processing time of the application processor. int can be programmed to active high or active low, when the event has happened.

There are many sources that can be mapped to the interrupt signal. The user can select different source to perform different task. If more than 1 source is selected, the int signal will be asserted when the event for 1 of the sources has happened. In this case, the user needs to read the register **ISR** to determine what event has happened. The different sources can be enabled/disabled through register **ICR**. Below is the list of available interrupt sources and their usage.

RDR

To indicate that return data from one of the MIPI slave is available for read.

BTAR

To indicate whether the SSD2831 has the bus authority or not. It can be used after SSD2831 makes a BTA. If the MIPI slave has returned the bus authority back to SSD2831, the interrupt will be set to indicate so. Please note that, on power up, the bus authority is already on the SSD2831. Hence, the SSD2831 will show that it has the bus authority.

ARR

To indicate whether the SSD2831 has received the acknowledge response from the MIPI slave. The acknowledge response can either report error or not error. This is to be determined by the **ATR** bit.

The above three interrupts are provided to the user to handle reading data from the MIPI slave or getting acknowledgement response from the MIPI slave.

PLS

To indicate whether the PLL has been locked or not. If the PLL is not locked, the programming speed at the external interface must be slow. After changing the PLL setting or changing the reference clock source, the user also needs to use this interrupt to determine the PLL status.

On power up, only **PLS** interrupt is enabled. This is to let the user determine the programming speed before configuring the SSD2831.

LPTO

To indicate that there is LP RX time out.

HSTO

To indicate that there is HS TX time out.

The above two interrupts are provided to the user for error handling.

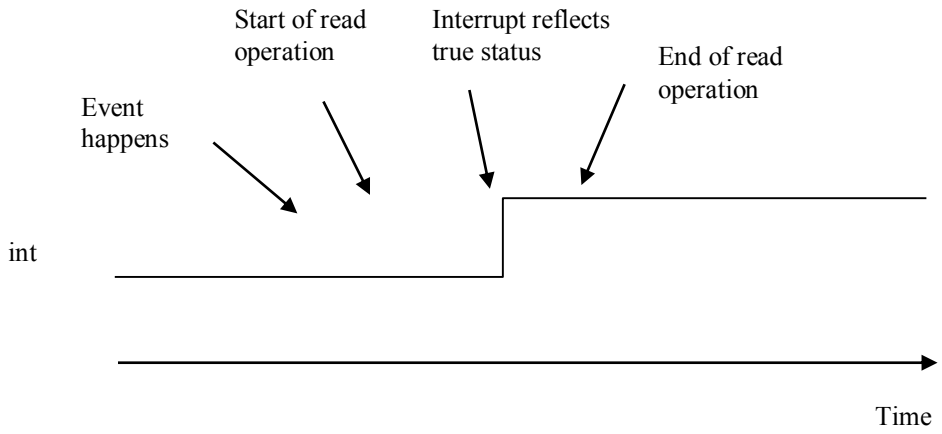
CBE, CBA, MLE, MLA

All these interrupts (CBE = command buffer empty, CBA = command buffer available, MLE = MCU line buffer empty, MLA = MCU line buffer available) are provided to indicate the status of the internal data buffers. They are used if the user is familiar with the buffer management of the SSD2831. Otherwise, it is recommended to use the **PO** interrupt.

One important thing to note is the interrupt latency. The output interrupt signal does not change immediately after an operation. This is due to the internal processing of the SSD2831. For example, after changing the interrupt source from one to another, the output int level will remain at the old level for a short period after the

programming is done. Another example is that after programming the **TDC** field, the interrupt will take a short period to reflect the correct **PO** status on int. There is always a delay between the actual event and the interrupt.

In order to guarantee that the user can get the correct interrupt, it is recommended that the user performs a read of any SSD2831 local register before taking in the interrupt signal or polling the interrupt status bits. The read operation will cover the interrupt latency period. Alternatively, the user can wait for certain amount of time to make sure the interrupt reflects the true status. Below is a diagram for illustration.



15.4.1 Internal Buffer Status

There are 2 types of buffers inside the SSD2831, which are MCU interface line buffer (ML) and SPI command interface buffer (CB).

The ML buffers are used to store the data (DCS command 0x2C and 0x3C) written through DSI RX when if_sel is '11'. They are also used to store the video data written through DSI RX when if_sel is '10'.

For CB buffers, all command packets will be stored into them. They can store multiple packets, up to 4096 bytes in total. Below is a list of possible packets

- Generic Short Write Packet
- Generic Read Packet
- DCS Short Write Packet
- DCS Read Packet
- Generic Long Write Packet
- DCS Long Write Packet

In case of automatic partitioning, the packet length is determined by the **PST** field. It is not recommended to make the **PST** field so small.

When the if_sel is "00", the user can write the data through SPI interface. All packets will be written into the CB buffers. Hence, the user needs to check the corresponding interrupts. The usage of the interrupts is listed below.

CBE

To indicate that the Command buffer is empty.

CBA

To indicate that the Command buffer can hold at least 1 more packet. The user can write 1 such packet into CB buffer.

MLE

To indicate that MCU Long buffer is empty. Since the ML buffer can hold 2 packets, the user can write up to 2 such packets into ML buffer without needing to look at the interrupt status.

MLA

To indicate that the MCU Long buffer can hold at least 1 more packet. The user can write 1 such packet into ML buffer.

The interrupts mentioned here can be used as flow control between the application processor and the SSD2831. However, it requires the user to know the buffer operation well. The **PO** interrupt is a combination of the eight. It makes decision according to the parameters provided by the user for the next packet to be written. Hence, the user does not need to know which buffer is going to be used and how the buffer status is.

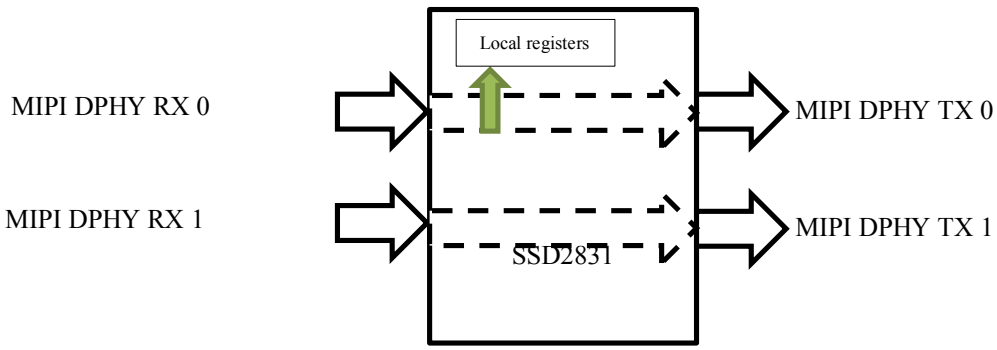
15.5 Command Mode Use Cases

The address range for the SSD2831 local register is from 0xB1 to 0xFF. The user can access the registers in this range to configure and control the SSD2831. For Generic packet that starts from 0xB1 to 0xFF, it can be written through the Packet Drop register. When the user writes data to it, the data will be sent over the serial link to the MIPI slave. The data packet sent will either be DCS or generic packet.

The following command mode use cases are possible:

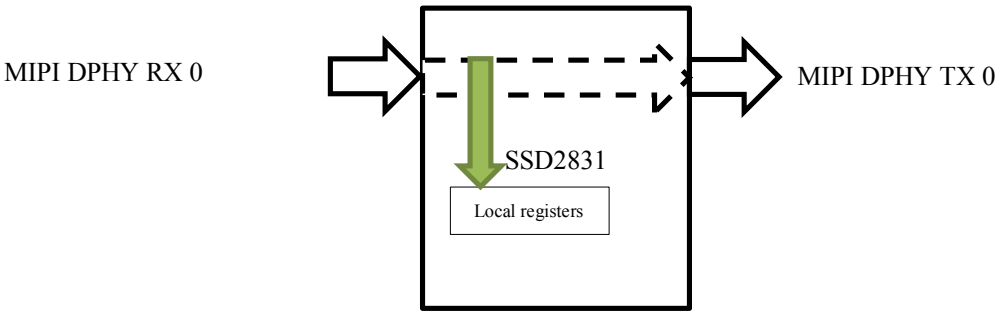
Dual MIPI DPHY Input, Dual MIPI Command Output

To select MIPI DPHY(s) input, if_sel[1:0] needs to be "11"



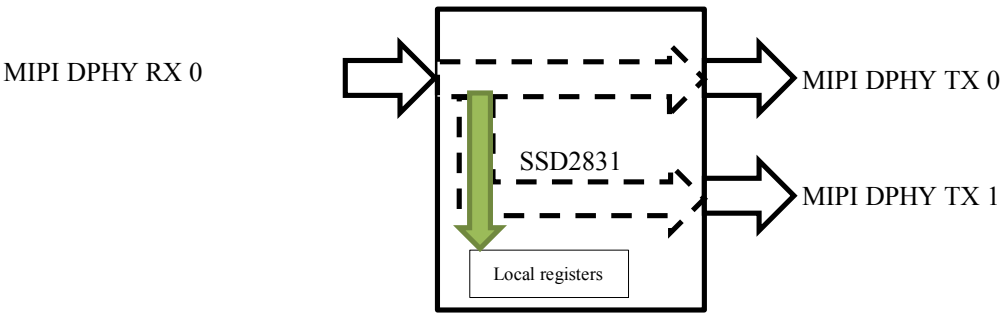
Single MIPI DPHY Input, Single MIPI Command/Video Output

To select MIPI DPHY(s) input, if_sel[1:0] needs to be "11"



Single MIPI DPHY Input, Dual MIPI Command Output

This is a broadcast use case. To select MIPI DPHY(s) input, if_sel[1:0] needs to be "11"



15.5.1 Write Operation

The SSD2831 can issue four kinds of packets for write operation, which are Generic Short Write Packet, Generic Long Write Packet, DCS Short Write Packet and DCS Long Write Packet. The VC ID of the outgoing packets can also be programmed through registers.

The SSD2831 needs to know the payload size of the outgoing packets. Hence, the user needs to program the corresponding control registers prior to sending the MIPI data.

To send a DCS or Generic Write Packet in address 0xB1 to 0xFF, the user needs to write the command/header and the payload to the Packet Data Drop register**.** If the size field is no more than 2 for Generic packet and 1 for DCS packet, the SSD2831 will send out DCS or Generic Short Write Packet with the correct type. Otherwise, DCS or Generic Long Write Packet will be sent out.

For DCS Write Packet, partition is supported for 0x2C or 0x3C DCS command. This is because the DCS command 0x2C and 0x3C are to write display data into the LCD panel display memory. The payload will be partitioned into a few packets where the payload of each packet is determined by the Partition register. The first byte is the DCS command and the following partition bytes are the payload. Only the last packet might contain less payload, as the total payload might not be integer multiple of partition size. If the incoming DCS command is 0x2C, the DCS command for the first packet is 0x2C and the DCS command for all other packets is 0x3C. If the incoming DCS command is 0x3C, the DCS command of all the packets is 0x3C.

For example, if the byte size field is 200 and partition field is 80, 3 packets will be sent. The first two have 80 bytes of payload. The last packet has 40 bytes of payload.

After performing a write operation, the user can optionally make a BTA to let the MIPI slave report its status. The SSD2831 will automatically make a BTA after each write operation.

15.5.2 Read Operation

The SSD2831 can issue two kinds of packets for read operation, which are Generic Read Packet, and DCS Read Packet. The bit **DCS** controls whether Generic Read Packet or DCS Read Packet will be sent out. The VC ID of the outgoing packets can also be programmed through registers.

Before the read packet is sent out, the SSD2831 will always send out the Set Maximum Return Size Packet. This is to limit the Read Response Packet sent by the MIPI slave such that there is no over flow. Two factors determine the maximum size. One is the limit of the SSD2831 and the other is the limit of the application processor. The user should choose the smaller one among these two limits to use as the maximum return size.

The parameter in the Set Maximum Return Size Packet is taken from local register. The user could program the Set Maximum Return Size Register before every read so that the correct value is sent through Set Maximum Return Size Packet. If the value is already the desired value, the user can choose not to program it. SSD2831 will always automatically send out Set Maximum Return Size Packet before the Read Packet.

To send a DCS Read or Generic Read Packet, the user just needs to write the DCS (as there is no parameter for DCS read) or Generic command, or write to Packet Drop Data register when the address is from 0xB1 to 0xFF.

Similar to the write operation, the Total Data Count Register field is used to determine the payload size of the outgoing packet. For DCS Read Packet, the payload is just the DCS command. There is no parameter associated. For Generic Read Packet, the SSD2831 will send out the correct packet type according to the Total Data Count value.

After sending out the read packet, the SSD2831 will automatically perform a BTA to wait for the Read Response Packet from the MIPI slave. The return data will be stored in a data register. No matter what read packet is sent out, there is only one packet returning data. Therefore, no matter whether the read is DCS read or Generic read, no matter what command is used in DCS read, the return data is always stored in the same data register. The user can read the data out when the read valid status bit is set to 1. After seeing read valid status bit been set to 1, the user should first check the number of bytes returned by the MIPI slave. By using this information, the user will know how many data should be read out from data register. After all the return data are read out, the read valid status bit will be set to 0 by the SSD2831.

Even the read valid status bit is set to 1, the user can choose not to read the data out from data register. The user can continue performing another operation. Once the user does so, the read valid status bit will be set to 0 by the SSD2831.

There might be Acknowledge and Error Report Packet sent by the MIPI slave at the same time.

Under certain circumstance, the MIPI slave might only send back Acknowledge and Error Report Packet without any data. Thus, the read valid status bit will not be set. Therefore, it is recommended that the user check the bus turnaround bit first. The bus turnaround bit is to indicate whether the MIPI slave has passed the bus authority back to the SSD2831 or not. Only when the bus turnaround is 1, there might be return data. If there is no return data, the user should follow Acknowledgement Operation to handle the acknowledgement.

15.5.3 State Machine Operation

The state machine controls the sending and receiving of the data packet over the serial link. It is triggered by an event from the application processor or the received data. Once a complete packet is written into the SSD2831 buffer, it will send it out through the serial link. The user can write 1 to bit **COP** (cancel-operation) at any time to cancel all the current operations.

When the SSD2831 is in high speed mode, the serial link is mainly used to send display data. If there is no data to send, it will send null packet to maintain the serial link timing. If the application processor does not have display data to send in a long period, it can turn the serial link into low power mode by setting the register bit **HS** to 0.

When the SSD2831 is in low power mode, the serial link is mainly used to send command and configuration data. If there are no data to be sent, the SSD2831 will be idle in LP TX stop mode.

The user can also enter sleep mode by writing 1 to **SLP** bit. Once the **SLP** bit is set to 1, the SSD2831 will automatically enter LP mode. If the **HS** bit is 1, the SSD2831 will clear the **HS** bit to 0 and switch from HS to LP mode. Afterwards, the SSD2831 will issue ULPS trigger message to the MIPI slave to enter Ultra Low Power State. During this state, the clock to SSD2831 can be switched off such that the SSD2831 only consumes leakage current. This will save the overall system power consumption. When exiting from the ULPS, the user can write 0 to **SLP** bit. However, the user should be aware that the time to exit from ULPS is relatively long (pleaser refer to MIPI DPHY specification). Hence, the user cannot perform any data transmission before the system exits from ULPS.

During reception, the state machine will disassemble the incoming data packet and put the received register content into the internal buffer for reading out. Once all the data are put into the buffers, it will set the register bit **RDY** to 1 to indicate that the SSD2831 is ready for read. The total number of received bytes will also be stored in **RDCR**.

After the reception is completed, the SSD2831 will perform a bus turn around to enter the transmission mode. It will always come back to the LP TX stop mode before it enters any other mode.

15.6 PHY controller Operation

PHY-controller controls the operation of the analog transceiver. It controls whether the serial link is in high speed or low power mode and whether it's in transmit or receive mode.
In transmit mode, the PHY controller will perform the handshaking procedure when switching between LP mode and HS mode according to the control from PCU. During HS mode, PHY controller will provide parallel data and clock to the analog transmitter for transmitting in differential signals serially. During LP mode, the PHY controller will provide the serial data to the analog transmitter.
In receive mode, the PHY controller will detect the handshaking sequence in LP mode and inform the PCU. Once entering escape mode, it will collect the serial data from analog receiver and put them in parallel form for the PCU to process.
Various timing parameter has been defined in MIPI DPHY specification. The timing parameters are a mixture of absolute time and cycle counts. Hence, for different operation speed, there is different timing requirement. The user can adjust the value in these registers to have different DPHY timing parameters. This gives maximum flexibility for different operation speed.

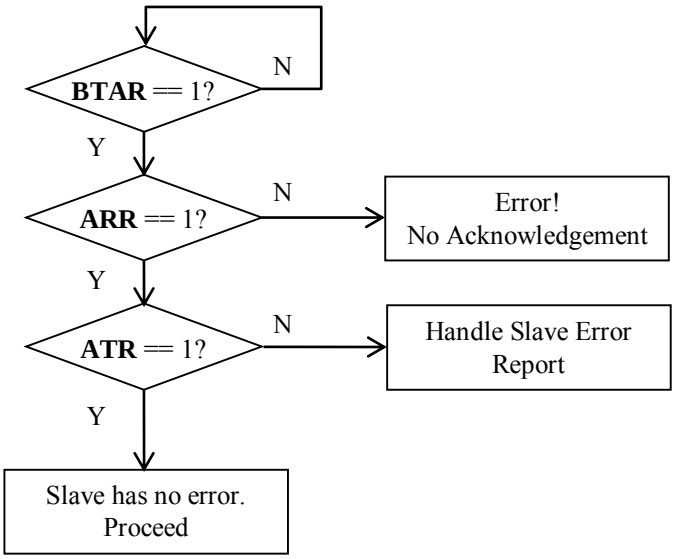
15.7 Acknowledgement Operation

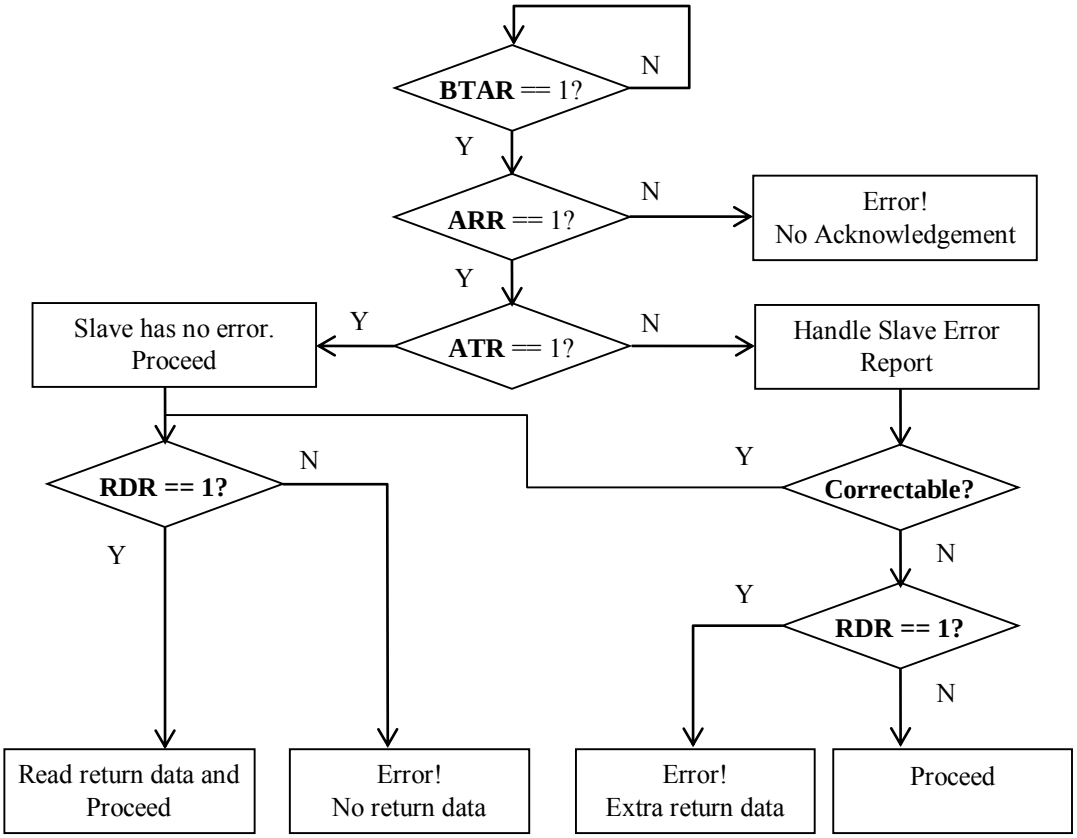
The SSD2831 can perform a BTA to give the bus authority to the MIPI slave and let it report its status. The BTA can be enabled by setting **FBW** bit to 1 and performing a write operation, or just performing a read operation. After the MIPI slave passes the bus authority back, the SDD2831 will set bit **BTAR** to 1.

If there is no error on the slave side, the MIPI slave will return ACK trigger message, if the packet before BTA is a write packet. The MIPI slave will return Read Response Packet, if the packet before BTA is a read packet. In this case, after receiving the response from the MIPI slave, SSD2831 will set bit **ARR** and **ATR** bits to 1. **ARR** indicates that response has been received from MIPI slave. **ATR** indicates that the MIPI slave has reported no error with ACK trigger message. Consequently, the register **ARSR** will be cleared to 0.

If there is error on the slave side, the MIPI slave will return Acknowledge and Error Report packet, if the packet before BTA is a write packet. The MIPI slave will return Read Response Packet (depending on the error type) and Acknowledge and Error Report Packet, if the packet before BTA is a read packet. In this case, after receiving the response from the MIPI slave, SSD2831 will set bit **ARR** bit to 1 and **ATR** bits to 0. **ARR** indicates that response has been received from MIPI slave. **ATR** indicates that the MIPI slave has sent Acknowledge and Error Report Packet instead of ACK trigger message. Therefore, the MIPI slave has reported error. The error reported by the MIPI slave will be stored in register **ARSR**. The user can read this register to see what error the MIPI slave has encountered.

For the detailed description of each error bit, please refer to MIPI DSI specification. Below are the flow charts of handling the MIPI slave acknowledgement. They are just for reference.




BTAR == 1?
N
Y
ARR == 1?
N
Error!
No Acknowledgement
Y
Slave has no error.
Proceed
Y
ATR == 1?
N
Handle Slave Error
Report
RDR == 1?
N
Y
Correctable?
Y
N
RDR == 1?
Y
N
Read return data and
Proceed
Error!
No return data
Error!
Extra return data
Proceed

15.8 PLL Configuration

The PLL output frequency is calculated by the equations below,

$$f_{PRE} = \frac{f_{IN}}{MS}$$

$$f_{OUT} = f_{PRE} * NS$$

where the f_{IN} is the input reference clock frequency and f_{OUT} is the output clock frequency of the PLL.

The clock frequencies need to satisfy the constraint below.

$5MHz < f_{IN} \leq 40MHz$

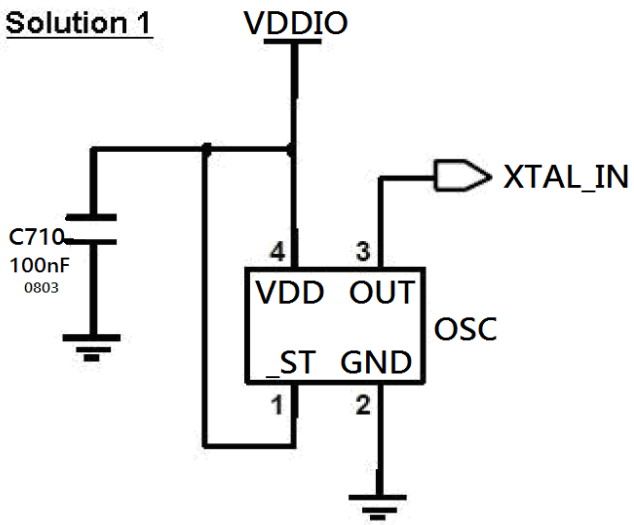
$5MHz < f_{REF} \leq 100MHz$

$62.5MHz < f_{OUT} \leq 1250MHz$

The value of FR, MS, and NS are controlled in the register **PLCR**.

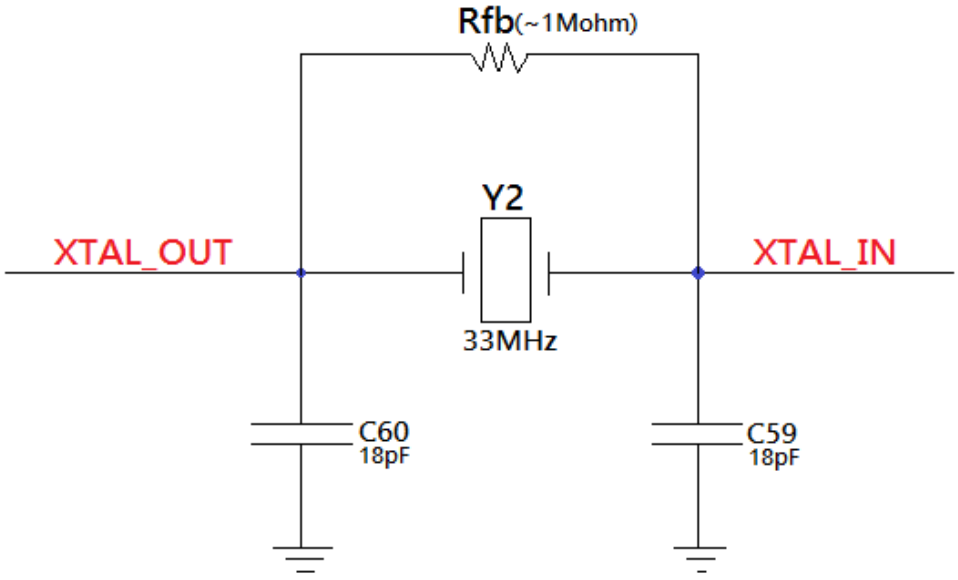
All the values of FR, MS and NS can only be modified when the PLL is turned off (**PEN**=0). Hence, the sequence for modification is to turn off PLL, modify register value, and turn on PLL.

15.9 Clock Source Example



Pin	Connection
XTAL_OUT	Open

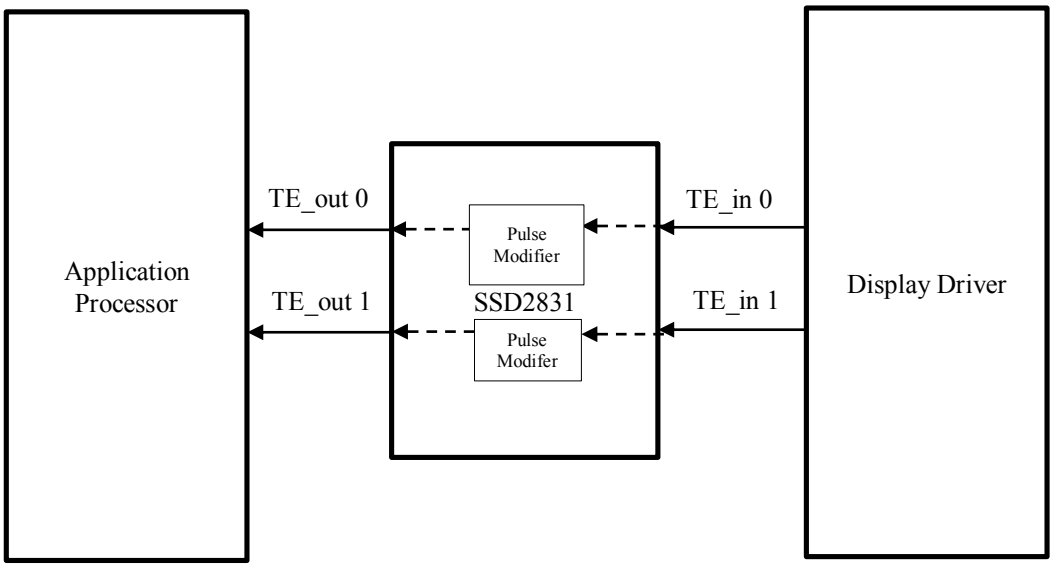
Solution 2



15.10 Tearing Effect (TE) Operation

15.10.1 Using IO Pins

SSD2831 takes in 2 TE pins, reshape them and output them to 2 TE pins. The programmable parameters are the pulse width, polarity, and delay.



15.11 Using MIPI Escape Mode

The TE operation is to perform a BTA following the previous BTA without transmitting anything in between. The bus is handed to the MIPI slave for providing TE information. After getting the TE event from display driver, the MIPI slave will pass the bus authority back to the SSD2831 by using BTA trigger message.

The TE operation can be enabled by setting bit **FBT** and **FBW** to 1 before writing the last command to the MIPI slave. Afterwards, the application processor can instruct the SSD2831 to send out the last command in a write packet. Since **FBW** is 1, the SSD2831 will automatically perform a BTA after the write operation. The MIPI slave will response and pass the bus authority back. Since **FBT** is 1, the SSD2831 will perform another BTA without sending any data. This makes the MIPI slave enter TE mode.

The MIPI slave will send a TE trigger message back when it gets the TE event. After getting the trigger message, the SSD2831 will set the TE pin to 1 to indicate that TE event has been received. At the same time, bit **TER** will be set to 1. The application processor can write 1 to this bit to clear it. As the TE trigger message only determines when the TE pin will be set to 1, a counter is used to determine when to set the TE pin to 0. The TE pin will be set to 0, once the counter reaches the value in **TEC**. The counter uses the reference clock to do counting.

If the MIPI slave does not send back the TE trigger message but just perform a BTA to pass the bus back, the SSD2831 will automatically perform another BTA to pass the bus to the MIPI slave again. It will continue do so until the MIPI slave respond with the TE trigger message, or the **FBT** bit is set to 0, or the LP RX timer expires.

If the MIPI slave does not send back the TE trigger message and still holds the bus, the user can set the bit **FBC** to 1 to force a bus contention. After bus contention is resolved, the slave will pass the bus back to SSD2831.

SSD2831 supports dual MIPI TX port. Hence there would be 2 TE outputs accordingly.

15.12 Contention Detection and Timer Operation

Two timers have been defined in SSD2831 to resolve the potential contention issue on the bus. The two timers are the HS TX timer and LP RX timer. Please see the register description for the detailed usage.

Whenever the SSD2831 sees a contention being detected, it will reset the state machine and enter the default mode, which is LP TX idle mode. The data line will be kept at LP11.

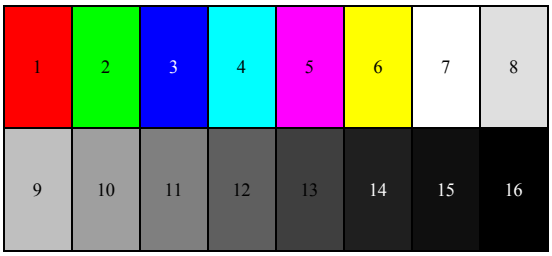
15.13 Video BIST

SSD2831 supports the following pattern generation for video BIST.

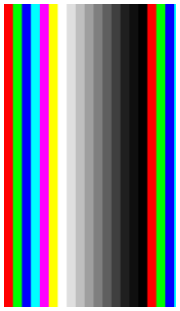
Parameter Required: 17 bytes

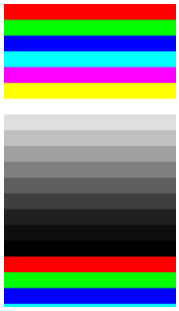
Offset	7	6	5	4	3	2	1	0	Default	R/W	Description
0	vb_mode						vb_cspf	vb_en	0x00	R/W	vb_mode : VBIST test mode selection vb_cspf: Enable color 1 & 2 swapping on every frame. (Note: This feature is intended to be used together with vb_mode=0xC. The usage in other vb_mode is not verified.) vb_en : VBIST enable
1	vb_repeat_cnt_h								0x00	R/W	Repeat count
2	vb_repeat_cnt_l								0x3C	R/W	
3	vb_r1								0x00	R/W	RGB value for color 1
4	vb_g1								0x00	R/W	
5	vb_b1								0x00	R/W	
6	vb_r2								0x00	R/W	RGB value for color 2
7	vb_g2								0x00	R/W	
8	vb_g2								0x00	R/W	
9	vb_x_start_h								0x00	R/W	
10	vb_x_start_l								0x00	R/W	
11	vb_x_end_h								0x00	R/W	
12	vb_x_end_l								0x00	R/W	
13	vb_y_start_h								0x00	R/W	
14	vb_y_start_l								0x00	R/W	
15	vb_y_end_h								0x00	R/W	
16	vb_y_end_l								0x00	R/W	

MODE 0x0		Parameter	Usage
Solid color loop in sequential order of 16 pre-defined color of (0XFF0000, 0X00FF00, 0X0000FF, 0X00FFFF, 0XFF00FF, 0XFFFF00, 0XFFFFFF, 0XDFDFDF, 0XBFBFBF, 0X9F9F9F, 0X7F7F7F, 0X5F5F5F, 0X3F3F3F, 0X1F1F1F, 0X0F0F0F, 0X000000)	1	vb_repeat_cnt_h	Number of frames pause between different colors
	2	vb_repeat_cnt_l	
	3	vb_r1	*Not used*
	4	vb_g1	
	5	vb_b1	
	6	vb_r2	*Not used*
	7	vb_g2	
	8	vb_g2	
	9	vb_x_start_h	*Not used*
	10	vb_x_start_l	
	11	vb_x_end_h	*Not used*
	12	vb_x_end_l	
	13	vb_y_start_h	*Not used*
	14	vb_y_start_l	
	15	vb_y_end_h	*Not used*
	16	vb_y_end_l	

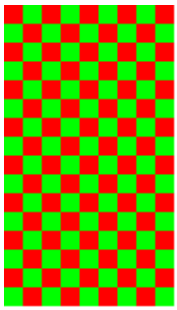


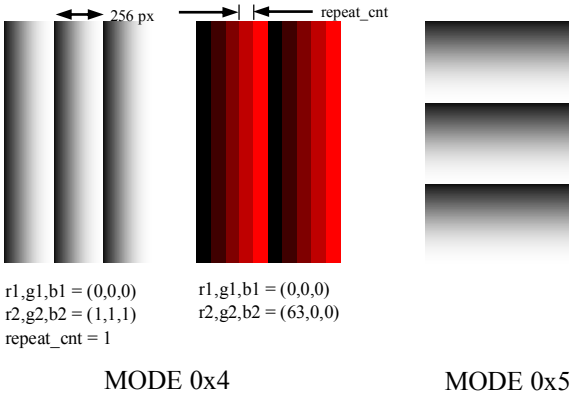
MODE 0x1, 0x2		Parameter	Usage
Vertical (mode 0x1) / Horizontal (mode 0x2) repeating 16 colors bars with configurable bar width. Color repeating order are (0XFF0000, 0X00FF00, 0X0000FF, 0X00FFFF, 0XFF00FF, 0XFFFF00, 0XFFFFFF, 0XDFDFDF, 0XBFBFBF, 0X9F9F9F, 0X7F7F7F, 0X5F5F5F, 0X3F3F3F, 0X1F1F1F, 0X0F0F0F, 0X000000)	1	vb_repeat_cnt_h	Color bar width in pixels (MODE 0x1 only : Must be even number)
	2	vb_repeat_cnt_l	
	3	vb_r1	*Not used*
	4	vb_g1	
	5	vb_b1	
	6	vb_r2	*Not used*
	7	vb_g2	
	8	vb_g2	
	9	vb_x_start_h	*Not used*
	10	vb_x_start_l	
	11	vb_x_end_h	*Not used*
	12	vb_x_end_l	
	13	vb_y_start_h	*Not used*
	14	vb_y_start_l	
	15	vb_y_end_h	*Not used*
	16	vb_y_end_l	

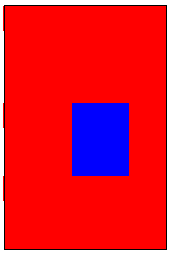




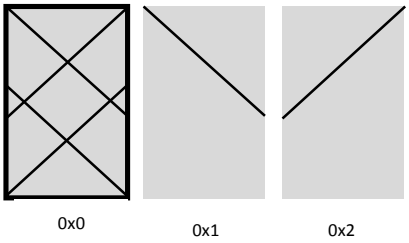
MODE 0x3		Parameter	Usage
Checker box with configurable width (>= 2) and color.	1	vb_repeat_cnt_h	Box width (>=2, must be even number)
	2	vb_repeat_cnt_l	
	3	vb_r1	Color 1 RGB value
	4	vb_g1	
	5	vb_b1	
	6	vb_r2	Color 2 RGB value
	7	vb_g2	
	8	vb_g2	
	9	vb_x_start_h	*Not used*
	10	vb_x_start_l	
	11	vb_x_end_h	*Not used*
	12	vb_x_end_l	
	13	vb_y_start_h	*Not used*
	14	vb_y_start_l	
	15	vb_y_end_h	*Not used*
	16	vb_y_end_l	



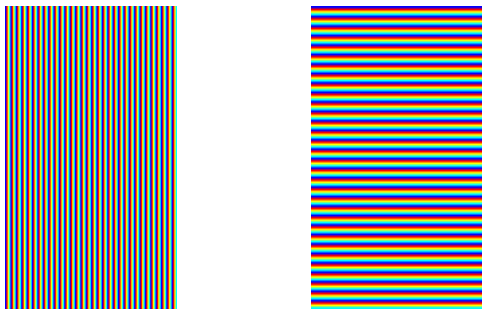
MODE 0x4, 0x5		Parameter	Usage
Horizontal (0x4) or vertical (0x5) gradient ramp with programmable line width and color increment value.  	1	vb_repeat_cnt_h	For Mode 0x4 - # of pixels for each color step. NOTE: It must be an even number. 0 – 1 pixel. 2 – 2 pixels. 4 – 4 pixels. … For Mode 0x5 - # of lines for each color step. 0 – 1 line. 1 – 1 line. 2 – 2 lines. …
	2	vb_repeat_cnt_l	
	3	vb_r1	Start color (common for mode 0x4, 0x5)
	4	vb_g1	
	5	vb_b1	
	6	vb_r2	Color increment value for each step (common for mode 0x4, 0x5)
	7	vb_g2	
	8	vb_g2	
	9	vb_x_start_h	*Not used*
	10	vb_x_start_l	
	11	vb_x_end_h	*Not used*
	12	vb_x_end_l	
	13	vb_y_start_h	*Not used*
	14	vb_y_start_l	
	15	vb_y_end_h	*Not used*
	16	vb_y_end_l	

MODE 0x6		Parameter	Usage
Solid filled rectangle with configurable position, size and foreground / background color 	1	vb_repeat_cnt_h	*Not used*
	2	vb_repeat_cnt_l	
	3	vb_r1	Foreground color
	4	vb_g1	
	5	vb_b1	
	6	vb_r2	Background color
	7	vb_g2	
	8	vb_g2	
	9	vb_x_start_h	Rectangle's left boundary (Must be even number)
	10	vb_x_start_l	
	11	vb_x_end_h	Rectangle's right boundary (Must be even number)
	12	vb_x_end_l	
	13	vb_y_start_h	Rectangle's top boundary
	14	vb_y_start_l	
	15	vb_y_end_h	Rectangle's bottom boundary
	16	vb_y_end_l	

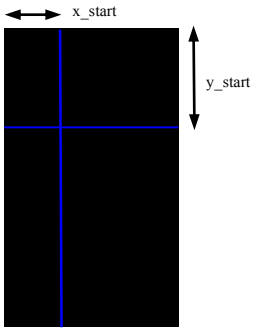
MODE 0x7		Parameter	Usage
Single pixel width full size rectangle with two 45° cross touching screen corners. Or single 45° diagonal line drawn from top left / top right corner. Foreground and background color are configurable.	1	vb_repeat_cnt_h	0x0 : Original Box + Cross 0x1 : Line from (0,0) - (W,W) 0x2 : Line from (0,W) - (W,0)
	2	vb_repeat_cnt_l	
	3	vb_r1	Foreground color RGB value
	4	vb_g1	
	5	vb_b1	
	6	vb_r2	Background color RGB value
	7	vb_g2	
	8	vb_g2	
	9	vb_x_start_h	*Not used*
	10	vb_x_start_l	
	11	vb_x_end_h	*Not used*
	12	vb_x_end_l	
	13	vb_y_start_h	*Not used*
	14	vb_y_start_l	
	15	vb_y_end_h	*Not used*
	16	vb_y_end_l	



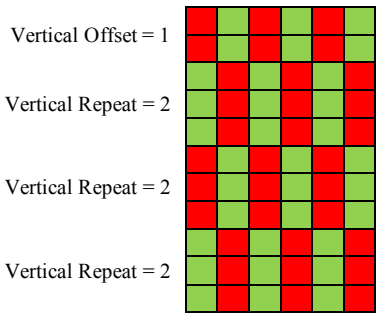
MODE 0x8, 0x9		Parameter	Usage
Vertical (0x8) or Horizontal (0x9) repeating color bars with width of 1 pixel per color. Color repeating order is [C1, !C2, !C1, C2]	1	vb_repeat_cnt_h	*Not used*
	2	vb_repeat_cnt_l	
	3	vb_r1	Color 1 RGB value
	4	vb_g1	
	5	vb_b1	
	6	vb_r2	Color 2 RGB value
	7	vb_g2	
	8	vb_g2	
	9	vb_x_start_h	*Not used*
	10	vb_x_start_l	
	11	vb_x_end_h	*Not used*
	12	vb_x_end_l	
	13	vb_y_start_h	*Not used*
	14	vb_y_start_l	
	15	vb_y_end_h	*Not used*
	16	vb_y_end_l	

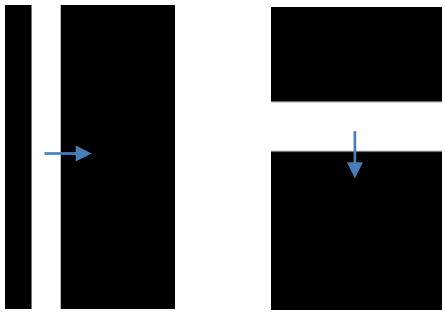


MODE 0xA		Parameter	Usage
Single pixel width vertical and horizontal line with configurable foreground and background color	1	vb_repeat_cnt_h	*No used*
	2	vb_repeat_cnt_l	
	3	vb_r1	Foreground color RGB value
	4	vb_g1	
	5	vb_b1	
	6	vb_r2	Background color RGB value
	7	vb_g2	
	8	vb_g2	
	9	vb_x_start_h	x-coordinate of the vertical line
	10	vb_x_start_l	
	11	vb_x_end_h	*Not used*
	12	vb_x_end_l	
	13	vb_y_start_h	y-coordinate of the horizontal line
	14	vb_y_start_l	
	15	vb_y_end_h	*Not used*
	16	vb_y_end_l	



MODE 0xB		Parameter	Usage
This mode is not used.	1 to 16		*Not used*

MODE 0xC		Parameter	Usage
Check box with configurable color, vertical offset and vertical repeat count. (Original single pixel checkbox can be obtained by setting offset=0 & repeat=0)  	1	vb_repeat_cnt_h	Vertical repeat in rows. 0: 1 line. 1: 2 lines. …
	2	vb_repeat_cnt_l	
	3	vb_r1	Color 1 RGB value
	4	vb_g1	
	5	vb_b1	
	6	vb_r2	Color 2 RGB value
	7	vb_g2	
	8	vb_g2	
	9	vb_x_start_h	*Not used*
	10	vb_x_start_l	
	11	vb_x_end_h	*Not used*
	12	vb_x_end_l	
	13	vb_y_start_h	Vertical Offset in rows. (Must be <= Vertical repeat) 0: "vertical repeat" - 0 lines. 1: "vertical repeat" - 1 lines. … Vertical repeat: 0 line. (Same as 0)
	14	vb_y_start_l	
	15	vb_y_end_h	*Not used*
	16	vb_y_end_l	

MODE 0xD, 0xE		Parameter	Usage
Vertical (0xD) or Horizontal (0xE) moving bar with configurable speed, width, step (with direction) and foreground / background color. 	1	vb_repeat_cnt_h	Number of frames pause between steps
	2	vb_repeat_cnt_l	
	3	vb_r1	Foreground color RGB value
	4	vb_g1	
	5	vb_b1	
	6	vb_r2	Background color RGB value
	7	vb_g2	
	8	vb_g2	
	9	vb_x_start_h	Move step (For mode 0xD, must be even number, signed)
	10	vb_x_start_l	
	11	vb_x_end_h	Bar width (For mode 0xD, must be even number)
	12	vb_x_end_l	
	13	vb_y_start_h	Move step (For mode 0xE, singed)
	14	vb_y_start_l	
	15	vb_y_end_h	Bar width (For mode 0xE)
	16	vb_y_end_l	
MODE 0xF		**Parameter**	**Usage**
Full screen solid fill with configurable color.	1	vb_repeat_cnt_h	*Not used*
	2	vb_repeat_cnt_l	
	3	vb_r1	Solid fill color RGB value
	4	vb_g1	
	5	vb_b1	
	6	vb_r2	*Not used*
	7	vb_g2	
	8	vb_g2	
	9	vb_x_start_h	*Not used*
	10	vb_x_start_l	
	11	vb_x_end_h	*Not used*
	12	vb_x_end_l	
	13	vb_y_start_h	*Not used*
	14	vb_y_start_l	
	15	vb_y_end_h	*Not used*
	16	vb_y_end_l	

15.14 Pixel Peek

SSD2831 supports pixel peek, which is allows user to peek at the pixel value on a programmable pixel location in the video frame. The pixel location can be configured to be marked out on the screen (through SSD2831 MIPI TX output) through a cursor (example shown below).

Note:

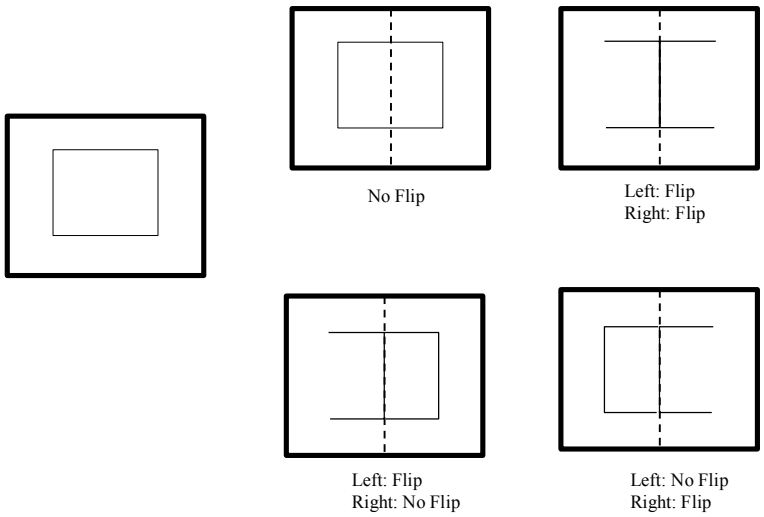
Pixel peek can only be supported for the following modes:

For dual DSI_RX input and 1 DSI_TX output(2 to 1)
RICR6.RGB_PACK_SEQ = 2: RGB0 lower order pixel = pixel[0], RGB0 higher order pixel = pixel[1]. RGB1 lower order pixel = pixel[n/2], RGB1 higher order pixel = pixel[n-1].

- The cursor shown crosses at the (x,y) location programmed by the user.
- The cursor is programmed to be visible, with 'blue'color.
- The actual pixel value of the location is stored in the register for user to read-back

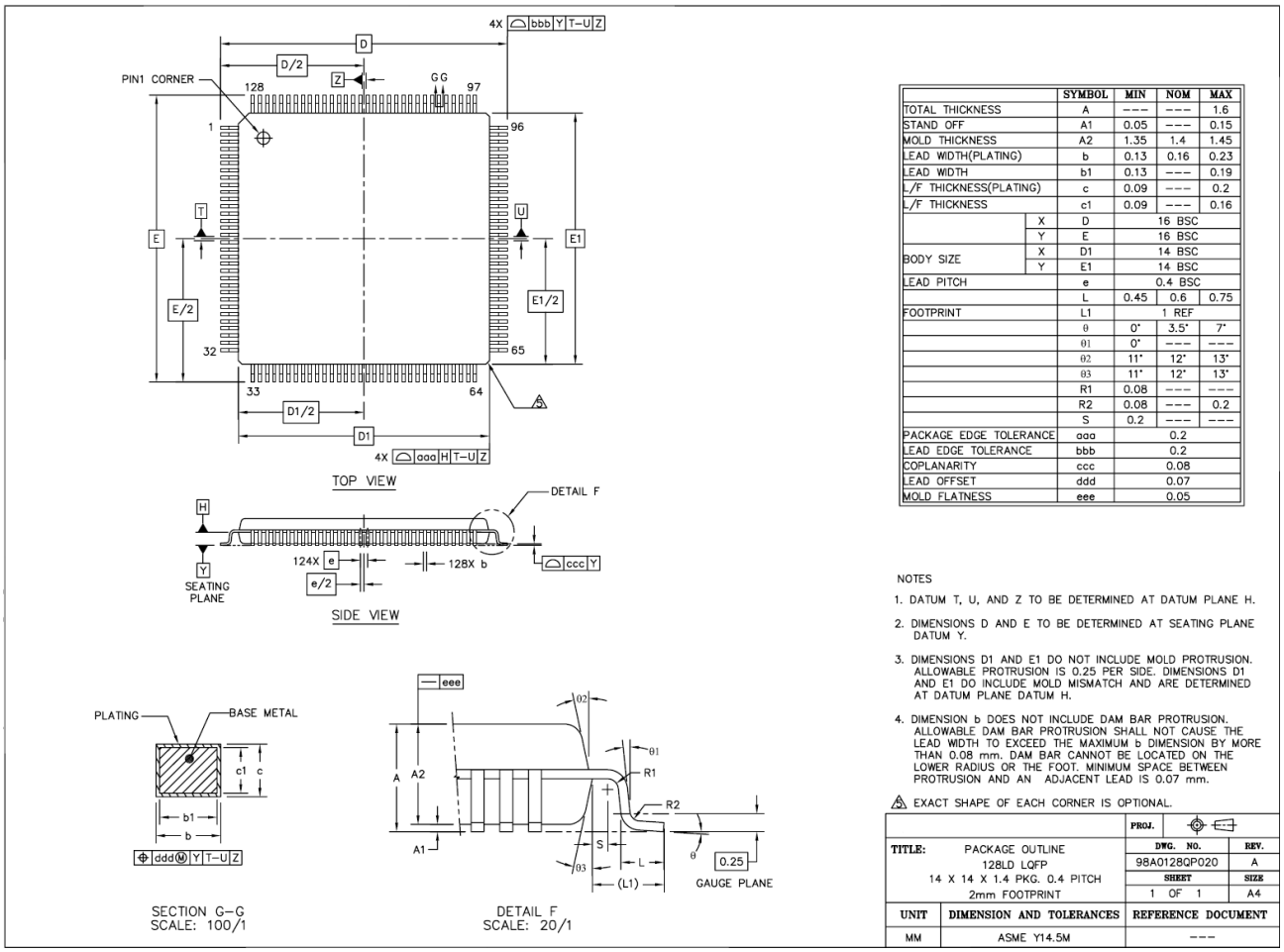
15.15 Image Flipping (Horizontal)

Each of the dual MIPI TX can be configured to perform horizontal flip independently of each other. For example:



16 PACKAGE INFORMATION

16.1 QFP 128 pins (14mm x 14mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.16	0.23
LEAD WIDTH		b1	0.13	---	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	16 BSC		
	Y	E	16 BSC		
	X	D1	14 BSC		
	Y	E1	14 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

NOTES

1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

5 EXACT SHAPE OF EACH CORNER IS OPTIONAL.

TITLE: PACKAGE OUTLINE 128LD LQFP 14 X 14 X 1.4 PKG. 0.4 PITCH 2mm FOOTPRINT		PROJ.	
		DWG. NO.	REV.
		98A0128QP020	A
		SHEET	SIZE
		1 OF 1	A4
UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT	
MM	ASME Y14.5M	---	

Figure 16-1: Package Information – LQFP 128 Pins

The product(s) listed in this datasheet comply with Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People's Republic of China Electronic Industry Standard GB/T 26572-2011 "Requirements for concentration limits for certain hazardous substances in electronic information products (电子电器产品中限用物質的限用要求)". Hazardous Substances test report is available upon request.

http://www.solomon-systech.com