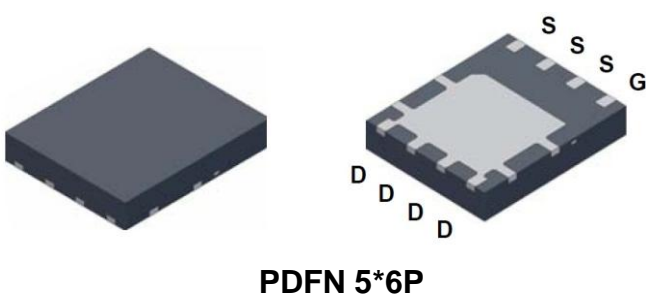


PZ0703EK

P-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D^3
-30V	7m Ω @ $V_{GS} = -10V$	-70A



PDFN 5*6P

ESD Protected Gate

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ³	$T_C = 25\text{ }^\circ\text{C}$	I_D	-70	A
	$T_C = 100\text{ }^\circ\text{C}$		-56	
Pulsed Drain Current ¹		I_{DM}	-150	
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	I_D	-13	
	$T_A = 70\text{ }^\circ\text{C}$		-10	
Avalanche Current		I_{AS}	-71	
Avalanche Energy	$L = 0.1\text{mH}$	E_{AS}	252	mJ
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	50	W
	$T_C = 100\text{ }^\circ\text{C}$		32	
	$T_A = 25\text{ }^\circ\text{C}$		2.5	
	$T_A = 70\text{ }^\circ\text{C}$		1.6	
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

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THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		2.5	°C / W
Junction-to-Ambient	$R_{\theta JA}$		50	

¹Pulse width limited by maximum junction temperature.

²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

³Package limitation current is -51A.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.4	-3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 16V$			± 30	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			-10	
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -4.5V, I_D = -20A$		5.7	10	m Ω
		$V_{GS} = -10V, I_D = -20A$		3.8	7	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -12A$		65		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1\text{MHz}$		5210		pF
Output Capacitance	C_{oss}			960		
Reverse Transfer Capacitance	C_{rss}			890		
Total Gate Charge ²	$Q_g(V_{GS}=10V)$	$V_{DS} = -15V, V_{GS} = -10V, I_D = -20A$		121		nC
	$Q_g(V_{GS}=4.5V)$			64		
Gate-Source Charge ²	Q_{gs}			12		
Gate-Drain Charge ²	Q_{gd}			27		
Turn-On Delay Time ²	$t_{d(on)}$			33		
Rise Time ²	t_r	$V_{DS} = -15V, I_D \cong -20A, V_{GS} = -10V, R_{GS} = 6\Omega$		25		nS
Turn-Off Delay Time ²	$t_{d(off)}$			100		
Fall Time ²	t_f			45		

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SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)

Continuous Current ³	I _S			-70	A
Forward Voltage ¹	V _{SD}	I _F = -20A, V _{GS} = 0V		-1.3	V
Reverse Recovery Time	t _{rr}	I _F = -20A, dI _F /dt = 100A / μS		26.5	nS
Reverse Recovery Charge	Q _{rr}			16	nC

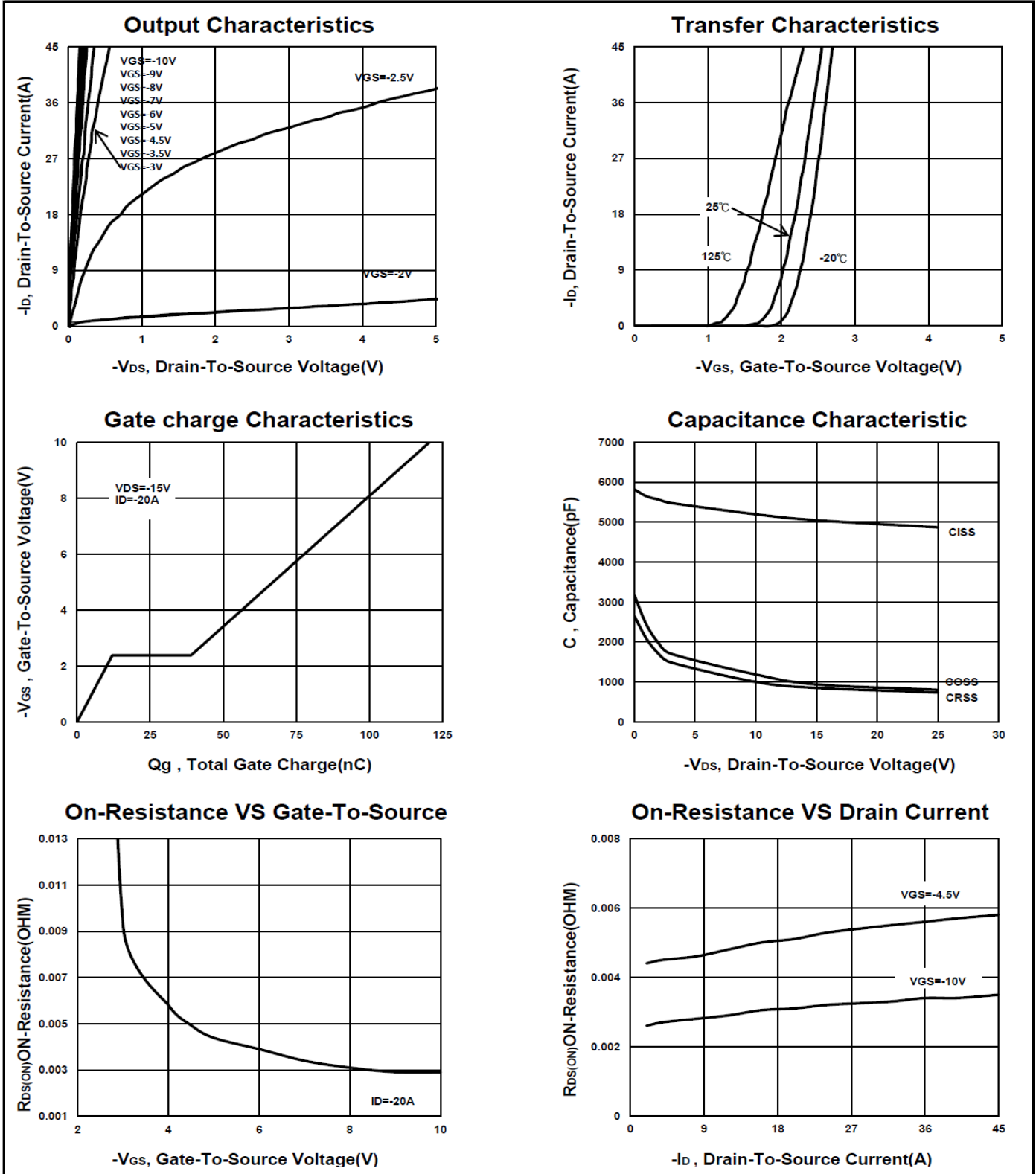
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Package limitation current is -51A.

PZ0703EK

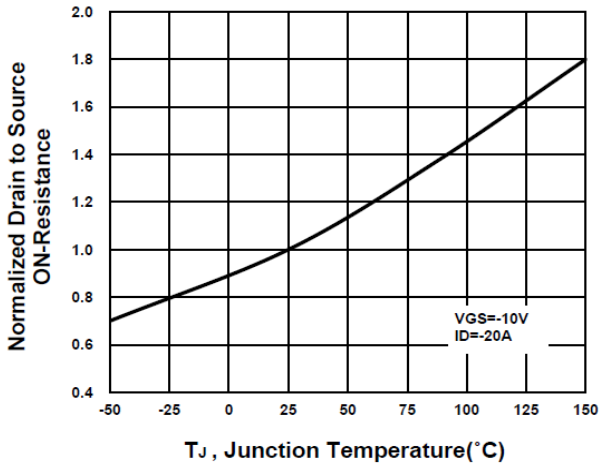
P-Channel Logic Level Enhancement Mode MOSFET



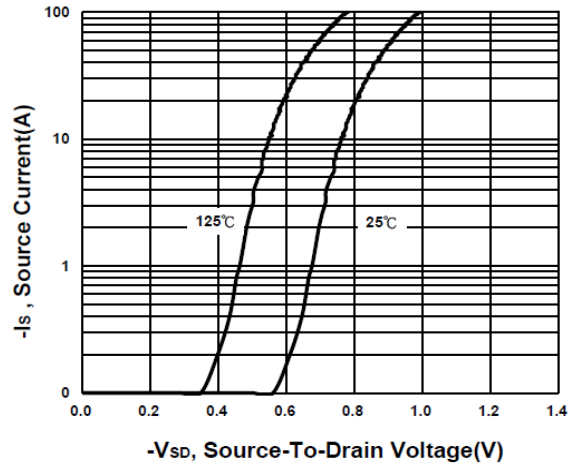
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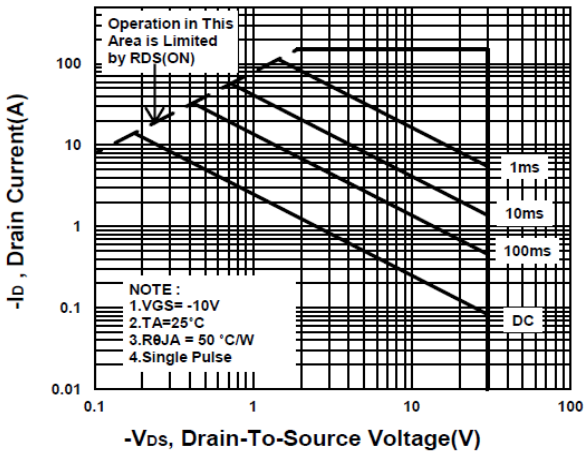
On-Resistance VS Temperature



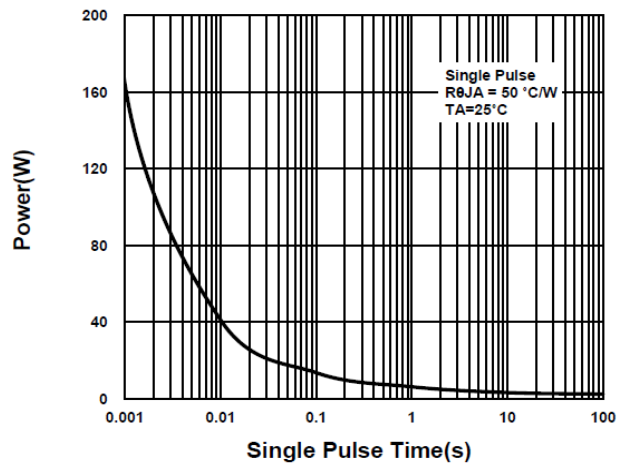
Source-Drain Diode Forward Voltage



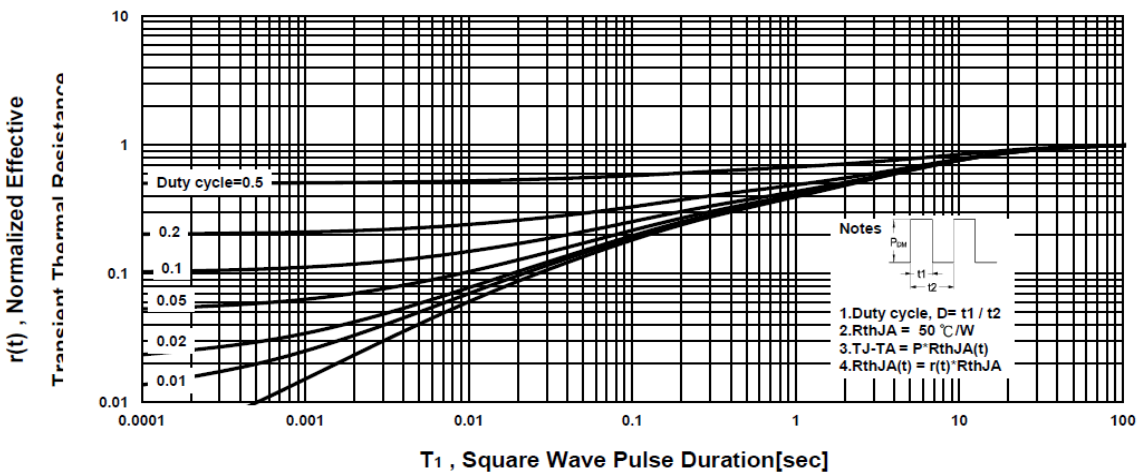
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



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Package Dimension

PDFN 5x6P MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8		5.15	J	3.33		3.78
B	5.44		5.9	K	0.9		
C	5.9		6.35	L	0.35		0.712
D	0.33		0.51	M	0°		12°
E		1.27		N	4.8		5.5
F	0.8		1.25	O	0.05		0.3
G	0.15		0.34	P	0.06		0.2
H	3.61		4.31	S	3.69		4.19
I	0.35		0.71				

